Written Examination EITP01 2019-03-21

Useful constants:

$$\hbar = 1.055 \times 10^{-34}\ Js$$

$$k_B = 1.381 \times 10^{-23}\ J/K$$

$$m_0 = 9.109 \times 10^{-31}\ kg$$

$$\epsilon_0 = 8.85 \times 10^{-12}\ Fm^{-1}$$

$$e = q = 1.602 \times 10^{-19}\ C$$

$$c = 2.998 \times 10^{8}\ m/s$$

1. Ballistic transport in QWFET **(15 p)**

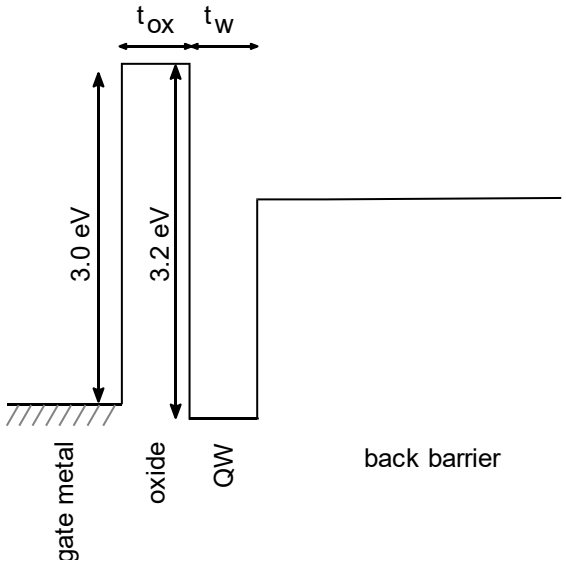
An InGaAs QWFET has the crossectional band structure shown below, with the following parameters:

$t_w = t_{ox} = 5$ nm

$\varepsilon_{ox} = 20, \varepsilon_s = 14$

$m^* = 0.04m_0$

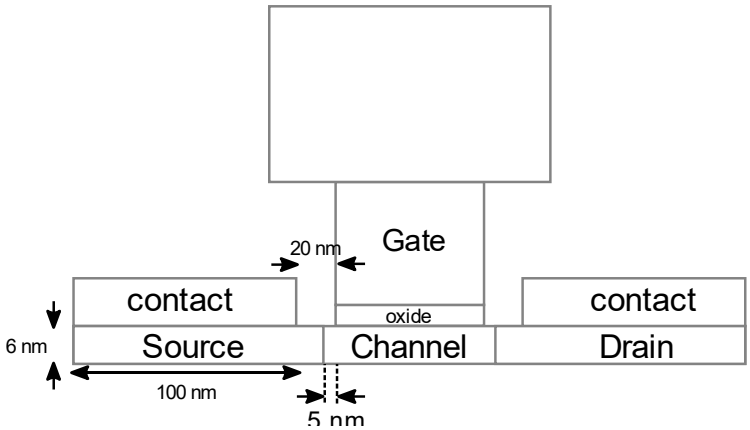
A gate length of 70 nm and a width of 10 µm.



a) Calculate the lowest two subband energy levels (E_1 and E_2) assuming an infinite well.
b) Calculate the gate capacitance of the device when operated in the on-state.
c) Explain the mechanism behind the current saturation in a ballistic transistor.
d) The device is operated at $V_{DS} = V_{GS} = 0.5$ V. Is the device in saturation?
e) Calculate the (quasi-)ballistic current I_{DS} assuming a transmission coefficient of 0.6.
f) Calculate the transconductance at these operation conditions.

2. High frequency operation (15 p)

Another QWFET device as seen below has $C_{ox} = 0.033\ F/m^2$, $C_q = 0.028\ F/m^2$ and $C_C = 0.057\ F/m^2$, width of 10 µm and gate length of 90 nm. g_m = 55 mS and g_d = 5 mS.



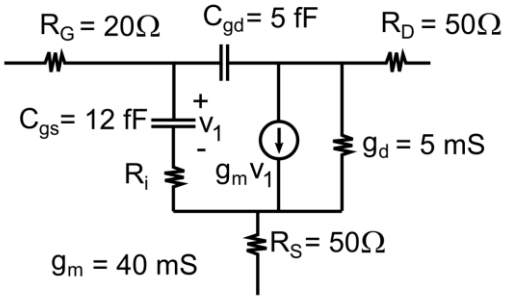
a. Calculate the intrinsic value of f_T for this device.

b. In reality, the contact and source and drain resistances lead to finite values of R_S and R_D. This device has a specific contact resistivity of 10 Ωµm^2, and a doping level of $1 * 10^{19}\ cm^{-3}$ and electron mobility of 500 cm^2/Vs in the source/drain regions, while the channel itself has a mobility of 10000 cm^2/Vs and doping level of $1.2 * 10^{16}\ cm^{-3}$. Due to a spacer process the low-doped channel region extends 5 nm outside of the gated area, while the gate-contact separation is 20 nm. Calculate R_S and R_D and comment on what is the largest contributor to the resistance.

c. The fact that the contacts and gate are so closely spaced leads to a significant parasitic capacitance of $C_{gs,p} = C_{gd,p} = 5\ fF$. Calculate f_T including the effect of source/drain resistance and parasitic capacitances.

3. Power Gain (15 p)

A transistor device is modelled by a hybrid-π small signal model (including parasitics):



Here we have assumed that $C_{sd} = C_{dg} = C_{dd} = C_m = 0$ for simplicity.

a) Explain the reason for introducing the channel resistance $R_i = 1/(1.4g_m)$.

b) Determine the z-parameters of the model at f = 100 GHz.

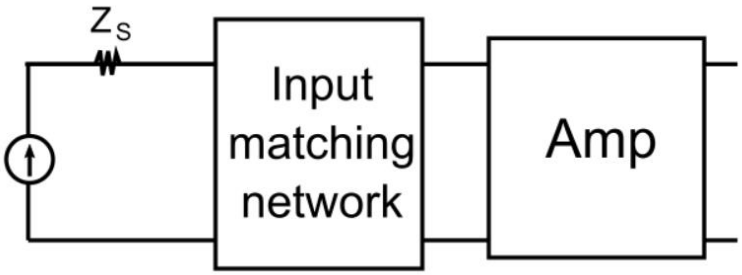
c) Will the device be stable at this frequency?

d) Use the proper metric to determine the power gain at this frequency.

e) Determine f_{max} of the device. What could be done to improve f_{max} further?

4. Designing a Low noise amplifier **(15 p)**

A transistor with $R = R_G + R_i = 44\ \Omega$, $g_m = 20$ mS, $\gamma = 2/3$ and $C_{gs} = 10.5$ fF is connected to a source with source impedance $Z_s = Z_0 = 50\ \Omega$ and will be used as a low-noise amplifier at f = 50 GHz.



a) Determine the source impedance that would optimize the noise figure and calculate the resulting minimum noise factor.

b) Design an input matching network using 2.0 µm wide microstrip transmission line and stub to obtain an optimal low noise amplifier. Assume a dielectric spacer with dielectric constant of $\varepsilon_r = 3$ and thickness of 5.0 µm. (hint: Use a Smith chart)

c) As an alternative, you now have the freedom to design the width of the transmission line freely. Design a matching network using a $\frac{\lambda}{4}$ transformer and a reactive element in series. (hint: Use a Smith chart)

d) Which of these two networks is the most preferable? Motivate your answer.

Good luck!

Maximum score: 60 points