Written Examination EITP01 2020-01-09

Allowed on exam: Textbook, handwritten notes, formula collection, printouts, calculator

Not allowed on exam: Mobile phone, computer (or anything else with internet access), solutions to old exam problems

Useful constants:

$$\hbar = 1.055 \times 10^{-34}\ Js$$

$$k_B = 1.381 \times 10^{-23}\ J/K$$

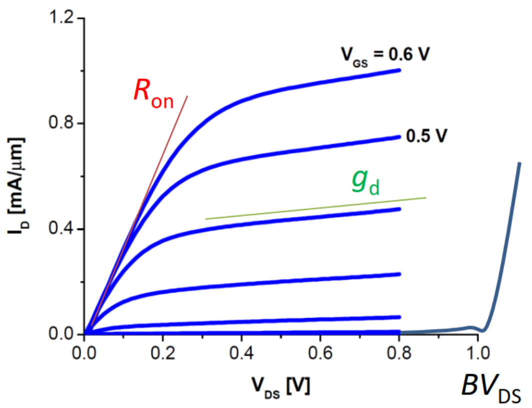
$$m_0 = 9.109 \times 10^{-31}\ kg$$

$$\varepsilon_0 = 8.85 \times 10^{-12}\ Fm^{-1}$$

$$e = q = 1.602 \times 10^{-19}\ C$$

$$c = 2.998 \times 10^{8}\ m/s$$

1. **Semiconductor Physics (10 p)**
   a) Under which circumstances is the Boltzmann approximation acceptable?
   b) E_F-E_C = 0.1 eV for a piece of Si and a piece of Ge. Which has the highest free electron concentration and how high is it?
   c) For a single sub-band the Density of States in two dimensions (D_{2D}) is constant. Derive the expression for D_{2D}.
2. **Ballistic Transistor (15 p)**
   a) For a quantum well FET, explain the origin of the semiconductor capacitance and the charge centroid capacitance.
   b) Calculate the total current through a single sub-band ballistic InAs QWFET in the linear regime, assuming E_{fs} - E(0) = 0.2 eV, E_{fs}-E_1 = 0.3 eV and V_{DS} = 0.15 eV, m* = 0.023m_0, W = 10 µm.
   c) In the output characteristics of the FET below one can identify R_{on}, g_d and BV_{DS}. Explain (1) the origin of these and (2) how and (3) why they are affected if the gate length L_G becomes very small.



   d) How does the current depend on L_G in a purely ballistic device, and how does this change if the transmission T < 1?

3. AC Transistor (20 p)

a) Assuming L_G >> λ, calculate the y-parameters for ω = 10 GHz in saturation for an InAs QW FET with 5 nm gate oxide ($\varepsilon_{ox} = 25$), L_G = 50 nm, t_w = 5 nm, $\varepsilon_s = 15$, W = 10 µm. Assume $C_{GG} = 10C_{GD}$ and g_m = 2 mS/µm = $10g_d$.

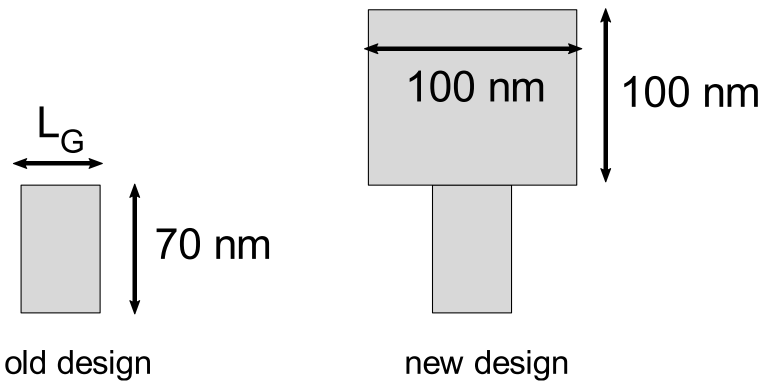
b) The y-parameters of an InAs QWFET biased in saturation with L_G = 60 nm >> λ, W = 10 µm are measured at f = 50 GHz to be

$$Y = \begin{bmatrix} 0.02 + j0.02 & -j0.002 \\ 0.03 & 0.006 \end{bmatrix}$$

Derive the hybrid-π model for the device and give values for all resistances/conductances and capacitances (i.e. C_{gs}, C_{gd}, C_{sd}, R_i, g_m and g_d).

c) If one wants to maximize f_T, which parameters should be targeted and how are these improved in practice?

d) A transistor with g_m = 2 mS/µm = $10g_d$, L_G = 50 nm, W = 10 µm and total C_{gs} = 2fF, C_{gd} = 1 fF, $R_S = R_D$ = 50 Ω starts out with a regular rectangular gate with $\rho = 15\ \mu\Omega cm$ obtains an improved T-gate design as shown below. The penalty is an additional parasitic $C_{gs,p}$ = $C_{gd,p}$ = 0.1 fF. How much (in percent) does f_{max} improve by the new design?
Hint: Use $R_G = \frac{1}{3} W\rho/A$ where A is the crossectional area of the gate.



4. **Amplifier Design (15 p)**

a) Given a unilateral transistor with g_m = 10 mS and C_{gg} = 5 fF and R_G = 50 Ω, $R_i = 1/(1.4g_m)$, calculate the optimal source impedance that minimizes the noise at f = 60 GHz. Also give the value of the minimal noise factor, NF. Assume $\gamma = 1$ for simplicity.

b) Given a transistor with measured S-parameters,

$$[S] = \begin{bmatrix} 0.7 + j0.03 & j0.2 \\ 1 & 0.7 + j0.1 \end{bmatrix}$$

check for stability and calculate the maximum gain for stable operation.

c) Design a matching network that conjugately matches the input of a transistor with Z_{in} = 50 + j25 Ω at f = 50 GHz to a 50 Ω source using a transmission line and a stub, assuming metal lines of 1 µm width and dielectric thickness of 2 µm, $\varepsilon_r = 3$.

d) Assuming that instead of the network in c) one could build a matching network using a $\lambda/4$ transformer and a stub, which would be preferable and why?

Good luck! Maximum score: 60p