Digitalteknik EITF65

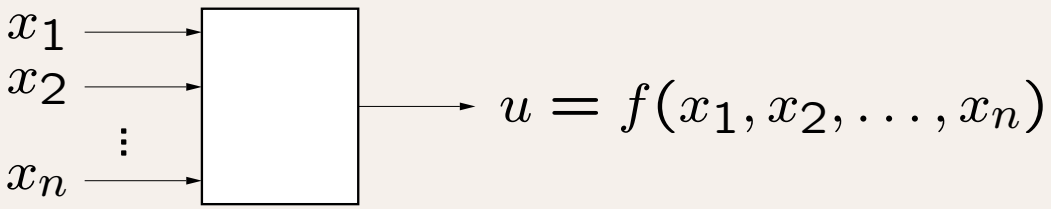
Lecture 3: Sequential Circuits

September 5, 2018

Boolean functions

Definition

A Boolean function is a mapping from n binary inputs $x_1, x_2, \ldots, x_n$ to one binary output u.



Four important Boolean functions are:

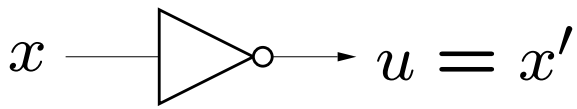
NOT, AND, OR and Modulo 2 adders.

NOT

The NOT gate, or inverter, gives the complement to the input x. It is denoted by

$$f_{\mathrm{NOT}}(x) = x'$$

x	u
0	1
1	0

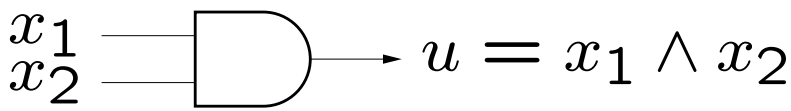


AND

The AND gate gives the output 1 when all inputs are 1. It is denoted by

$$f_{\mathrm{AND}}(x_1, x_2) = x_1 \wedge x_2$$

$x_1 x_2$	$x_1 \wedge x_2$
0 0	0
0 1	0
1 0	0
1 1	1



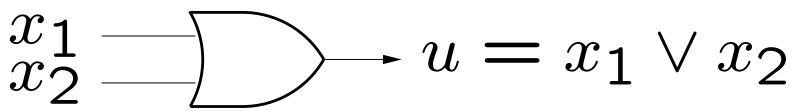
Note: We often omit the $\wedge$-sign in the expressions, cf. multiplication.

OR

The OR gate gives the output 1 when at least one of the inputs are 1. It is denoted by

$$f_{\mathrm{OR}}(x_1, x_2) = x_1 \vee x_2$$

$x_1 x_2$	$x_1 \vee x_2$
0 0	0
0 1	1
1 0	1
1 1	1

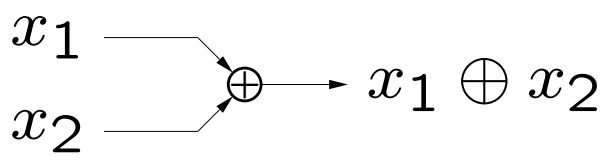


Modulo 2 adders (XOR)

The Modulo 2 adder gives the output 1 when the sum of the inputs is odd. It is denoted by

$$f_{\mathrm{M2A}}(x_1, x_2) = x_1 \oplus x_2$$

$x_1 x_2$	$x_1 \oplus x_2$
0 0	0
0 1	1
1 0	1
1 1	0



Combinational circuits

Definition

A **combinational circuits** is a circuit that consists of Boolean functions and no loops (feedback).

Majority function

Example

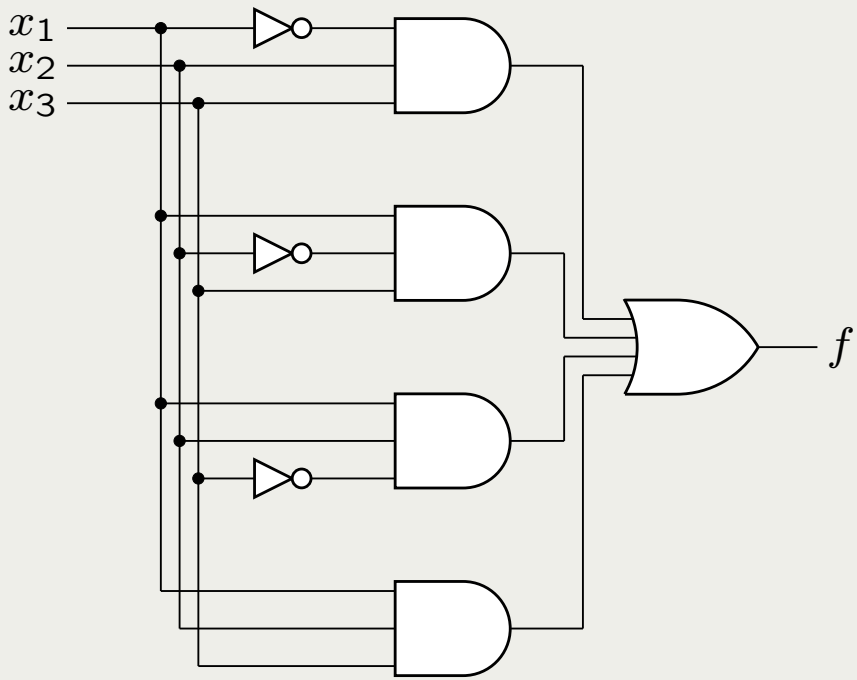
Let $f(x_1, x_2, x_3)$ be the majority function. Then

$x_1x_2x_3$	f	A $x_1'x_2x_3$	B $x_1x_2'x_3$	C $x_1x_2x_3'$	D $x_1x_2x_3$	$A \vee B \vee C \vee D$
0 0 0	0	0	0	0	0	0
0 0 1	0	0	0	0	0	0
0 1 0	0	0	0	0	0	0
0 1 1	1	1	0	0	0	1
1 0 0	0	0	0	0	0	0
1 0 1	1	0	1	0	0	1
1 1 0	1	0	0	1	0	1
1 1 1	1	0	0	0	1	1

Majority function (realisation)

Example (cont'd)

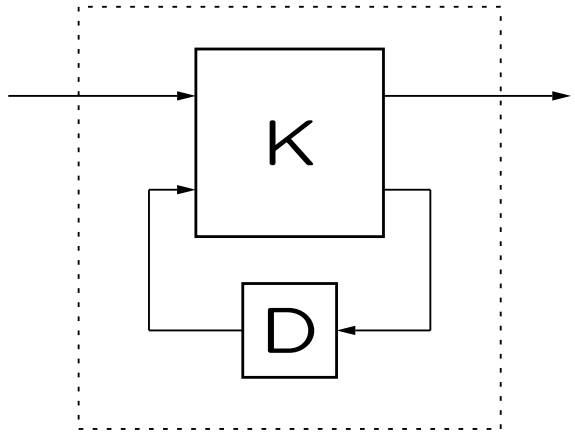
$$f(x_1, x_2, x_3) = x_1' x_2 x_3 \vee x_1 x_2' x_3 \vee x_1 x_2 x_3' \vee x_1 x_2 x_3$$



Sequential circuits

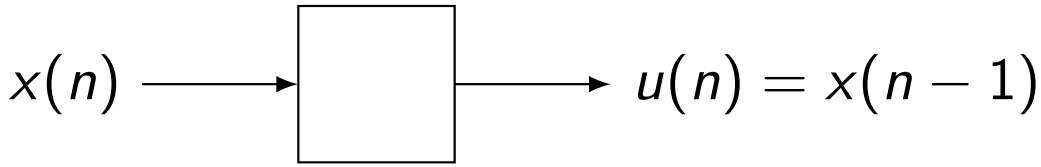
The behaviour of a graph can be realised by a sequential circuit. For that we need two kind of components,

- Delay elements or D-elements. These realise the memory of the system (the state).
- Boolean functions. They realise the output function and the state transition function.

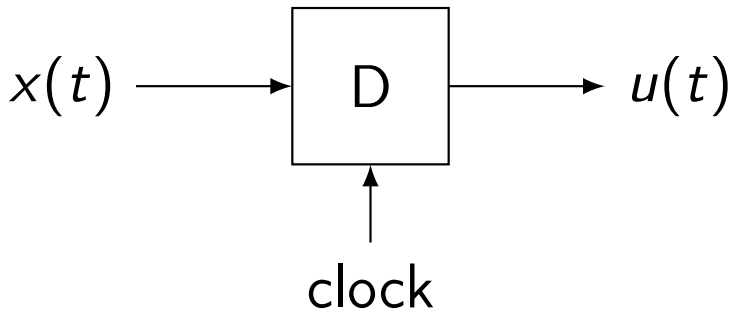


Delay element

A delay element has one input and one output. The output is the input delayed one time unit, $u(n) = x(n-1)$.



The output from a *D*-flip flop is updated (to the value of the input) at a specific occasion given by the clock signal.

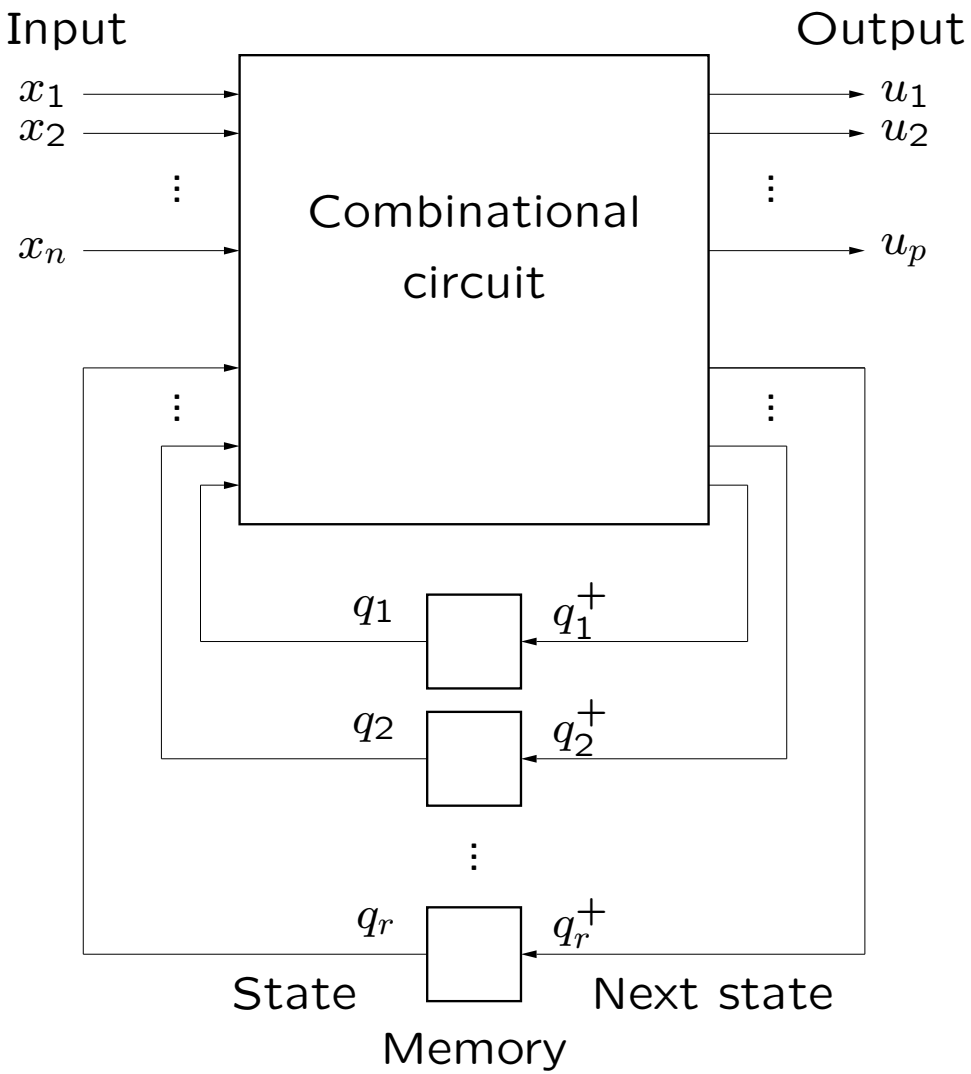


Sequential circuits

Definition

A **sequential circuit** is a circuit that contain feedback (via delay elements) with a well defined behaviour.

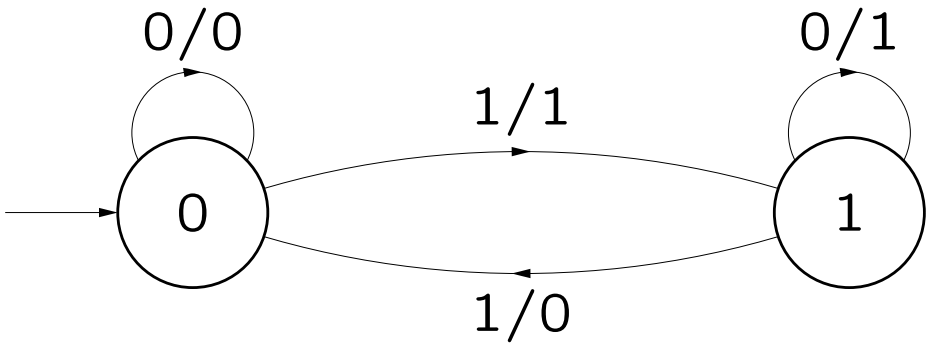
Sequential circuit (canonical form)



Parity check

Example 2.13

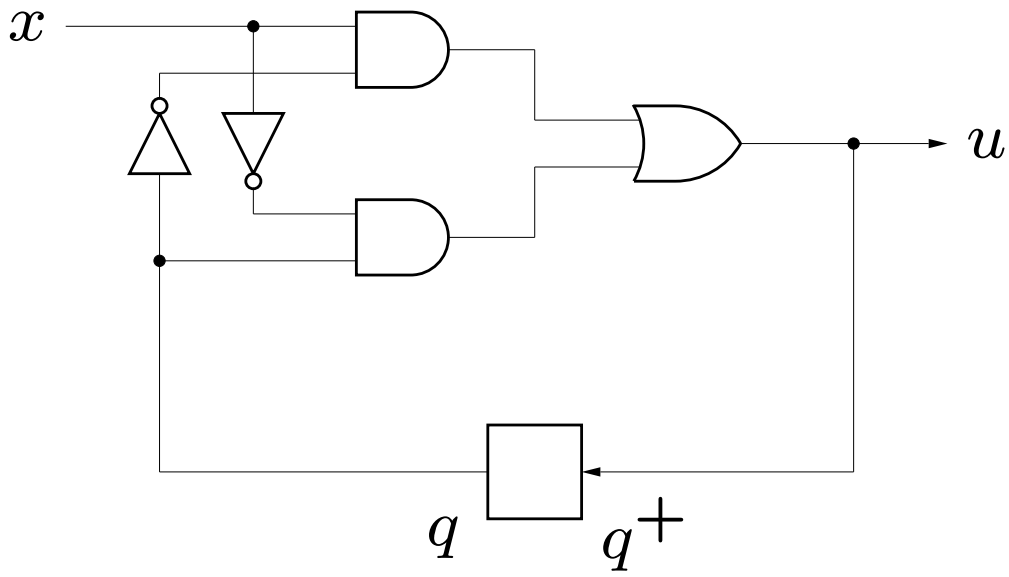
Construct a circuit that gives as output the parity symbol (modulo 2 sum) of the received sequence.



qx	q^+u
00	0 0
01	1 1
10	1 1
11	0 0

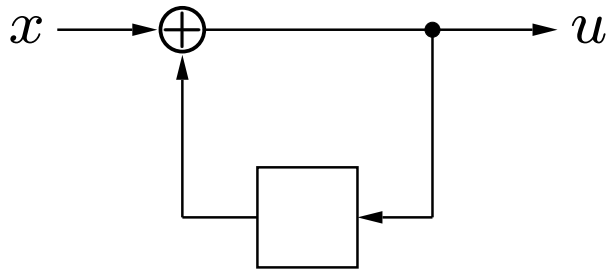
Parity check (cont'd)

$$q^+ = q'x \vee qx'$$
$$u = q'x \vee qx'$$



Alternative solution

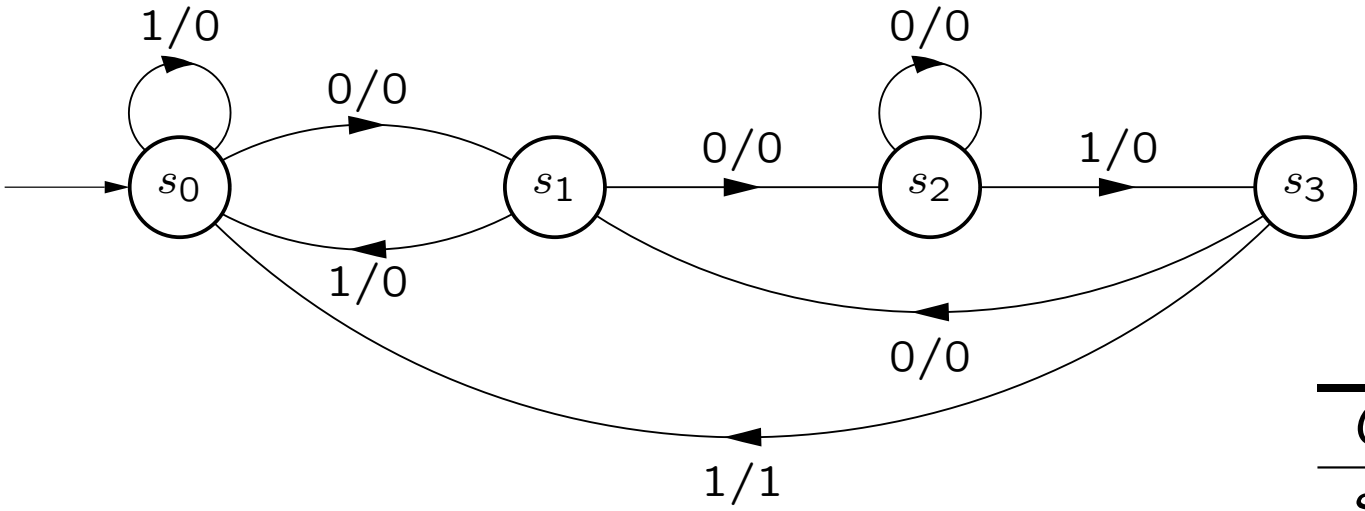
$$q^+ = q \oplus x$$
$$u = q \oplus x$$



Detector

Example 2.14

Realise a detector for the bit pattern 0011.



Q	$q_1\,q_2$
s_0	0 0
s_1	0 1
s_2	1 0
s_3	1 1

Detector

The combinational circuit must realise the following tabular.

$q_1\,q_2\,x$	$q_1^+\,q_2^+\,u$
0 0 0	0 1 0
0 0 1	0 0 0
0 1 0	1 0 0
0 1 1	0 0 0
1 0 0	1 0 0
1 0 1	1 1 0
1 1 0	0 1 0
1 1 1	0 0 1

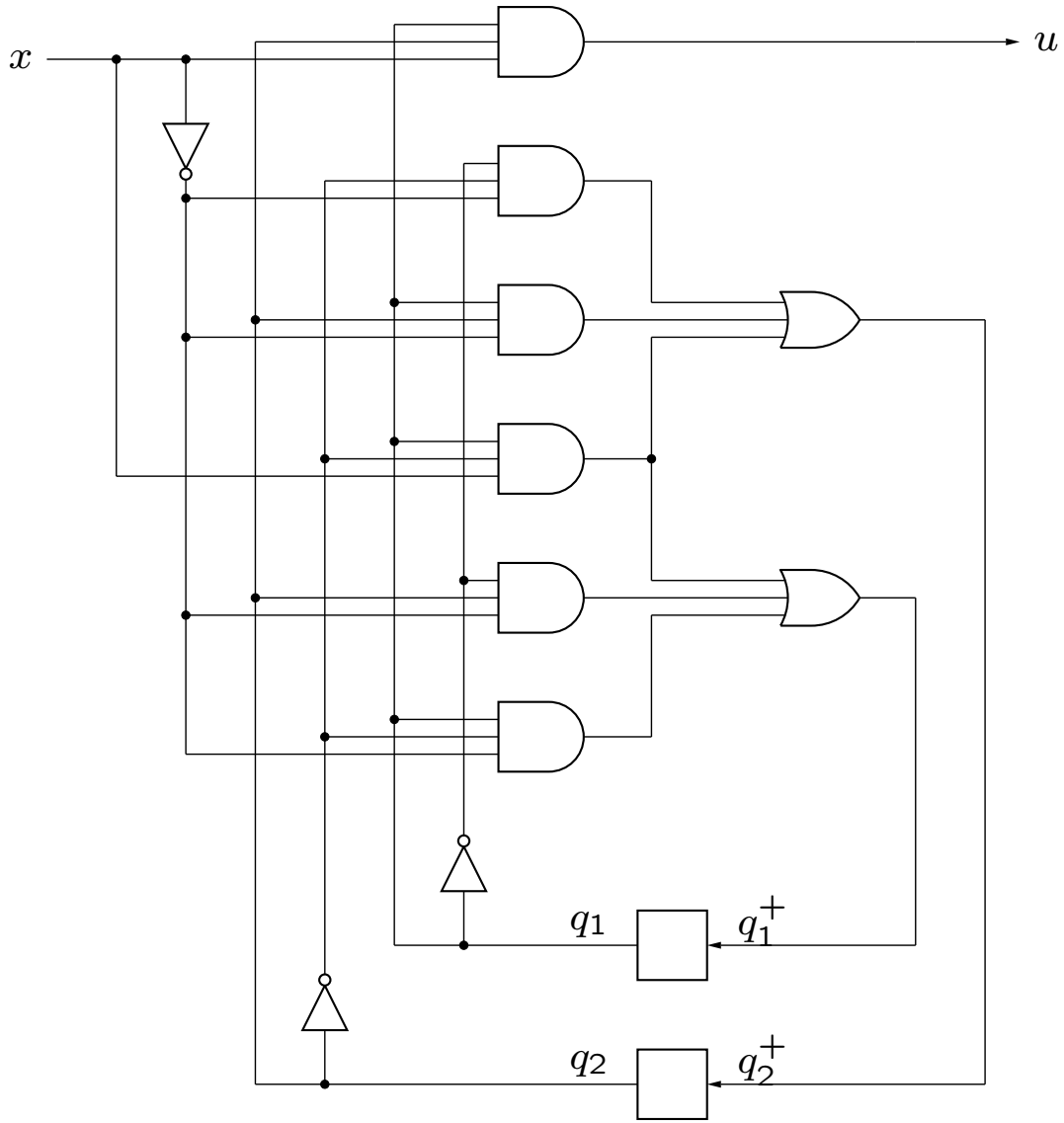
This can be done with:

$$q_1^+ = q_1' q_2 x' \vee q_1 q_2' x' \vee \underline{q_1 q_2' x}$$

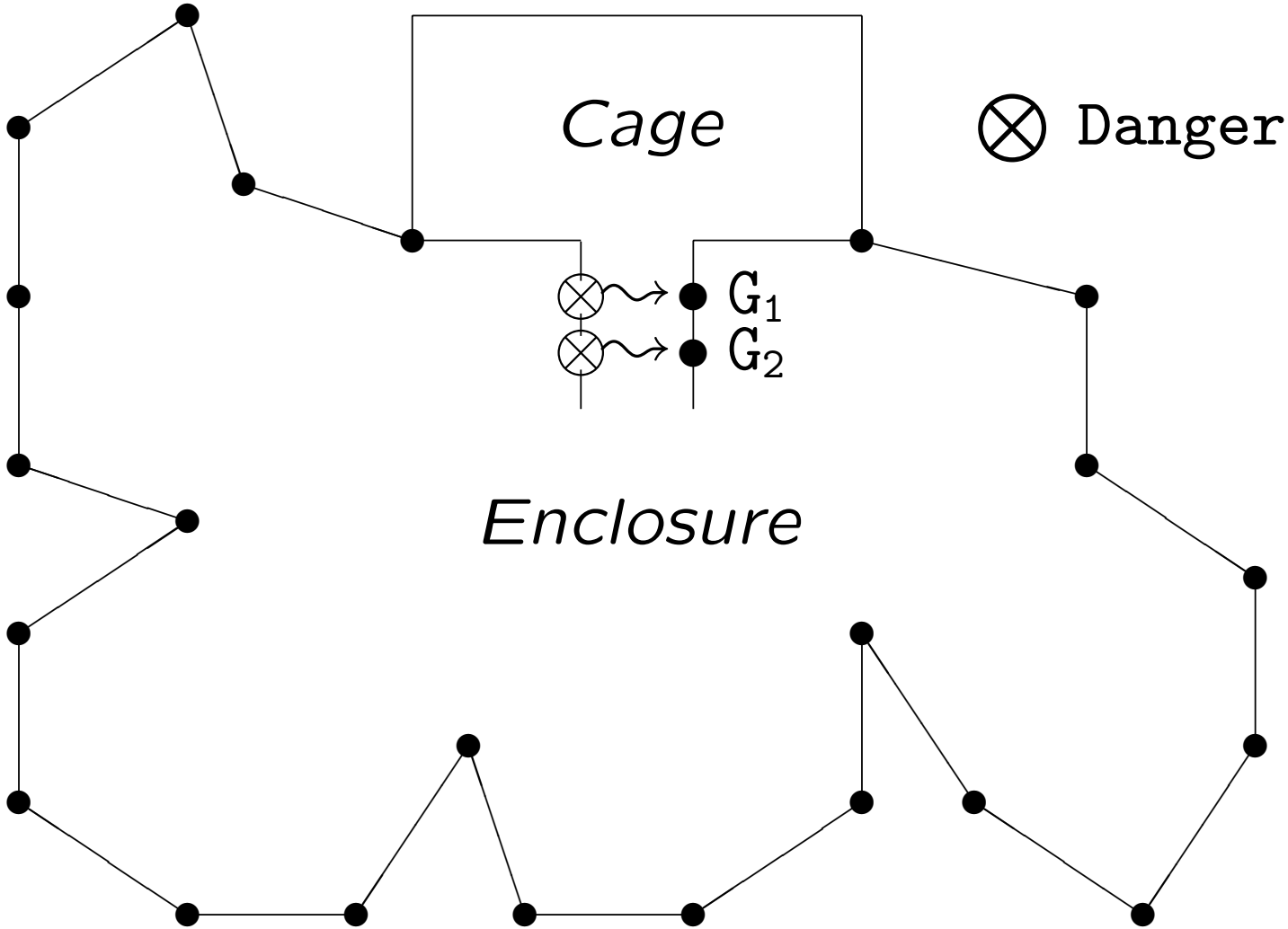
$$q_2^+ = q_1' q_2' x' \vee \underline{q_1 q_2' x} \vee q_1 q_2 x'$$

$$u = q_1 q_2 x$$

Detector (realisation)



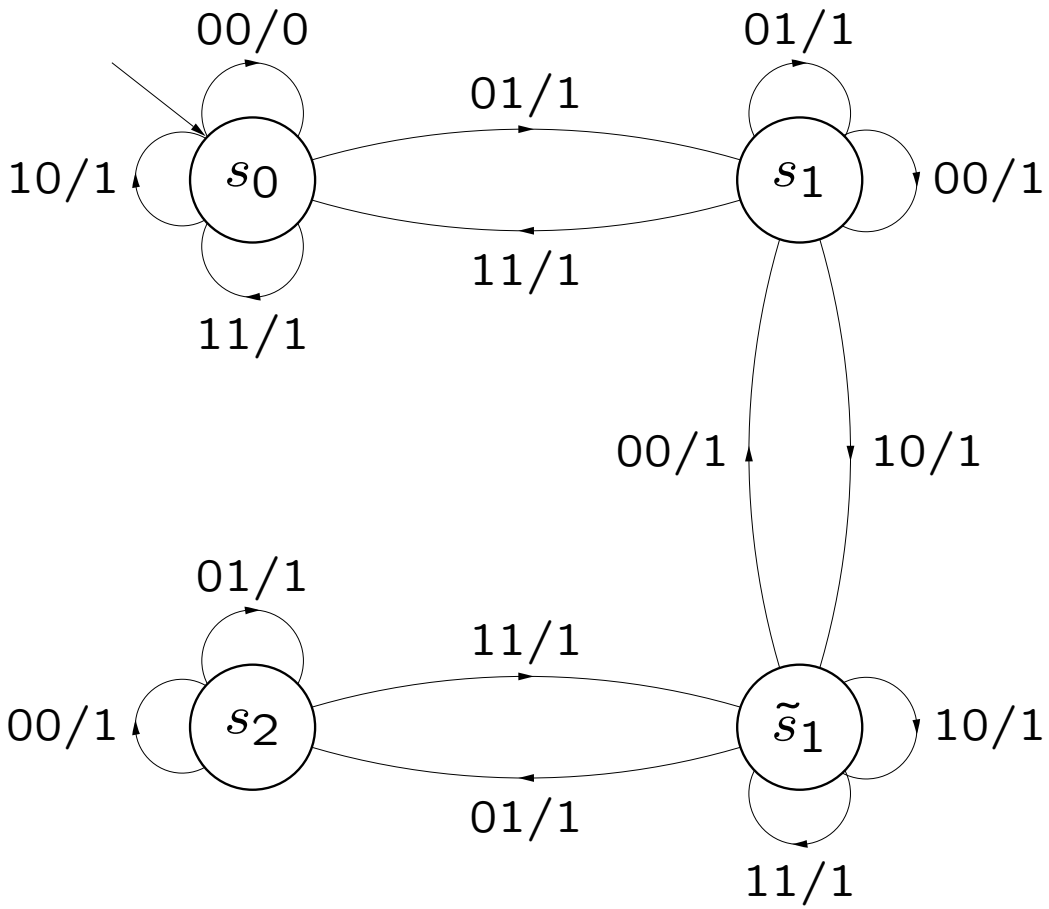
The lion threat (figure)



Lion threat

Example Lion Threat

Realise the lion threat problem for two lions.



$\mathcal{S}$	$q_1 q_2$
s_0	0 0
s_1	0 1
$\tilde{s}_1$	1 1
s_2	1 0

Lion threat (truth table)

$q_1\,q_2$	$G_1\,G_2$	$q_1^+\,q_2^+$	Danger
0 0	0 0	0 0	0
0 0	0 1	0 1	1
0 0	1 0	0 0	1
0 0	1 1	0 0	1
0 1	0 0	0 1	1
0 1	0 1	0 1	1
0 1	1 0	1 1	1
0 1	1 1	0 0	1
1 0	0 0	1 0	1
1 0	0 1	1 0	1
1 0	1 0	- -	-
1 0	1 1	1 1	1
1 1	0 0	0 1	1
1 1	0 1	1 0	1
1 1	1 0	1 1	1
1 1	1 1	1 1	1

Lion threat (functions)

Realisation:

$$q_1^+ = q_1' q_2 G_1 G_2' \vee q_1 q_2' G_1' G_2' \vee q_1 q_2' G_1' G_2 \vee q_1 q_2' G_1 G_2 \vee q_1 q_2 G_1' G_2 \vee q_1 q_2 G_1 G_2' \vee q_1 q_2 G_1 G_2$$

$$q_2^+ = q_1' q_2' G_1' G_2 \vee q_1' q_2 G_1' G_2' \vee q_1' q_2 G_1' G_2 \vee q_1' q_2 G_1 G_2' \vee q_1 q_2' G_1 G_2 \vee q_1 q_2 G_1' G_2' \vee q_1 q_2 G_1 G_2' \vee q_1 q_2 G_1 G_2$$

$$\texttt{Danger} = (q_1' q_2' G_1' G_2')' = q_1 \vee q_2 \vee G_1 \vee G_2$$

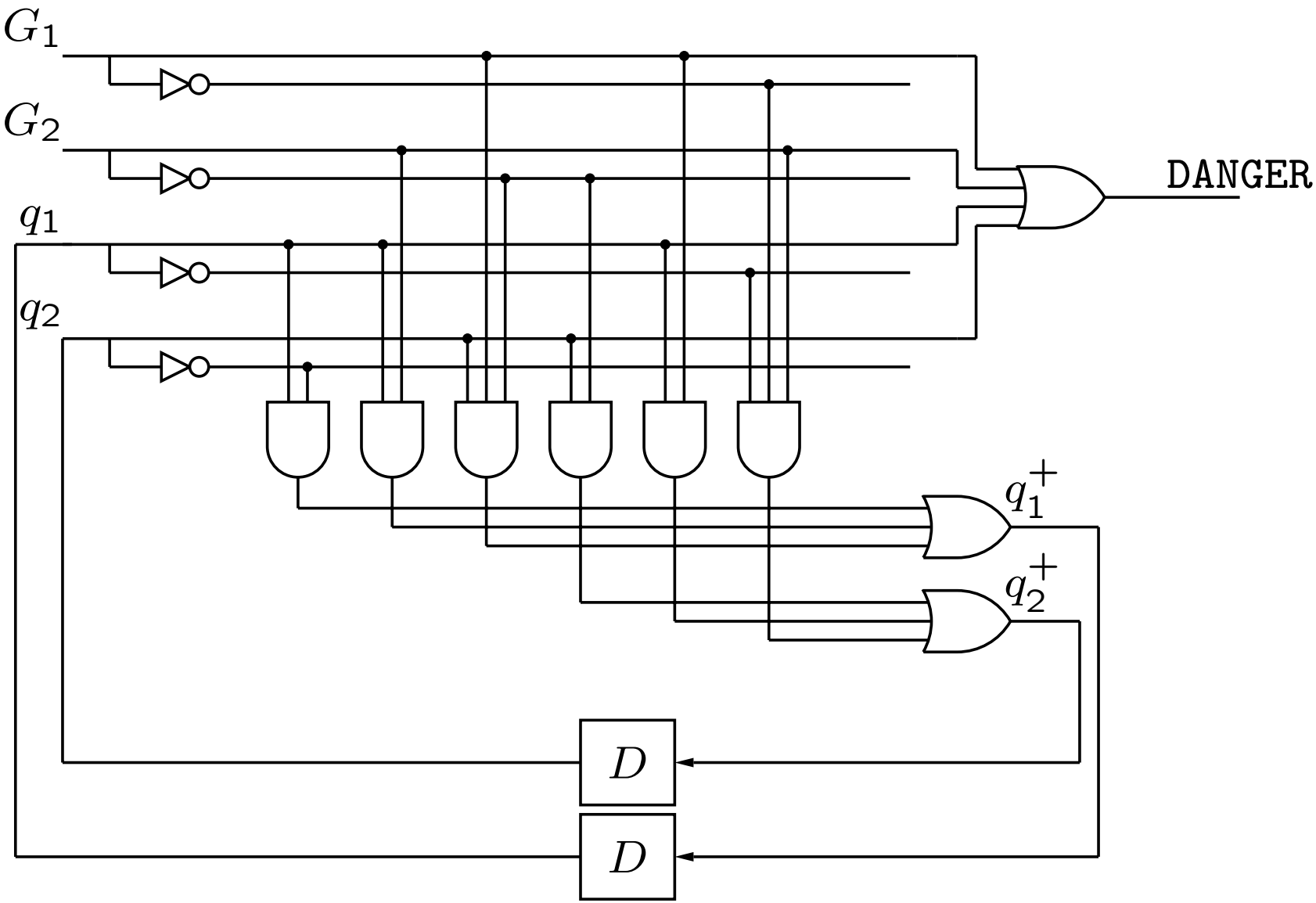
Alternative (minimal) realisation:

$$q_1^+ = q_1 q_2' \vee q_1 G_2 \vee q_2 G_1 G_2'$$

$$q_2^+ = q_2 G_2' \vee q_1 G_1 \vee q_1' G_1' G_2$$

$$\texttt{Danger} = q_1 \vee q_2 \vee G_1 \vee G_2$$

Lion threat (realisation)



Problems to solve

Combinational circuits

- Find smaller (minimal) solutions.
- Mathematical meaning of $\wedge$, $\vee$, $'$, and $\oplus$?
- Representation of functions.

Sequential circuits

- Small realisations?
- Graphs with few states.
- Assignment of states.
- Other types of graphs.
- Linear systems.