Digitalteknik EITF65

Lecture 12: Programmable Logic
Standard Components
CMOS Realizations

August 27, 2020

PLA

Programmable Logic Array

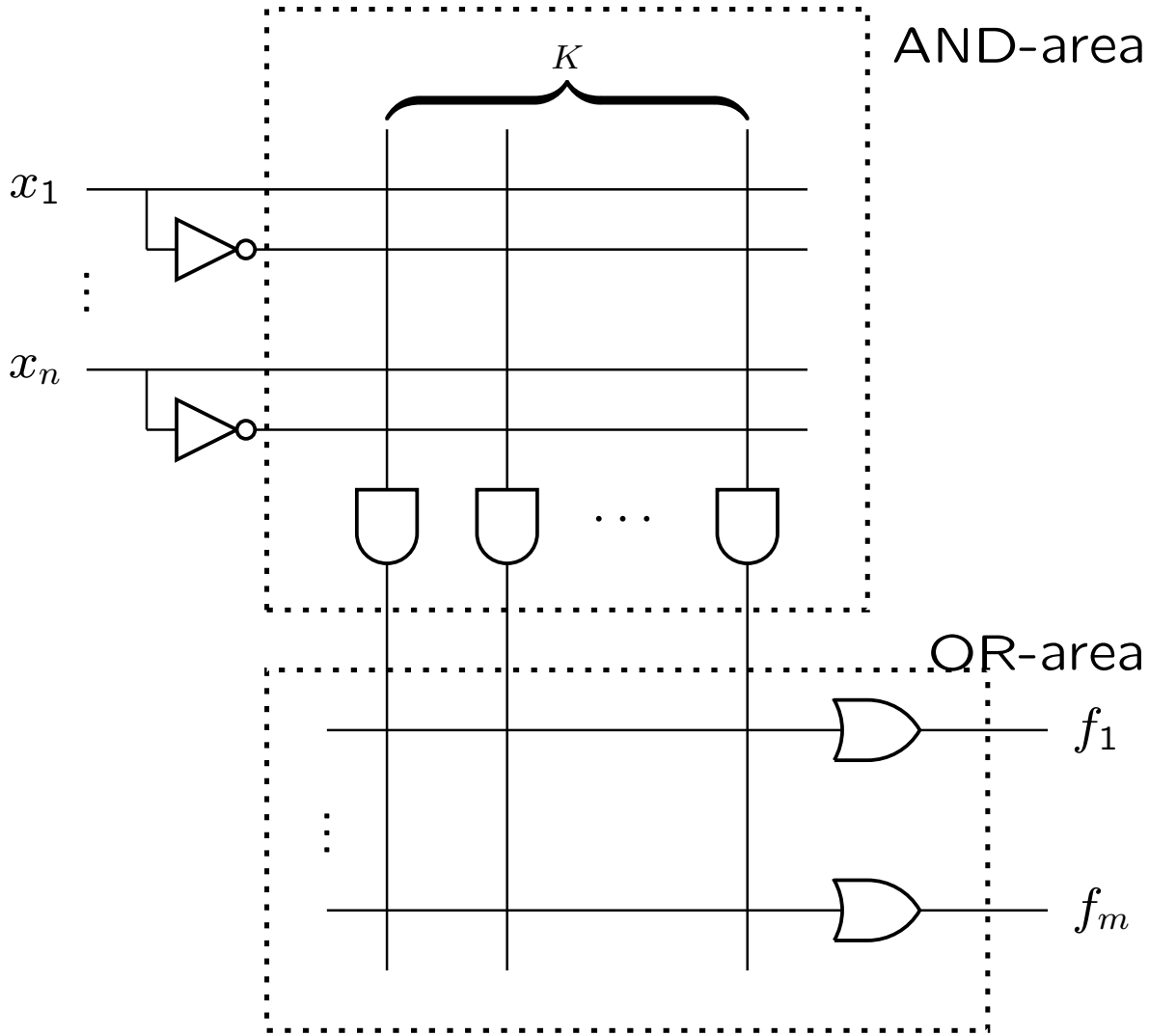
A PLA (Programmable Logic Array) is a programmable circuit containing a two layer circuit with

- n inputs and m outputs
- one AND area
- one OR area

The number of implicants is a measure of the size.

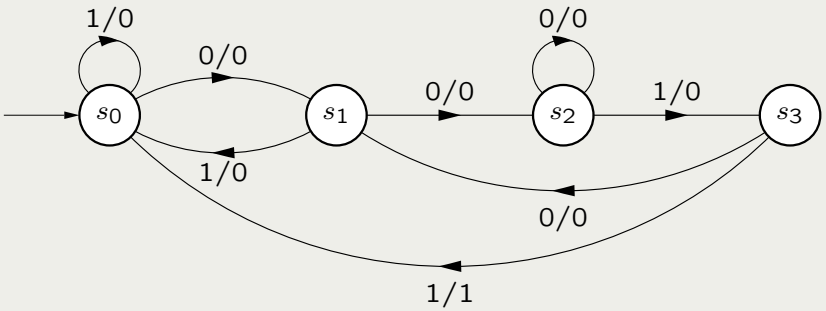
Mark the connections with a *plopp* (•)

PLA



PLA Ex

Example: Detector (NBCD)



Assignment:

s	$q_0 q_1$
s_0	00
s_1	01
s_2	10
s_3	11

Karnaugh maps:

q_1^+	$x=0$	$x=1$
00	0	0
01	1	0
11	0	0
10	1	1

q_2^+	$x=0$	$x=1$
00	1	0
01	0	0
11	1	0
10	0	1

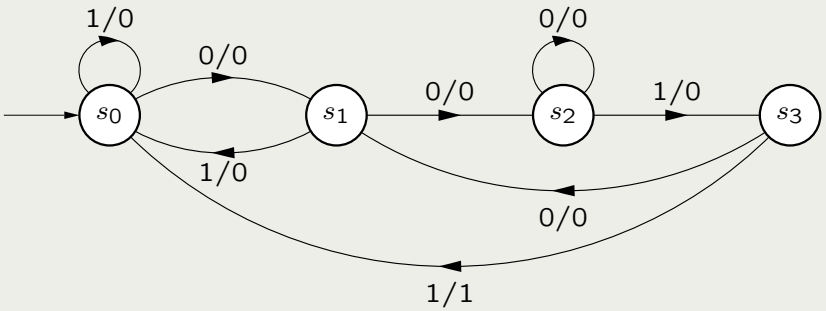
u	$x=0$	$x=1$
00	0	0
01	0	0
11	0	1
10	0	0

Minimal functions:

$$u = q_1 q_2 x$$
$$q_1^+ = q_1 q_2' \vee q_1' q_2 x'$$
$$q_2^+ = q_1' q_2' x' \vee q_1 q_2 x' \vee q_1 q_2' x$$

PLA Ex

Example: Detector (Gray)



Assignment:

s	$q_0 q_1$
s_0	00
s_1	01
s_2	11
s_3	10

Karnaugh maps:

q_1^+	0	1
00	0	0
01	1	0
11	1	1
10	0	0

($q_1 q_2$ rows, x columns)

q_2^+	0	1
00	1	0
01	1	0
11	1	0
10	1	0

($q_1 q_2$ rows, x columns)

u	0	1
00	0	0
01	0	0
11	0	0
10	0	1

($q_1 q_2$ rows, x columns)

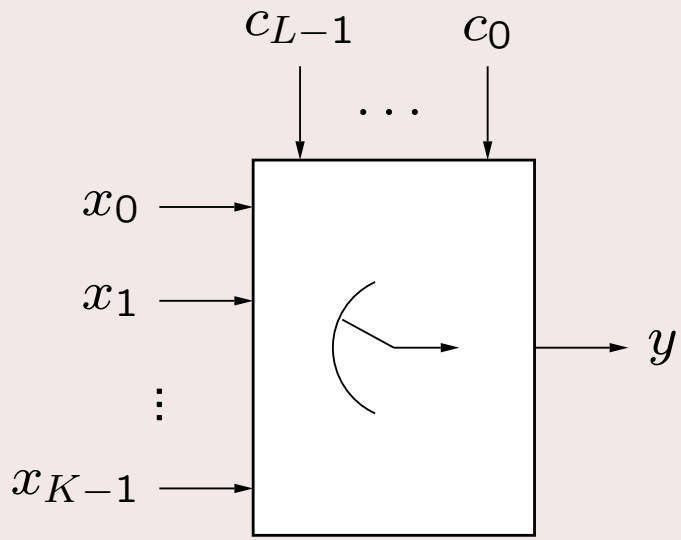
Minimal functions:

$$u = q_1 q_2' x$$
$$q_1^+ = q_2 x' \vee q_1 q_2$$
$$q_2^+ = x'$$

Multiplexer (Dataväljare)

MUX

A multiplexer, or switch, is a circuit where L bits choose one of $K = 2^L$ inputs.



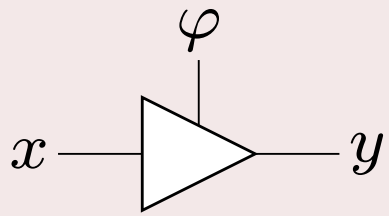
The output is given by

$$y = x_{\phi(c_{L-1},\ldots,c_0)}$$

Tri-state

Tri-state

A tri-state buffer is a buffer with a control signal φ. If $\varphi = 1$ the buffer is active, otherwise the output is high impedance (disconnected).

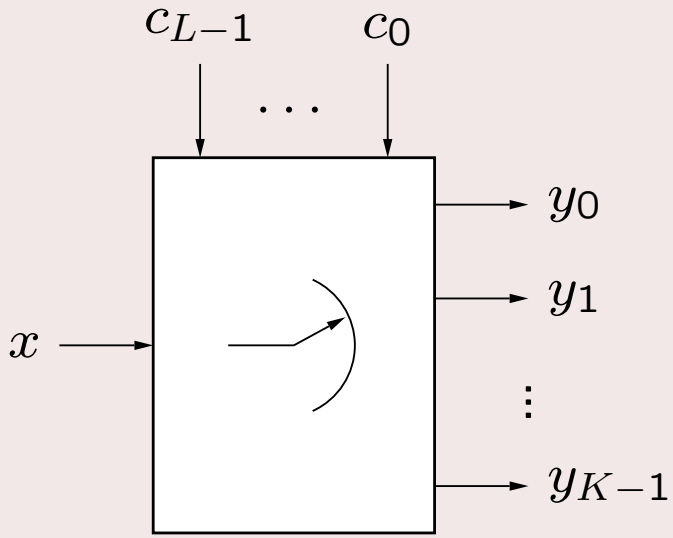


x	φ	y
–	0	High impedance
0	1	0
1	1	1

Demultiplexer (Avkodare)

DeMUX

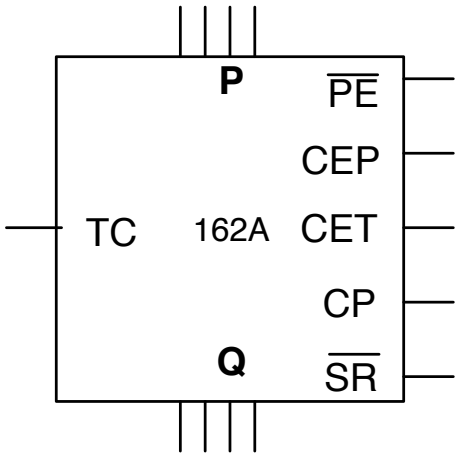
A demultiplexer, or decoder, is a circuit where L bits choose one of $K = 2^L$ outputs.



The output is given by

$$y_i = \begin{cases} x, & \text{if } \phi(c_{L-1}, \ldots, c_0) = i \\ 0, & \text{o.w.} \end{cases}$$

Counter 74LS162A



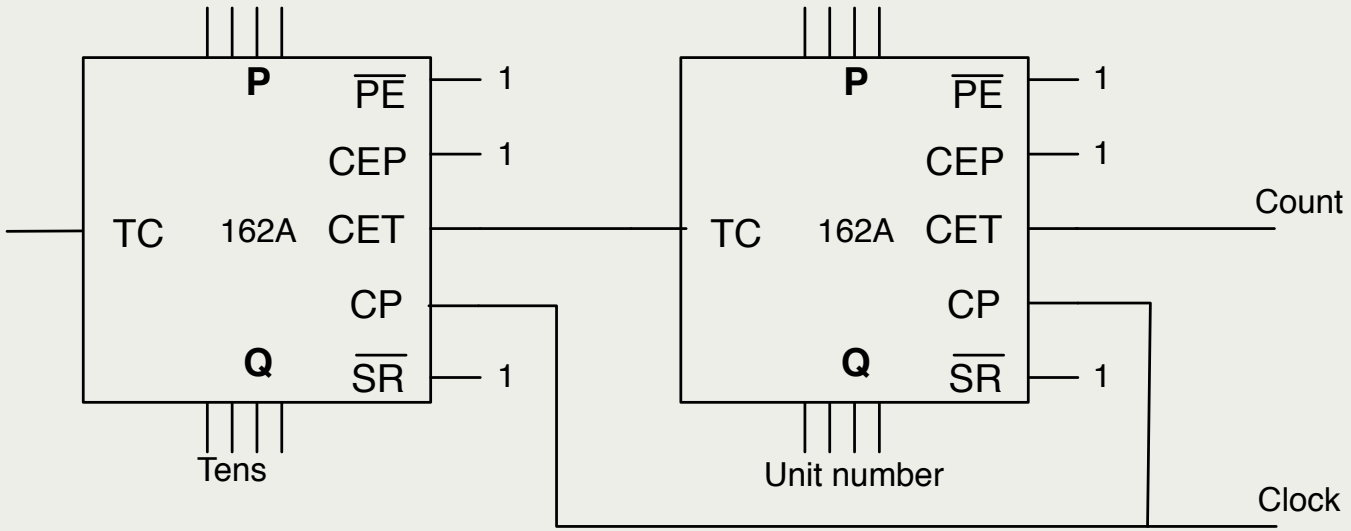
Pins	Action
$\mathbf{P} = P_3 - P_0$	Parallel input
$\mathbf{Q} = Q_3 - Q_0$	Parallel output; The state
$\overline{\mathrm{SR}}$	Synchronous reset, active low $Q \leftarrow 0$
$\overline{\mathrm{PE}}$	Parallel enable (Load), active low $Q \leftarrow P$
CEP	Count enable
CET	Count enable
TC	Terminal count output, $\mathrm{TC} = \mathrm{CET} \wedge Q_3 \wedge Q_2' \wedge Q_1' \wedge Q_0$ Used for cascading counters
CP	Clock

Counter 74LS162A

Example: Cascade

Since $\mathrm{TC} = 1$ when $\mathbf{Q} = 9$ and $\mathrm{CET} = 1$, this can be used to cascade several counters.

To build a modulo 100 counter cascade two modulo 10:



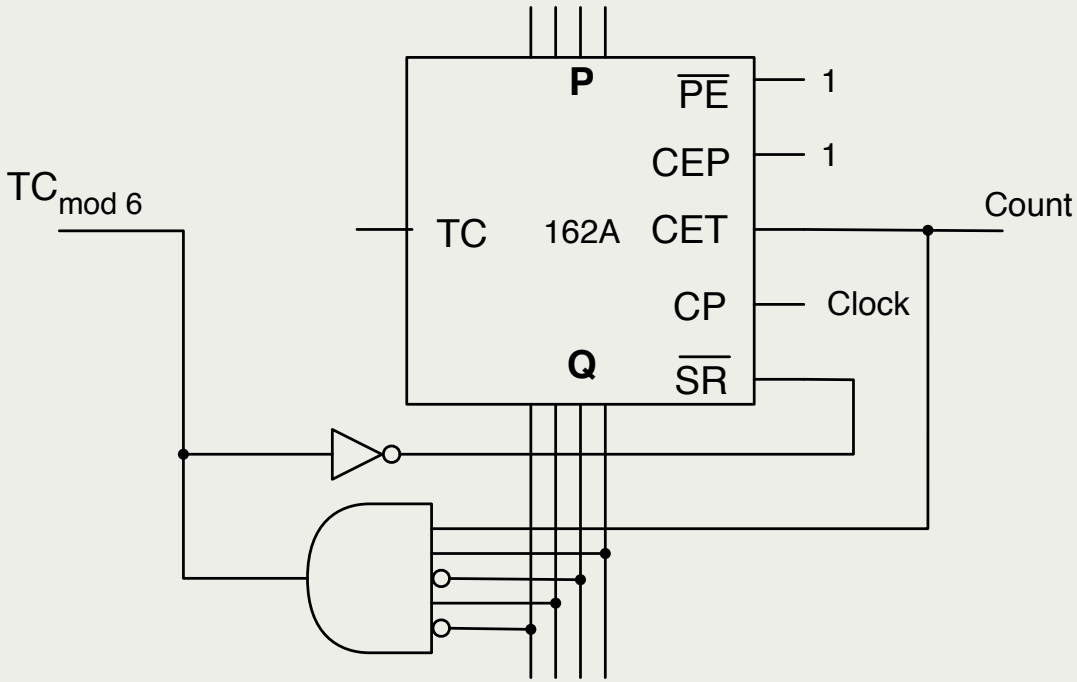
Counter 74LS162A

Example: Modulo 6 counter (Alt 1)

Construct a modulo 6 counter.

When $Q = 5$ and $\mathrm{CET} = 1 \Rightarrow \overline{\mathrm{SR}} = 0$ (Reset to zero).

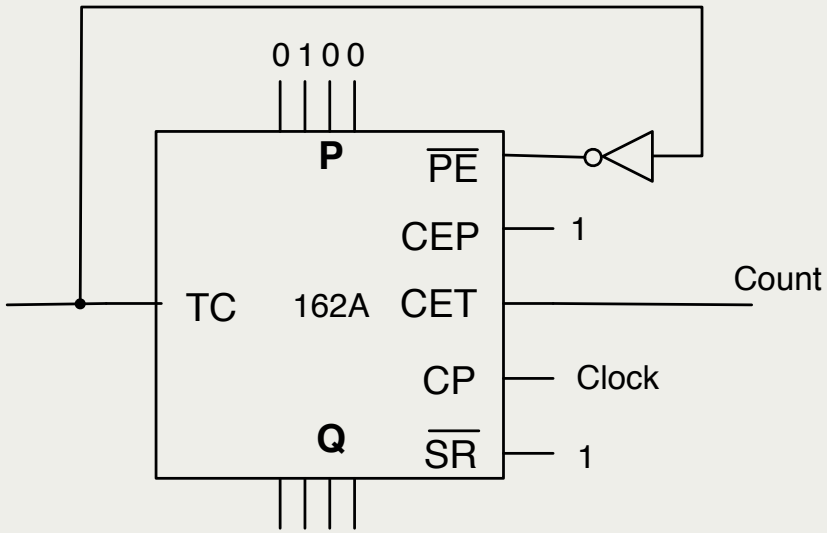
The new TC: $\mathrm{TC}_{\mathrm{mod6}} = Q_3' \wedge Q_2 \wedge Q_1' \wedge Q_0 \wedge \mathrm{CET}$



Counter 74LS162A

Example: Modulo 6 counter (Alt 2)

If the value of **Q** not important.
Use that $Q = 9$ and $\mathrm{CET} = 1 \Rightarrow \mathrm{TC} = 1$,
Then load $Q \leftarrow 10 - 6 = 4$.



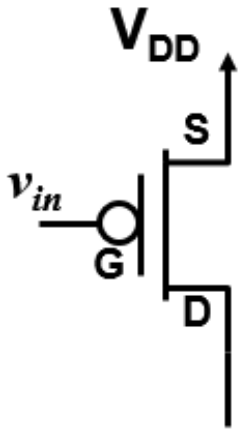
CMOS

- MOS: Metal Oxide Semiconductor (also MOSFET)
- CMOS: Complementary Metal Oxide Semiconductor
- CMOS was patented in 1963
- One of several ways to build digital circuits
- Attractive properties
  - Noise resistant
  - Very low static power consumption
  - Can fit into small area

CMOS, P-type and N-type

P-type

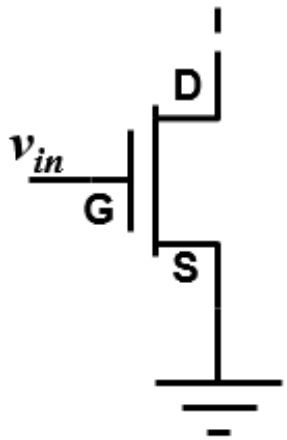
- Must have source connected to either V_{DD} or another P-type MOSFET
- Low resistance (conducting) between source (S) and drain (D) when input is low (0)
- High resistance between source and drain when input is high (1)
- Model as switch: Closed when gate (G) is low, open when gate is high



CMOS, P-type and N-type

N-type

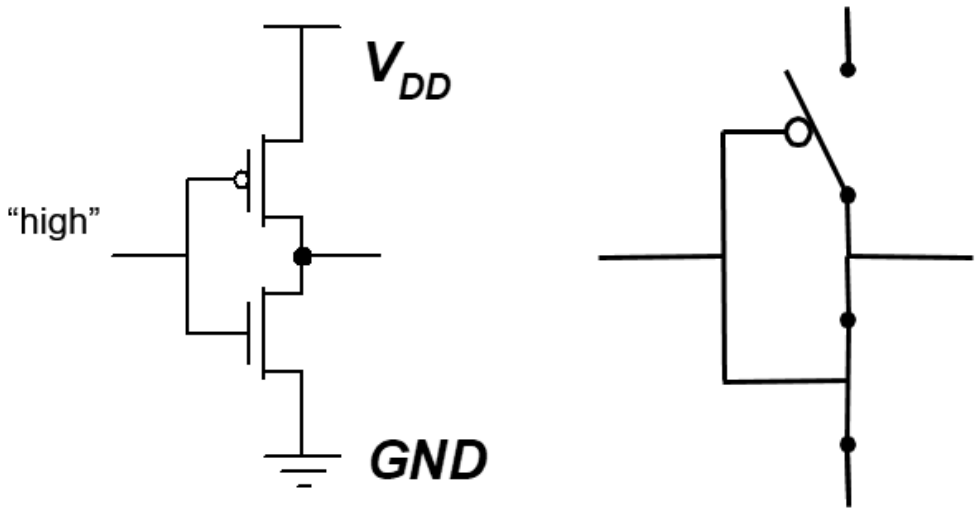
- Must have source connected to either GND or another N-type MOSFET
- High resistance between source (S) and drain (D) when input is low (0)
- Low resistance (conducting) between source and drain when input is high (1)
- Model as switch: Closed when gate (G) is high, open when gate is low



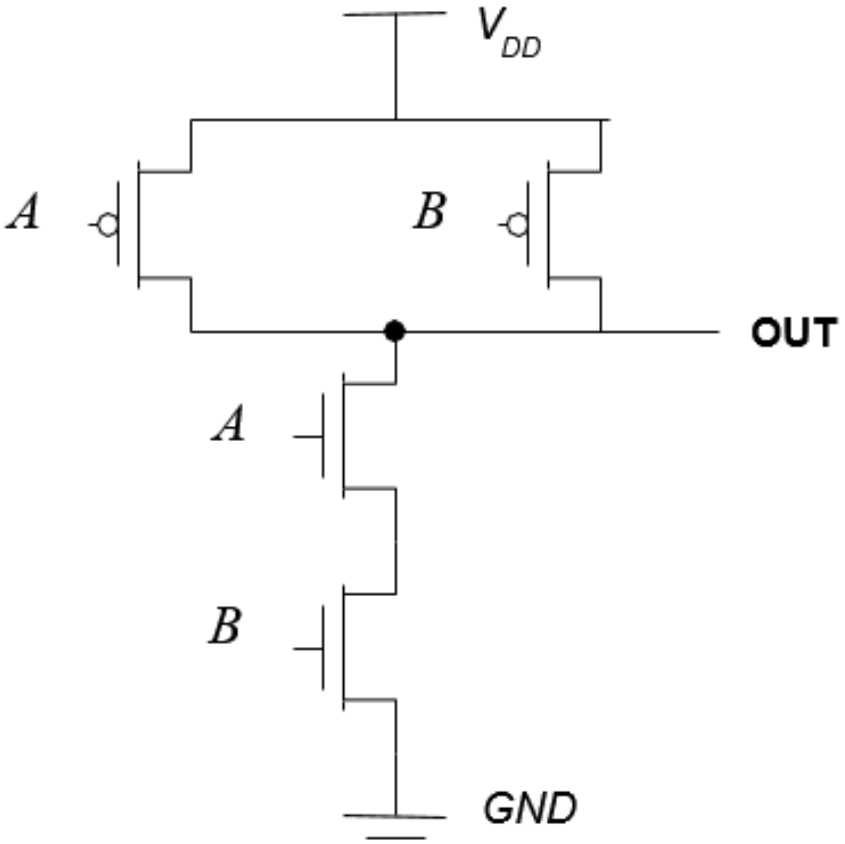
CMOS, Complementary design

- For each N-type, complement with a P-type transistor
- Connect input to gate of both transistors

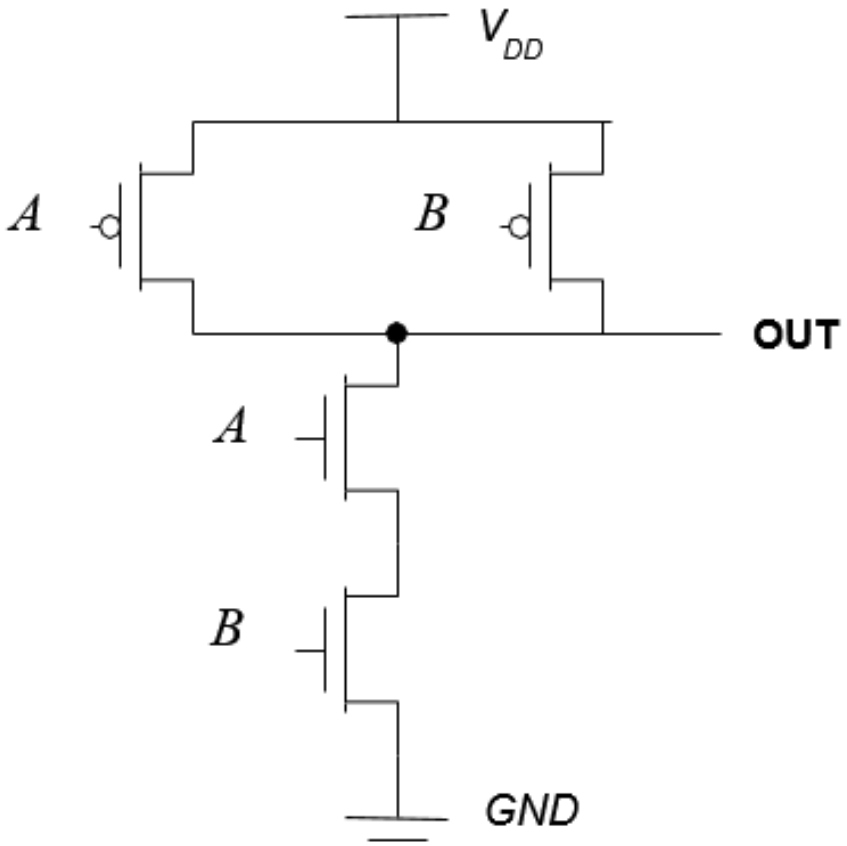
$\Rightarrow$ Only one is open at a time $\Rightarrow$ Very low power consumption when state is not switching



CMOS, Gate



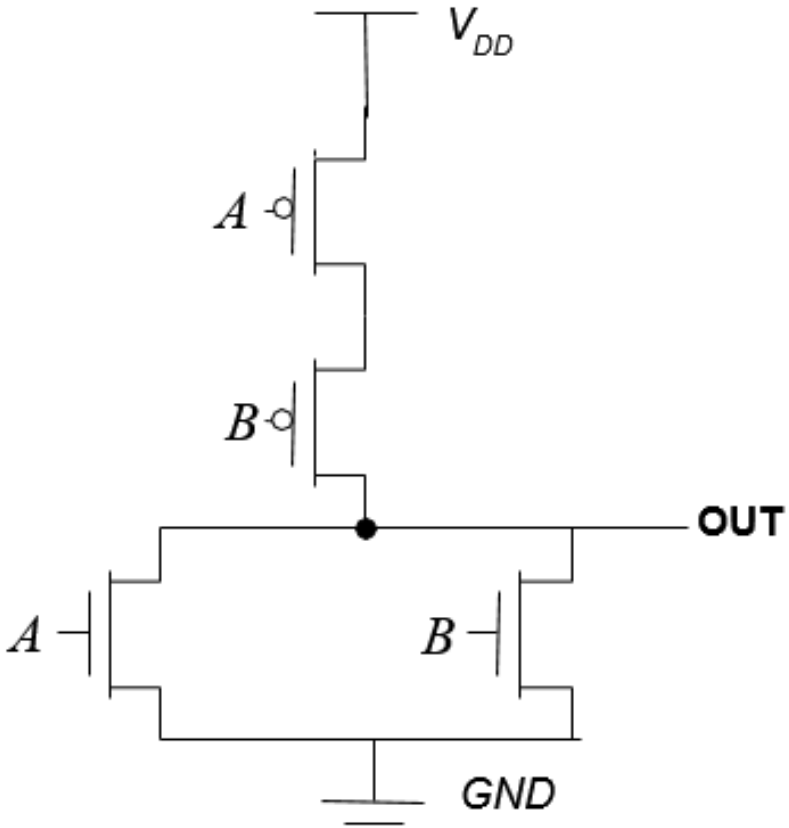
CMOS, Gate



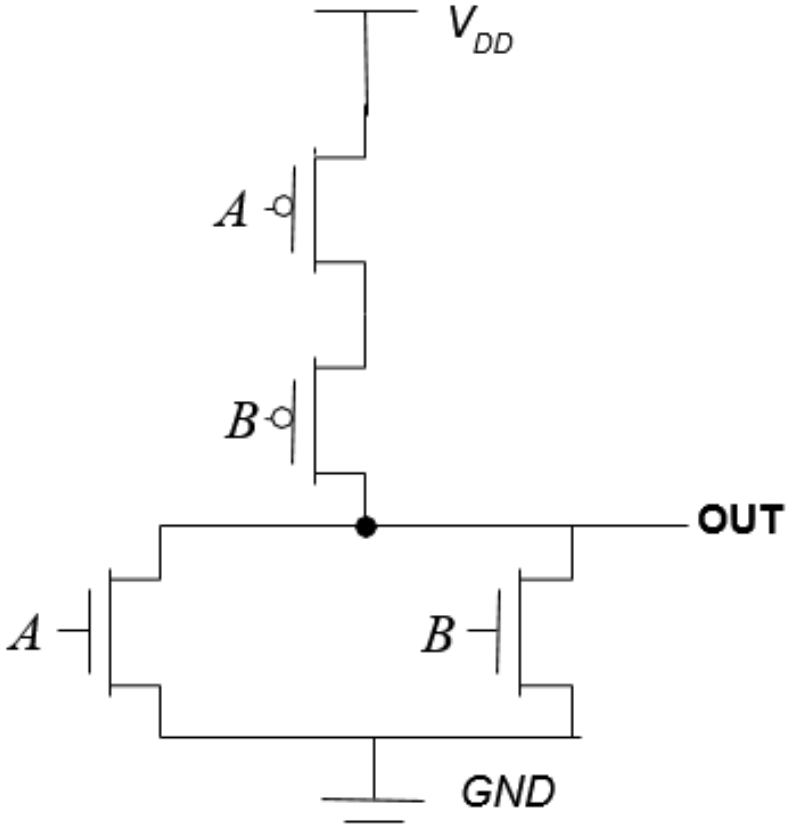
AB	OUT
0 0	1
0 1	1
1 0	1
1 1	0

NAND gate

CMOS, Gate



CMOS, Gate



AB	OUT
0 0	1
0 1	0
1 0	0
1 1	0

NOR gate

CMOS, Design

Basic design rules (informal)

- For each input combination, there must be a path between OUT and either V_{DD} or GND.
- For each input combination, there must not be a short circuit between V_{DD} and GND.

If N-type are in series, then P-type must be in parallel. And vice versa.