LUNDS UNIVERSITET

Design of Digital Circuits, 2017

EITF65, 9 credits (hp)

The objective of the course is to describe structured methods for construction of digital circuits, based on the concept of state transition graphs. The state transition graph is a powerful tool when building a model of the system. This model can then be realised by a sequential machine, which is a realisation with logic components and delay elements. It is central to the course to understand the concept of state transition graphs, and to understand how different methods can be applied in the realisation chain so the resulting circuit has few gates, which leads to a small hardware.

The course consists of 42 hours of lecture, 42 hours of problem solving classes, and 24 hours of laboratory lessons.

Scheduled time In the first study period there are two lectures each week and in the second period there is one lecture each week. The lecturer is Thomas Johansson (`thomas@eit.lth.se`).

For each lecture there is a problem solving class (övning), where problems connected to the lecture are solved. The teaching assistants are Linus Karlsson and Erik MÃěrtensson.

There are scheduled six laboratory lessons (four hours each) in the course. The first two in study period one (week 3-4 and 6) and the remaining four in study period two (week 2, 3, 4, and 5). Connected to each laboratory there are home problems that should be solved in advance. Andreas Johansson is in charge of everything connected to the laboratory part of the course.

Registration All students must be registered in LADOK. The first two weeks there will be a list circulated. If you do not have possibility to attend the lectures, please send an e-mail with your name, date of birth, and programme.

Web All information will be published on `www.eit.lth.se/course/eitf65`. The site will be updated continuously during the course.

Literature The literature is sold by KFS

- Rolf Johannesson and Ben Smeets: *Design of Digital Circuits - A Systems Approach*
- *Laborationer i Digitalteknik*
- *Solutions to Selected Problems*

Exam The next written exam is scheduled to Wednesday January 3, 14-19, in MA 10. Previous exams will be distributed on the web site.

Preliminary plan of the lectures

Study period 1

Lecture	**Part**	**Topic**
Lectures 1-3	Chapter 2	Introduction to digital systems, finite state machines, and sequential circuits
Lectures 4-6	Chapter 3	Discrete Mathematics (Rings and Boolean algebra)
Lectures 7-10	Chapters 4-5	Boolean functions (normal forms, minimizing, aritmethics)
Lectures 11-13	Chapter 6	State minimisation, assignment, and asynchronous sequential circuits
Lecture 14	Section 5.4	Standard components
Lectures 15-18	not in the textbook, notes will be distributed	Modern design of digital systems (transistor-level, FPGA development tools, the VHDL language
Lectures 19-20	Chapter 7	Linear sequential circuits (Time domain and D-domain), LFSRs
Lecture 21		extra