Special instructions for home exam in

EITF65 Digitalteknik

Dept. of Electrical and Information Technology Lund University

10.00 on August 26, 2021, until latest 12.00 on August 27.

- Hand-out of exam: at 10.00 on August 26 the exam will be available on the course web page for download. Use your own white sheets for writing solutions. Alternatively, a copy of the exam and empty sheets of paper can be picked up in boxes outside EIT (third floor in E-building) from 10.00.
- Hand-in of exam: During 10.00-12.00 on August 27 you can hand in your exam solutions at the department (third floor in E-building, hand-in boxes in stairwell). Alternatively, you can hand in by scanning your solutions and email them to the examiner on email address: thomas@eit.lth.se no later than 12.00! But you must then also send the original solutions and this first page with original signature by regular mail to the address below.[1] The exam will not be corrected until this is received.
- Exam contents: In the home exam there will be problems similar to a standard exam. The grading will require 25/35/45 points for grade 3/4/5, respectively, out of a total of 50. To get grade 5 you additionally need to be approved on an oral exam.
- Sign-up: You need to have signed up to take the exam.
- Help and assistance: You are allowed to use any written information you have access to and you are allowed to use computers and programming for computations. **You are not allowed to get assistance in any way from any other person to help you with your solutions.** This includes asking people to post information on forums, etc. It also includes assisting any other person doing the exam. To assure this, you have to formally sign such a statement.[2] **This first page with original signature must be handed in together with your solutions!**

Name:

Personal Code Number:

I solemnly declare that I have not used help from any other person in the process of preparing the exam solutions that I now hand in.

Signature:

Hand in this page with original signature!

[1] Address: Thomas Johansson, Dept. of EIT, Box 118, 22100 Lund, Sweden

[2] Overstepping the rules of help and assistance may lead to suspension from the university.

LUNDS
UNIVERSITET

Electrical and Information Technology

Exam in
Digitalteknik, EITF65

26-27 augusti 2021

- Write your anonymous code and identifier, or personal number, on all papers you hand in.
- Start a new solution on a new sheet of paper. Use only one side of the sheet.
- The solutions must clearly show the line of reasoning.
- If asked for, the circuits for realizations should be drawn.
- You are allowed to use the course book and lecture notes.

Good Luck!

Problem 1

Consider the following Boolean function in 5 variables given by its on-set and don't care set,

$$f^{-1}(1) = \{0, 3, 5, 7, 10, 15, 19, 21, 24, 28, 31\}$$
$$f^{-1}(-) = \{1, 2, 8, 11, 17, 23, 26, 30\}$$

Derive and write down all prime implicants and determine which of them are essential. Then express f in the minimal disjunctive form.

(10p)

Problem 2

Consider the case where we have two binary inputs s_1 and s_2 and an output y in a discrete system. The output $y(t)$ is 1 if and only if at least five of the six bits in

$$s_1(t), s_1(t-1), s_1(t-2), s_2(t), s_2(t-1), s_2(t-2)$$

are one. Assume that $s_i(t) = 0$ if $t < 0$, $i = 1, 2$. The following example gives inputs and the corresponding output sequence $y(t)$ as follows,

$$s_1(t) = 11101111000101\ldots$$
$$s_2(t) = 01110011001100\ldots$$
$$y(t) = 00110001000000\ldots$$

Construct a sequential circuit for the problem, using a minimum number of delay units (D-element). Construct the circuit using standard gates and make a picture of the full construction!

(10p)

Problem 3

Consider the linear feedback shift register (LFSR) illustrated in Figure 3.1. Let the initial state be $(u_0, u_1 \ldots, u_4) = 01000$, and let the sequence $\mathbf{u}$ be generated as in the figure.

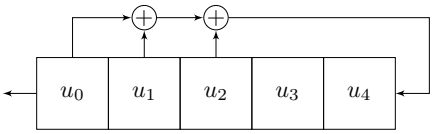


Figure 3.1: An LFSR generating the sequence $\mathbf{u}$.

(a) Determine the D-transform of the sequence $\mathbf{u}$.
(b) Determine the period of the sequence $\mathbf{u}$.
(c) Find the shortest LFSR that can generate $\mathbf{u}$. Make a picture of this LFSR!
(d) Assume that we add the sequence $[01]^\infty$ (addition positionwise modulo 2) to the sequence $\mathbf{u}$. Determine the connection polynomial for the shortest LFSR that can generate this new sequence.

(1+2+3+4=10p)

Problem 4

You are responsible for a digital construction handling four suveillance cameras connected to a monitor. Every camera has as input to the construction a sequence of 4-bit values $\mathbf{u}_i(t)$, $i = 0, \ldots, 3$ at rate 1Mbit/s representing the image of that camera. Assume the notation $\mathbf{u}_i(t) = (u_i^{(0)}(t), u_i^{(1)}(t), u_i^{(2)}(t), u_i^{(3)}(t))$, $i = 0, \ldots, 3$.

Each camera has one more input signal $v_i(t)$, $i = 0, \ldots, 3$. If it is high (1) it indicates that the alarm, where the camera is located, is active. Your construction should work in such a way that if any alarm signal is high, then the image from that particular camera should be shown on the monitor. If there is no alarm signal high, then camera 0 should be displayed. The output in your construction should be a sequence of 4-bit values connected to the the monitor and one additional output, connected to a red lamp that will flash red when its signal is high. The lamp should flash when an alarm is active.

(a) Construct a minimal combinatorial circuit K with $v_i(t)$, $i = 0, \ldots 3$ as input, and three outputs (Alarm, k_0, k_1). The output Alarm is one if any alarm is active, and k_0, k_1 is then the numerical representation of the camera where the alarm is active. If Alarm $= 0$ then $(k_0, k_1) = (0, 0)$. Use standard gates and make a picture of the circuit!
(b) Now make a full construction, using components of type: multiplexer according to the data sheet in the appendix, 1 MHz clock, standard gates, delay units and the combinatorial circuit K from (a). Draw a picture of the construction in detail!

(2+8=10p)

Problem 5

Let $x_1(t), x_2(t)$ be two binary signals with $t \in \mathbb{R}$. If $x_i(t) = 1$ during $t_0 < t < t_1$ with $x_i(t_0) = x_i(t_1) = 0$ then we call this a pulse. The length of pulses and the distance inbetween them are assumed to be much larger than the delay in a gate. Construct a minimal asynchronous sequential circuit where the output $y(t)$ is $y(t) = 1$ from the time when at least one pulse on each input signal has been detected, otherwise we should have $y(t) = 0$. The sequential circuit can be of Moore type. Realizera asynchronous sequential circuit using standard gates and make a detailed picture!

(10p)

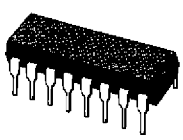
Good luck!

SGS-THOMSON MICROELECTRONICS

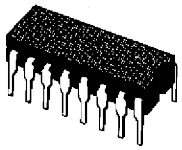
M54HCT157/158
M74HCT157/158

HCT157 QUAD 2 CHANNEL MULTIPLEXER
HCT158 QUAD 2 CHANNEL MULTIPLEXER (INV.)

- HIGH SPEED
  t_{PD} = 21 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS157/158



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

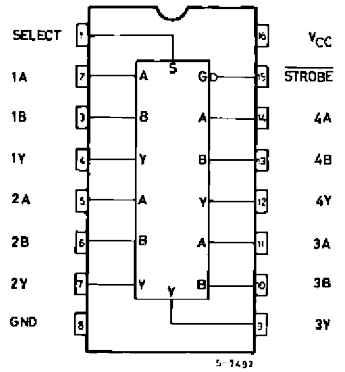
C1R
(Chip Carrier)

ORDER CODES :

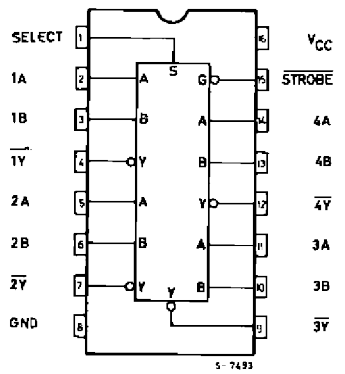
M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

PIN CONNECTIONS (top view)

HCT157



HCT158



NC =
No Internal
Connection

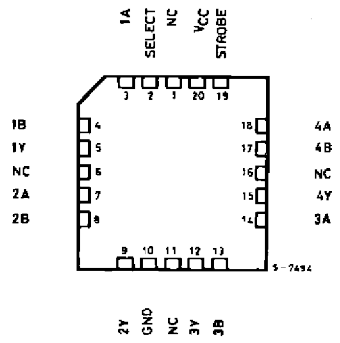
DESCRIPTION

The M54/74HCT157 and the M54/74HCT158 are high speed CMOS QUAD 2-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

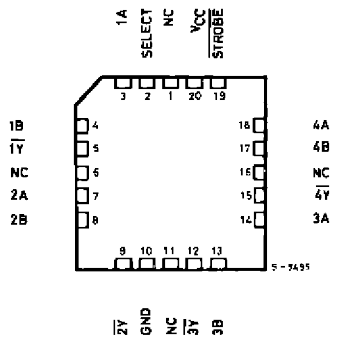
These devices consist of four 2-input digital multiplexers with common select and strobe inputs. The HCT158 is an inverting multiplexer while the HCT157 is a non-inverting multiplexer. When the $\overline{\text{STROBE}}$ input is held High, selection of data is inhibited and all the outputs become Low in the M74HCT157 and High in the M74HCT158. The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

CHIP CARRIER

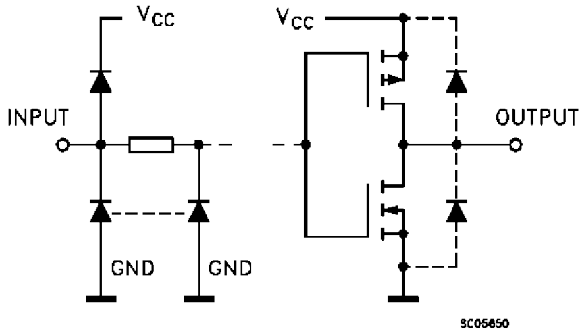
HCT157



HCT158



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (for HCT157)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Output
15	$\overline{\text{STROBE}}$	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

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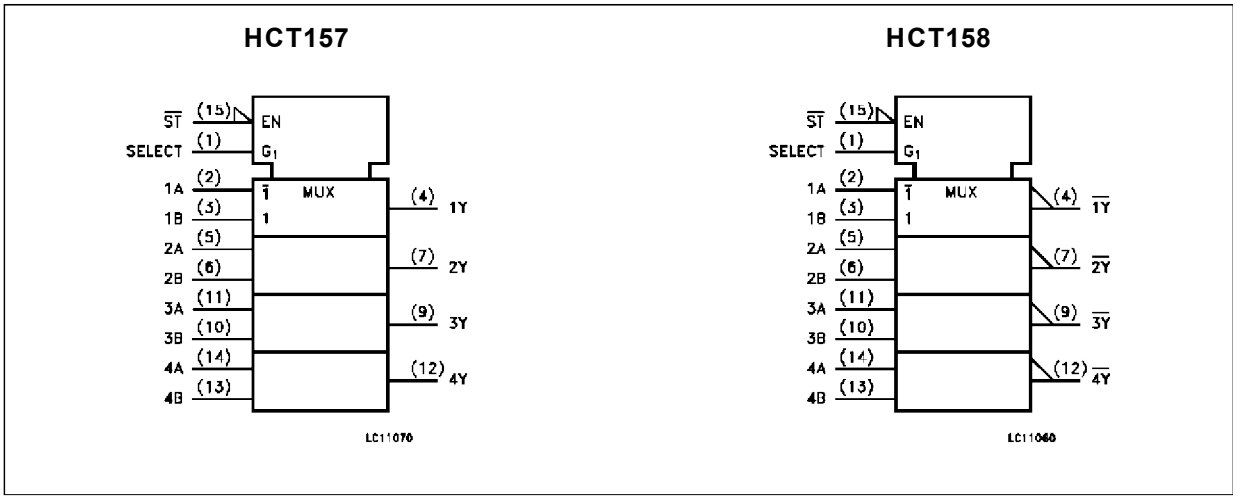
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{STROBE}$	SELECT	A	B	Y (HCT157)	$\overline{Y}$ (HCT158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: DON'T CARE

IEC LOGIC SYMBOL



LOGIC DIAGRAM