The invention of the network camera

and the VLSI technology behind

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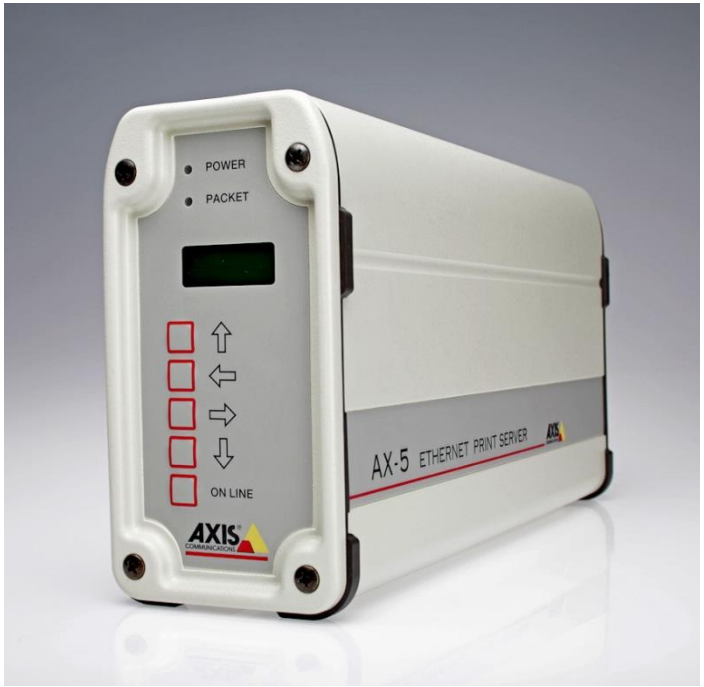
Axis Mission

Axis

- Founded in 1984 at IDEON in Lund
- IT company focused on Network Video Solutions
- 2788 employees (Q2, 2017)
- Sales 2016, 7400 MSEK
- Listed on NASDAQ OMX under acquisition by Canon
- Head office in Lund, close to LTH
- Own presence in more than 50 countries
- 90000 partners in 179 countries

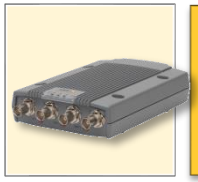
Original products



The market's broadest portfolio

Fixed cameras

Thermal cameras



Encoders/ decoders

Fixed dome cameras

Onboard cameras

Software & recording

PTZ cameras

Accessories

Physical access control

AXIS Q3709-PVE Network Camera

Multi-sensor, multi-megapixel - 180° overview. One camera.

> 180° panoramic **overview**

> Smooth video of movements at up to **30 fps in 3 x 4K**

> Efficient one-camera **installation**

Small business – AXIS Camera Companion

Video surveillance made simple

- Optimized solution for 1-4 camera systems, with support for up to 16 cameras
- Recording on SD cards, removes the need for central recording
- Mobile app for freedom of use
  - Axis Secure Remote Access for a secure and easy-to-install way to access the system remotely
  - Axis Mobile Streaming for efficient bandwidth usage
- VMS and mobile viewing app **free** for download

AXIS A8004-VE Network Door Controller

Reliable audio visual identification and entry control

> A perfect complement to any surveillance installation to effectively control entry:
  - Identify and talk to visitors
  - Record what happens at the entrances

> Suitable for small- and mid-size installations as well as advanced enterprise systems

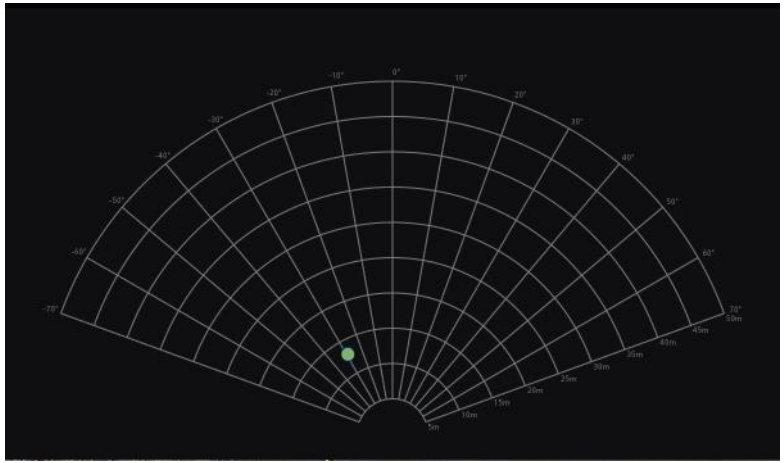
AXIS D2050-VE Network Radar Detector

Why a radar? What's the problem

- Many customers are searching for a solution that can minimize repeatedly false detections.
- Video Motion Detection (VMD) can be challenging to use outdoor.
  - During night time and
  - Bad weather conditions
  - Spiders and bugs are present.
- Radar can serve as a complement to video surveillance
  - Suitable for area protection and makes it possible to positively detect movement with high accuracy

PTZ live autopilot

> Radar data can control Pan-Tilt-Zoom cameras
  - Enables PTZ camera to be pre-positioned when operator take control
  - Follows object during day, night or bad weather conditions



30+ years of intelligent networks

Internet of Security Things

Network video

Storage

Network print servers

IBM protocol converters

2012

1984 1992 1996 1998 2001 2011 2013

Europe

Asia

USA

Global

Our business model

Why is the sales model so important ?

- Everyone can trust Axis
- Integrators never compete with their main partner
  - But they do compete with each other
  - Axis never “steals from the channel”
- Distributors always make money
  - Axis often has no set-up to bypass
- Rebate system to ensure correct pricing
  - Deal pricing, partner pricing, etc.
- Make sure this model fits
  - Analytics, use partners
  - ACS – use for low end, not large systems

Axis regional update

Market share in revenues for security camera, security network camera and video encoder

Americas

> # 1 in all categories**
> 52 percent of sales*

EMEA

> # 1 in all categories**
> 37 percent of sales*

Asia (excluding China)

> # 1 in video encoders**
> # 3 in network security cameras**
> # 6 in security cameras**
> 11 percent of sales*

*Axis sales 2015
**Results based on IHS Technology Video Surveillance Intelligence Service, 2016. Results are not an endorsement of Axis Communications. Any reliance on these results is at the third party's own risk. Visit www.technology.ihs.com for more details.
Source: IHS Video Surveillance Intelligence Service, 2016

Regional development Q2, 2017

Americas

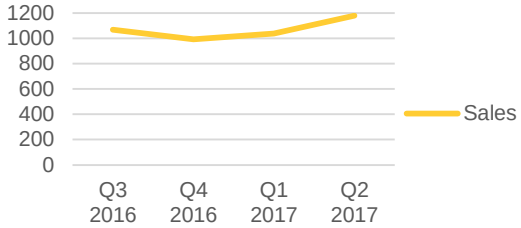
56%

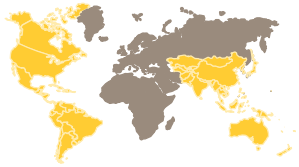
of sales

> Total sales of SEK 1,180 M (984)

> Growth of 20%

> Local growth of 11%





EMEA

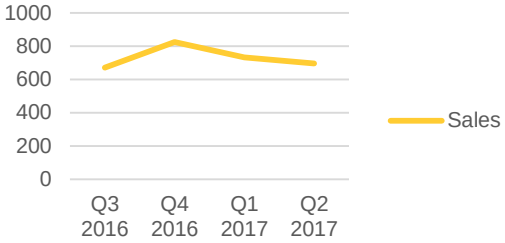
33%

of sales

> Total sales of SEK 696 M (565)

> Growth of 23%

> Local growth of 15%



Asia

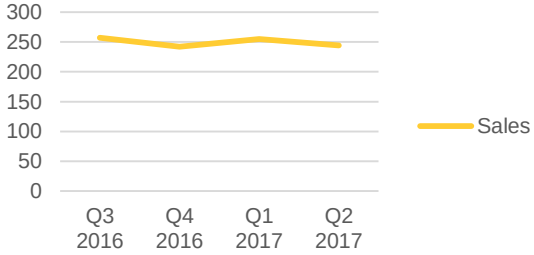
11%

of sales

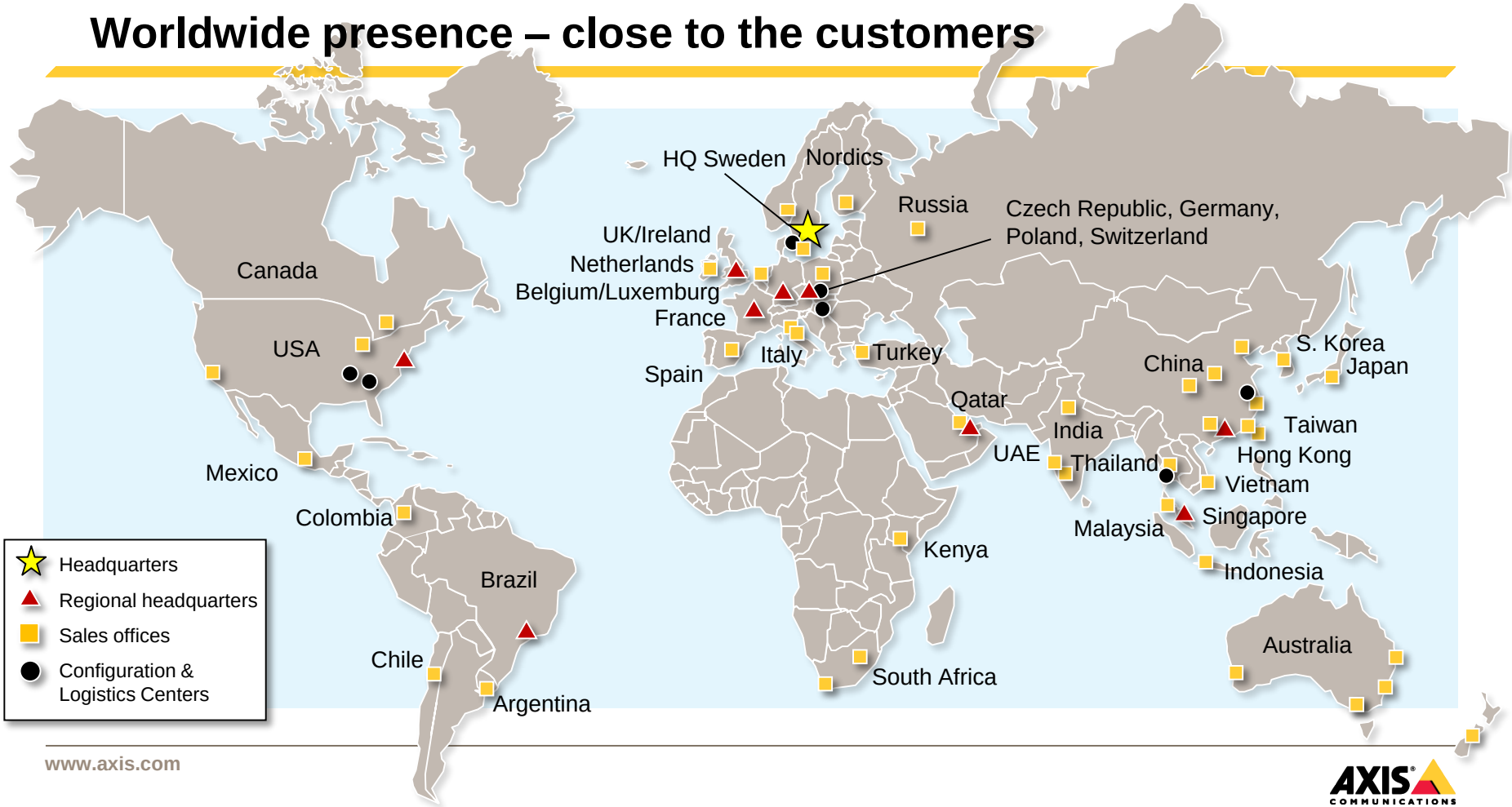
> Total sales of SEK 244 M (213)

> Growth of 14%

> Local growth of 8%



Worldwide presence – close to the customers



Taking long-term responsibility by thinking big

Sustainability highlights

> Continued to enhance and reduce product packaging

> Optimized logistics

> Energy-efficient, more environmentally friendly products

> Anti-Corruption policy

Axis – continuously driving innovation

1996

World's first network camera

1998

World's first video encoder

1999

World's first network video chip

2004

First MPEG-4 and Motion JPEG compression camera

2008

First H.264 compression standard for network camera

2009

First network cameras with HDTV, and with remote focus & zoom functions

HDTV NETWORK VIDEO

SMPTE

2010

First thermal network camera

2011

Lightfinder technology

2012

Unique high-performance WDR camera

2012

First network camera with active cooling

2013

Physical Access Control

2015

Zipstream technology & Sharpdome technology

2015

Open standard network loudspeaker & Open IP-based door station

2016

Pan, Tilt, Roll, Zoom (PTRZ) technology & laser focus technology

AXIS COMMUNICATIONS

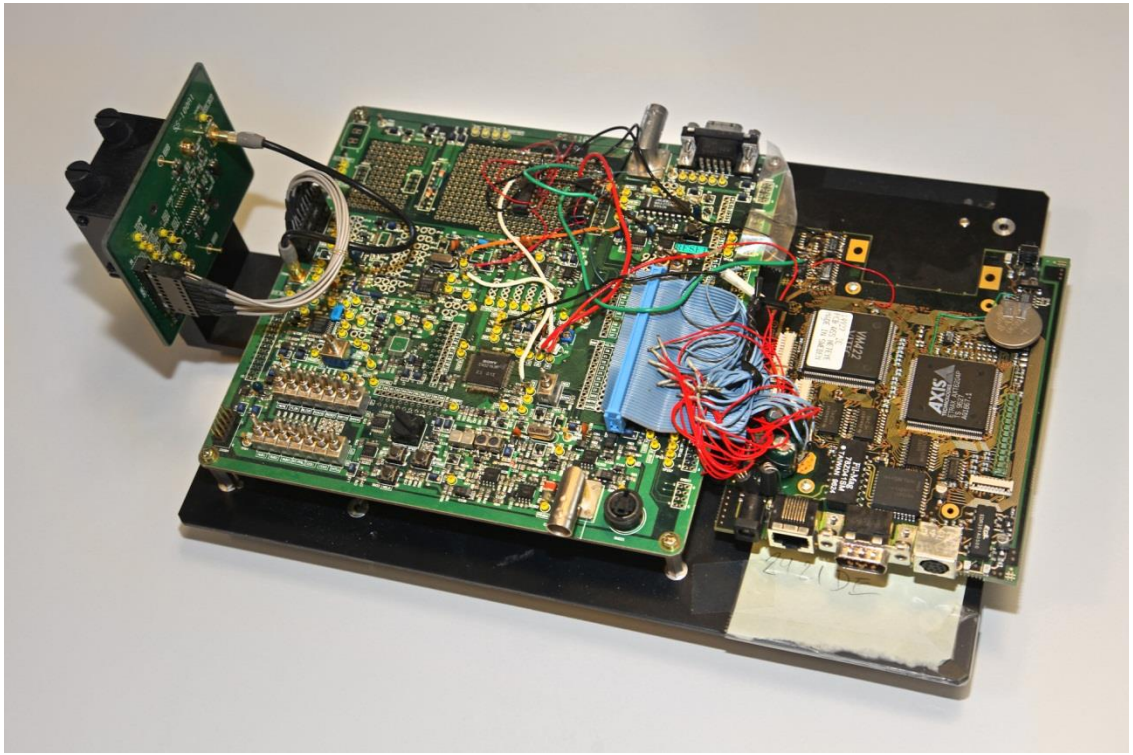
20 years of network cameras 1996-2016

Axis invented the world's first network camera

Technology leader with many industry firsts

Continuing to drive innovation for a smarter, safer world

The fourth phase - the invention of the network camera



1996 - AXIS NetEye 200

- The world's first network camera
- Launched at Interop Atlanta, September 18th, 1996
- Performance
  - 1 image/second in 352*288 pixel
  - 3 frames/minute in 0.4 Mpixel

More than 10,000 sold!

One of our first camera customers…

> Steve Wozniak, co-founder of Apple

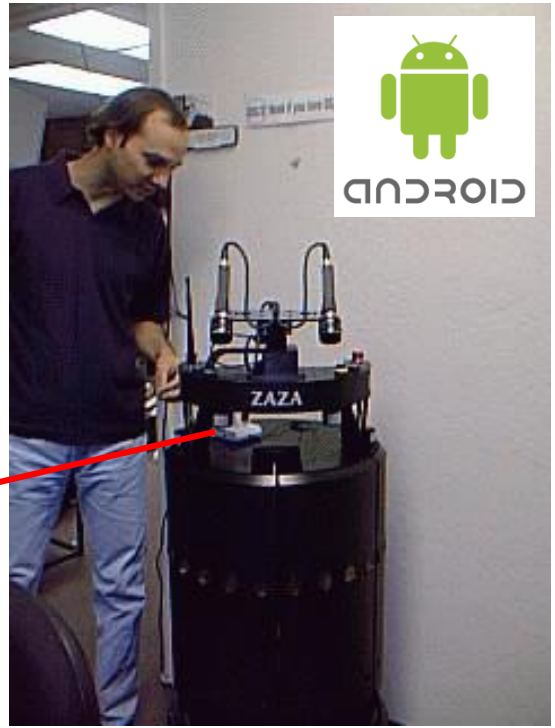
> Was in a car accident during a tech support call

> No injuries and problem was solved

World's first video encoder in 1998

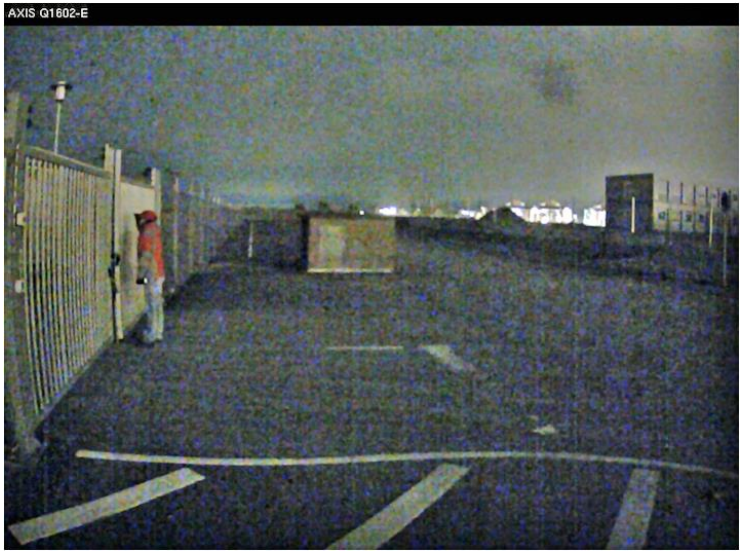
> AXIS 240 – the world's first video encoder

> Andy Rubin, CTO & founder of Android at Google, in 1997 when he was testing AXIS 240
prototypes



Lightfinder technology, Wall Street Journal Technology Innovation Award

AXIS 221



AXIS Q1602

Perimeter surveillance with no street illumination during night time and approximately 0.1 lux.

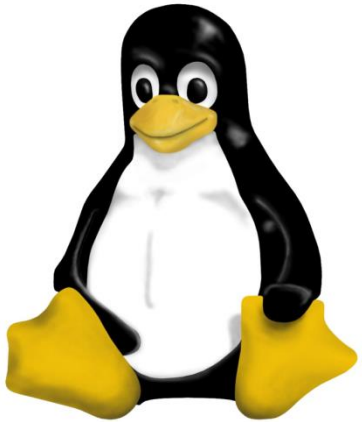
In-house R&D – where the coming successes are made

- Substantial R&D investment
  - 15% of revenue
- Strong network camera patent portfolio
- Canon is very strong on patents
- 3 corner stones
  - Innovation
  - Openness
  - Quality

More than 800 engineers work in Lund

Mechanics

Software



Electronics

ASIC´s

”ASIC” stands for ”Application Specific Integrated Circuit”.

ASIC development at AXIS

Axis – continuously driving innovation in network video

1999
ARTPEC-1
Worlds first Network camera ASIC

1996
Off the shelf Components (VITEC)

2003
ARTPEC-A

2004

ARTPEC-2
Dualstream MPEG-4/MJPEG

2008

ARTPEC-3
HDTV/H.264

2009
ARTPEC-B

2011

ARTPEC-4
Lightfinder technology

2012
Amabrella
(ARTPEC-C)

2014

ARTPEC-5
Forensic capture
Zipstream

2017

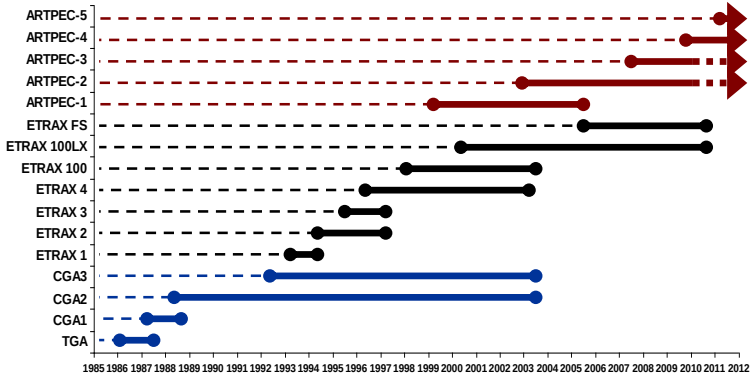
ARTPEC-6
Forensic WDR
Radar

AXIS ASIC history

- AXIS has developed SoC ASICs since late 80ths
- 80s ASICs
  - where used for network protocol converting
- 90s ASICs
  - In-house developed RISC CPU (ARM-style) where added and the proprietary Canon printer protocol Page 21 where added forming the ETRAX chip family.
  - A separate image processing ASIC ARTPEC was developed for the camera business.
- During 2000 to 2010 the ASICs became large unified SoC where more and more external IPs where.
- Today AXIS is focusing on development of differentiating functions such as image processing, analytics, scaling, overlay and the overall specification of the SoC.

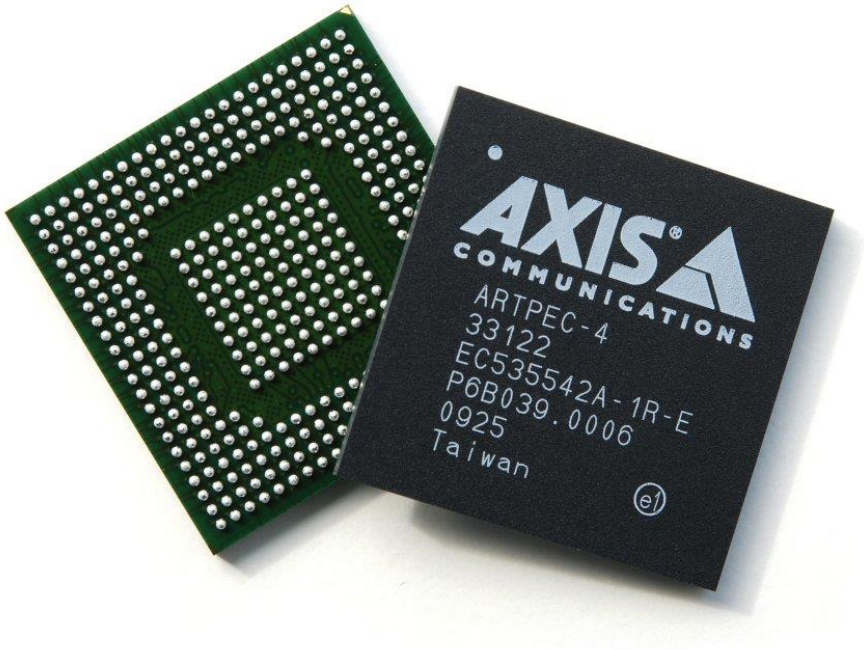
AXIS ASIC history

- From start all functionality was developed in-house by a few designers
- There where no market for general building blocks (IP blocks) such as CPUs, Memory Ctrl, Interfaces etc but this has changed over the years,
- Today we need about 60 man years and still half of the functionality is developed by external parties.
- Number of transistors has multiplied by 2500 since then.
  - Moores Law: Number of transistors doubles every 18th months
  - AXIS has historically been one to two step behind latest technology
  - But are now closing in to be able to fulfill requirements



Typical Axis SoC content

- > Embedded CPU running Linux
- > Image processing pipeline
- > Image scaler with dewarping
- > Image compression subsystem
- > Crypto accelerator
- > Ethernet controller
- > I/O controller
- > Interfaces etc



An ASIC often combines the different functions needed for a complete system on one single chip. This is called ”System on a Chip” or ”SoC”.

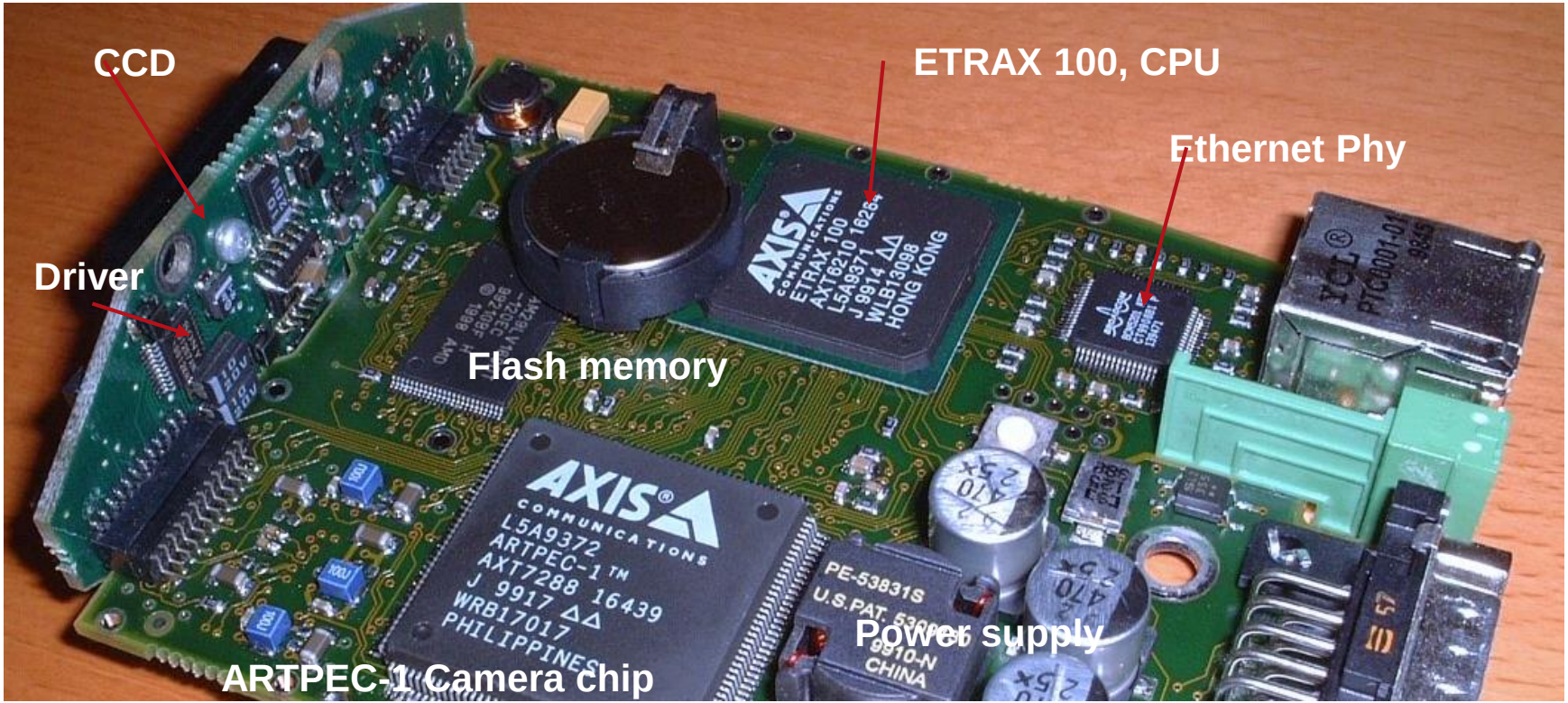
ARTPEC 1 - 6

> Six generations of dedicated network camera ASIC’s

ARTPEC-1

- Worlds first network camera ASIC
- uCLinux on ETRAX CPU
- CCD/CMOS IPP, MJPEG compression
- Latch based design, 2-phase clocking
  - Clock gating to save power
- 160 pin PQFP

ARTPEC-1 product



ARTPEC-2

- Worlds first dualstream MPEG-4/MJPEG network camera ASIC
- CCD/CMOS IPP
- Latch based design, 2-phase clocking
  - Clock gating to save power
- 208 pin PQFP

ARTPEC-3

- Worlds first HDTV/H.264 network camera SoC
- HDTV 1080p30
- LFBGA400 17x17mm

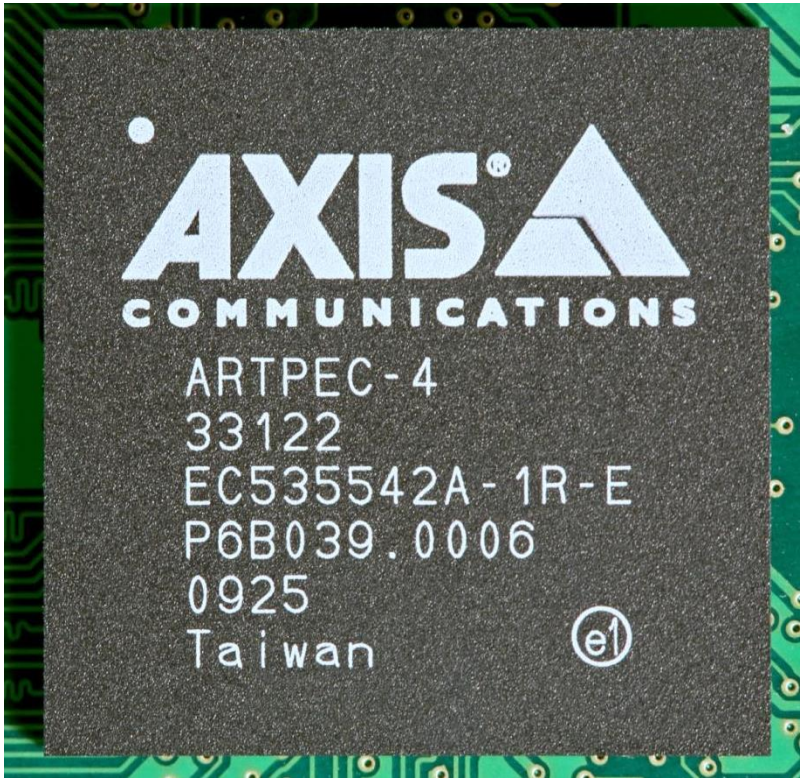
ARTPEC-4

> Lowlight/WDR network camera SoC

> HDTV 1080p30

> MIPS CPU

> 400 ball TFBGA



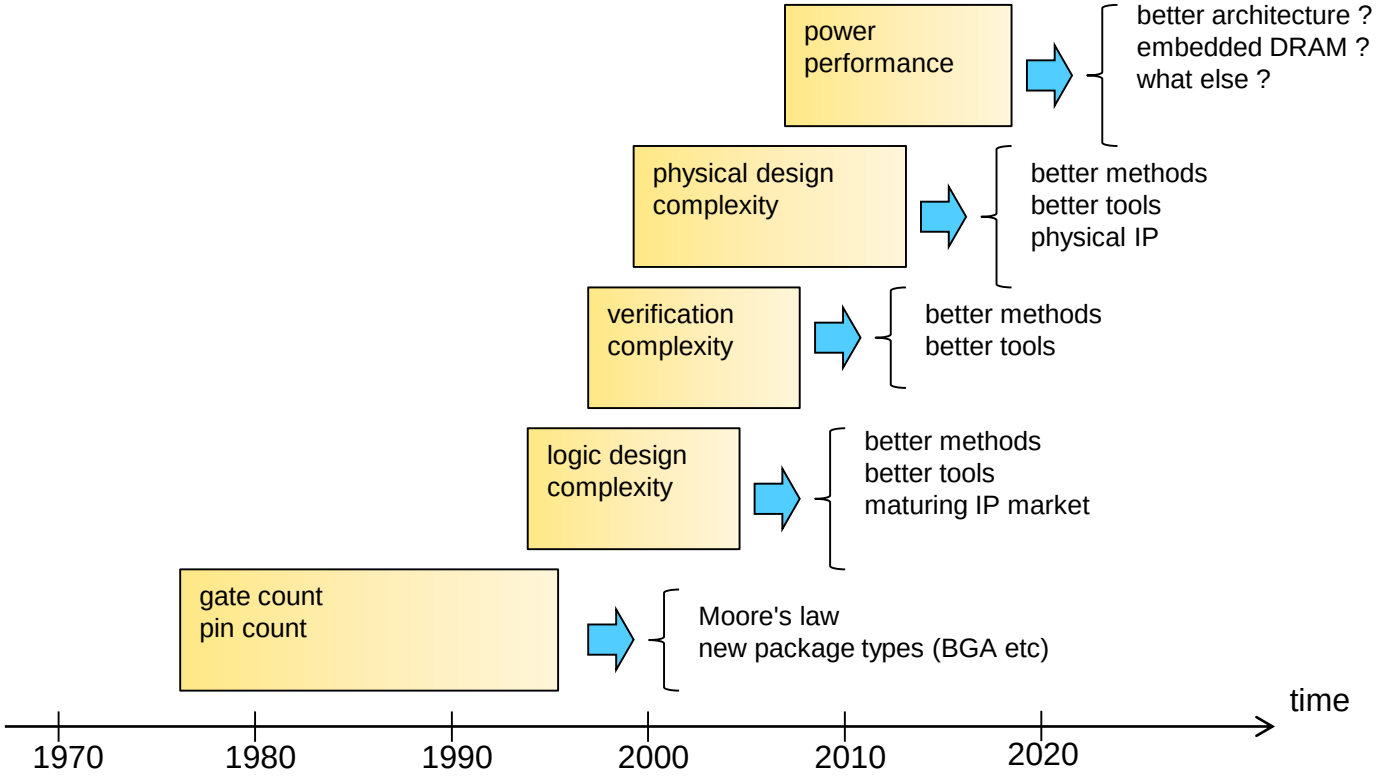
ARTPEC-5

- Faster general purpose CPU
  - Dual core
    - Independent execution units
    - Dual hw threads per core
    - Parallel computing architecture
- Higher memory throughput
- Faster Video Analytics
- New camera features
  - Improved image quality
  - WDR
- Zipstream

ARTPEC-6

- High quality 4k30 products
- Faster general purpose CPU
  - ARM
- Higher memory throughput
- Faster Video Analytics
- Faster Graphics
- New camera features
  - Improved image quality
  - Forensic WDR
- HDMI

Electronic design obstacles, history and future



Why ASIC development?

> Benefits:
  - Product performance
  - Product size and power (Size 70 to 100 times less than FPGA in same technology)
  - Unique features (hard to copy by competitors)
  - Secured access to technology (still there are not many external ”Platforms” for video market)
  - Unit cost reduction

> Challenges:
  - Time to market
  - Development costs
  - Complexity
  - Project risk (Size/Time/Spec)
  - Technology risk

Description of AXIS ASIC development

- We use partners/ASIC vendors for the back-end design and manufacturing of our ARTPEC chips. We have used both partners that has their own fab and fabless companies.
- Design and verification (VCS) using SystemVerilog, main reason to SystemVerilog is verification but we are also using advanced structures that makes design work more effective.
- We have done VMM based random verification since 2005 and are now moving to UVM. Modelling is TLM2.0 and C based
- We do Verilog netlist handoff with timing constraints to our partner. We do both synthesis (DC) and floorplan (DC Graphical) to ensure quality and decrease number of iterations

Chip development

- The written code will be translated by running a synthesis tool to a specific cell of the selected library of a specific process (e.g 28nm TSMC Low power library)
- When all functionality is described in System Verilog and synthesized we call it a Netlist.
- We can simulate functionality, performance (speed), power (dynamic and static) and do an approximate placement and routing (connection).

```
module ff (q, d, clk)
output q; input d, clk;
reg q;
always @(posedge clk) q = d;
endmodule
```

EDA tools

- Tool supplier
  - We have been using Synopsys tools for a long time.
  - The license model is Time Based License with pool of tools
  - Mix changed based on project flow
- Design & Implementation - SystemVerilog
- Synthesis – Design Compiler
- Verification - VCS
- Floor planning – DC Graphical
- STA – Primetime
- DFT – we do not do DFT but we prepare our design for DFT
- Using other point tools for specific design purposes
  - Power - Power Compiler
  - High-level modulation - QUEMU, TLM2.0
- Continually evaluation tools and vendors

How to handle risk and development cost?

- Luckily specification of mobile devices is more similar to Surveillance Camera than old Mobile phone i.e. always ”On”, which gives us benefit from using same IP
- Increased design complexity must be managed
  - Improved design tools and design methods
  - Modularization and reuse
  - Make use of External competence for Top Level integration and General System implementation
  - Make use of external chips for parts of our product portfolio that has specific needs
- NRE (external design and manufacturing cost) cost increase dramatically with newer technologies
  - Carefully specify new designs to reach enough volumes
- Make use of external chips in some products to ensure second source

Two teams

- **Chip Platforms**
  - Manager Lars Branzen
  - Product Manager
  - Project Manager
- Competence Groups
  - Backend group
  - System Architecture group
  - FPGA

- **Chip Platforms IP**
  - Manager
  - Architect
  - Project Manager
- Competence Groups
  - Front End Design Group
  - Verification Group

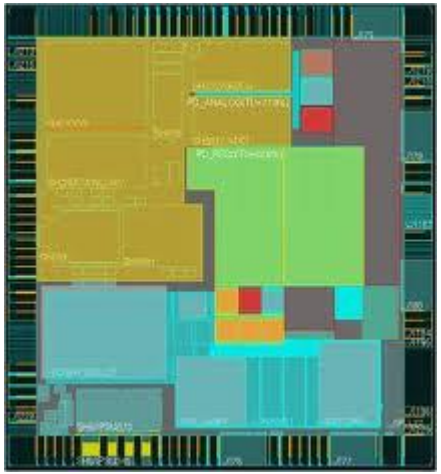
Responsibilities

- ASIC and FPGA methodology for System-On-Chip
- Models for early SW development (TLM/System-C)
- Suggest chip platform technology solutions
- Chip platform roadmap
- Chip product ownership
  - User documentation
  - HW support during lifetime
- ASIC and IP purchasing
- FPGA development for early SW development, algorithm validation and product functionality extensions

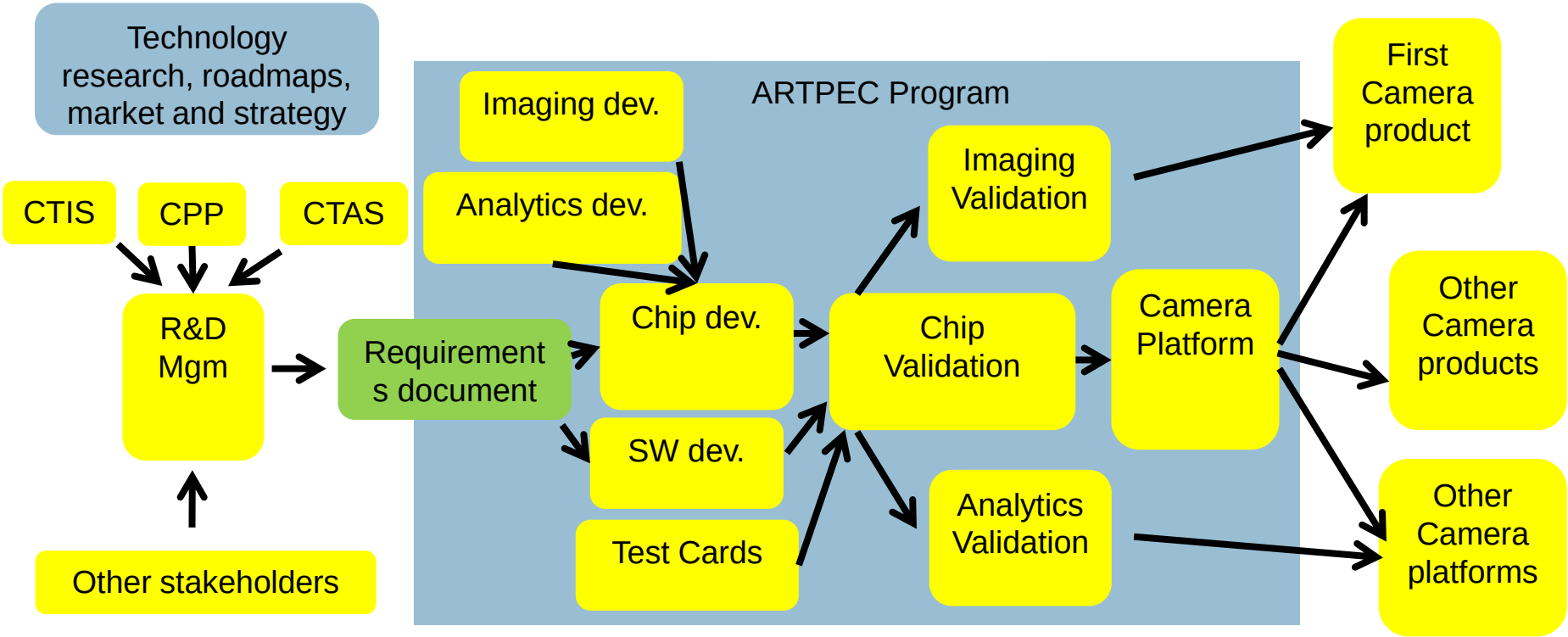
Chip Project

Chip development

- Axis develop critical functionality
- ASIC Vendor integrate CPU subsystem
- The netlist is then assembled by the ASIC Vendor who will add functionality for test and manufacturing followed by exact placement and routing.
- After iterations between Axis and Vendor (changing floorplan, RTL, specification etc.) the final version of the circuit will be written out in GDSII format which will be used for producing production Masks.
- Prototype production
- Engineering Samples sent to to Axis



Chip development as a Program



Chip IP project

A parallel project develop new specific functions (IP)

> Driven by CP-IP team
  - ~15 ASIC design engineers + 5-10 consultants

> Assisted by
  - Core Technologies Imaging Systems (CTIS)
  - Core Technologies Analytics&System (CTAS)
  - Core Product Platforms team (CPP)
    - HW/SW interface reviews
    - Linux driver development
    - Prototype/sample validation
  - Core Technologies – Media and Graphics (CTMG)

Chip project

Vendor selection and integration

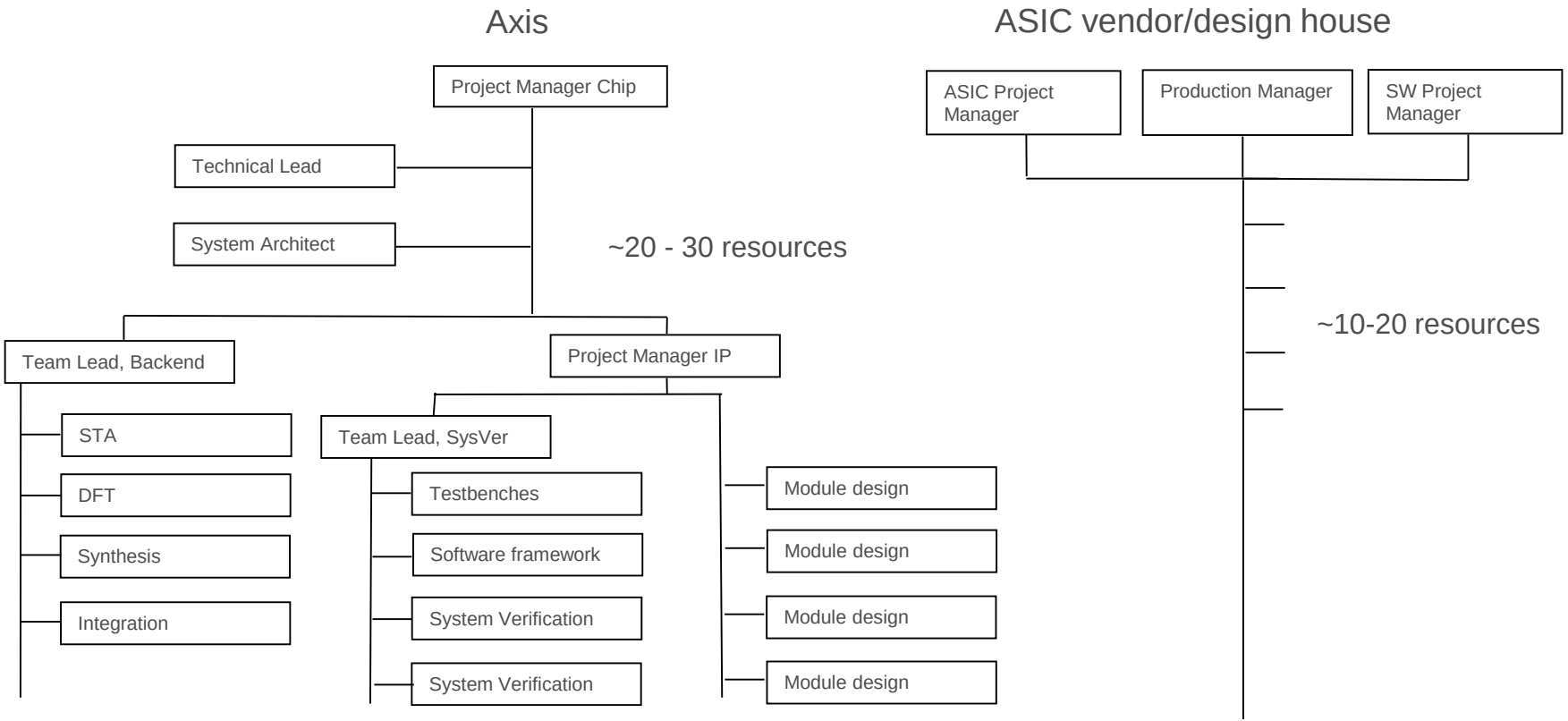
> Driven by our Chip Platforms team
  - ~7 ASIC design engineers

> Assisted by:
  - Tech-Ref and PCB-CAD
    - Electronics
      - Package (ball-out)
      - PCB layout (incl. X-talk and SI-analysis)
    - Mechanics
      - Thermal design and analysis

Chip project

- Modular design flow
  - Design implemented in the RTL (Register Transfer Level) language System Verilog
    - Parallel processes
    - Synchronous design style
  - Fully verified sub-designs, comprehensive random testing (UVM/VMM)
  - Synthesis, STA and DFT clean sub-designs
  - Design guidelines and checklists
  - Documentation and reviews
  - Predictable integration in ASIC project

Chip Project - Typical ASIC project organization

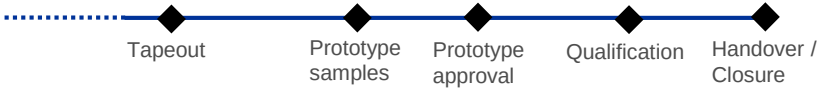


Chip project - Cooperation with ASIC vendor/design house

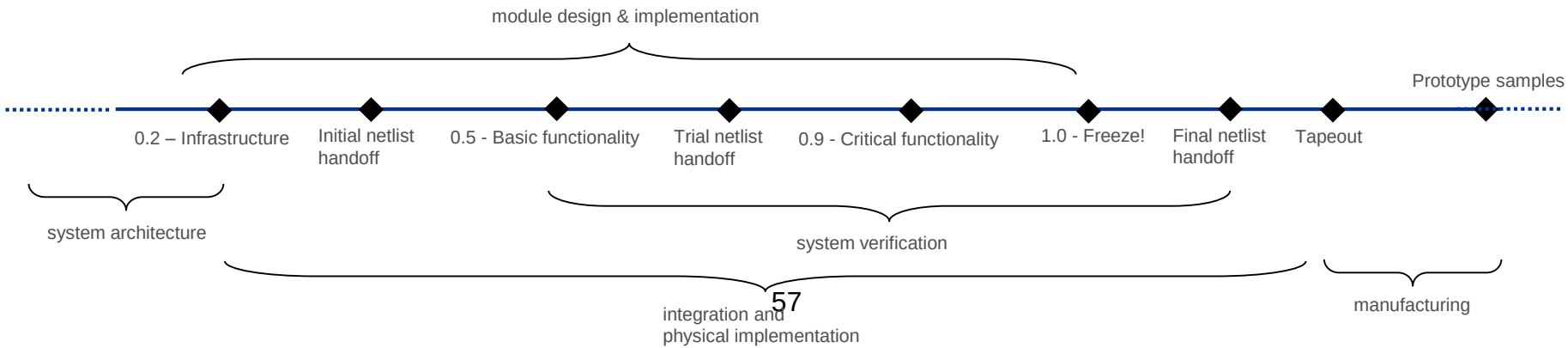
- Generally 3 main phases in project
  - 0.5 – initial netlist
  - 0.9 – trial netlist
  - 1.0 – final netlist
- Traditional ASIC design flow for ARTPEC
  - Verilog netlist and SDC (Static timing Design Constraints) handover
- Joint work on
  - Package / pinout
  - Power simulations
  - IP integration
  - DFT
  - Floorplanning
  - Timing closure

18-month ASIC design cycle

Project A ending phase



Project B main phase



Project C starting phase

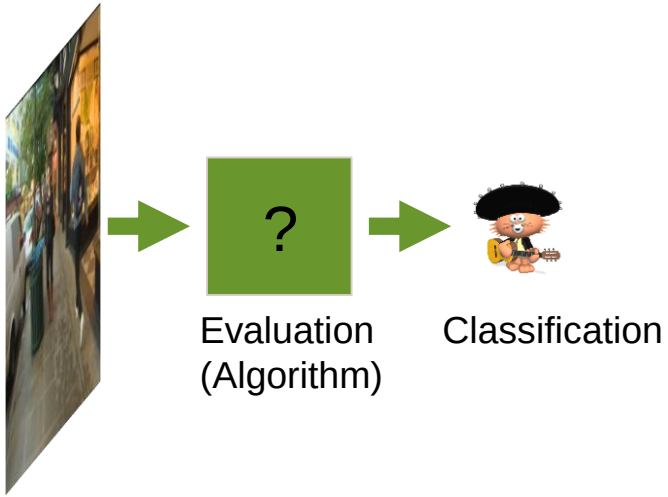
Deep learning

Definitions – machine learning

Machine learning - In 1959, Arthur Samuel defined machine learning as a "Field of study that gives computers the ability to learn without being explicitly programmed".

Picture -> algorithm -> “It’s a cat!”

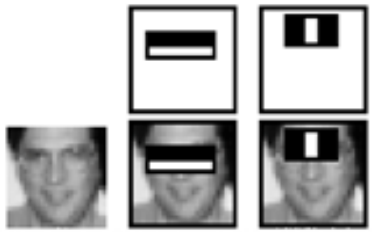
Variation is the problem: Viewport, Scale, Deformation, Occlusion, Illumination, Background clutter, Intra-class differences



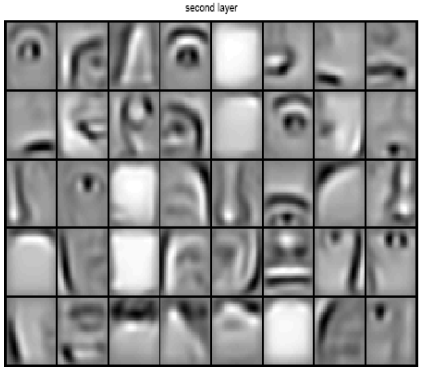
Definitions – deep learning

Deep learning: Inspired by how the human brain learns to see.

Hand-crafted features



Data-driven features



Deep learning – framework, architecture, model

- **Framework** – The tools used to create and train and execute Deep Convolutional Neural Networks (DCNN)
- **Architecture** – A description of the algorithm, the ”blueprint”
- **Model** – A realization of the architecture. That is, the architecture with the trained weights of its internal filters, needed to make predictions.

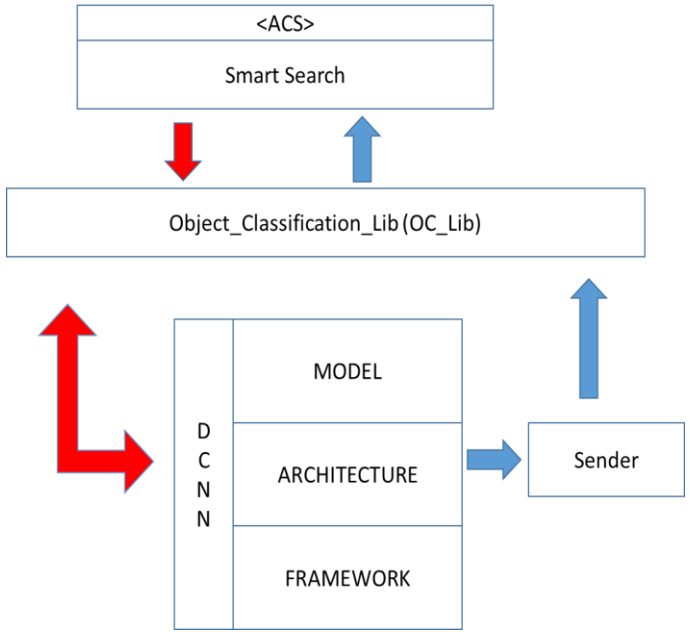
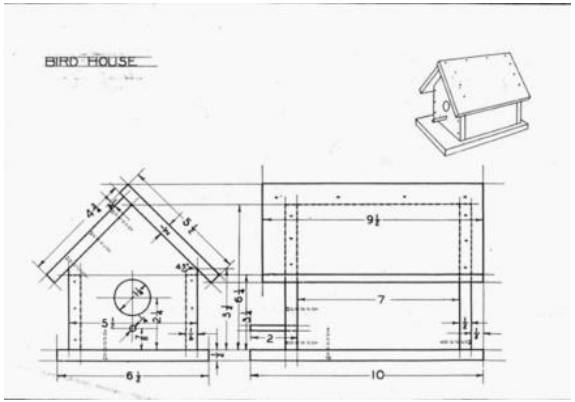


Illustration – building a house

Framework

Architecture



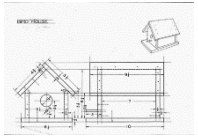
Model

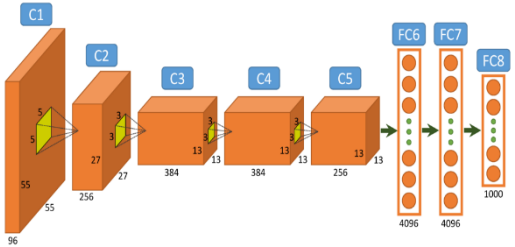
Illustration – Definitions for Deep Learning

Framework

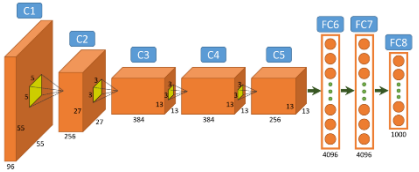
Caffe

Architecture





Model



The weights (parameters)

Nearest Neighbor Classifier (Not a CNN)

Problem: Based on N measures, sort into **fixed** number of classes

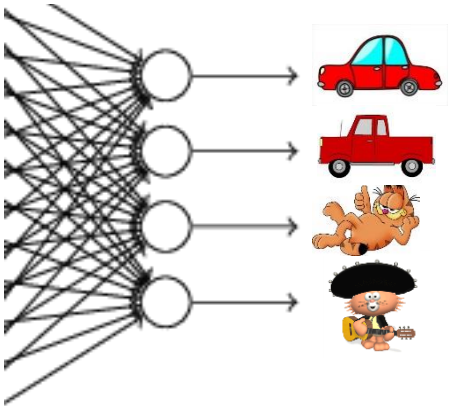
> Measure the difference
  - Pixel-wise distance (L1)
  - Euclidean distance (L2)

> K-Nearest Neighbor classifier
  - Use more than the best match
  - Example k=3, uses the 3 best matches to better classify the data

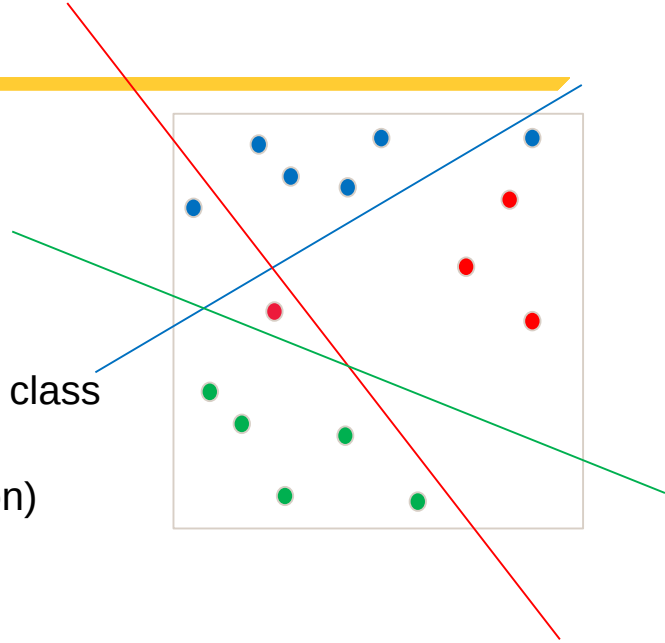
> How to select k or other basic option? (Tune the hyperparameters)

> Divide the data training set into parts, with different usage
  - Training set, fake test set (validation set)

> Problem: We need to keep the training set and run through all new data every time.

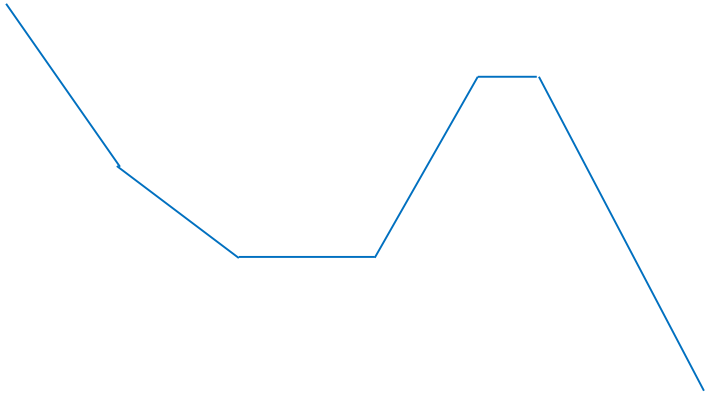


Linear classification



- Linear classification
  - Score function is a weighted sum of all values
  - Write as a Matrix multiplication f(x1;W,b)
  - 2-dim example:
    - On a plane: straight lines will be the borders for each class
  - Loss function
    - To measure the error (eg how bad is this classification)
  - SVM classification (hinge loss)
  - Soft-max classification (cross-entropy loss)
    - Provides probabilities
- Major benefit: When the parameters (W,b) is known the dataset might be discarded

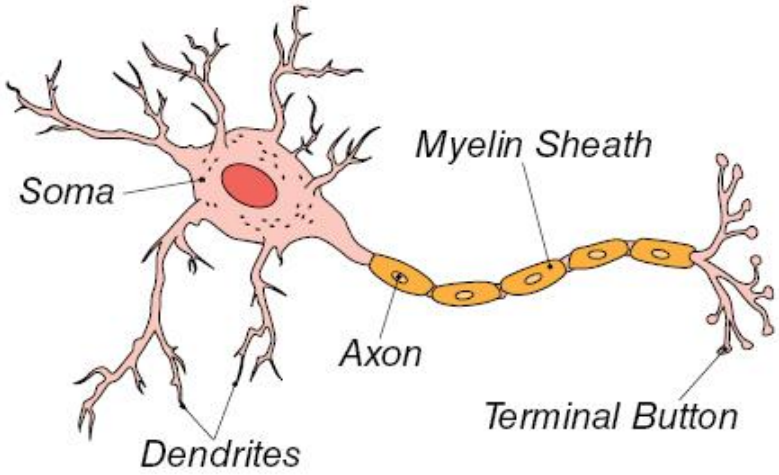
Optimization



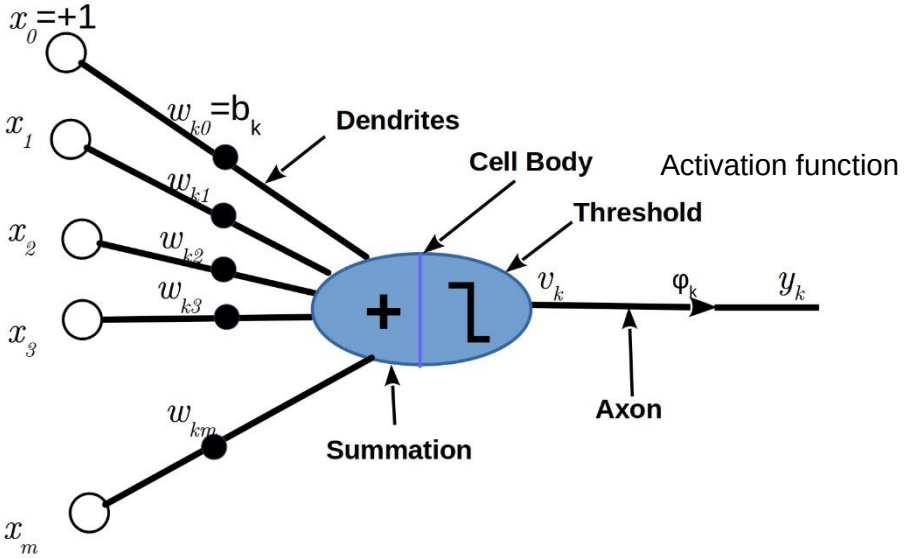
- How to find W (and b)
- Random search (bad idea)
- Follow the gradient (good idea)
  - Numerical gradient
  - Analytic gradient
- Algorithm:
  - Start with random set
  - Refine parameters using iteration and a step-size
  - Use the analytics gradient and a gradient descent algorithm
- Backpropagation
  - Use a network with simple nodes where you can solve the gradient

The architecture: Alexnet, Resnet, GoogLeNet...

Brain neuron



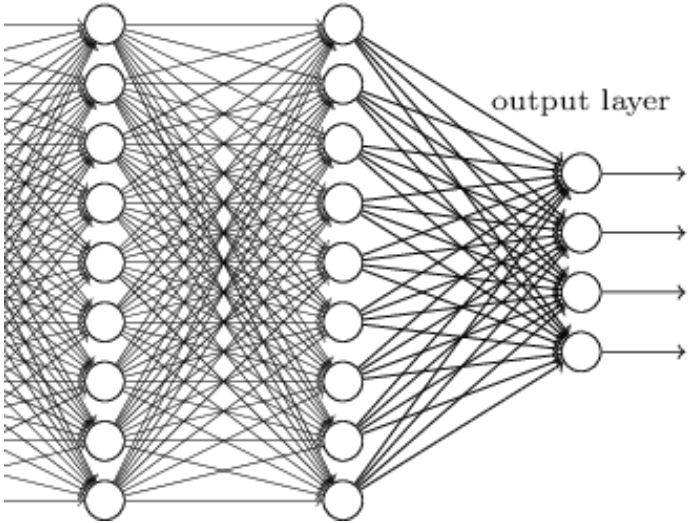
Artificial neuron



Coarse model of biological neuron

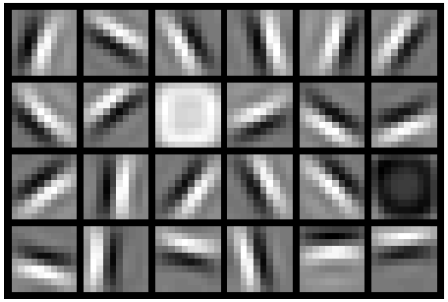
Neural network architectures

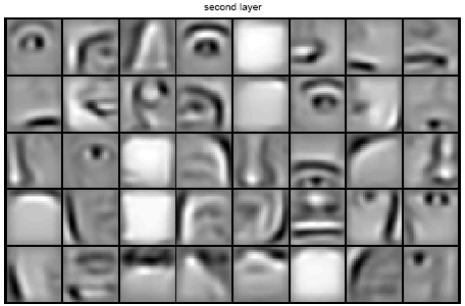
- Neural networks are neurons in a graph
  - Input layer
  - Hidden layer(s)
  - Output layer
- No loops
- Reason to use layers
  - Express them as vector matrix multiplications
  - Groups of neurons will approximate non-linear function
- Good properties
  - Cheap to use
  - Difficult to train
- Modern CNN have 10-20 layers and 100M parameters
  - Deep learning

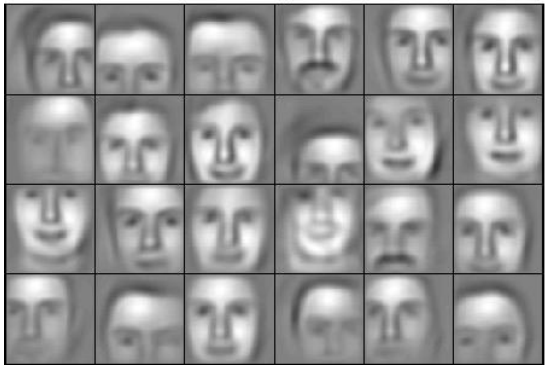


The architecture: Feature extraction

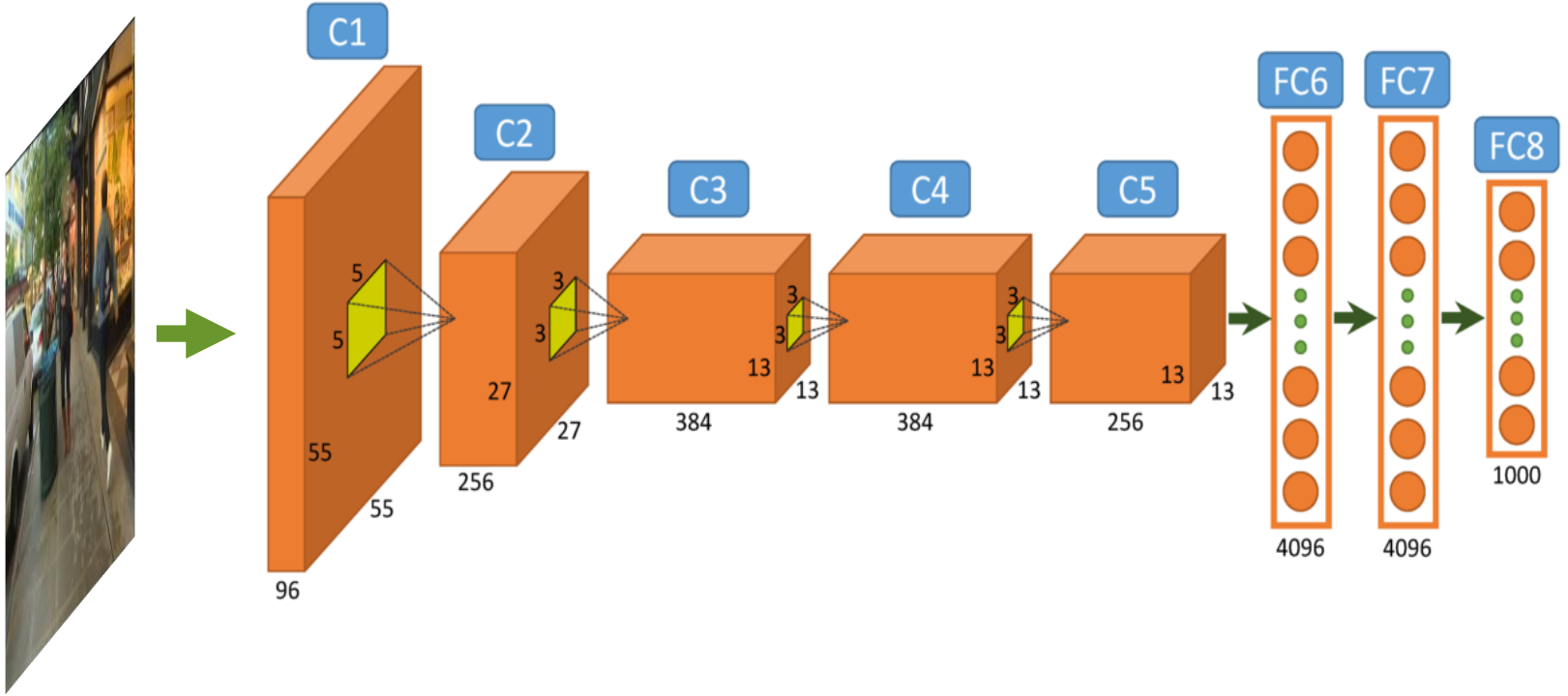
Simple filters get combined into more complex shapes in later layers



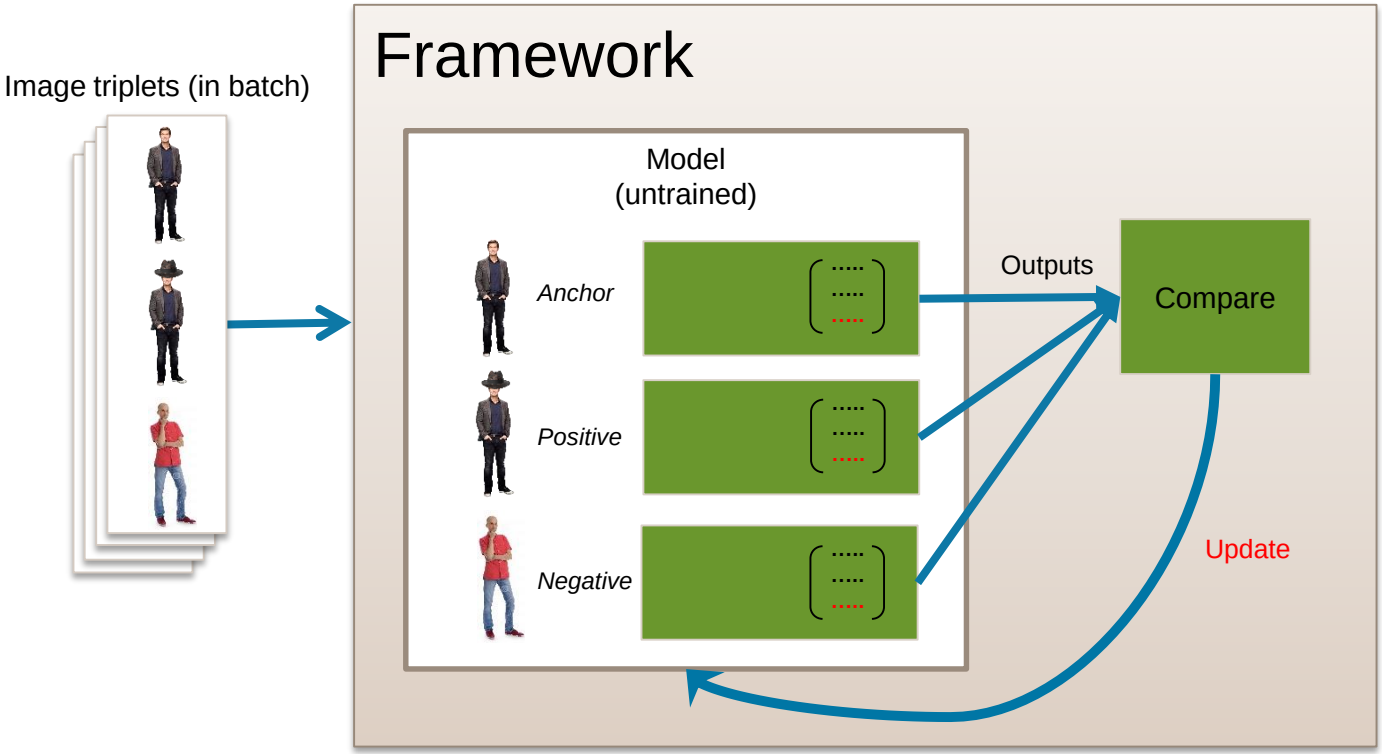




The architecture: Example, modified Alexnet (ZF-5)

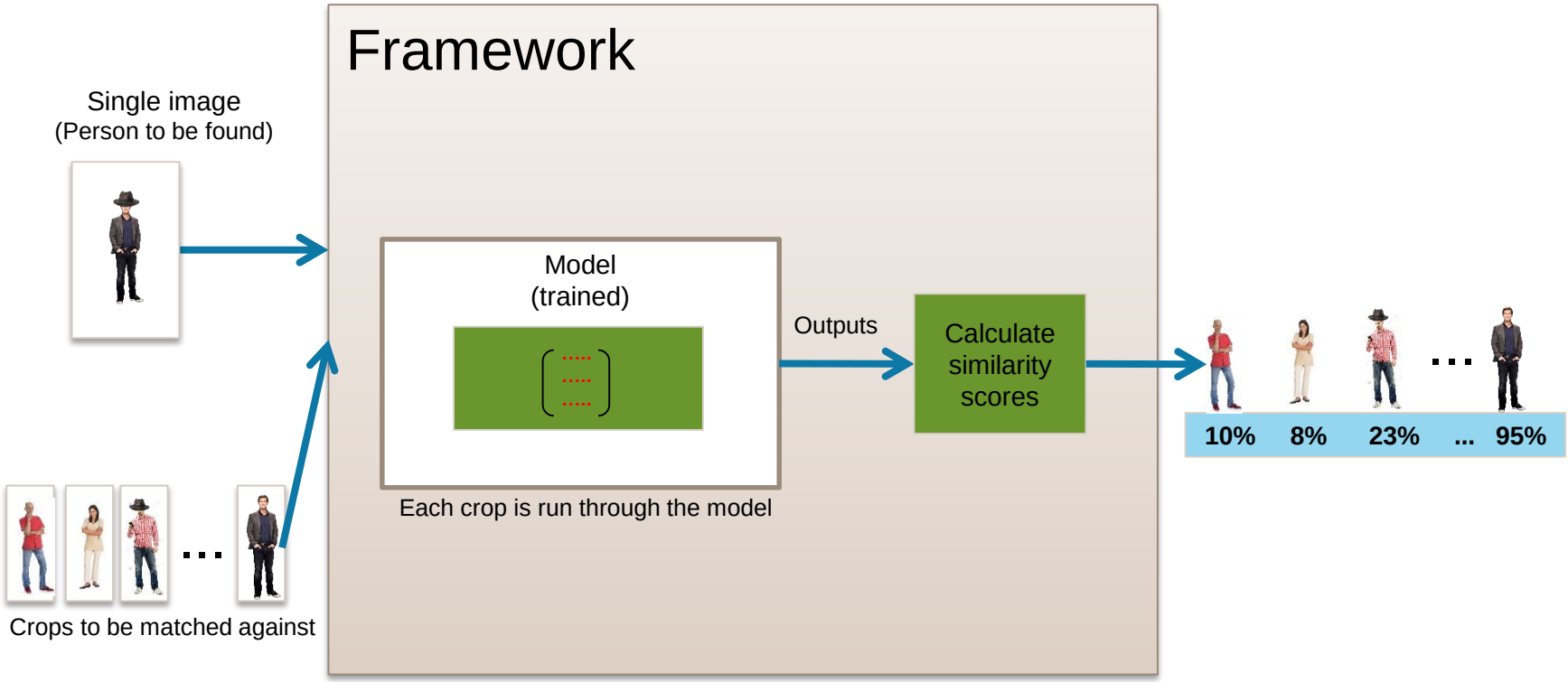


Training phase (in principle)



Framework used during training
- Executed on internal PC
- Done before deployment
- HW intense

Deployment (in principle)



On chip CNN

- Easy to build the forward path
- Requires a lot of memory storage and bandwidth
- Currently a parameter movement problem
- Hot research area
- Algorithm optimizations
  - Pruning
  - Compression
  - Retraining

Learn more about CNN

Stanford CS class CS231n:

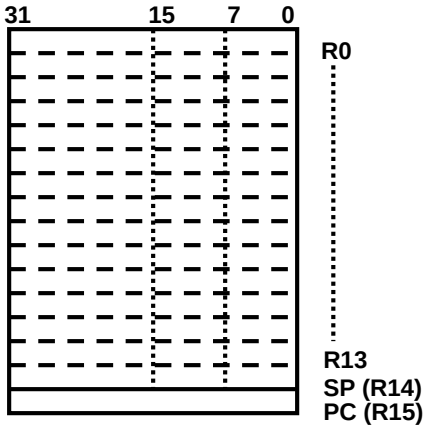
Convolutional Neural Networks for Visual Recognition

http://cs231n.github.io

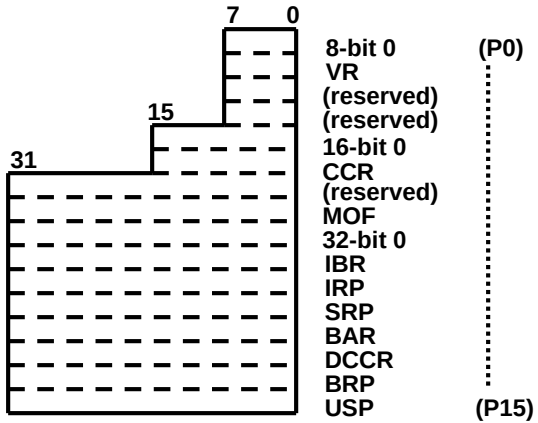
CRIS

CRIS CPU architecture

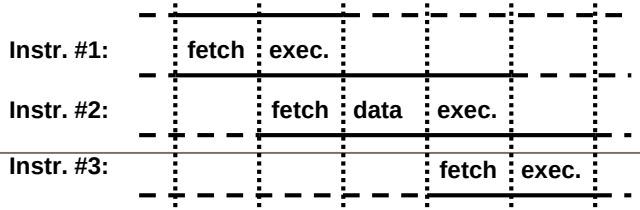
General Registers:



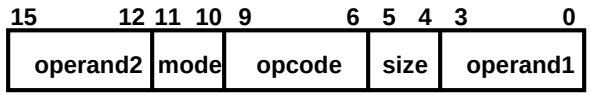
Special Registers:



Pipelining scheme:



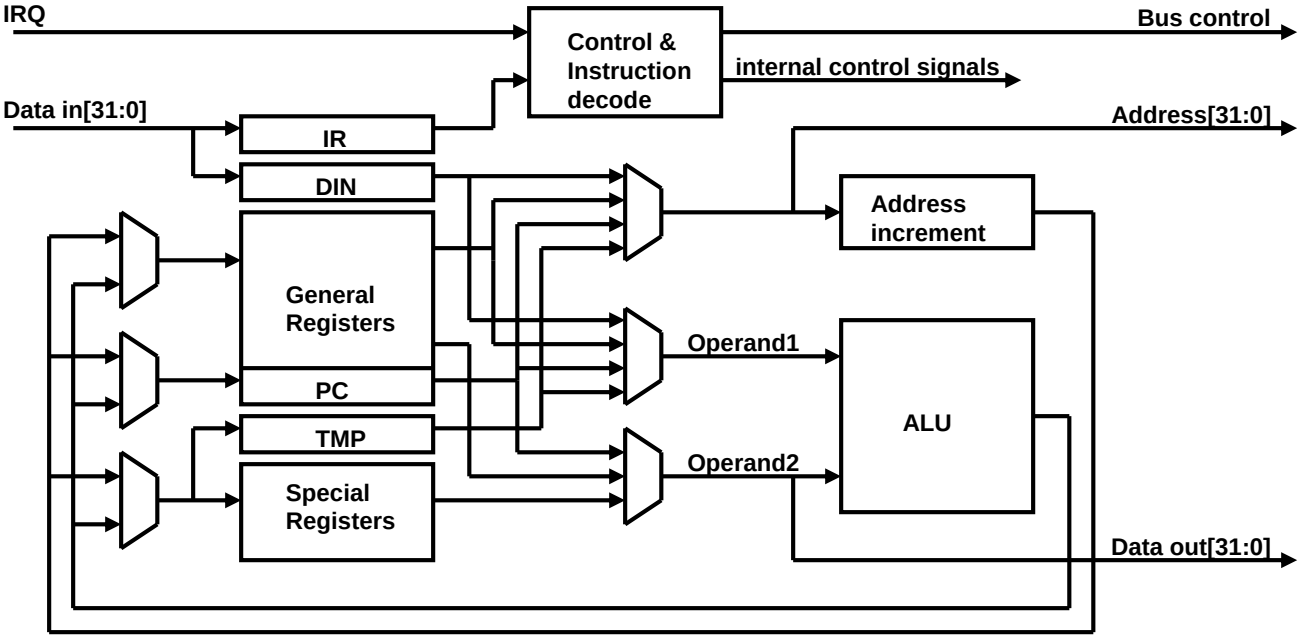
16-bit Instruction Format:



CRIS architecture history

- Development started in 1991.
- First implementation in silicon in ETRAX 1 (1993).
- GCC backend
- C/C Cache added in ETRAX 100 (1998).
- MMU and multiply added in ETRAX 100LX (2000).
- Part of the official Linux distribution
- Will be used in AXIS new camera controller chip (2001).

CRIS Block Diagram



Future of the CRIS architecture

- ASIC technology improvements will finally make the original architecture obsolete.
- Alternatives for future high end products:
  - Select a commercial core. (high cost, low flexibility).
  - Design a new architecture.
  - Improve the existing architecture. (Add more pipelining, multiple issue etc.)
  - Multi-processor approach. (Will have large impact on software design.)
- CRIS will still have a long life in low end applications. (e.g. man CPU offloading).

What to do if you start today

- Embedded processor market has matured.
  - You can find suitable and well supported cores for most applications today.
  - License and royalty fees are still rather expensive.
- Gate count is no longer critical.
  - The high gate count of the commercial alternatives can be accepted today, because the total area will still be small.
- Embedded memories change the scenario.
  - Large memories on-chip open up new architecture possibilities.

Security electronics

Example of security electronics

- Alarm systems
  - Property protection
  - Loss prevention
- Fire
  - Detection
- Gates
  - Automatic gates
  - Toll systems
- Communications equipment
  - Sound
  - Radio
  - Datacom
- Law enforcement
- Lighting
  - Visible
  - IR
- Camera systems
  - CCTV
  - IP Cameras
- Access control
  - ID’s, badges and readers
  - Door ctrl
- Vehicles
  - Equipment
  - Protection
- Locks
  - Doors
  - Safe
- IT security
  - Computer security
  - Network security
- Home automation
  - IoT
- Personal emergency
- Public safety
- Special equipment
  - Gas detectors
  - Radar
- Services

Trade shows

- IFSEC London
  - http://www.ifsec.events/international/
- ISCWest LasVegas
  - http://www.iscwest.com
- Security Essen Germany
  - http://www.security-essen.de/
- Conference/Seminars
  - Education
  - Certifications
- Exhibit
  - Meet the vendors
  - See the equipment

Alarm systems

- Technology
- Equipment
  - Detectors
  - Panels
  - Keypads
  - Wireless modules
  - GSM/3G callers
  - Lights/Sirens
  - Smoke generators
  - etc
- Vendors
  - 1000+ far east
  - Large western
    - Like www.dsc.com

New requirements

- > Wireless
- > App controlled
- > email, whatsapp notifications
- > Facebook/Google login
- > alarm.com compatible
- > ifttt.com/recipes (If this, then that)

Developing electronics

Development challenges

> Distance to production

> China

> Open source

> Free information

> Crowd founding (Kickstarter etc)

> Time to market

> Quality

Mandatory certifications

- UL
  - Certification for professional US market
  - The “Underwriters laboratories”
  - American safety and certification company
- CE-marking
  - Mandatory conformity marking for the European economic area
  - ***Conformité Européenne***, meaning **European Conformity**
- FCC compliance statement
  - Mandatory marking for all electronics
  - Federal communications Commission

Other certifications

- Consumer technology
  - HDMI, USB
  - WiFi
  - SD-Card
- 2G/3G/4G/5G
  - Carrier certification
- Vendor specific requirements
  - Apple Lightning
  - Apple App Review
  - Windows hardware certification
- Non mandatory testing
  - Technischer Überwachungsverein – TÜV
  - Technical Research Institute of Sweden - SP

- Technology license
  - Dolby
  - H.265
- Known difficult areas:
  - Onboard equipment for train and aircrafts
  - Vehicles

Trends

Consumer Electronics Trends

- **Staying Connected**
  - Consumers want to stay connected, at home and while traveling.
  - Portable equipment with the latest features (More important than ever)
  - Pokémon Go – Who is the real winner?
- **Media and Data Convergence**
  - Media-centric TV and the data-centric computer will merge.
  - New gadgets has to handle both types of tasks and be synchronized
- **In-Home Entertainment**
  - 1080p will be replaced by 4K
  - Video/Movies/Music on demand
  - User interface centric equipment
- **Smart home**
  - Embedded devices for everything
  - Smart/Cost-efficient device integration

More trends

- **IT**
  - Cheaper and better tablets and computers
  - Moving to App-oriented business models
  - Corporate cloud solutions
  - Wider use of P2P/streaming media
- **Mobile communications**
  - Phone will be user-interface for everything
  - Mobile payments (ApplePay/SamsungPay/Swish)
  - IPv6
  - Wearable devices (Google Glass failure, Apple Watch…)
  - Real time automatic voice translation
- **Other**
  - 3D printing going mature – and disappearing!
  - Autonomous cars and flying robots (Drones)
  - Screen technology (Large, Unbreakable, Bendable)

Industry Trends in Consumer Electronics

- Difficult to earn money on software
  - App-centric world
  - Customer lock-in
    - Force customer to the cloud
- Business critical technology development
  - Vertically oriented business trend
    - Apple, Microsoft…
  - Outsourced development is now moved home
- IPR
  - Patents

Ultra high definition

- Aggressive 4K rollout
- Old pixel technology (TFT, TN, IPS, etc)
- OLED is finally arriving, yield issues
- Quantum dots are enhancing LCD technology
- QLED = LCD + Quantum dot + LED backlight
- Every manufacturer has now 4K in production
- 50” and bigger
- 50% higher panel cost
- Apple is leading the hires conversion

Ultra high definition / 4K

- Easy in store demo:
  - Visible difference 0.5-2m from the screen
- Lack of content has never stopped set makers before
- Up scaling looks great
- Blu-ray benefit from 4K up scaling
- Ultra Blu-ray player launched at IFA 2015
- PC and consoles will soon be 4K
- Consumers want to be future proof
- Still images on 4K display is perfect
- 4K production is much more easy than 3D
- 4K display with proper content gives 3D feeling

Axis view on 4K / Ultra-HD

IP-Camera

Storage

Network

Viewer

4K

4K

RAID disk array

Server

2K

2K

2K

RAID disk array

4K

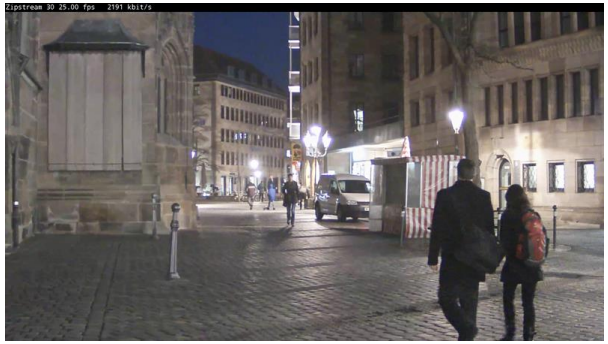
Innovative product portfolio

AXIS D2050-VE

Axis' Zipstream technology – More video, less storage

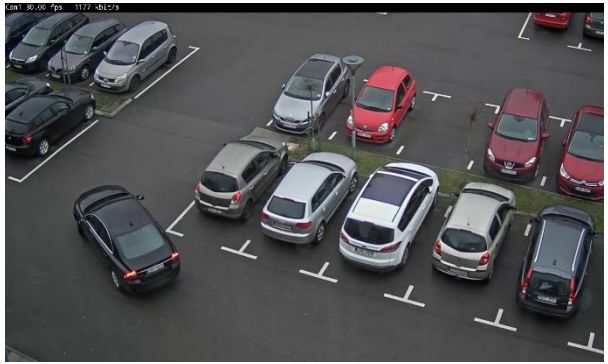
- Reduce storage and bandwidth by an average 50% or more
  - Optimized for video surveillance
  - Fully compatible with H.264
  - New unique method
    - Acts on motion, details and noise
  - Radically lowering bandwidth and storag
    - Keep the essence

How much do I gain?



City surveillance:
Street level recording with small movements most of the time

Zipstream strength:	Dynamic GOP:	
High	On	60%

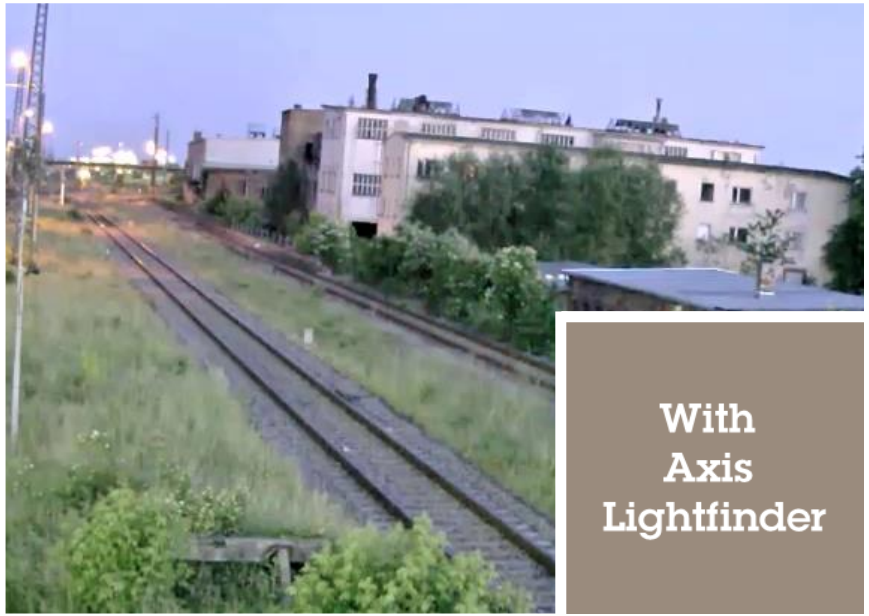


Outdoor VMD triggered recording:
Night time, average reduction for 12h surveillance.

Zipstream strength:	Dynamic GOP:	
High	On	75%

Lightfinder technology – an Axis innovation

Without Axis Lightfinder



With Axis Lightfinder

Extreme light sensitivity

Thermal network cameras – an Axis innovation

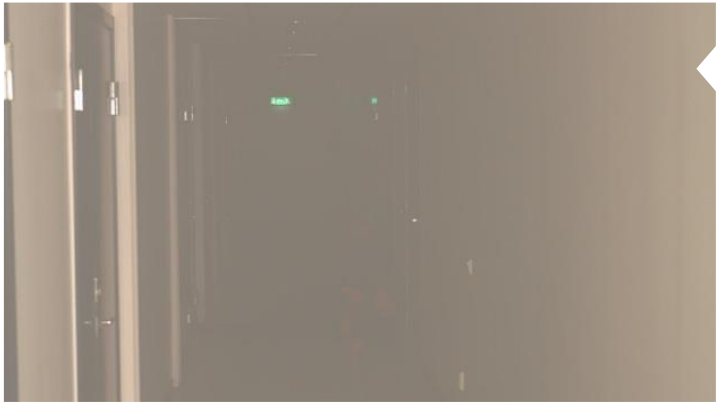
24/7 detection in tough conditions

> Bright lights

> Deep shadows

> Rain, snow and fog

> Smoke



Thermal camera OFF

Thermal camera ON


AXIS


Megapixel
Quality
Ease of use
Network video
Reliability
open
Innovation
Easy installation
Protect
Service
all the way
support
integration
Thank you!
Image
usability
Thermal
Convergence
HDTV
Access
control
World
Leader
Partners
Quality
Intelligent
Competence
Focus
Video
encoder
Safe
Cameras
Outdoor
Secure
Global