EITF35: Introduction to Structured VLSI Design

Part1.1.1: Course Introduction

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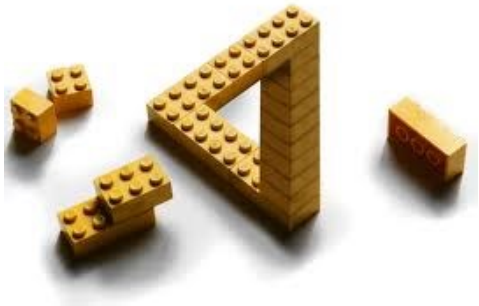
Course Factor

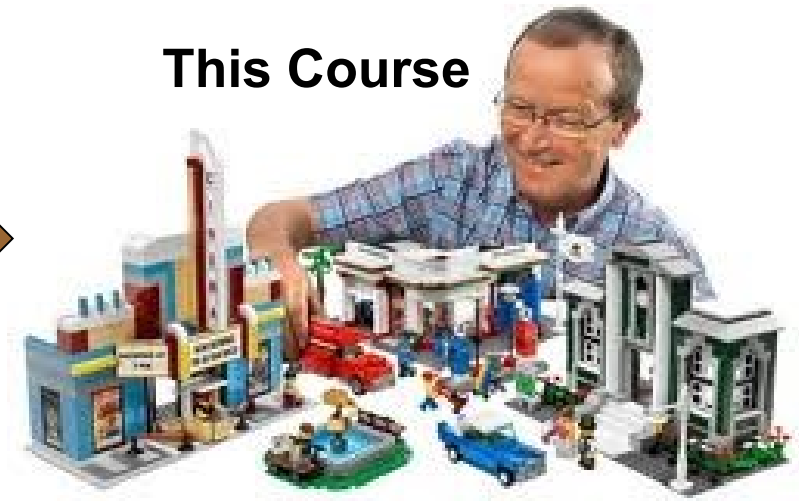
- **Introduction to Structured VLSI (very large scale integration) Design (7.5HP)**

http://www.eit.lth.se/course/eitf35

Digital IC



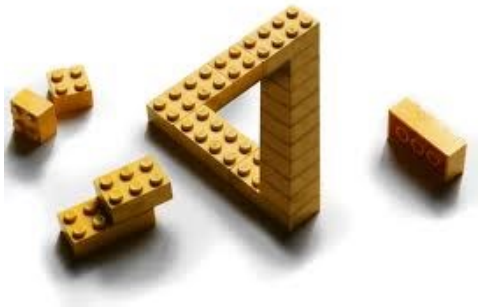
This Course



Taks1

- Build two identical houses (color does not matter)
- 3 min plan & discuss
- 30 sec build

Digital IC



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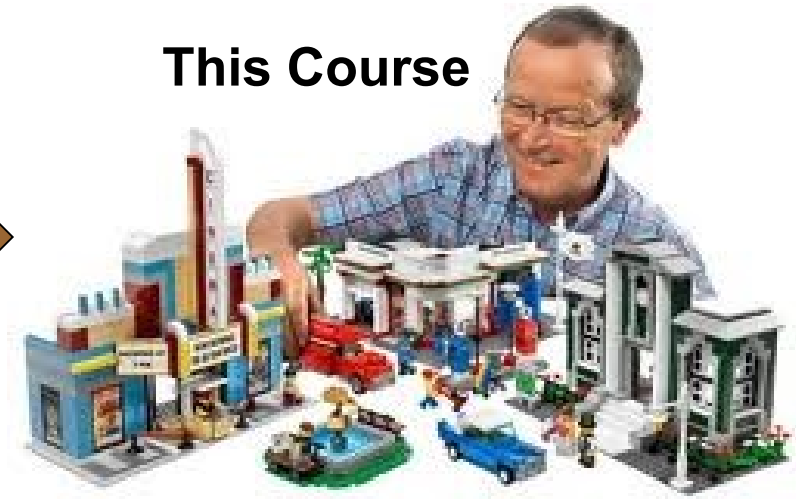


Structured design

- Know the basic building blocks
- Plan, know your design before coding
- Design flow
- Parallelism
- Hierarchic design, modules, IPs….
- Verification
- Design trade-offs, complexity, quality, time-to-market…
- ”Good enough” is the ”best” enginering
- Teamwork
- …

Outline

- Course Objective
- Teachers
- Lectures and Labs
- Language, Tools, Device
- Assignments
- Examination
- What's next

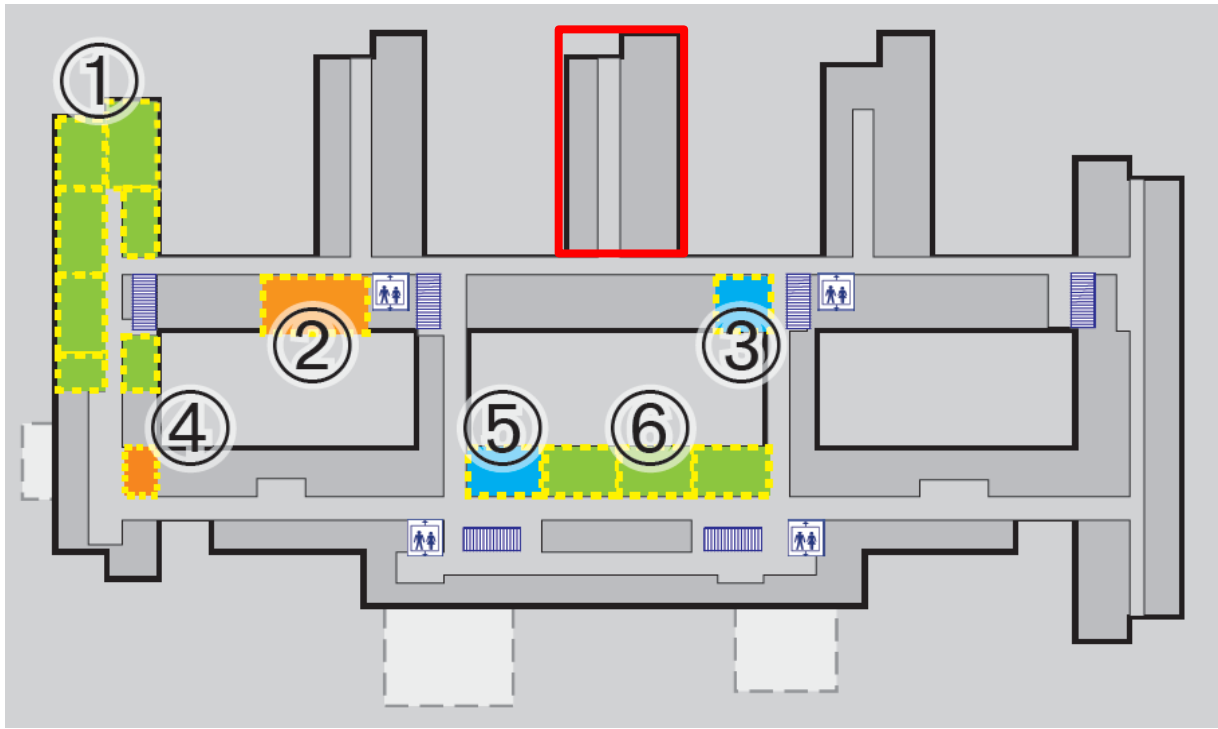
Course Objective

- **To introduce the basic concept and knowledge on digital VLSI realization**
  - Basic function blocks of a large digital system: controller (state machines), data-paths, storage elements
  - Optimization techniques for area, speed, and power
- **To provide the basic VHDL knowledge, design flow and (FPGA) tool training**
- **To provide hand-on digital VLSI design experience**
  - Fast prototyping several assignments and projects on commercial FPGA platform

Teachers

Lecture

- Liang Liu, Associate Professor
- Email: liang.liu@eit.lth.se
- Room: E2342
- Homepage: http://www.eit.lth.se/staff/Liang.Liu



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Teaching Assistants

- Jesus Rodriguez
- Lucas Ferreira
- Mohammad Attari
- Arturo Prieto
- Masoud Nouripayam

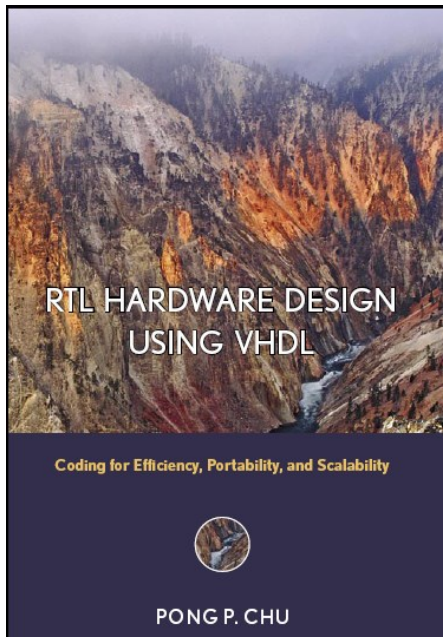
Book Recommendation

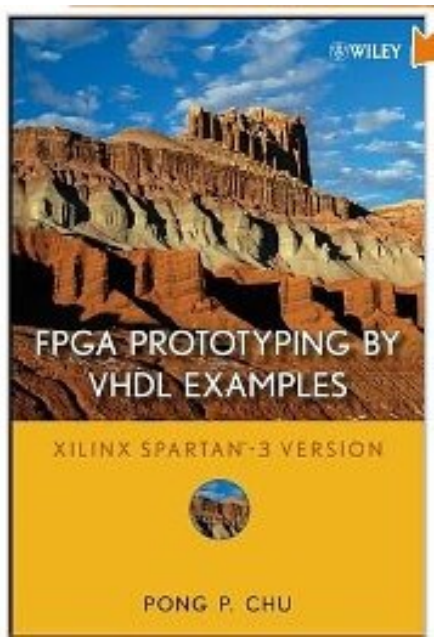
RTL Hardware Design Using VHDL

- Coding for Efficiency, Portability, and Scalability, Pong P. CHU

FPGA Prototyping by VHDL Examples

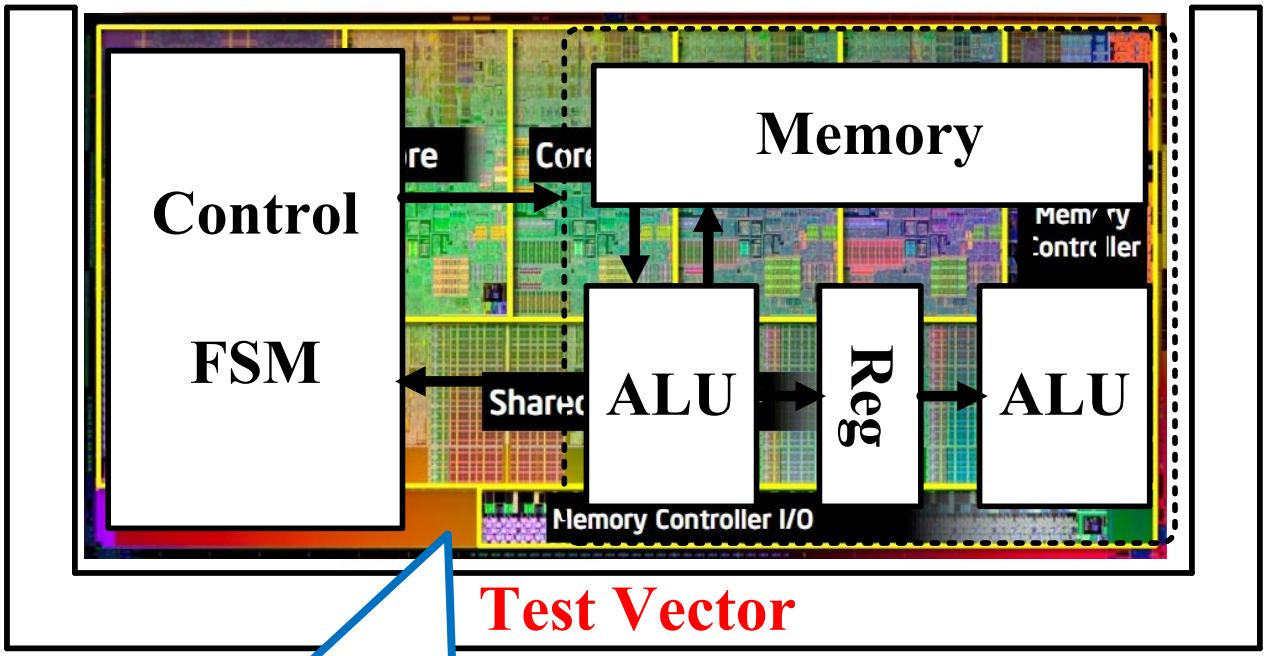
- Xilinx Spartan-3 Version, Pong P. CHU





Lund University Library

Course Content & Schedule



- Concept &Theory
- VHDL Knowledge
- Assignment & Project

- Overview
- Controller
  - FSM
- Data-Path
  - Combinational circuit
  - Sequential circuits
  - Storage elements
- Test & Verification
- FPGA
- Design Optimiz

Guest Lecturers

Guest Lecturers from Academia

- **Liesbet Van der Perre**, Professor, KU Leuven and Ulund
- **Erik Larsson**, Professor, EIT, on Design for test

Invited Lecturers from Industry

- **Torsten Larsson**, Digital Hardware IP, Ericsson Lund
- **Stefan Lundberg**, Expert Technologies Engineer, Axis
- **Shkelqim Lahi**, SoC Verification, Ericsson Lund

ERICSSON

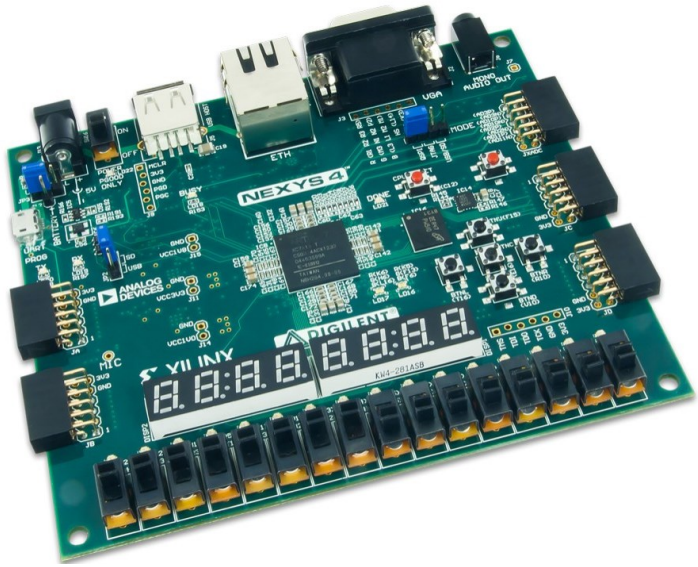
AXIS COMMUNICATIONS

Lectures and Labs

- Lectures (10)
  - Monday: 13:15-15:00
  - Tuesday: 13:15-15:00
  - Room E:2311
  - In the 1st Week an extra lecture will be given for Friday at 13:15
- Labs E:4121 TimeSlotA, TimeSlotB
  - Wednesday 10:00-12:00
  - Wednesday 13:00-15:00, 15:00- 17:00
  - Thursday 13:00-15:00, 15:00-17:00
  - Friday 08:00-10:00
  - Friday 13:00-15:00, 15:00- 17:00
  - Will present the assignments before the lab
  - Each time slot will have 2TAs helping with lab for 1 hour
- Labs are accessible 24/7 if not occupied by other courses
- You need to sign up for the lab before you can get access
  - Regisit as team of 2 students

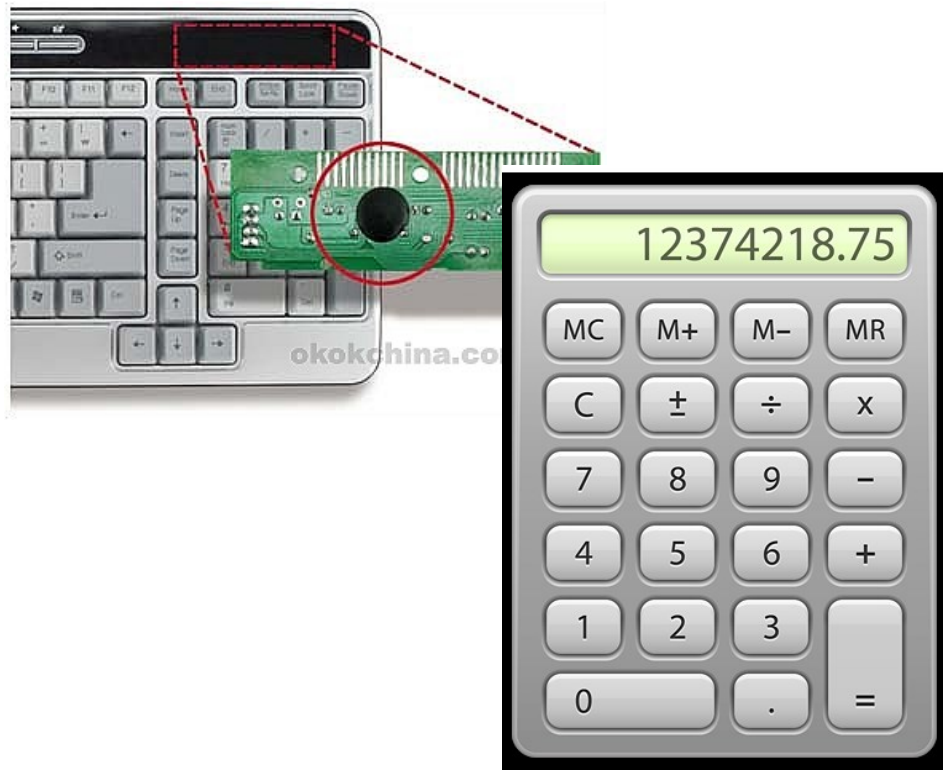
Language, Tools, Device

- **Language**
  - VHDL (Verilog) will be used to develop the circuits
- **Tools**
  - Xilinx Vivado
- **Device**
  - XILINX Nexys 4



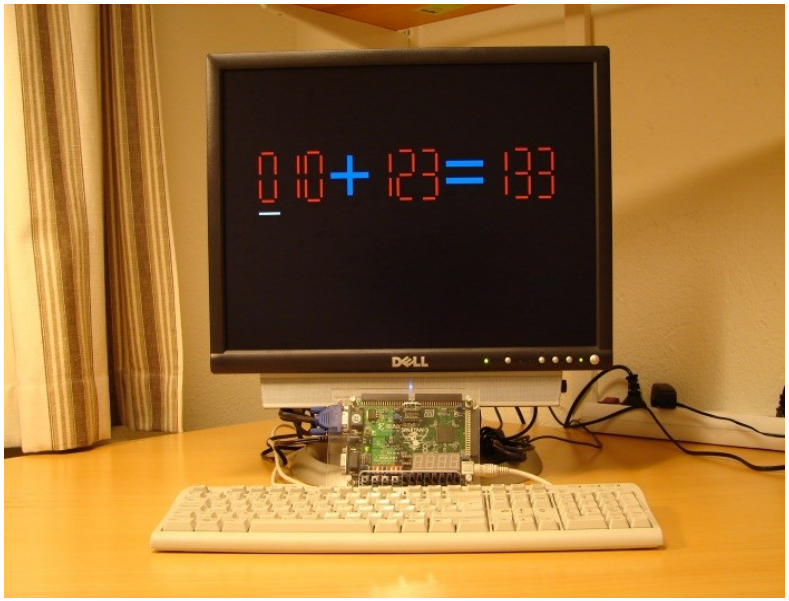
Assignments

- **To pass the course, 3 assignments need to get approved**
  - Sequence Detector
    - ***Simulation***
  - Keyboard Controller
    - ***FPGA implementation***
  - Alrithmetic Logic Unit (ALU)
    - ***FPGA implementation***

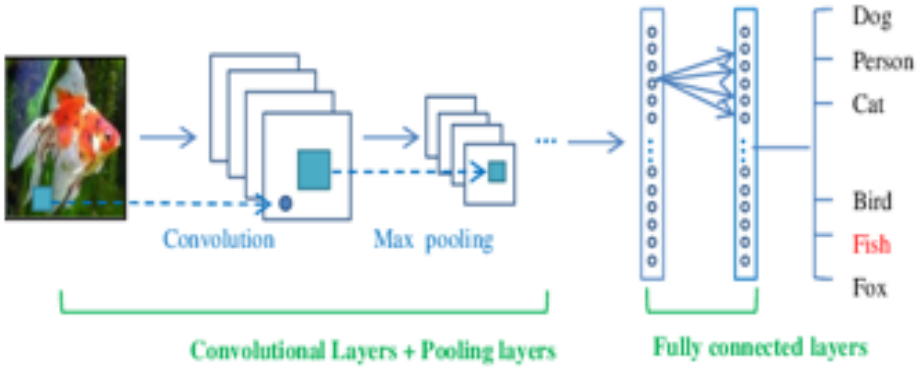


- **Assignments approved in time will result in grad**

Assignments cont'd



- **Extra projects are required to get grade 4 /5**
  - FPGA implementation (4)
    - ***ALU with input memory***
    - ***ALU output on VGA***
  - Advanced arithmetic funtion in the ALU (5)
    - **CORDIC** (for Coordinate Rotation DIgital Computer)
    - ***Area/timing***
  - Open Project (4 & 5)
    - ***Convolutional Neural network (CNN)***



Examination

Before the lab

- All assignments must be prepared and handed in
- Without preparation you are NOT allowed to continue the lab

Examination cont'd

Design Approval

- **All assignments must be demonstrated to the TA's to get approved before deadline**
- **Students need to demonstrate their understanding of the assignment to get it approved**
- **Graded as a team, but individual grading may be applied if an "unbalance" is discovered**
  - Both team members need to be present at design approval
  - Oral test will be given to **BOTH** team members

Examination cont'd (new from last year)

Good news

Before

- Assignment 1
  - ***Deadline 1***
- Assingment 2
  - ***Deadline 2***

  ...
- Assingment 5
  - ***Deadline 5***

This year

- Assignment 1
- Assingment 2

  ...
- Assingment 5

- ***Deadline: Nov, 1st 17.00***

Examination cont'd (”new” this year)

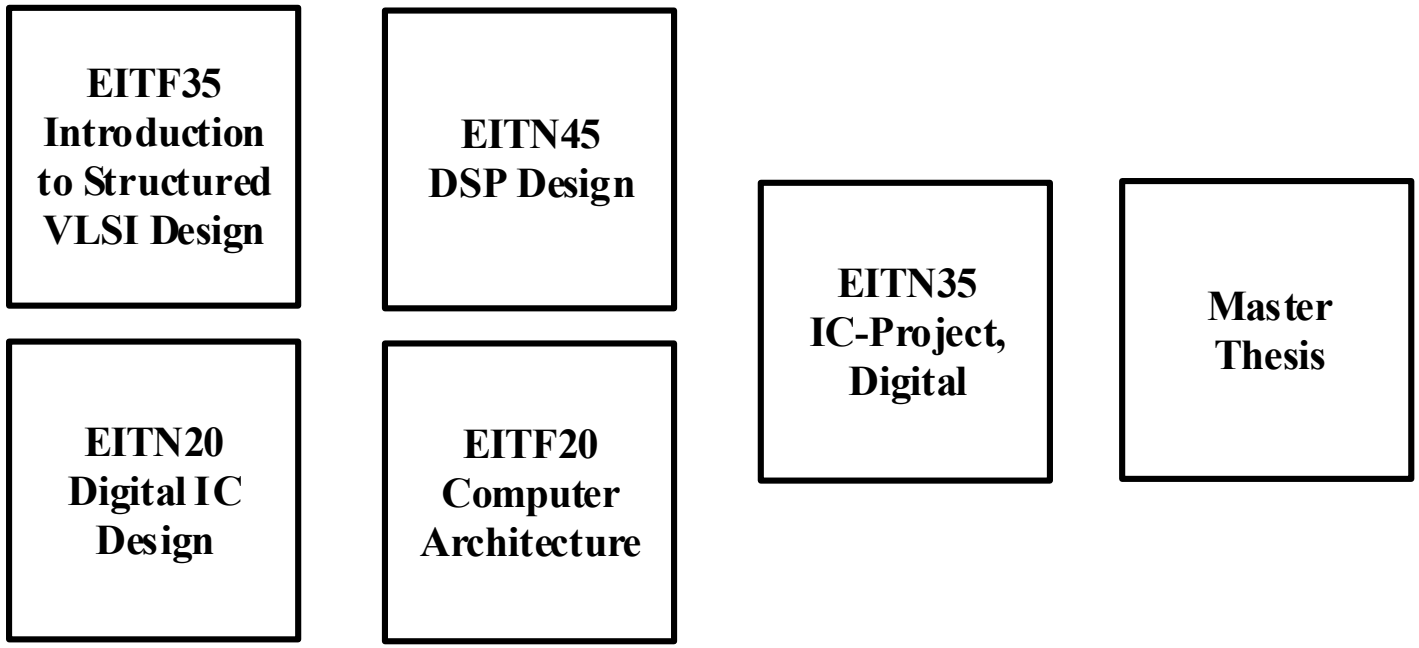
”Bad” news

- **Very strict check during project approval**
  - Application of learned knowledge
  - Good HDL coding style
  - Understanding of circuits and timing
  - Check list (but not limited to) for each Lab
  - Report needed for Lab4 & 5
  - ...

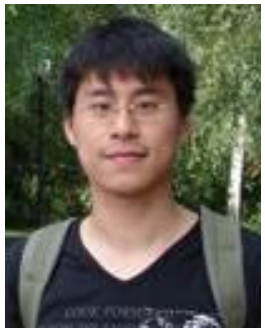
Next Step

What can we do after finishing this course?

Digital Path



Digital Path



Chenxin Zhang

Intro. VLSI (mouse control)	DSP Design IC Project Comp. Arc. (MIPS processor)	Master Thesis (multi-core MIPS)	PHD (Processor for 4G)	MediaTek (Processor for 4/5G)	Ericsson (5G Processor)

Projects and Thesis (industry)

FINGERPRINTS

Mistbase: low-power IoT chip

The acquisition

Mistbase is Lund-based startup that develops less expensive hardware and software for wireless communication between connected devices. Founded in 2015 by Michal Stala and Magnus Midholt together with Lund University's holding company, LU Holding AB, Mistbased has now been acquired by hardware giant ARM.

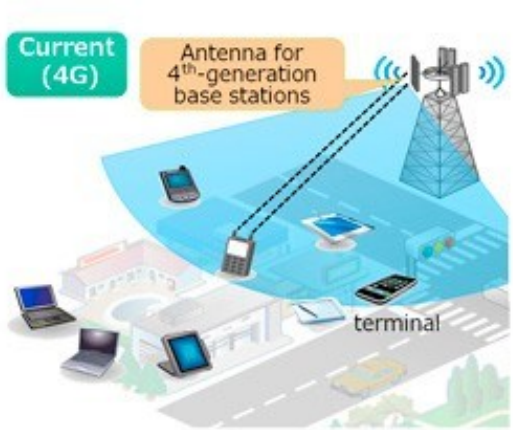
Neither party shared the details of transaction, but in April last year Mistbase took in 4 million SEK (400 000 euro) investment from Johan Qviberg Qiunary (NTL), Minc's former CEO Marten Öbrink (NTL), Body Trace-founder Andy Ketskes (NTL) and business angel Anders Berglund (NTL). Then the company was valued at 20 million SEK (2 million euro). According to DiDigital, the investment seems to have given a return of 6-8 times. Reportedly, the deal landed somewhere between 120 and 150 million SEK (12-15 million euro).

Research at EIT

Leading 5G and beyond research

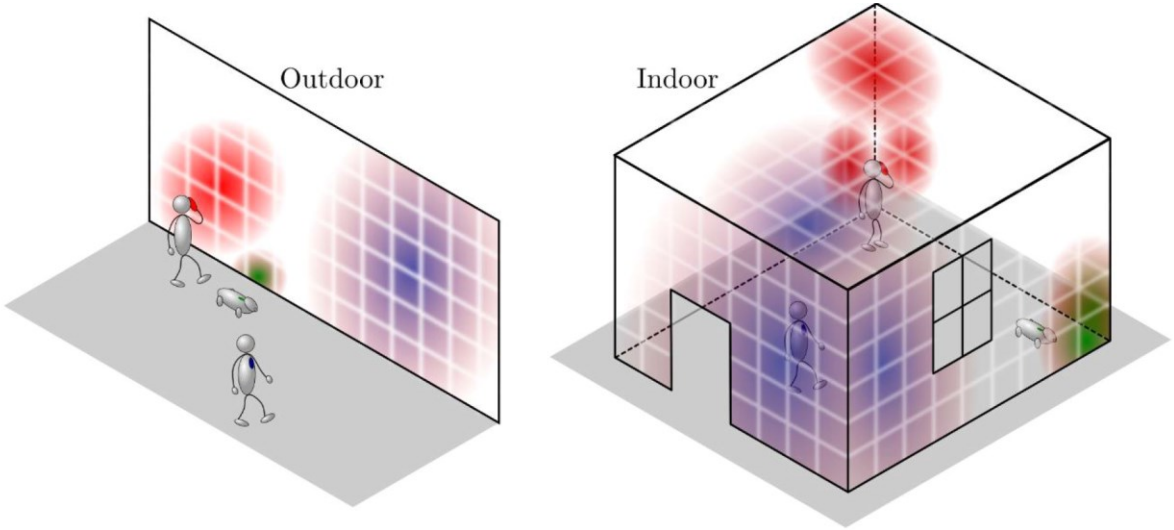
Bristol and Lund once again set new world record in 5G wireless spectrum efficiency

Press release issued: 17 May 2016



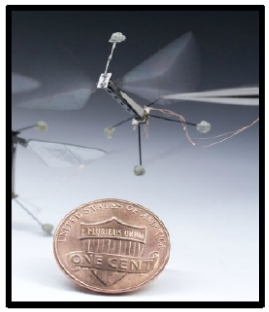
Research at EIT

Leading 6G research



Research at EIT

AI & Autonomous Vechicles



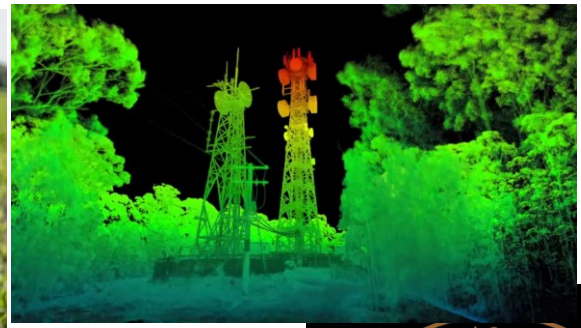
Insect-scale UAV (100mg)

Lifting	Sensing	CPU, GPU
100 mW	100 mW	10 - 100 W

Delivery

Agricultural Support

Mapping



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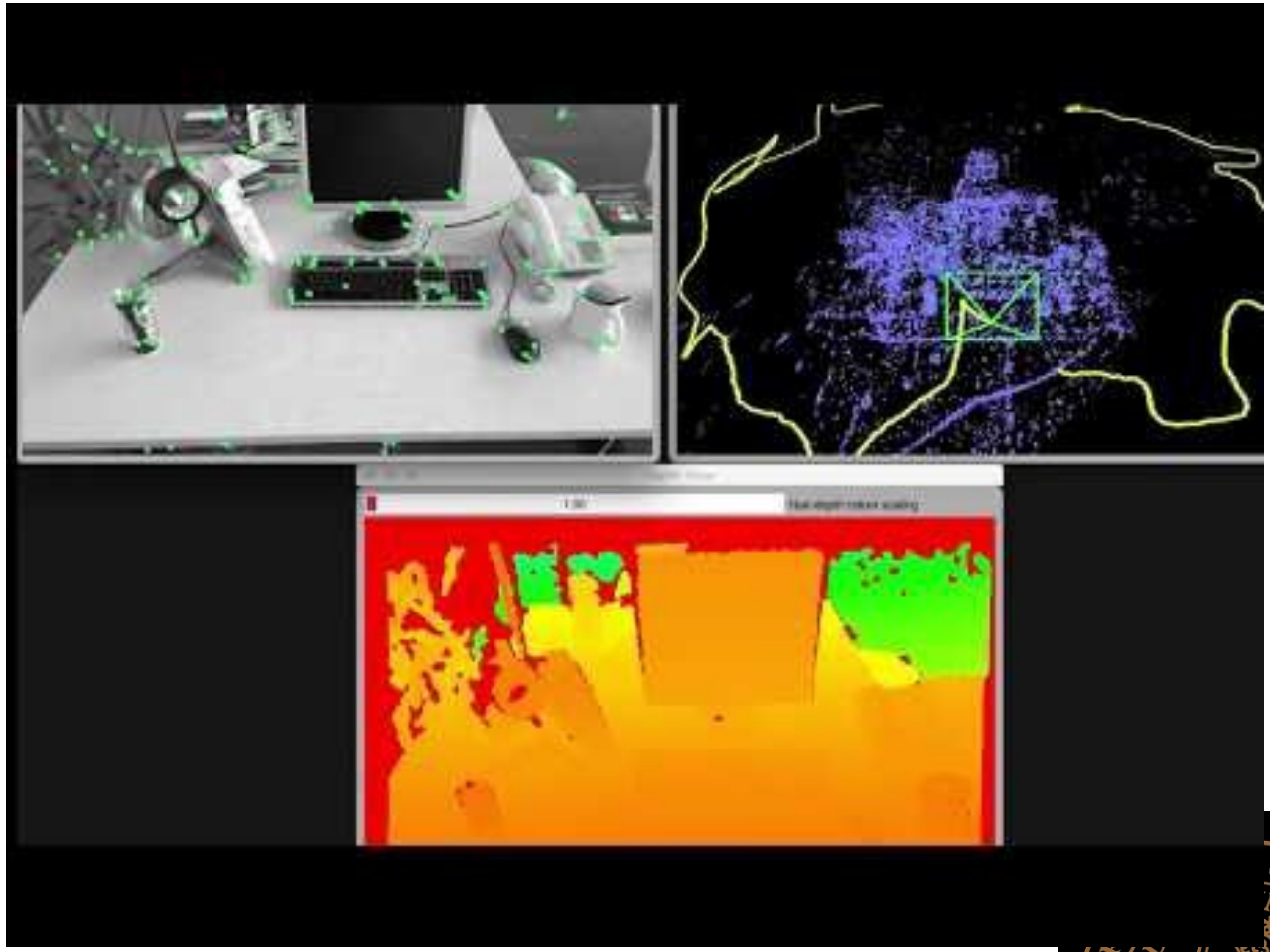
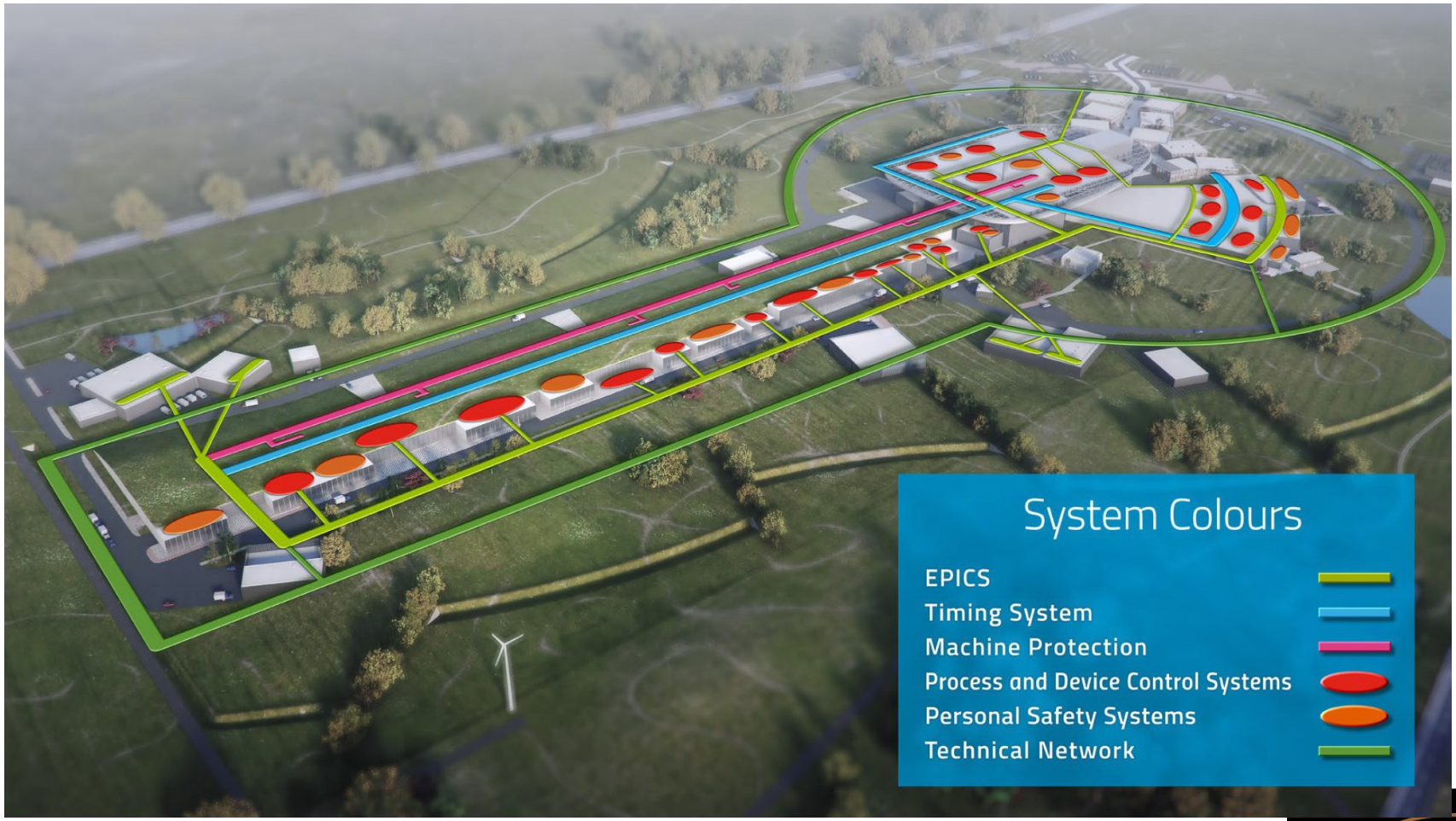


Projects and Thesis
(Other Deartments of Lund University)

- Chemical Physics: Ultra-fast laser measurement
- CERN: Implementation of readout system for a prototype detector in particle physics
- ESS: Particle simulation on hybrid computing platform

ESS


System Colours
EPICS
Timing System
Machine Protection
Process and Device Control Systems
Personal Safety Systems
Technical Network

Other Opportunities

ISCAS 2017

NORCAS

JTRES 2016
29 Aug. - 2 Sept.
Lugano, Switzerland

International Conference and Journal

Xilinx FPGA and SOC University Design contest

The Xilinx Open Hardware Design Contest gives students the opportunity to showcase their technical and creative skills.

There are two project categories:

- **Embedded Design**
- **Digital design**

A prize of €1500 will be awarded to the best PhD, and under-graduate project in each category (4 prizes in total).

The winning participants will also receive sponsored travel to the Open Hardware awards ceremony in August 2016.

Questions?