



arm

Introduction to structured VLSI design

# Guest Lecture

2017-10-09

# Agenda

- About Arm
- What is Verification
- Day-to-day challenges of a Verification Engineer
- A story from “real life”
- Wrap up and Questions

# Who am I?

LTH 98E

- “Introduction to VLSI design” meant pushing around rectangles
- Strong SW focus: Algorithms, more algorithms, functional programming, OO, compilers, ...

19 years in ASIC industry

- SwitchCore (networking), eSilicon (service), Ericsson (wireless), ARM (video, graphics)
- System design, digital design, verification, project, product and line management
- Finally back to verification
- Verification is a great entry point to an organisation
  - Get to know the system means get to know the product, the organisation and, sometimes, the customers

# About Arm

What does Arm do?  
What do you know about Arm?  
Do you own an Arm based product?





# Arm Technology

- Advanced consumer products are incorporating more and more ARM technology – from processor and multimedia IP to software

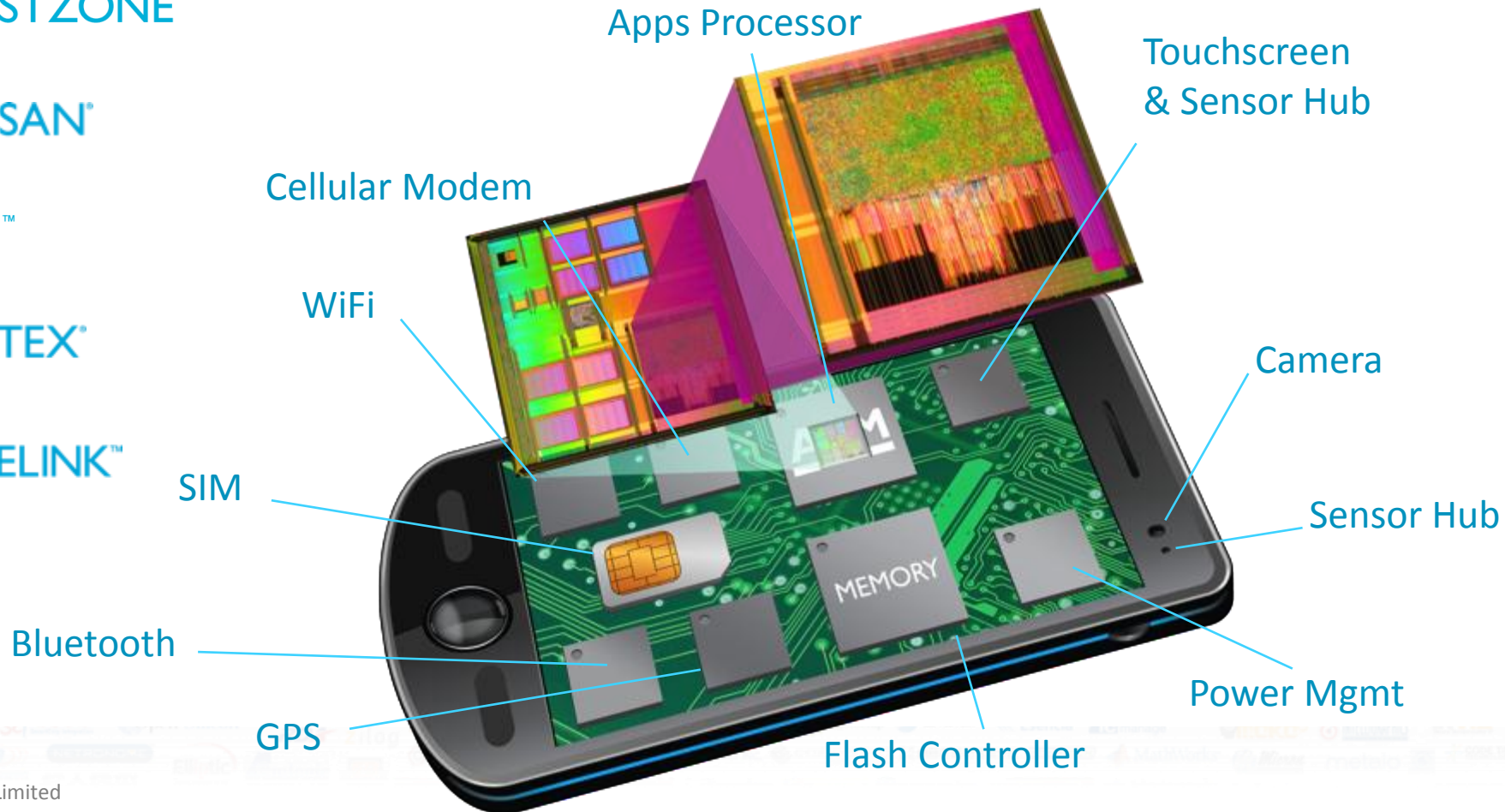
**ARM® TRUSTZONE®**  
System Security

**ARM® ARTISAN®**  
Physical IP

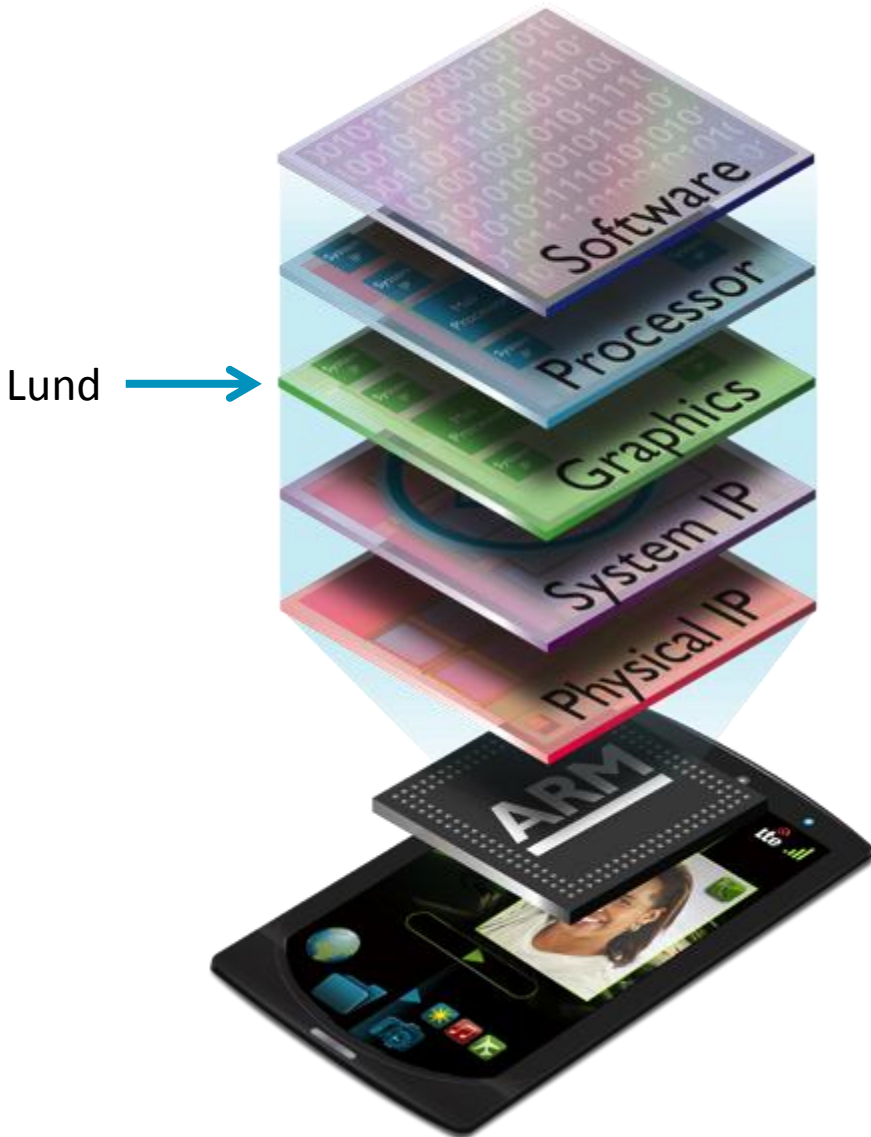
**ARM® MALI™**  
Visual Technology

**ARM® CORTEX®**  
Processor Technology

**ARM® CORELINK™**  
Processor System IP



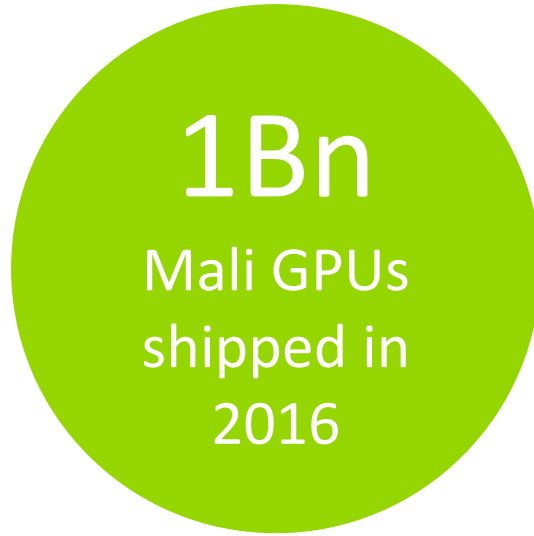
# What do we do, in Lund in Specific?



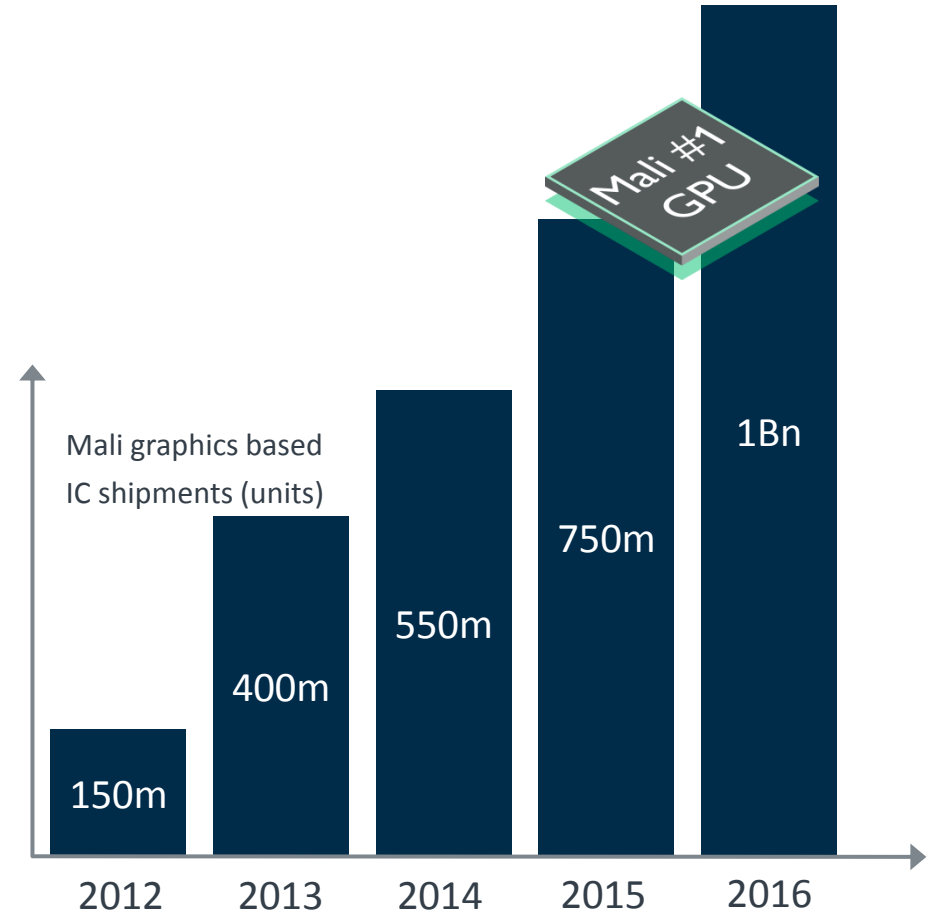
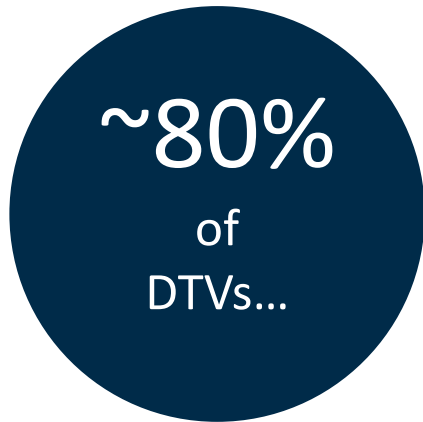
- Part of MPG – Media Processing Group
- Products:
  - Mali GPUs and VPUs
  - IoT wireless radio (Mistbase)
- HW engineering
  - System design
  - RTL design and verification
  - Content validation
- SW engineering
  - Functional and performance models
  - Firmware, driver, compiler, etc...



# Arm Mali GPUs: The world's #1 shipping graphics processor



Mali GPUs are in:



# Arm's Partnership Model



Arm's partners shipped nearly **15 billion** chips with ARM technology in 2015.

Over **86 billion** chips accumulated over 26 years

# Arm Offices Worldwide



# What is verification?

## - and why is it important?

# What is verification?

A development project is a set of translations/interpretations of documents

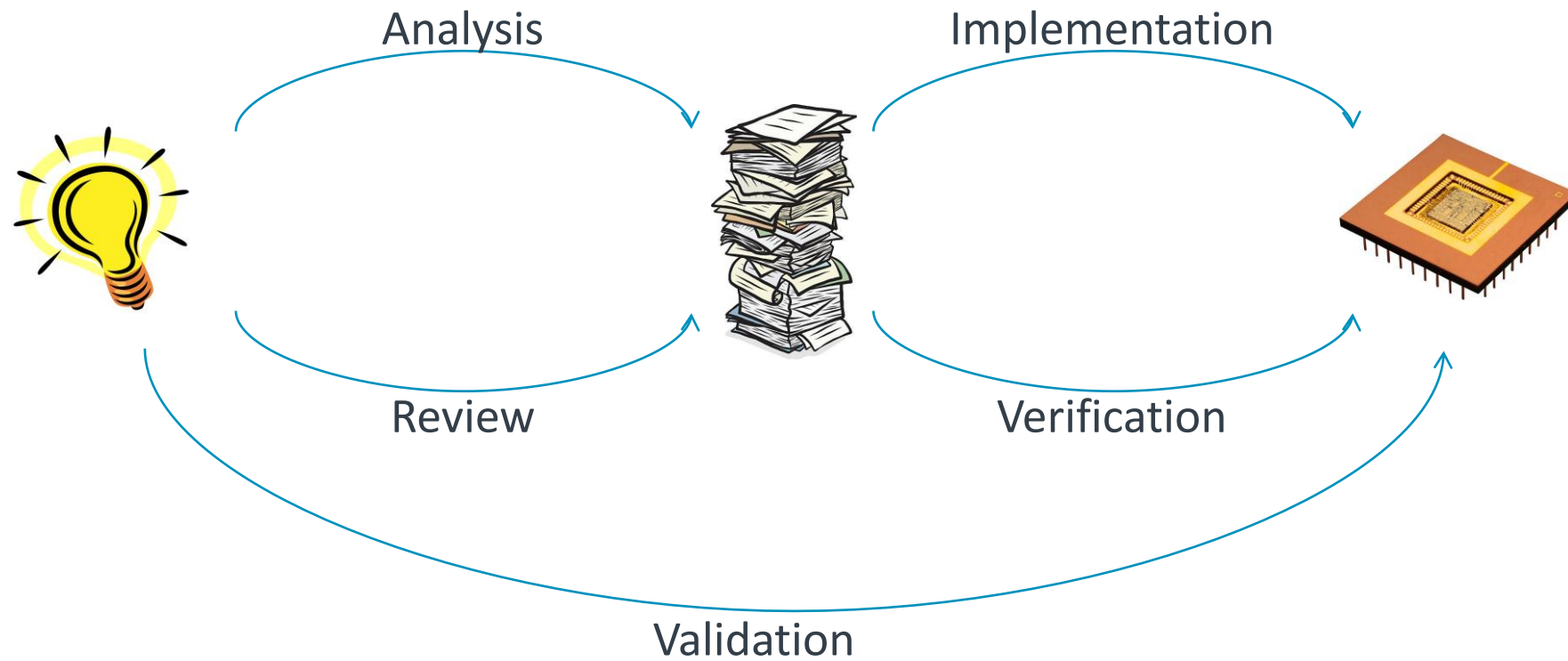
Each step has a number of constraints, e.g. size, speed and power

Verification is to independently confirm that a step has been executed correctly

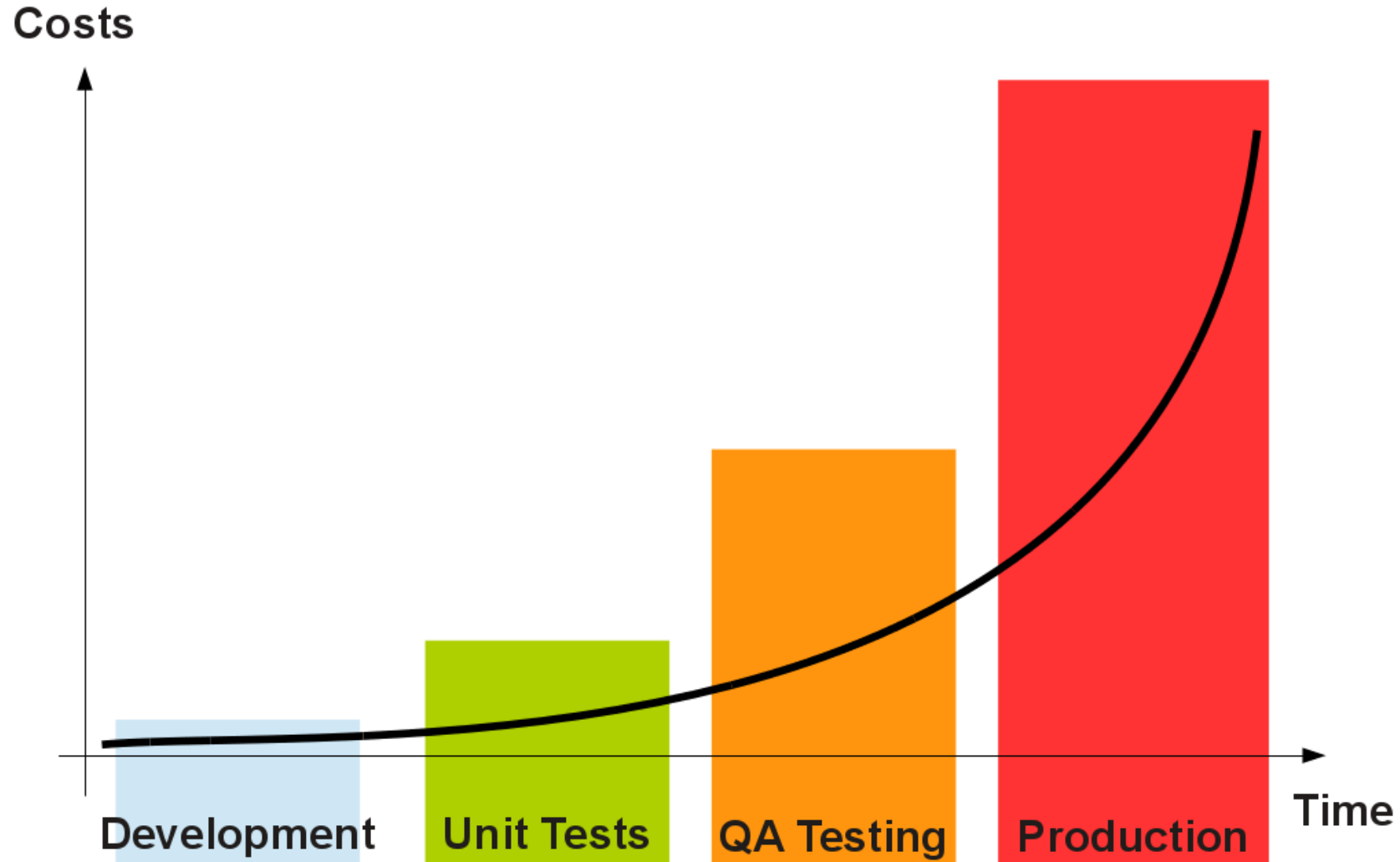
“A product will always be verified, either by you, or by the customer.”

“A man with a watch knows what time it is. A man with two watches is never sure.”

# Verification is everywhere



# Find bugs as early as possible



# Industry trends in functional verification

Verification engineers outnumber and outgrow design engineers

Design engineers spend half their time doing verification

SystemVerilog is most common language for verification

UVM is most common methodology for verification

Complete study available from Mentor Graphics



# Intel floating point division bug

Problem: 0.001% error in some floating point calculations

- Q: How many Pentium designers does it take to screw in a light bulb?
- A: 0.99904274017, but that's close enough for non-technical people.

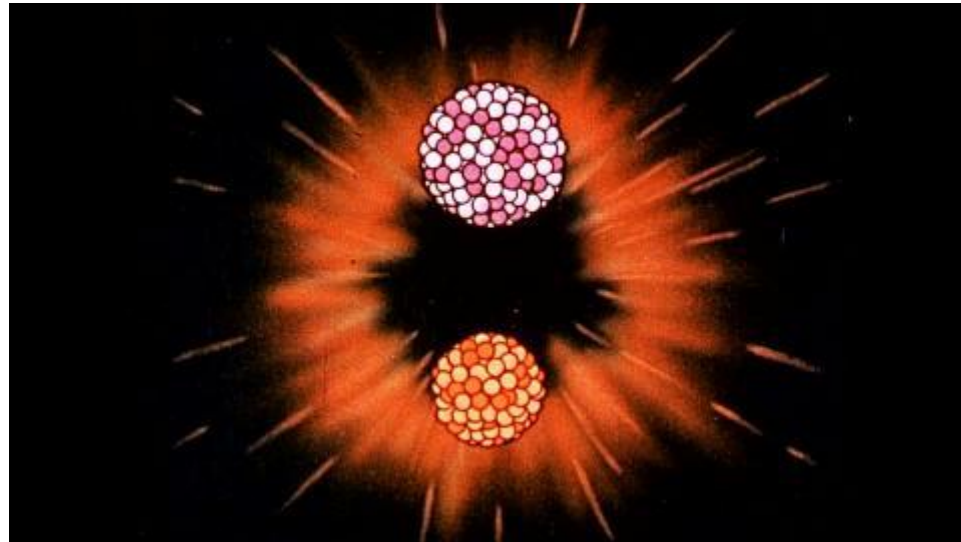
Solution: Make key-chains for employees



# AMD Phenom TLB bug

Problem: The processor operation to change the accessed or dirty bits of a page translation table entry in the L2 cache from 0b to 1b may not be atomic.

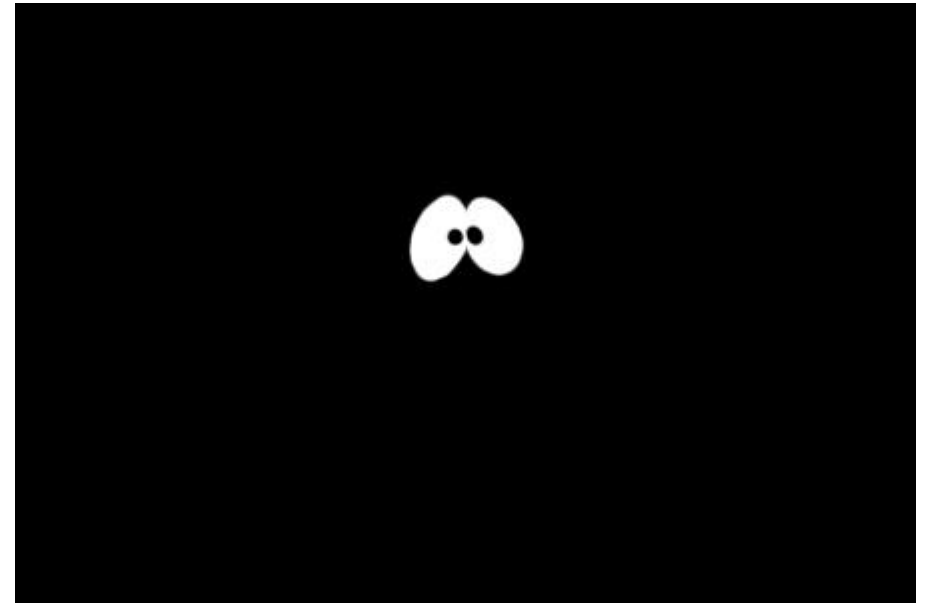
Solution: Workaround using other TLB bits, resulting in some performance hit



# Intel 820 Memory Translator Hub bug

Problem: The Memory Translator Hub can, while doing simultaneous switching, produce noise that may cause the computer to hang mysteriously or to spontaneously reboot

Solution: Recall all chips

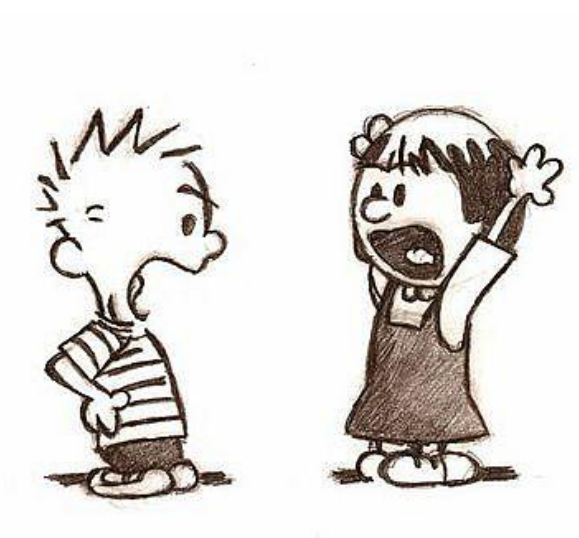


# Mars Pathfinder priority inversion bug (SW)

Problem:

- The low priority process holds a resource that the high priority process needs
- But the high priority process stops the low priority process from proceeding

Solution: Enable priority inheritance (remotely, through sw backdoor)



# ARM Cortex-A53 load/store bug

Problem: A load or store might access an incorrect address

- Under very specific circumstances!

Solution: Scan mobile apps and update code to avoid sensitive instruction sequence



# Day-to-day Challenges of a Verification Engineer

# Verify a calculator

Input: 16 buttons

Output: 64 LCD segments

State: ~32 bits

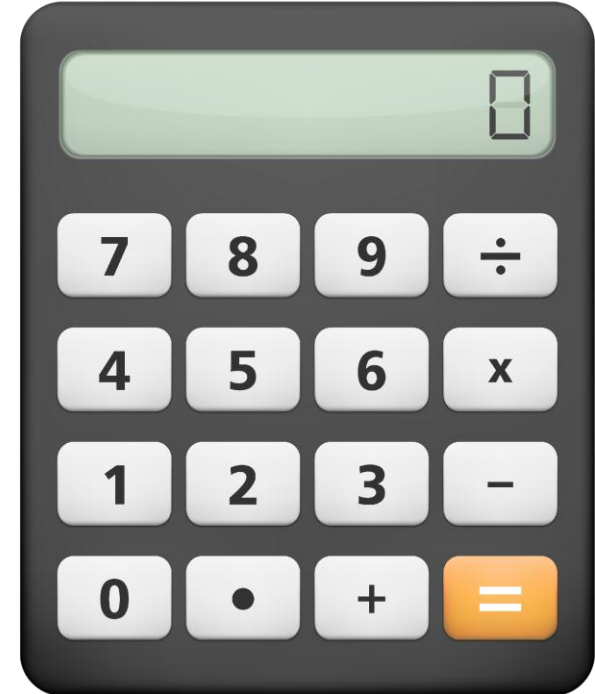
Users: 1

Exhaustive:  $1+1=2$ ,  $1+2=3$ ,  $1+3=4$ , ...

Toggle coverage:  $1+1=2$ ,  $2+2=4$ ,  $4+4=8$ , ...

Is there a better way?

How do you know when you have tested enough?



# Verify an IP block

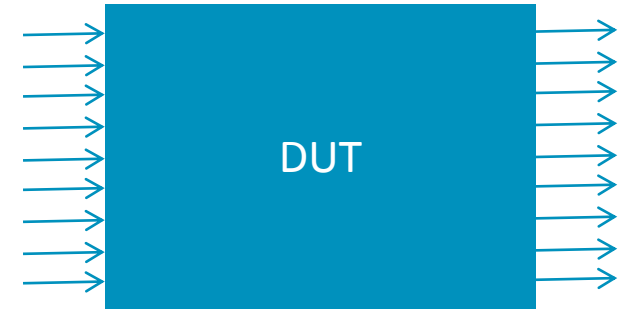
Input: ~250 pins

Output: ~250 pins

State: ~1000 bits

”Users”: ~20

Modularisation, abstraction, structure, ...





# Verification skills

## Mind set

- Curious – Take things apart, break them down
- Meticulous – “Which one is right? It must be this or the other!”
- Systematic – Modularisation, abstraction, structure, ...
- Prestigeless – You’re not measured in how many bugs you find, but how many bugs the customers don’t find

## Skill set

- System, hardware and software design
  - Data structures, multi-threading, scripting, LRM
- Domain knowledge
- Project management
  - Manage requirements, balance time and effort
- People skills
  - Interact with many stakeholders

# General verification advise

## Design re-usable components

- Re-use improves quality by increased usage
  - Re-use can be temporal (between projects) or spatial (between test benches)
- Separate active and passive parts
- Separate transaction and pin-wiggling parts

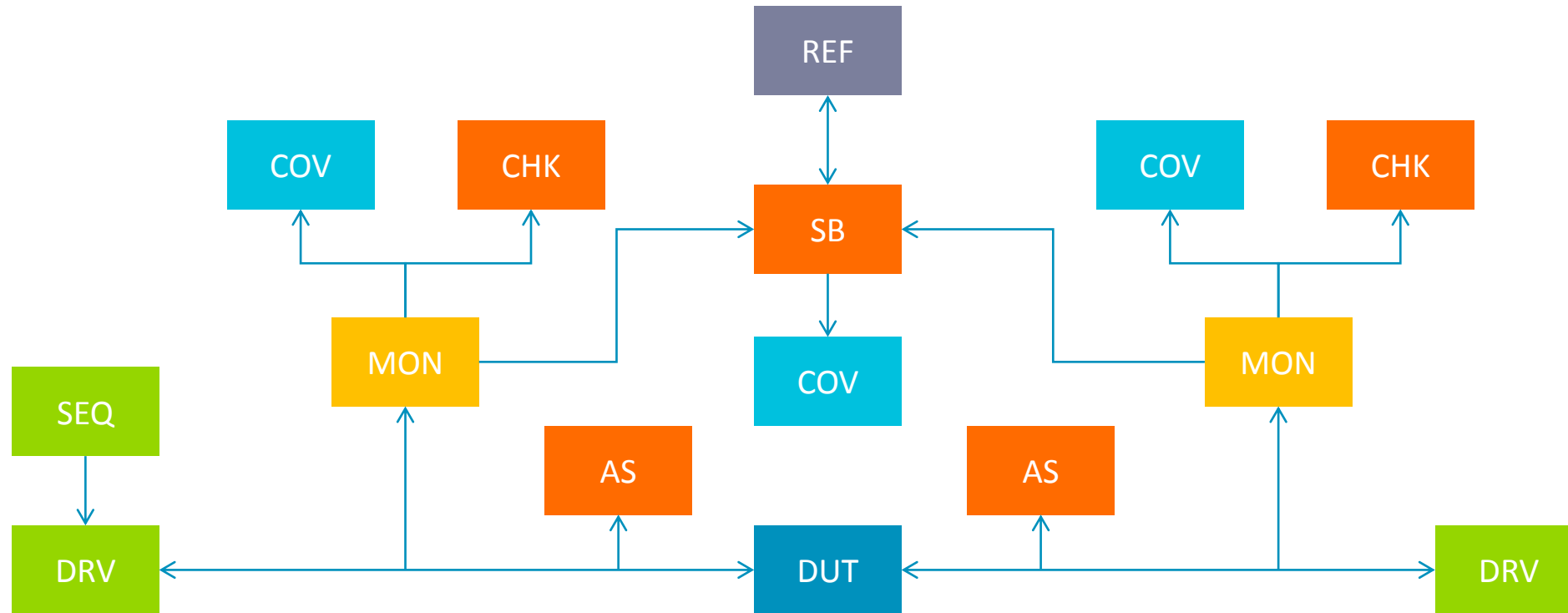
## Keep it simple

- Verification constraints are different than design constraints
  - Readability, maintainability, debugability, correctness
  - Timing, area, power

## Better safe than sorry

- If “evidence of OK” then OK else FAIL

# Testbench structure



# What were all these abbreviations?

DUT – Device Under Test

DRV – Driver

- Constrained random stimuli generation
- You cannot think of all possible scenarios
- Constrain to valid transaction and specific use case

SEQ – Sequence

- Abstract high-level transaction, e.g. RAM access, Ethernet packet

AS – Assertion

- Executable specification, written in SystemVerilog
- Checks protocol (pin-wiggles)
- Automatic, triggered by event

MON – Monitor

- Collects pin-wiggles into transactions

CHK – Checker

- Checks a transaction (values, transitions)
- Automatic, triggered by event

COV – Coverage

- Evidence that certain function has been exercised

SB – Scoreboard

- Keeps track of outstanding transactions

REF – Reference Model

- Executable specification, written in regular software programming language like C++

# Design for Verification

Divide and conquer

- Smaller modules are easier to verify

Black box approach

- Consistent on boundary
- Magic happens inside

Standard interfaces and components

- AMBA, SRAM, READY/VALID, REQ/ACK
- RAM, FIFO, FSM

No exceptions!

- Save now in power, timing or area
- Pay later in debugability, maintainability and uncertainty

# Day to day tasks

Clarify specifications

Implement new features

Debug failures

Debug tools

Optimize performance

Review others code

Learn and develop best practices

Plan for future projects

# Fika



# A story from “real life”



# Wrap-up and Questions

# Opportunities

Internships - [www.arm.com/careers](http://www.arm.com/careers)

- Part time during a semester or full time during summer

Thesis - [student-se@arm.com](mailto:student-se@arm.com)

Graduate positions - [www.arm.com/careers](http://www.arm.com/careers)

Want to know more?

- LTH Pit stop – October 10<sup>th</sup> (tomorrow!)
- ARKAD – November 15<sup>th</sup>-16<sup>th</sup>
- Teknikfokus – February 2018
- [student-se@arm.com](mailto:student-se@arm.com)

# Our jobs and how to get there

## Hardware design

- Digital electronics, computer architecture, algorithms

## Firmware design

- Software design, embedded systems, algorithms, real time systems

## Driver design

- Software design, embedded systems

## System test

- Software design, embedded systems, digital electronics

## Hardware implementation

- Digital electronics, analog electronics

## Hardware verification

- All of the above

# Resources

## Verification

- Verification Academy
- EDA Playground
- IEEE 1800-2012 (SystemVerilog specification)
- Accellera UVM
- Doulos

## Design, industry news, ...

- OpenCores
- SemiWiki
- [www.arm.com](http://www.arm.com)

# Questions?

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