INSTRUCTION MANUAL FOR CNN LAB

FILE CONFIGURATIONS:

1. Each module comprises of the following files:
    - **Behave_vhdl** : Functional simulation representation of the IP's
    - **Constraints** : Clock Definition for the respective module
    - **edif_to_ip** : Design Netlist
    - **xcix** : IP management file
2. You are expected to use files in behave_vhdl by creating test benches and understand the simulations in order to mimic the same features into your own source codes
3. Use the .xcix and component file to add the IPs into the design for implementation of the design flow in FPGA.
4. The remaining files above are defined for IP generation, so no changes are required.

Initial Steps:

1. Change the data types in CONV_TOP that are unsigned and signed into std_logic_vector data type since the IP's related components can only support either std_logic or std_logic_vector data types for their ports.
2. Initialize the modules in RAM_IP_TOP as distributed memories
3. Address: 16 , Data: 64, radix:2
4. Initialize the .coe files to the respective memories, check Xilinx documentation for defining the format for a coe file for single port RAM.
5. Once all the design sources are completed with their respective IP's , then in the simulation sources add the behave_vhdl of each module to simulate it respectively.

Happy Coding!!