Introduction to Structured VLSI Design
EITF35

LAB 3

Simple ALU

Arturo Prieto
arturo.prieto@eit.lth.se

Introduction

❑ **A**rithmetic **L**ogic **U**nit **(ALU)** is the fundamental building block of the CPU in a computer.

- ▪ "Heart" of a processor
- ▪ Each processor needs at least one ALU

❑ ALU is a digital circuit that performs:

- ▪ Arithmetic operations (Add, Sub, . . .)
- ▪ Logical operations (AND, OR, NOT)

Objective of Lab3

❑ Design a simple ALU to perform the following functions for its inputs (i.e. A, B):

- Addition: (A + B)

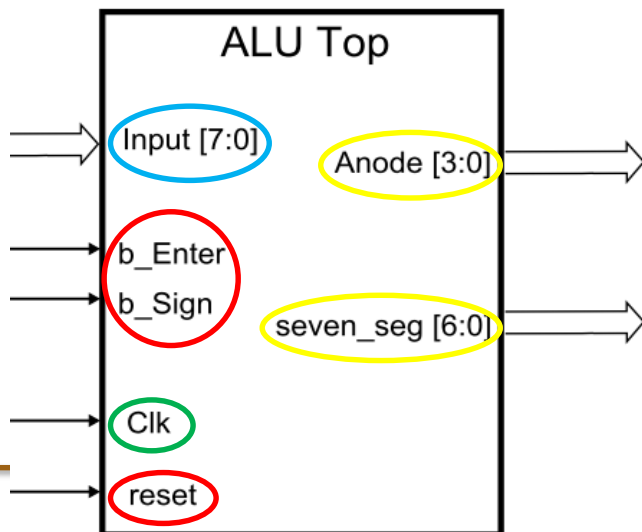- Subtraction: (A - B)

- Modulo 3: (A mod 3)

❑ It should support:

- Sign/unsigned operations

- Overflow detection

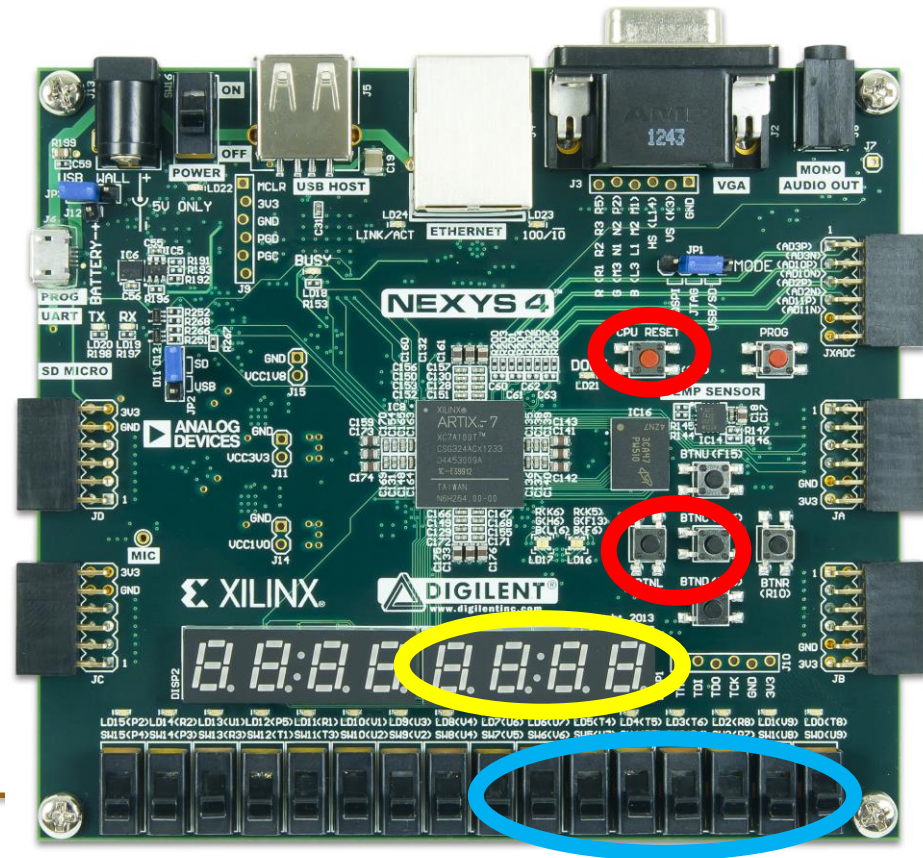# Inputs/Outputs of Design

Inputs:

- 8 bits for input operands

  DIP Switches (SW7..SW0)

- 3 control signals

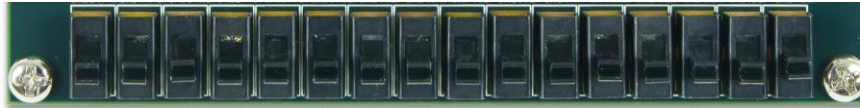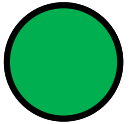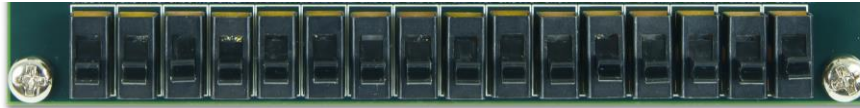 Push buttons (BTNL, BTNC, CPU Reset)
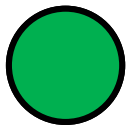
- 100 MHz Clock

Outputs:

- 7-segment display

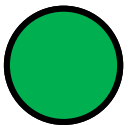# Assignment
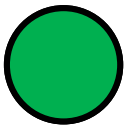
Assignment

Assignment

A + B
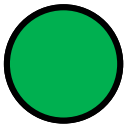
Assignment

A + B

A - B

Assignment

A + B

A - B

mod(A,3)

Assignment

A + B

A - B
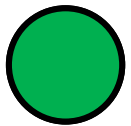
mod(A,3)

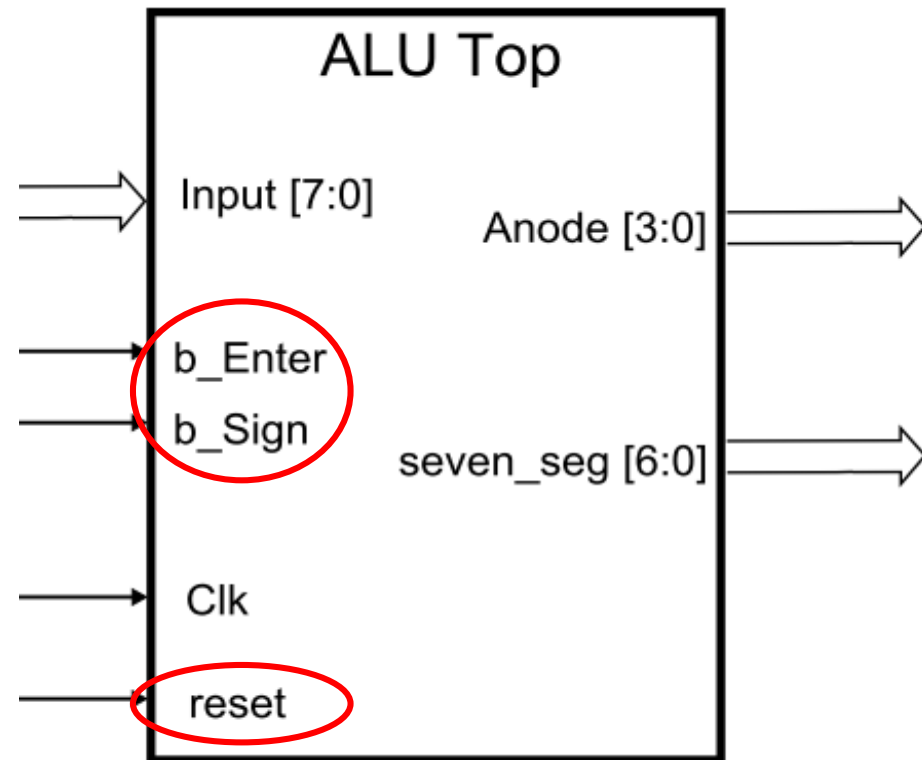# Assignment

❏Signed representation for

Negative results

❏Overflow

Top Module

➢ Generate a proper *.xdc* file based on the I/Os.

➢ Instantiate the *Debouncer* block in the top design.

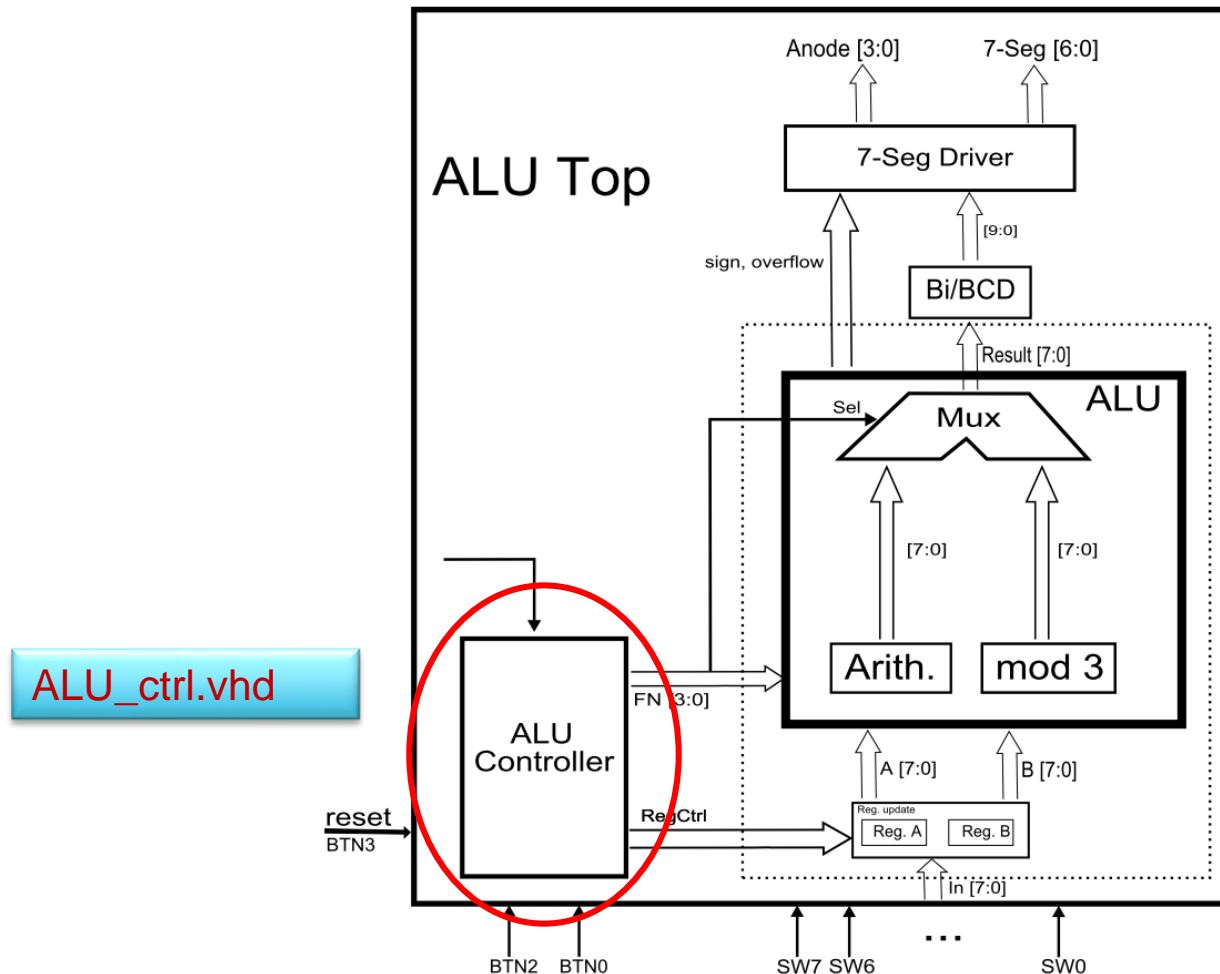ALU_top.vhd

ALU Architecture

Lund University / EITF35/ 2019

ALU Controller
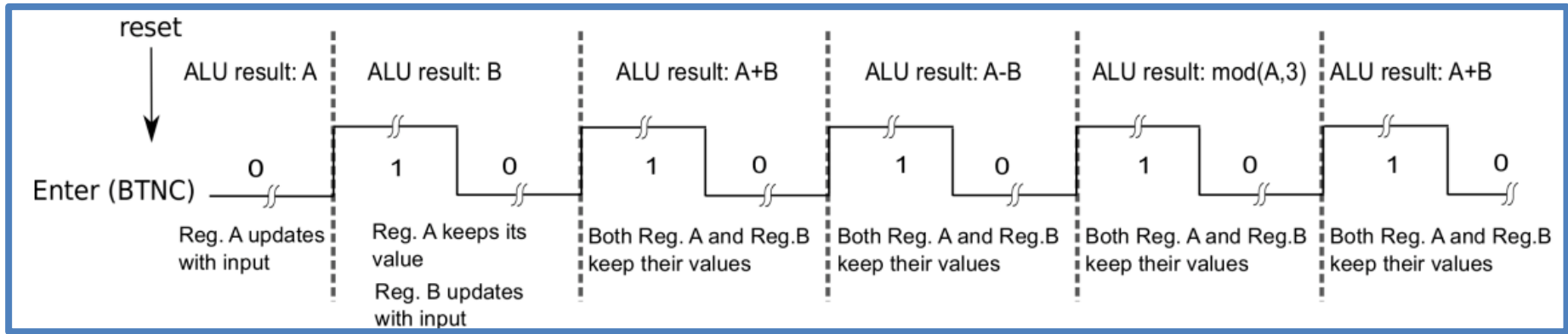
FN [3 : 0]	Operation
0000	Input A
0001	Input B
0010	Unsigned (A + B)
0011	Unsigned (A - B)
0100	Unsigned (A) mod 3
1010	Signed (A + B)
1011	Signed (A - B)
1100	Signed (A) mod 3

ALU Architecture
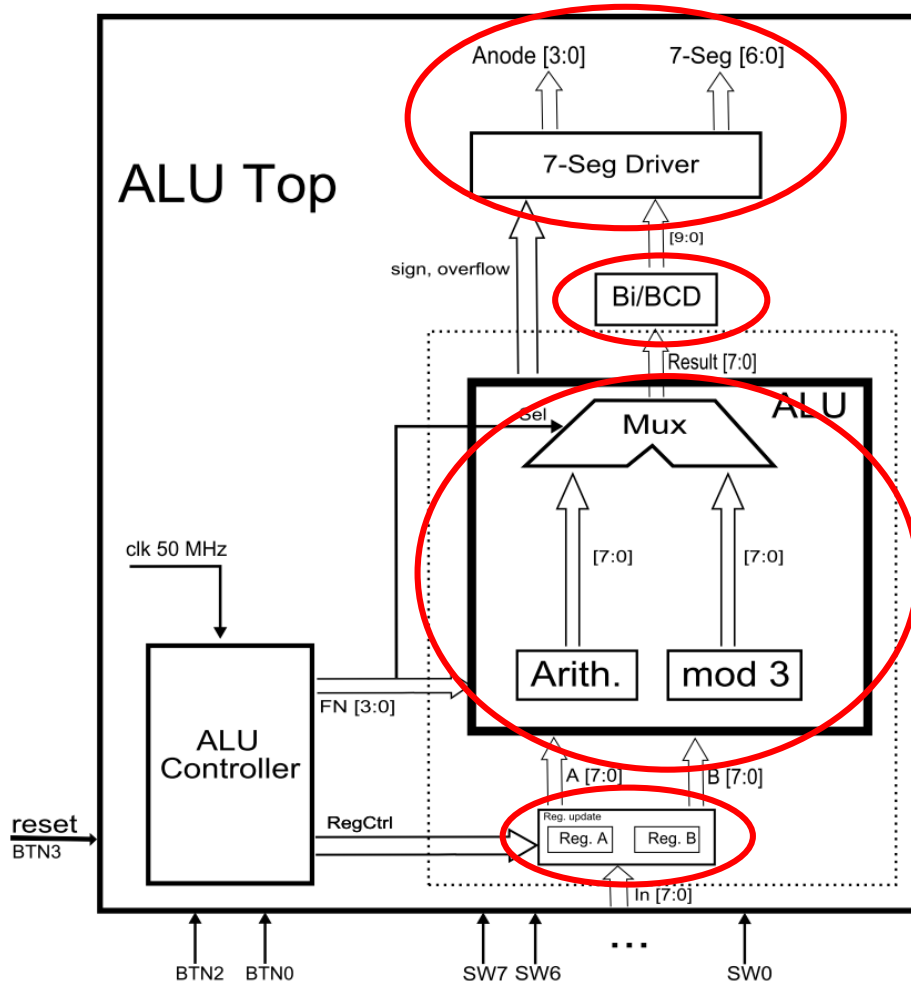
Similar Blocks in Lab 2
7SegDriver.vhd

binary2BCD.vhd

To do Arithmetic Operations
ALU.vhd

Separate Seq. & Comb. Logic
regUpdate.vhd

Lab Preparation

❑ Read the lab manual carefully to understand all the details.

❑ Read the checklist file and prepare the requirements of Lab 3.

❑ Read the *Modulo3.pdf* paper to design the modulo 3 operation.

❑ Design a hardware-friendly architecture for Binary to BCD conversion.

Some Notes

➢ Think about each block and its functionality before coding!

➢ Start early!

➢ Do the simulation as much as possible for your design and sub blocks.