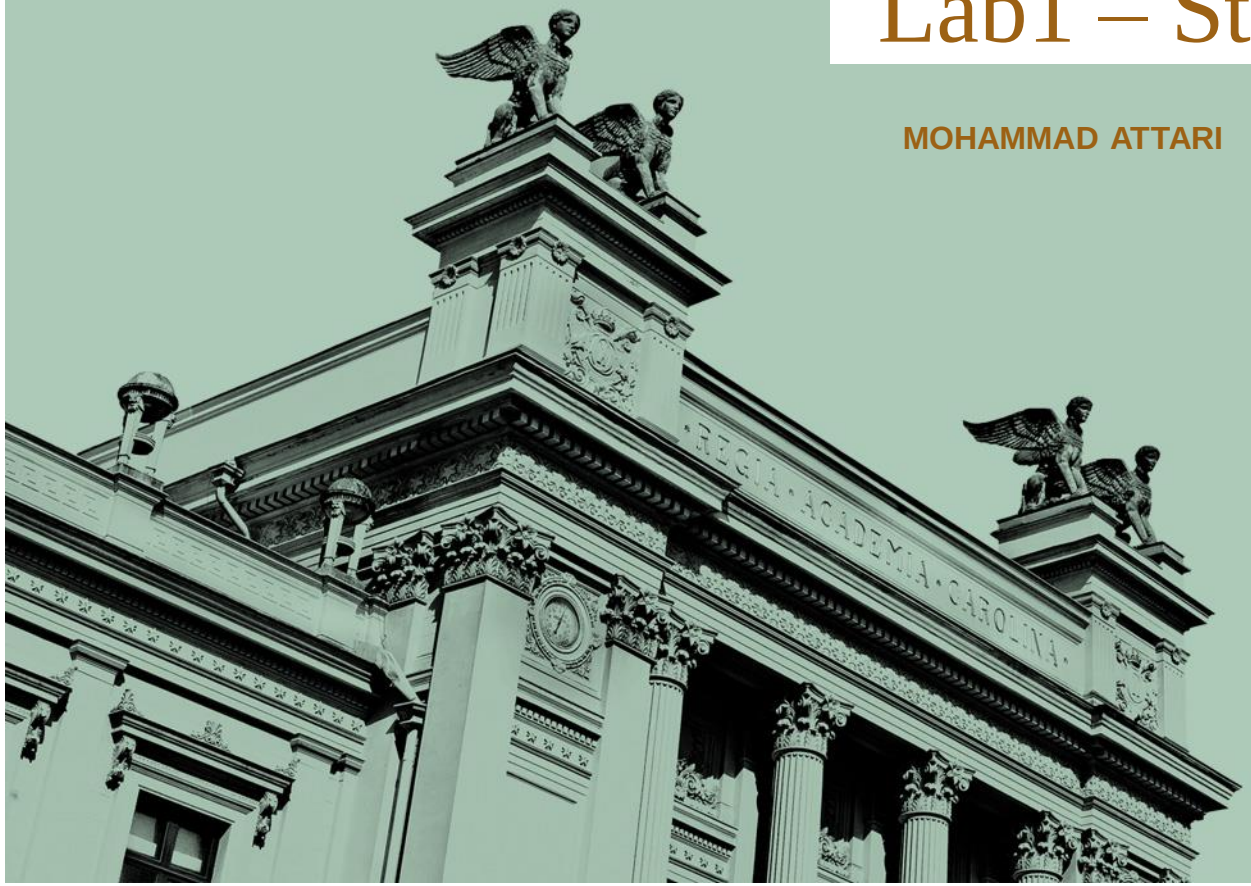
Introduction to Structured VLSI Design

Lab1 – State Machine Modeling

MOHAMMAD ATTARI SEPTEMBER 4, 2019

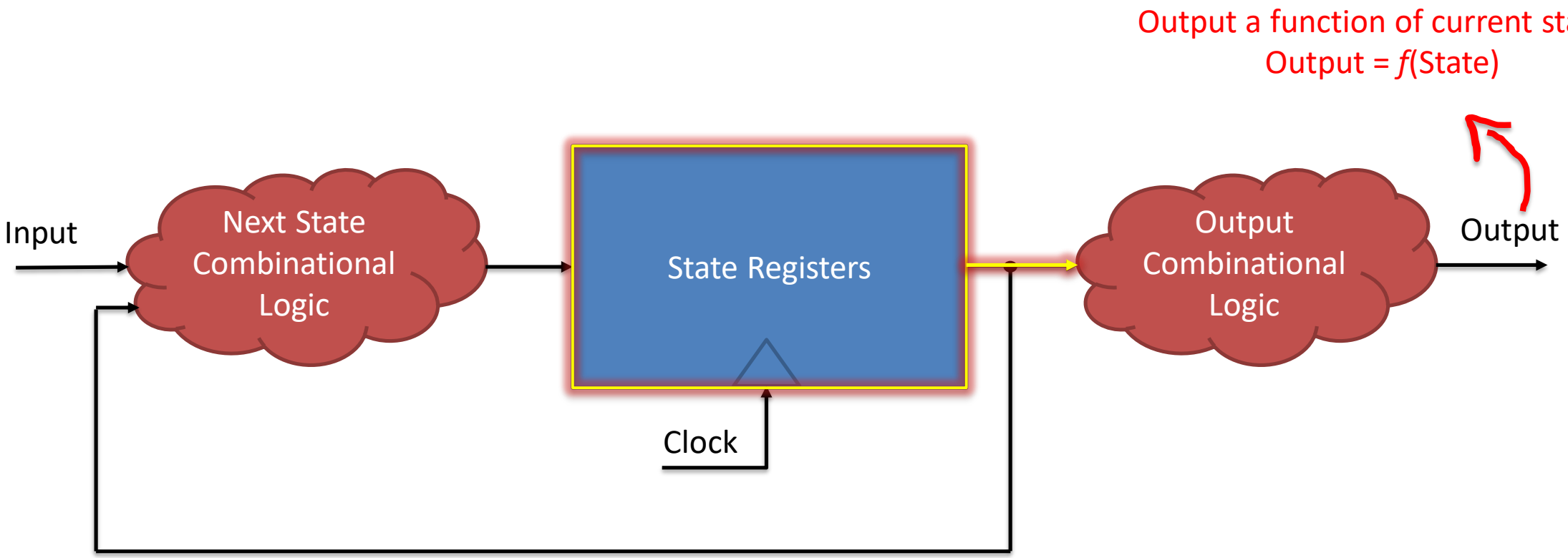


Learning Outcomes

- VHDL modelling for synthesis
  - Registers (state)
  - Combinational logic
  - Latches
- State machines
  - Mealy
  - Moore
- Testbench
- Xilinx Vivado

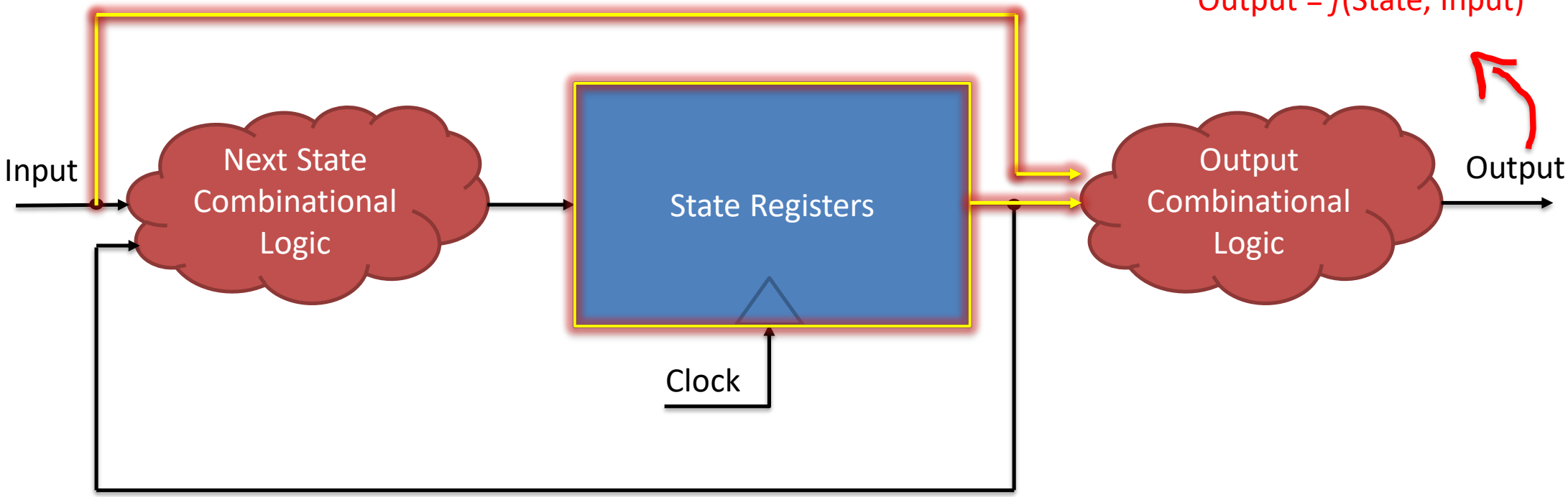
VIVADO™

Moore Machine



Mealy Machine

Output a function of current state and input
Output = *f*(State, Input)

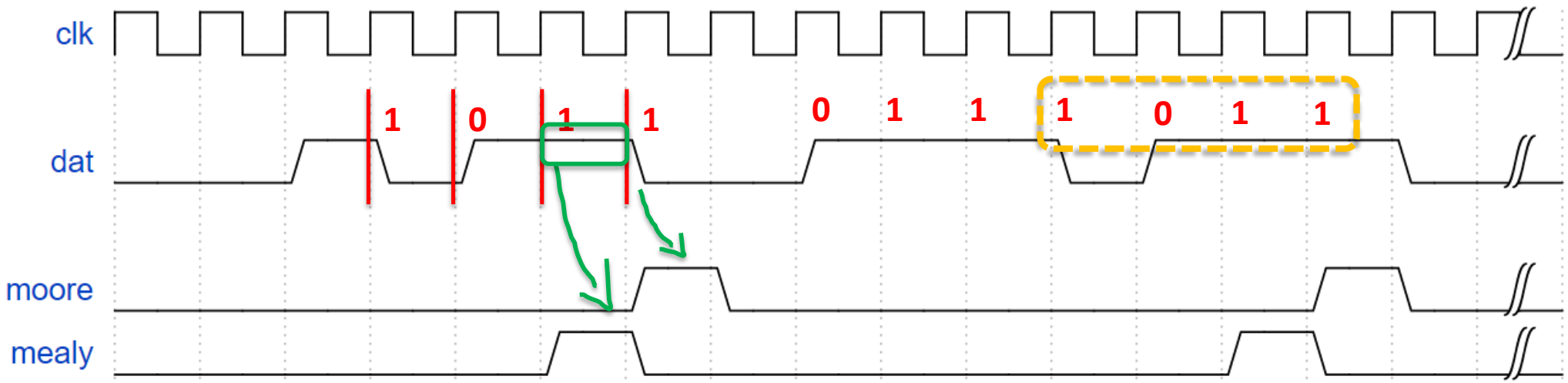


Moore vs. Mealy

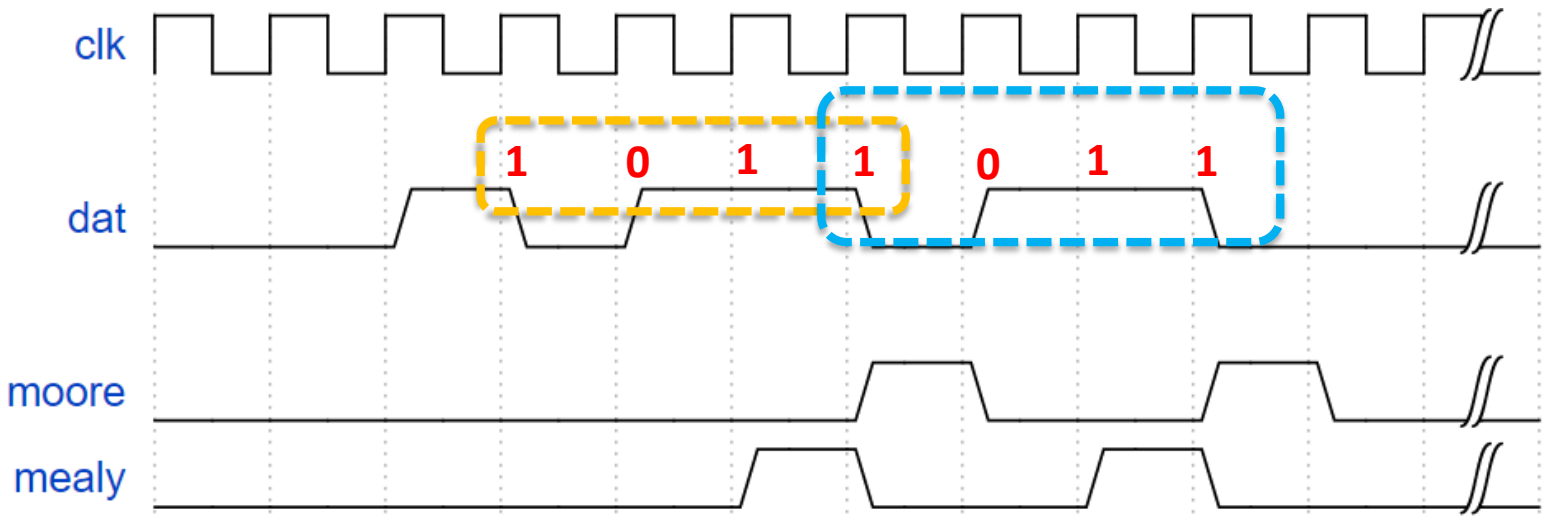
- Mealy
  - Fewer states
  - React faster
- Moore
  - Safer
  - Synchronous

Sequence Detector

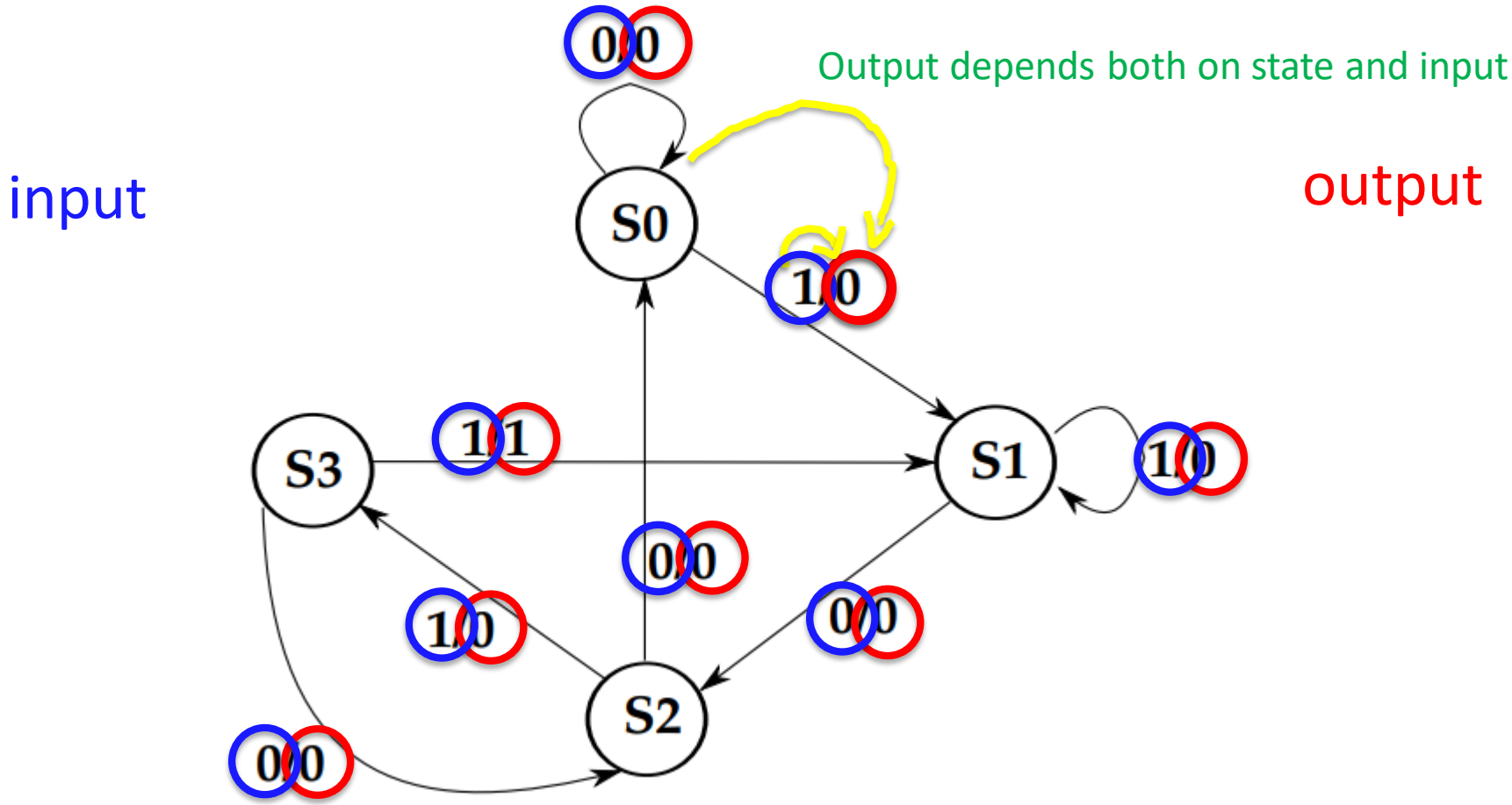
- Detect the sequence **1011**



Sequence in Sequence



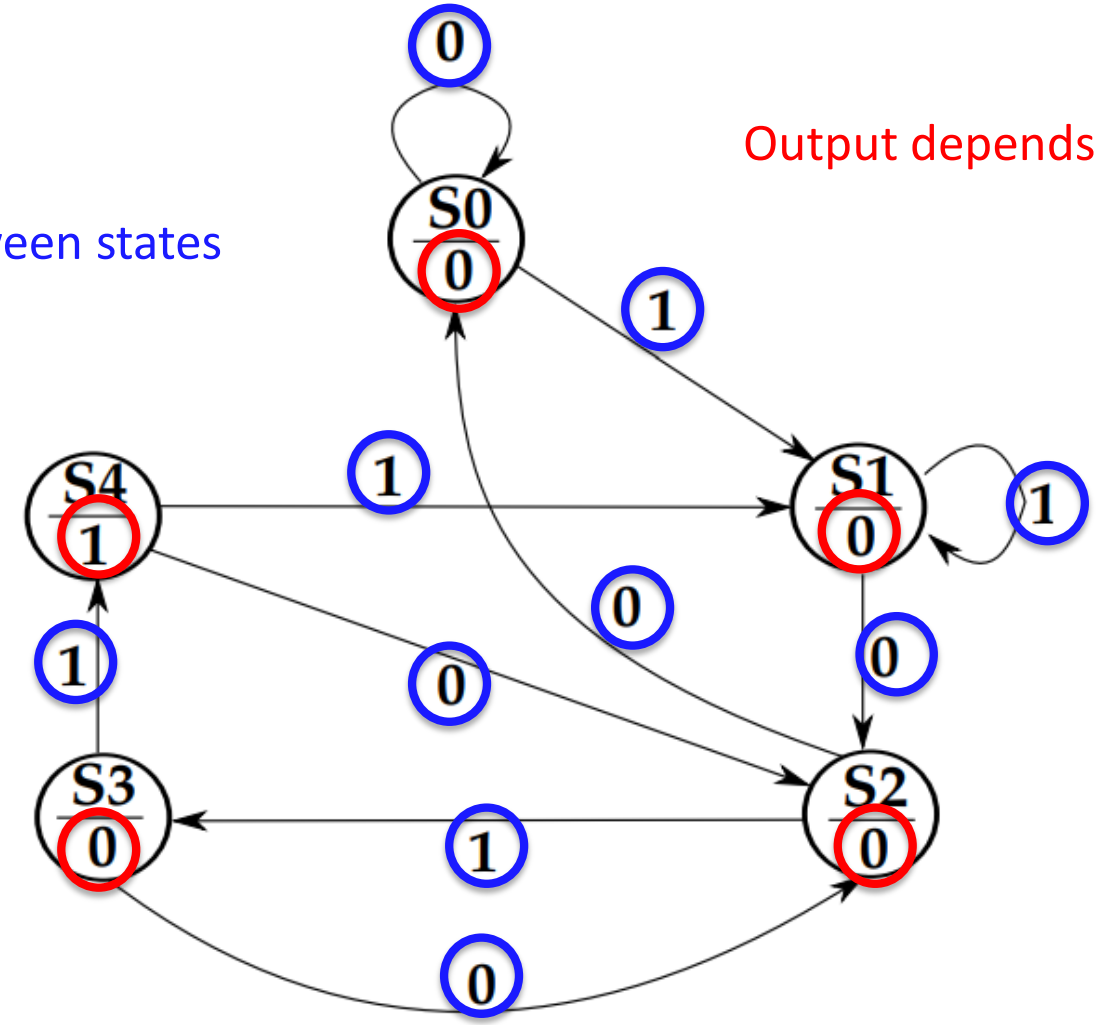
Mealy State Machine



Moore State Machine

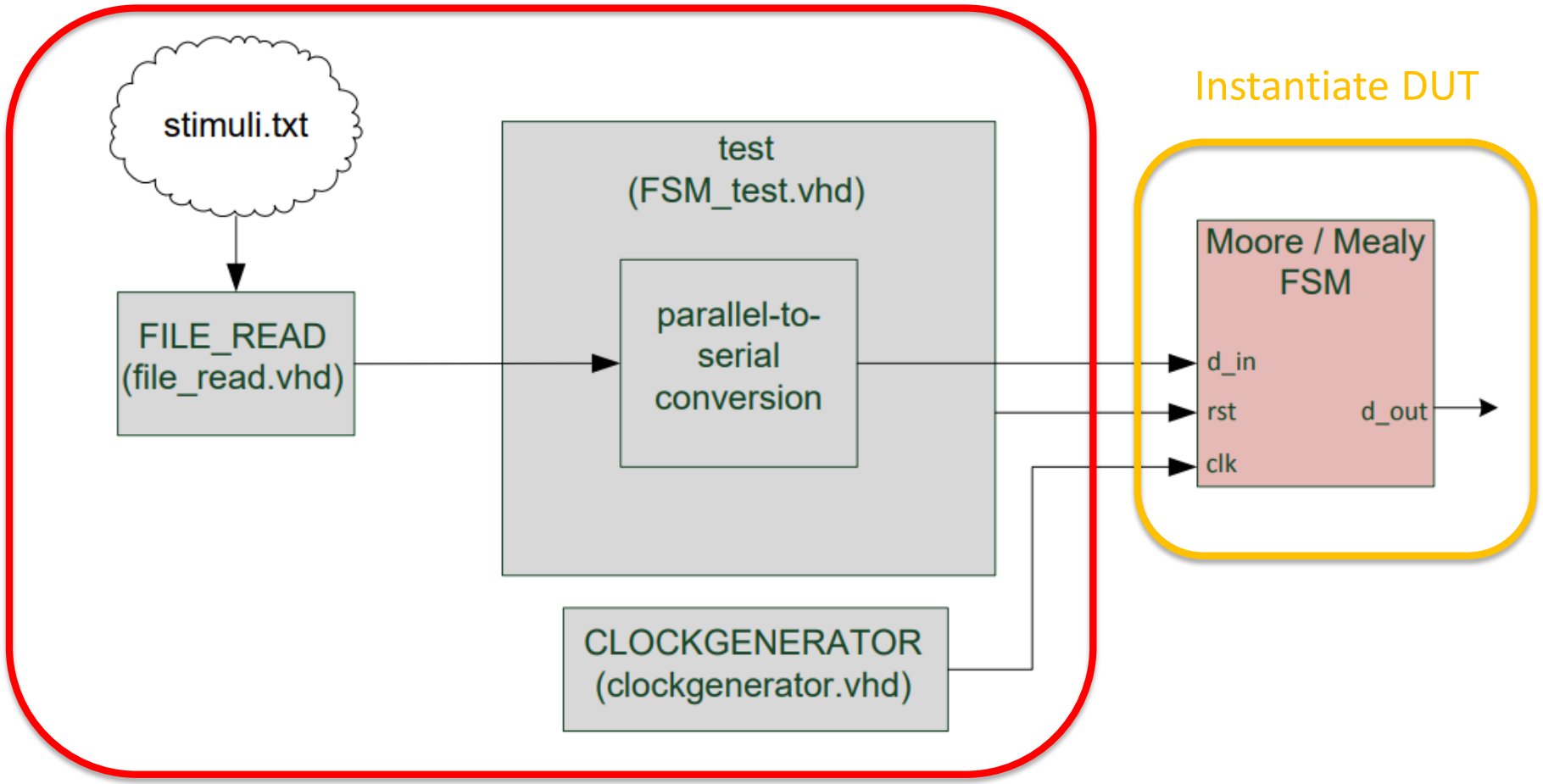
Input causes transition between states

Output depends only on state

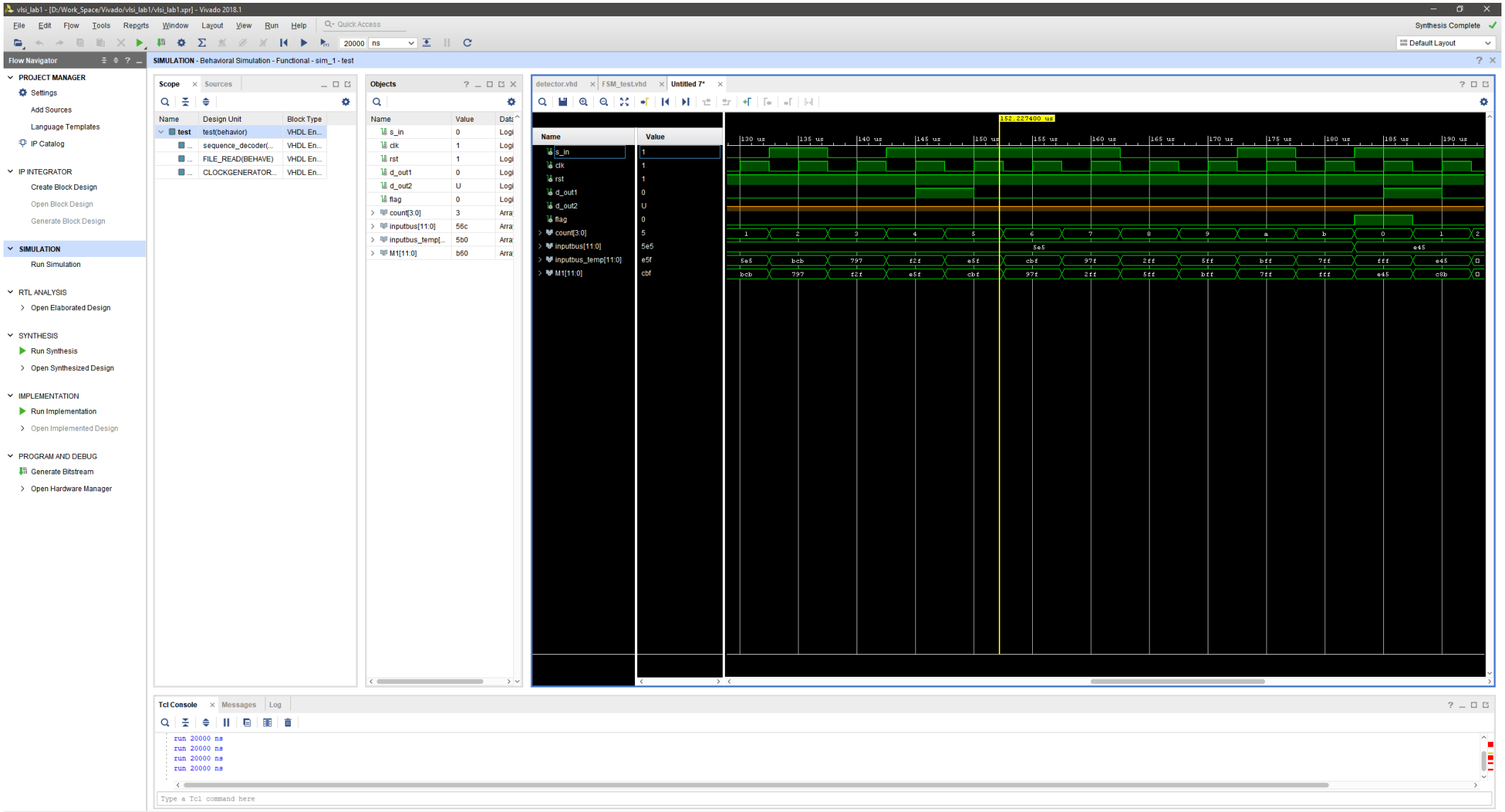


Testbench

All provided as templates



Vivado Design Suite



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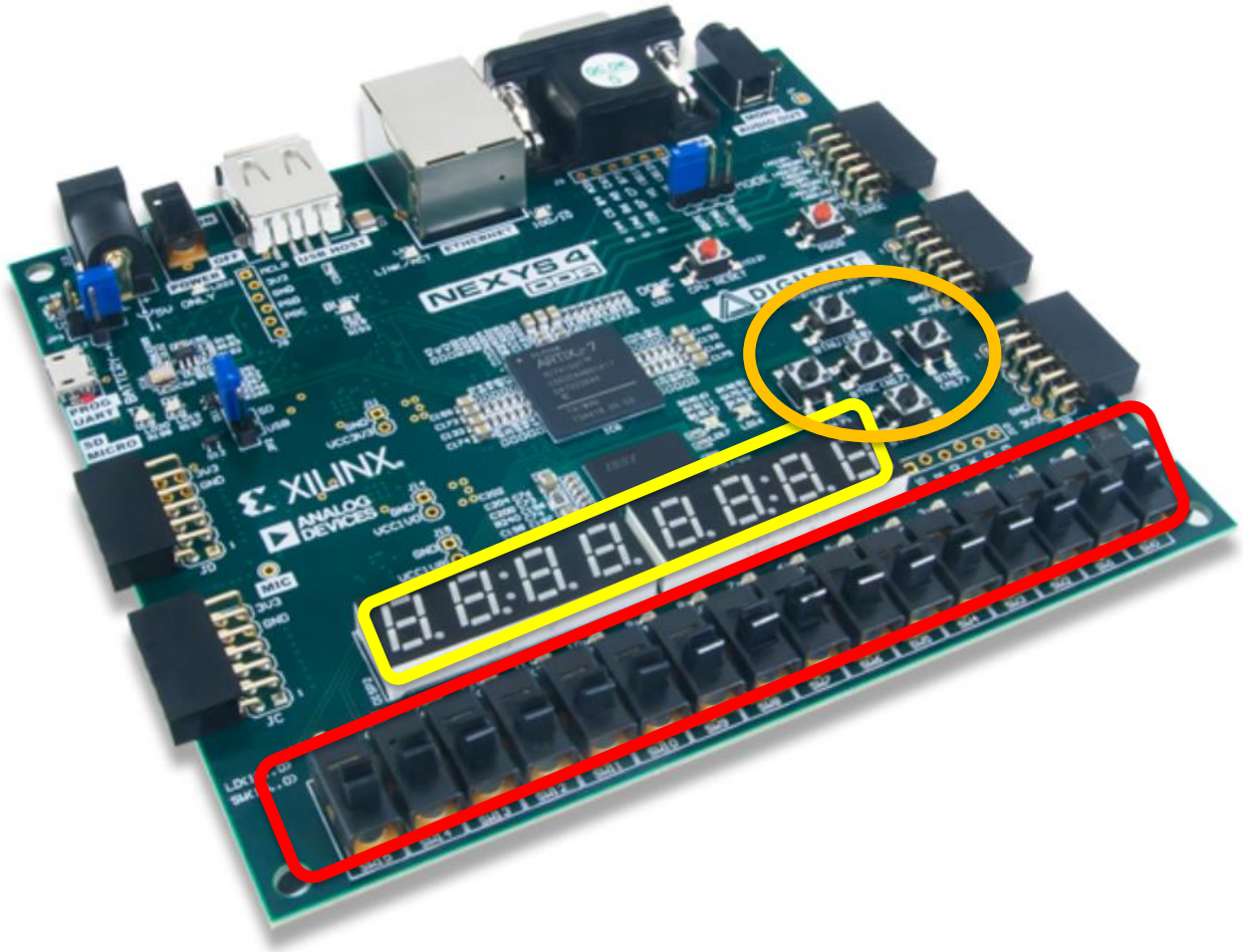
Nexys 4 FPGA (Labs 2-5)



Lab1 Assignment

- Draw the state diagrams
  - Cross check
- Implement FSM in VHDL
- Show simulation
- Demonstrate understanding

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