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Vivado IPs & Integrated Logic Analyzer

MOHAMMAD ATTARI



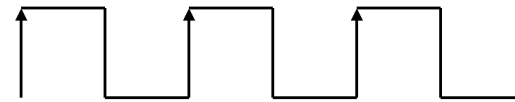
Topics



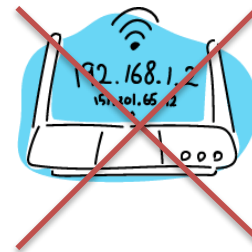
Logic analyzer



Clock

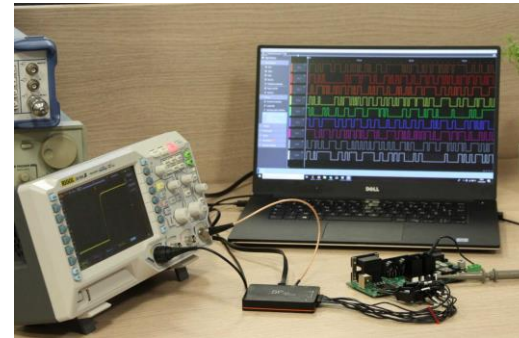
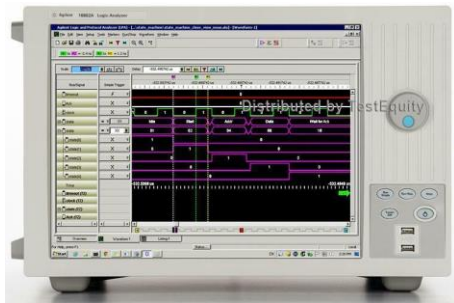


IP = ~~Internet Protocol~~
= Intellectual Property

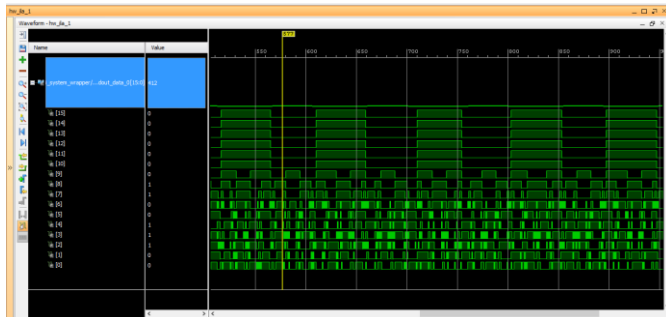


Logic Analyzers

- What are they?
 - Digital signal capturing instruments



- Vivado Integrated Logic Analyzer (ILA)



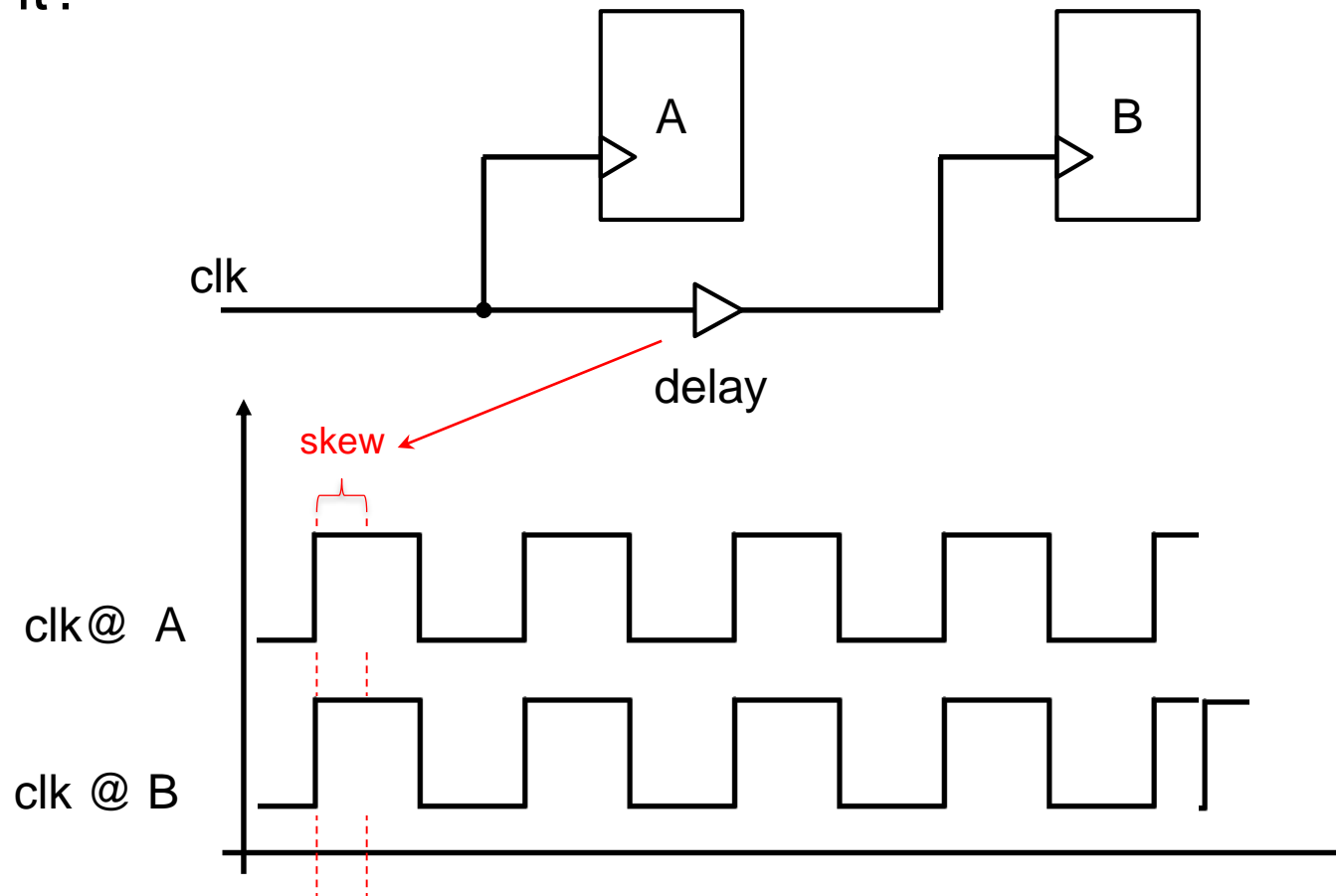
Vivado ILA

The screenshot displays the Vivado IDE interface for an ILA (In-System Logic Analyzer) project. The main window is divided into several panes:

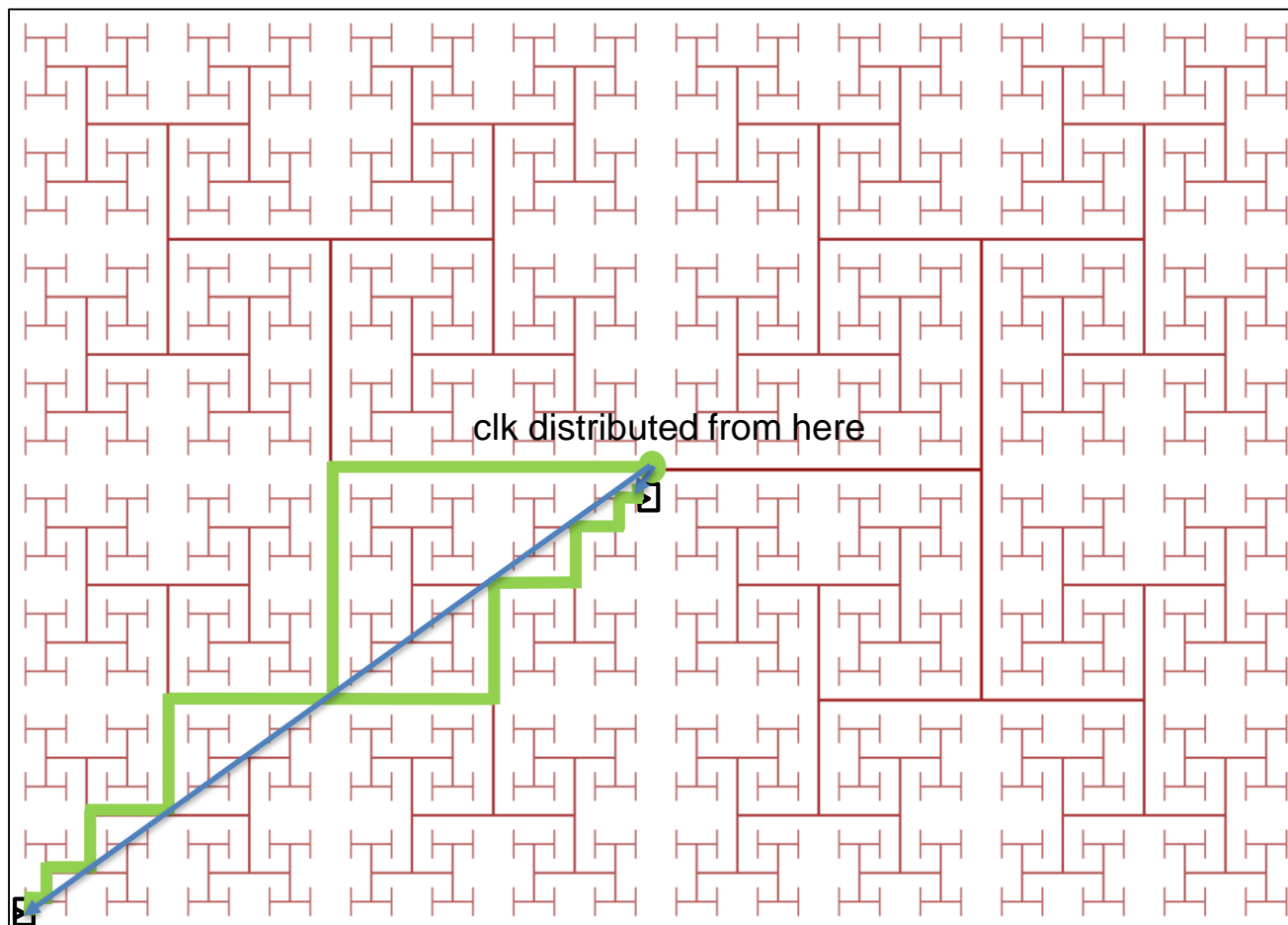
- Hardware Manager:** Shows the hardware configuration for the target device. The ILA core is named "hw_ila_1" and is currently in an "Idle" state.
- Debug Probes:** Lists the debug probes connected to the device, including "clk_delay", "clk_new", "switches_IBUF[0:0]", and "switches_IBUF_1[4:1]".
- Waveform Viewer:** Displays a digital waveform for the selected signals. A red box highlights a specific region of the waveform, likely indicating a trigger event or a specific data capture.
- ILA Core Properties:** Provides details about the ILA core, including its name ("hw_ila_1"), cell ("my_ila"), device ("xc7a100t_0"), and core ("core_15").
- Trigger Setup:** Shows the trigger configuration for the ILA core, including the trigger signal ("switches_IBUF..."), operator ("=="), radix ("B"), value ("1"), port ("probe0[2]"), and comparator usage ("1 of 1").
- Tcl Console:** Displays messages and warnings, including a critical warning about timing requirements: "[Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations."

Clock Skew

- What is it?



Clock Tree



H tree



Clocking Question

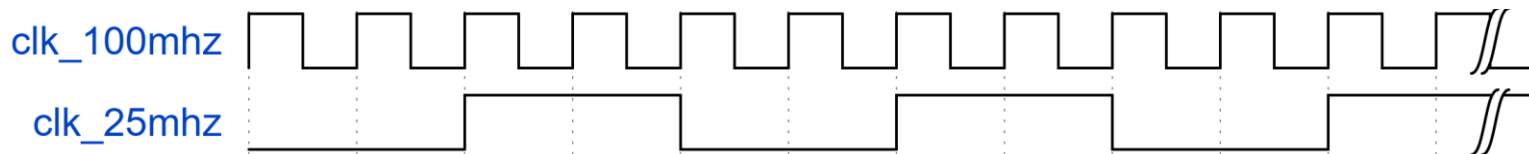
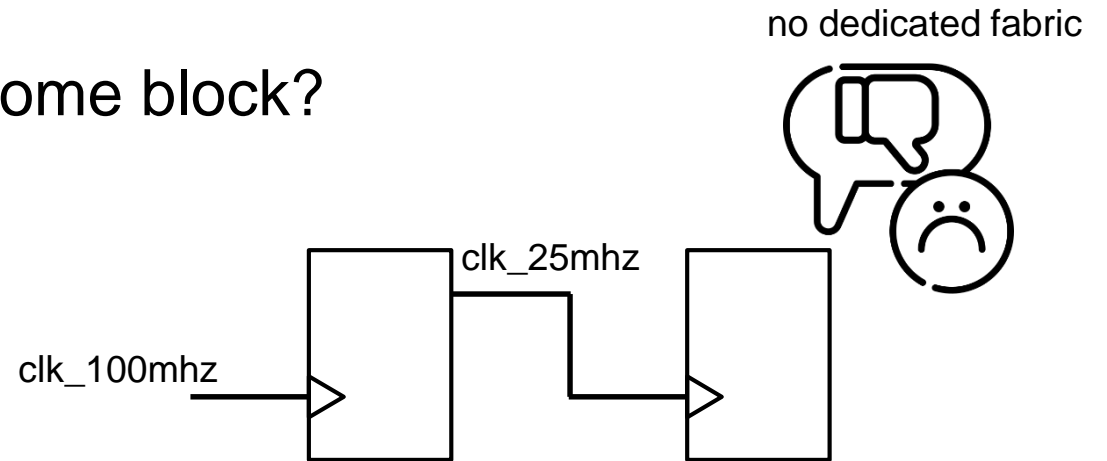
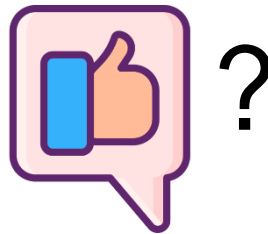
- Nexys4's clock speed?
 - 100 MHz

- What if you need a different speed for some block?

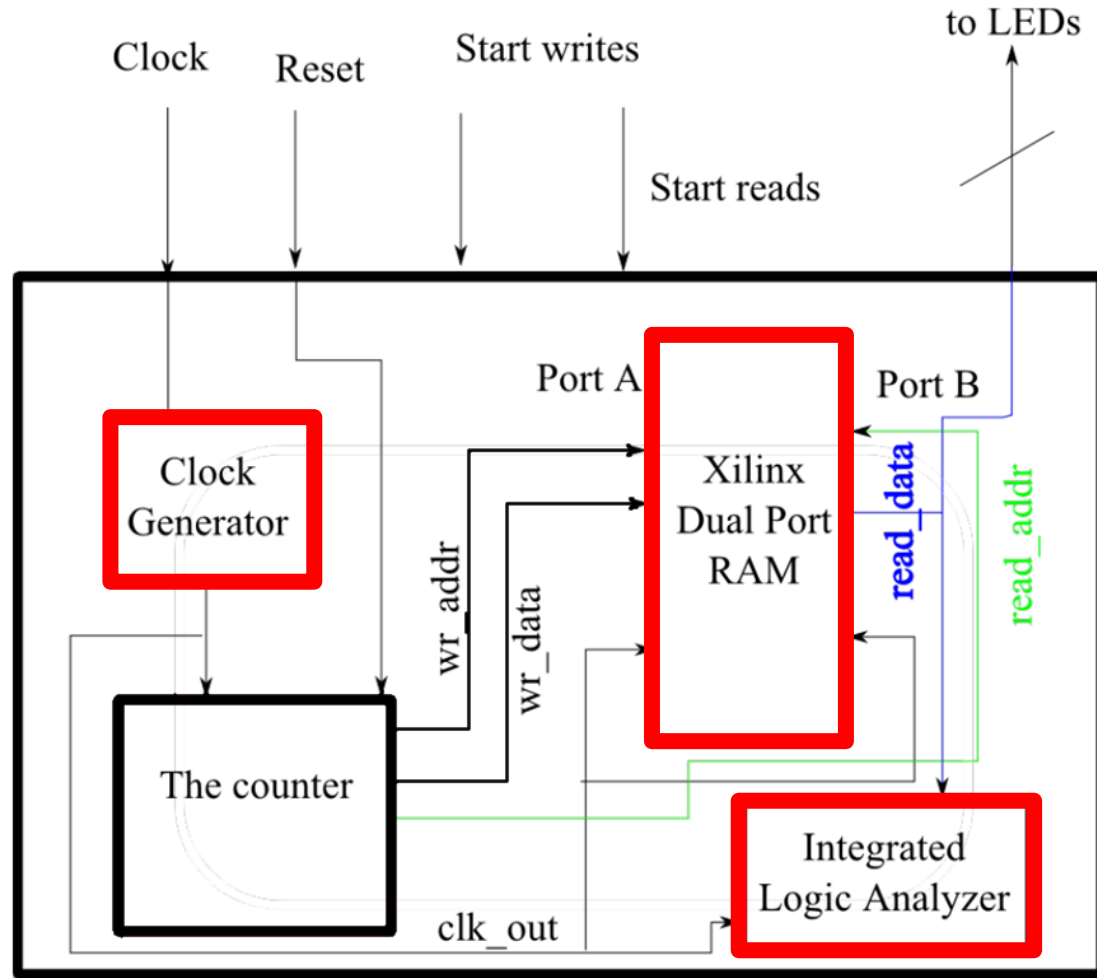
```
signal clk_counter : integer range 0 to 3;
-- ...

-- logic using a 100 mhz clock
if rising_edge(clk_100mhz) then
  clk_counter <= clk_counter + 1;
  if clk_counter = 2 then
    clk_25mhz <= not clk_25mhz;
  end if;
end if;
-- ...

-- logic using a 25 mhz clock
if rising_edge(clk_25mhz) then
  -- ...
end if;
```



IP & ILA Example







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