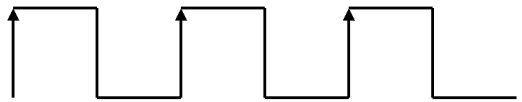
Vivado IPs & Integrated Logic Analyzer

MOHAMMAD ATTARI

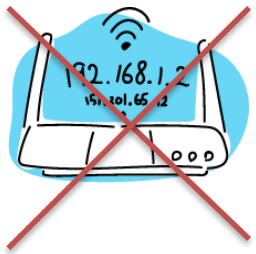
Topics

Logic analyzer

Clock



IP = ~~Internet Protocol~~
= Intellectual Property



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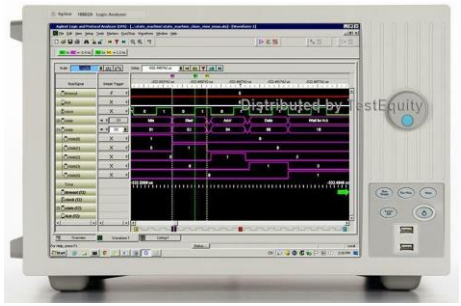
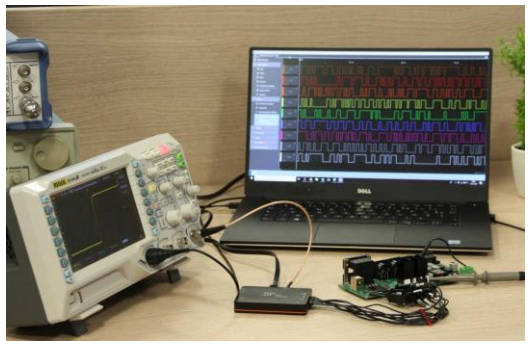
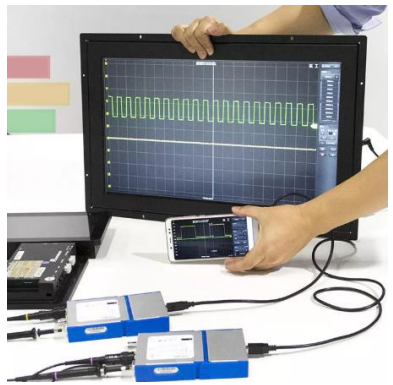
Logic Analyzers

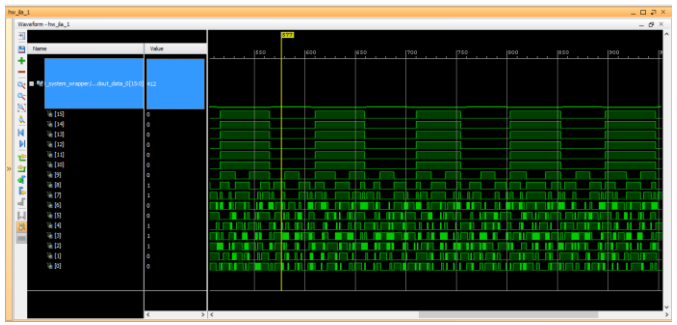
- What are they?
  - Digital signal capturing instruments



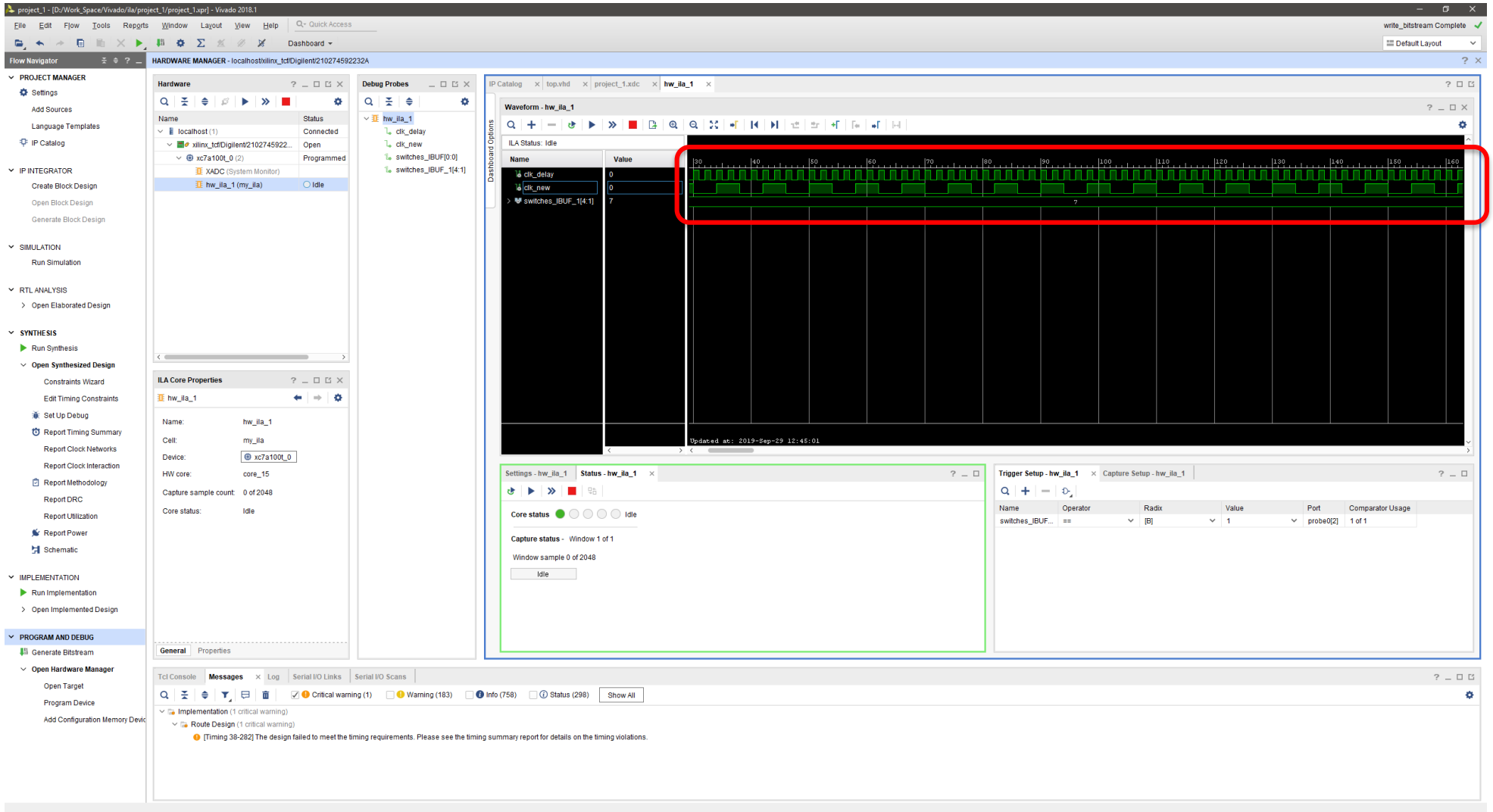




- Vivado Integrated Logic Analyzer (ILA)

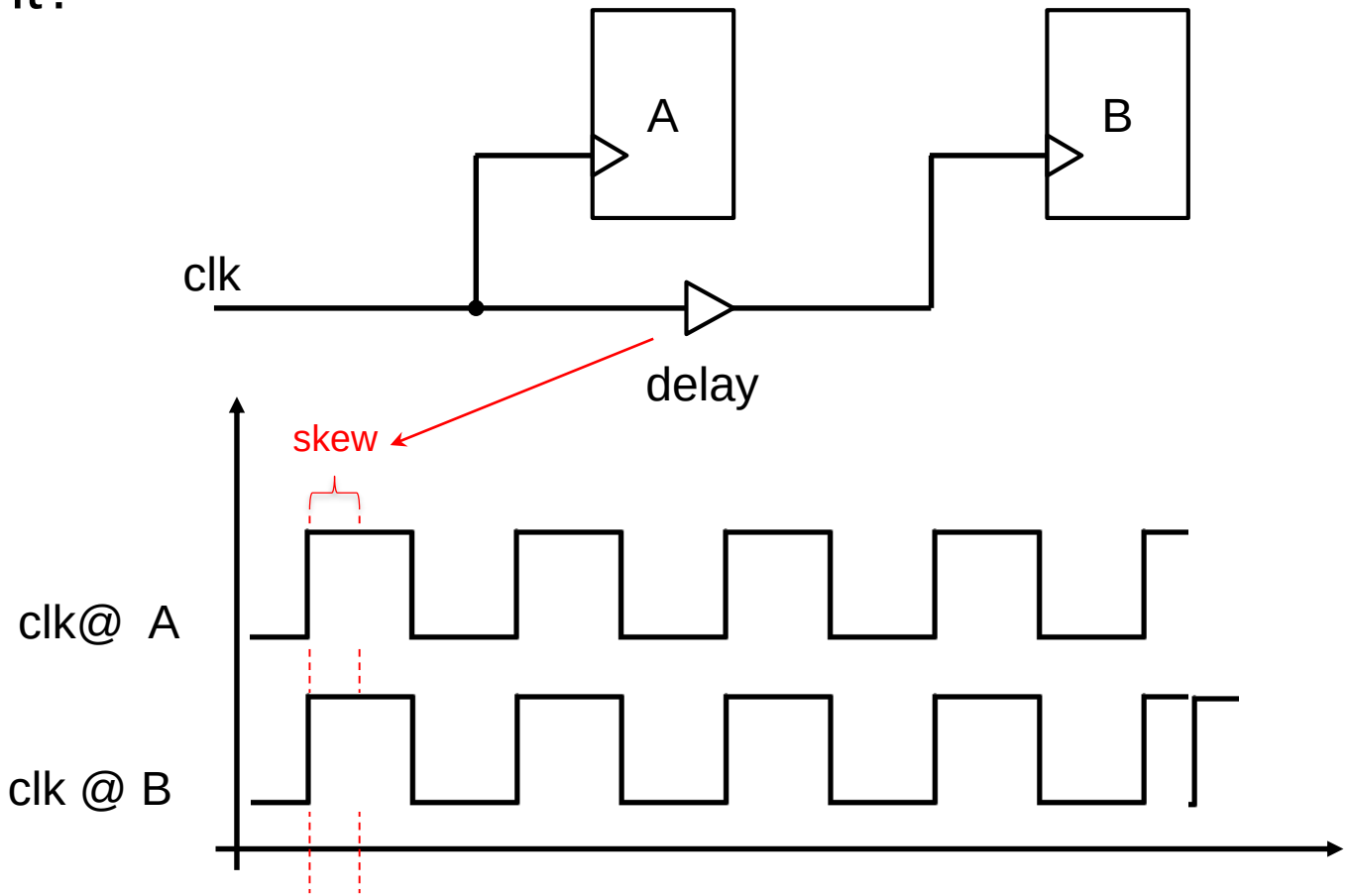


Vivado ILA

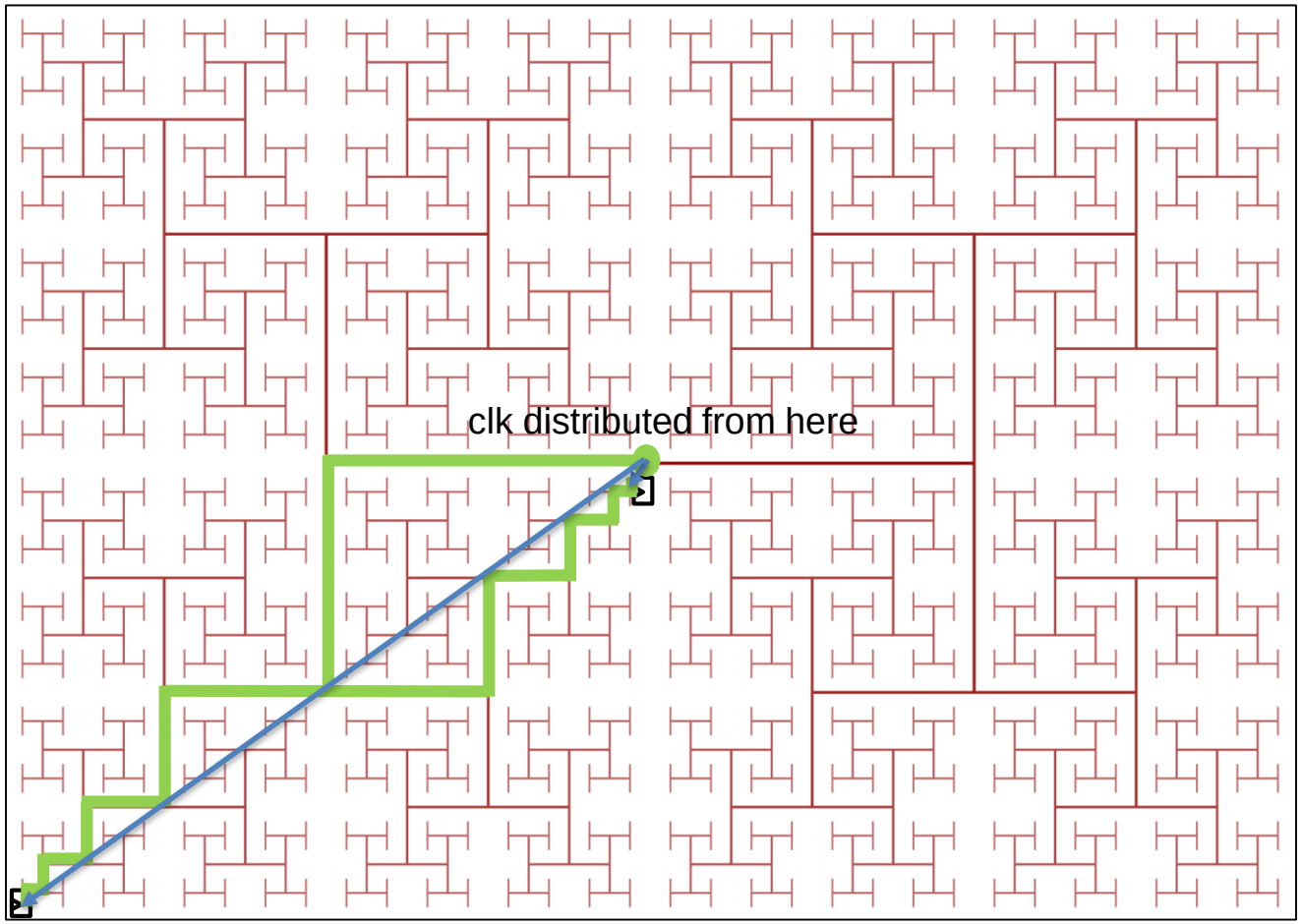

project_1 - [D:/Work_Space/Vivado/ila/project_1/project_1.xpr] - Vivado 2018.1
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210274592232A
Waveform - hw_ila_1
ILA Status: Idle
clk_delay
clk_new
switches_IBUF_1[4:1]
Updated at: 2019-Sep-29 12:45:01
ILA Core Properties
Core status
Capture status - Window 1 of 1
Window sample 0 of 2048
Trigger Setup - hw_ila_1
[Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.

Clock Skew

- What is it?



Clock Tree

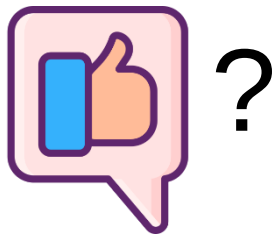


H tree

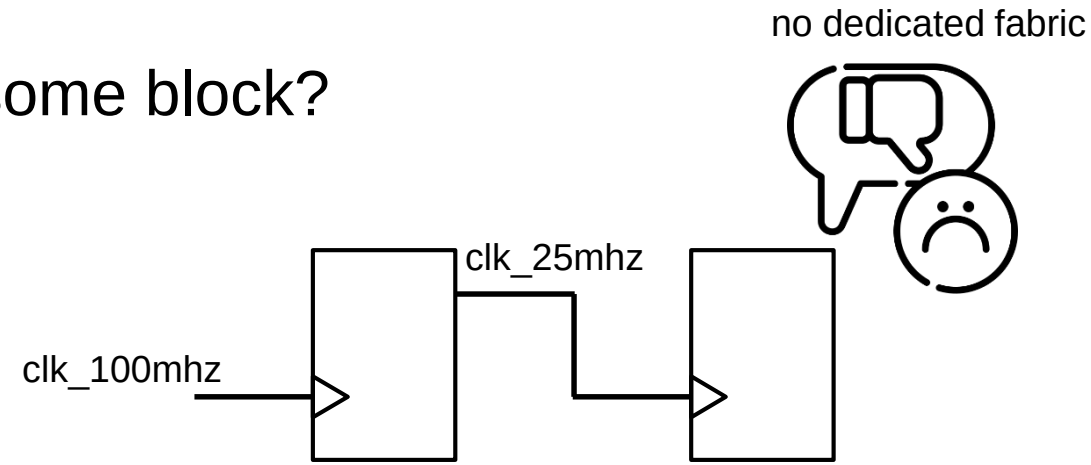
Clocking Question

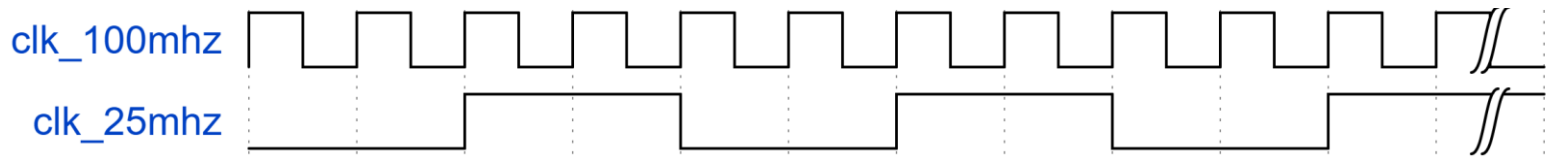
- Nexys4's clock speed?
  - 100 MHz
- What if you need a different speed for some block?

```
signal clk_counter : integer range 0 to 3;
-- ...

-- logic using a 100 mhz clock
if rising_edge(clk_100mhz) then
    clk_counter <= clk_counter + 1;
    if clk_counter = 2 then
        clk_25mhz <= not clk_25hmz;
    end if;
    -- ...

-- logic using a 25 mhz clock
if rising_edge(clk_25mhz) then
    -- ...
```

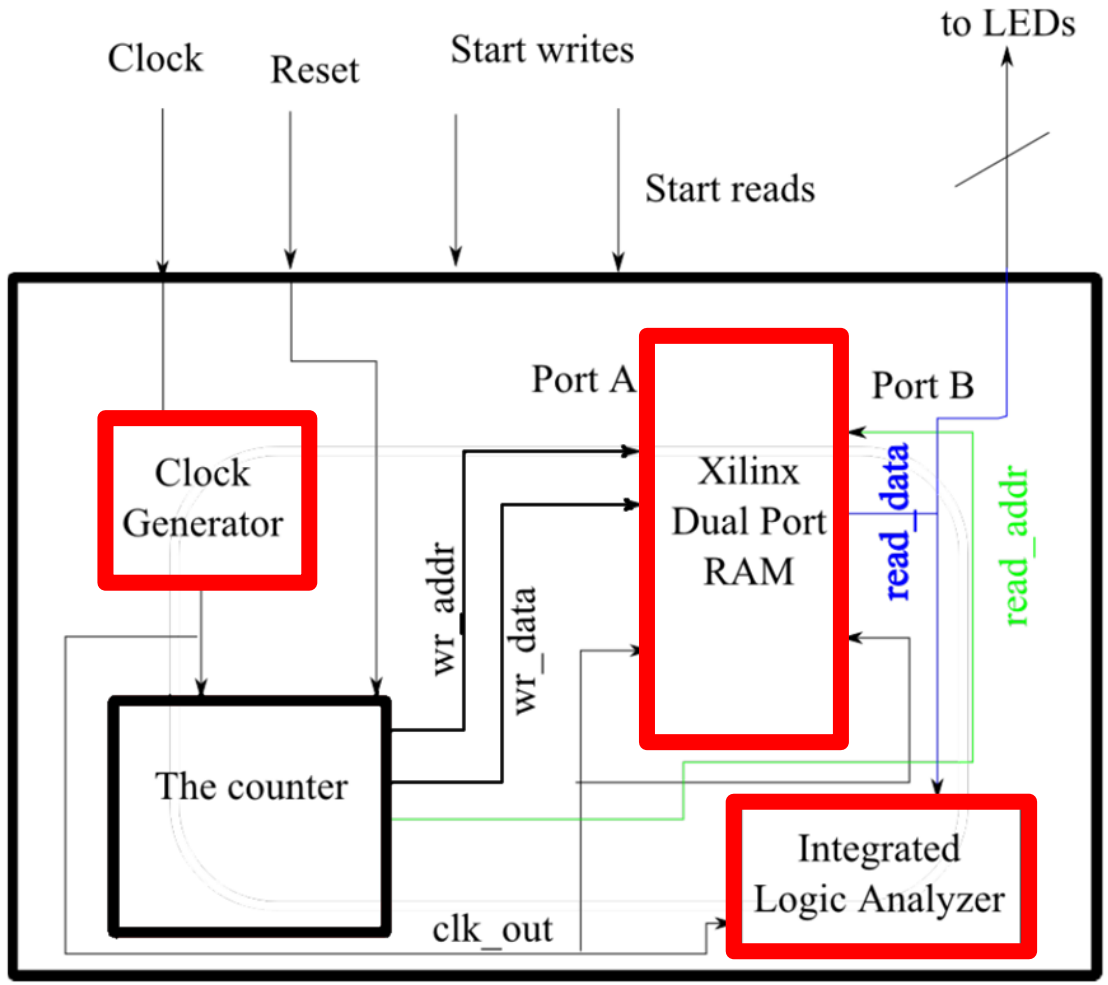


?





IP & ILA Example



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