In order to get approved, students should perform the following tasks and also answer to the TA's questions:

IMPORTANT NOTE:

*Most of these tasks should be done **before** the lab session. So, please prepare as much as you can before your lab session.*

Lab 1:

1) Draw the state diagram and cross check it, i.e. group 1 checks group 2 and group 2 checks group 1 and so on. This is a prerequisite to get access to the labs.
2) Draw the timing diagram for both the Mealy and Moore machines with sample input demonstrating when the output goes high.
3) Implement the FSM for the sequence detector in VHDL using both Mealy and Moore state machines.
4) Write/modify the testbench and simulate your design and show the results to confirm the functionality of your design in the LAB.
5) Explain the VHDL code and the corresponding testbench.
6) Specify combinational blocks and sequential blocks in your design. You need to be able to explain when your description turns into flip-flops and when into combinational logic. Additionally, how can you avoid creating latches in your designs?

Lab 2:

1) Explain different parts of your VHDL code and your coding style.
2) Write/modify the testbench for the design (i.e. top module) and simulate your design and show the results to confirm the design functionality. You should be able to show the internal signals of different subblocks in the waveform window and explain their behavior.
3) Draw a high-level block diagram for your design and show/explain the subblocks, connection between the modules, important internal signals, and IOs.
4) Determine the type of subblocks in your block diagram (comb. and Seq.).
5) Explanation of the timing of your design, critical path, maximum operation frequency, and other timing issues.

Lab 3:

1) Explain different parts of your VHDL code.
2) Write/modify the testbench for the design (i.e. top module) and simulate your design to confirm the design functionality. You should be able to show the internal signals of subblocks in the waveform window and explain their behavior.
3) You should be able to put a suggested value for A and B in the testbench and show the corresponding results in the simulation.
4) Determine the type of subblocks in your block diagram (comb. and Seq.).
5) Show and explain the timing diagram of 7seg module.
6) Explanation of the timing of your design, critical path, maximum operation frequency, and other timing issues.