EITF35 - Introduction to Structured VLSI Design

Fall 2017

Introduction

This course provides knowledge on very large-scale integrated (VLSI) digital circuit realization, targeting for fast prototyping on an FPGA platform. The participants will gain knowledge required to implement typical blocks of a large digital system, e.g., state machines for control, data-path for processing, etc. Moreover, it will be taught to optimize a digital implementation, mainly on the VLSI architecture level, for area, speed, and power. Basic knowledge of design for test (DFT) and verification will also be included to get good understanding of a complete digital VLSI design flow. The knowledge gained during the lectures will be implemented through practical assignments in the lab. The course teaches the basic concept of VHDL and tool training required for the compulsory assignments, i.e., *Sequence Detector*, *ALU*, *Keyboard Controller, and a small processor*. Based on the experience gained through compulsory assignments the students may continue with a small project implementing more advanced VLSI digital circuit. The course material is based on handouts provided on the course page.
EITF35 is a prerequisite for *Digital IC-Project and Verification ETIN01*.

Practicalities

Course Responsible:
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Teaching assistants:
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Textbook
If you do not already have a book on VHDL we recommend as a companion textbook: *RTL Hardware Design Using VHDL* by Pong Chu.

Location
Most lectures will take place on
The first lecture will be **08:15-10:00, 2017-08-29** (Tuesday), room **E:C.**

- Mondays (13:15-15:00)
- Tuesdays (13:15-15:00)
- **Checking lecture room here**: https://se.timeedit.net/web/lu/db1/lth1/ri12565750000YQQ25Z0587057y5Y2013gQ7g5X6Y55ZQ376lZ6Qu00.html

Most labs will take place in E:4121 on

- Wednesdays (13:00-17:00)
- Thursdays (13:00-17:00)
- Fridays (08:00-12:00, 13:00-17:00)

We will present the assignments and the corresponding tool tutorial before the lab

Homepage

All material and information regarding the course will be on the course page.

Lecture notes

Handouts will be available the day before the lecture on the course page. If necessary the handouts will be updated after the lecture.

Lab preparation

The assignments require some compulsory preparation. The preparation must get approved by the TA's ahead of the lab.

Lab-equipment

The labs are equipped with Windows PC's and Nexys-4 FPGA boards from XILNX. A similar setup, i.e., Xilinx VIVADO and ModelSim MXE may be installed on each student's PC. These tools can be downloaded from the Xilinx webpage free of charge. (Go to: www.xilinx.com - Products - Design Tools - VIVADO WebPACK, and register for the download. We are not able to support anything installed on your PC's.

Design project

You will be working in teams of 2 students. You need to register as a team in the 2nd week of the course. Teaching assistants will be available 50% of the assigned lab hours (normally Tuesday 13:00-15:00, Wednesdays 13:00-15:00, Thursdays 13:00-15:00, and Fridays 08:00-10:00). In addition to these lab hours, you are expected to spend some extra time, either in the labs any time the lab is available, or at home.

All assignments will be presented in the class room as indicated in the schedule. The preparation to the assignments must be handed in at the beginning of the lab session. If a group does not hand in the preparation the group members need to pass a test in order to be able to continue the lab. A student may not fail such test more than twice to pass the course.

Grading

Deadlines: All assignments must be demonstrated to the TA's to get approved. Furthermore, the students need to demonstrate their understanding ("oral examination") of the assignment to get it approved. To pass the course (grade 3), 3 assignments must be delivered on time. The difficulty level of the assignments is in increasing order. If a group should miss a deadline another assignment will be accepted, e.g., if the deadline for assignment 2 is missed the group may deliver

assignment 4 instead.

For grade "3" following assignments need to get approved:
1. Sequence Detector: Suggested finishing time, September 9, 15:00 (A), 17:00 (B)
2. Keyboard Controller: Suggested finishing time, September 23, 15:00 (A), 17:00 (B)
3. ALU: Suggested finishing time, September 30, 15:00 (A), 17:00 (B)

Students who want to aim for a higher grade than "3" need to select a small project. It is recommended to start the projects earlier than the deadline for the assignment 3. The projects will get approved like the assignments ("oral examination").

4. Grade 4: ALU with memory, output on VGA: Suggested finishing time October 14, 17:00
5. Grade 5: All previous assignments and project for grade 4 in time. Implementation of square root function in the ALU and achieve required constraint on speed and area.

The suggested time is for optimal project plan based on previous experience.
The DEADLINE for all the grades is Oct. 28. 17.00

The VGA controller that needs to be implemented for grade 4 may be reused in the project for grade 5. You will be graded as a group. However, if we suspect an unbalance in workload or understanding, individual grading may be applied.

Lecture plan

The lecture plan may receive some minor updates.

Week	Date	Topic	Lecturer	Lab
35	Monday		LL	
	Tuesday	Intro, FSM , VHDL1, FPGA, Assign. 1 SD	LL, ST	
	Wednesday			
	Thursday			
	Friday	Invited Lecture, Liesbet	LL	
36	Monday	Combinational, VHDL2	LL	
	Tuesday	Sequential, VHDL3 , Assign.2 Keyboard	LL,HP	
	Wednesday			
	Thursday			
	Friday			**Assign. 1 due**
37	Monday	FSMD, VHDL4,	LL	
	Tuesday	Memories, Advanced FPGA	LL, RG	
	Wednesday			
	Thursday			
	Friday			
38	Monday	Advanced, Assign. 3 ALU	LL, OA	
	Tuesday			
	Wednesday			
	Thursday			
	Friday			**Assign. 2 due**
39	Monday		EL, RG	
	Tuesday	DFT, Assign. 4 Display ALU+Memory		
	Wednesday			
	Thursday			
	Friday			**Assign. 3 due**
40	Monday	Axis		
	Tuesday	Ericsson		
	Wednesday			
	Thursday			
	Friday			
41	Monday	Course Evaluation + wrap up	LL	
	Tuesday	no lecture		
	Wednesday			
	Thursday			
	Friday			**Assign. 4 due**