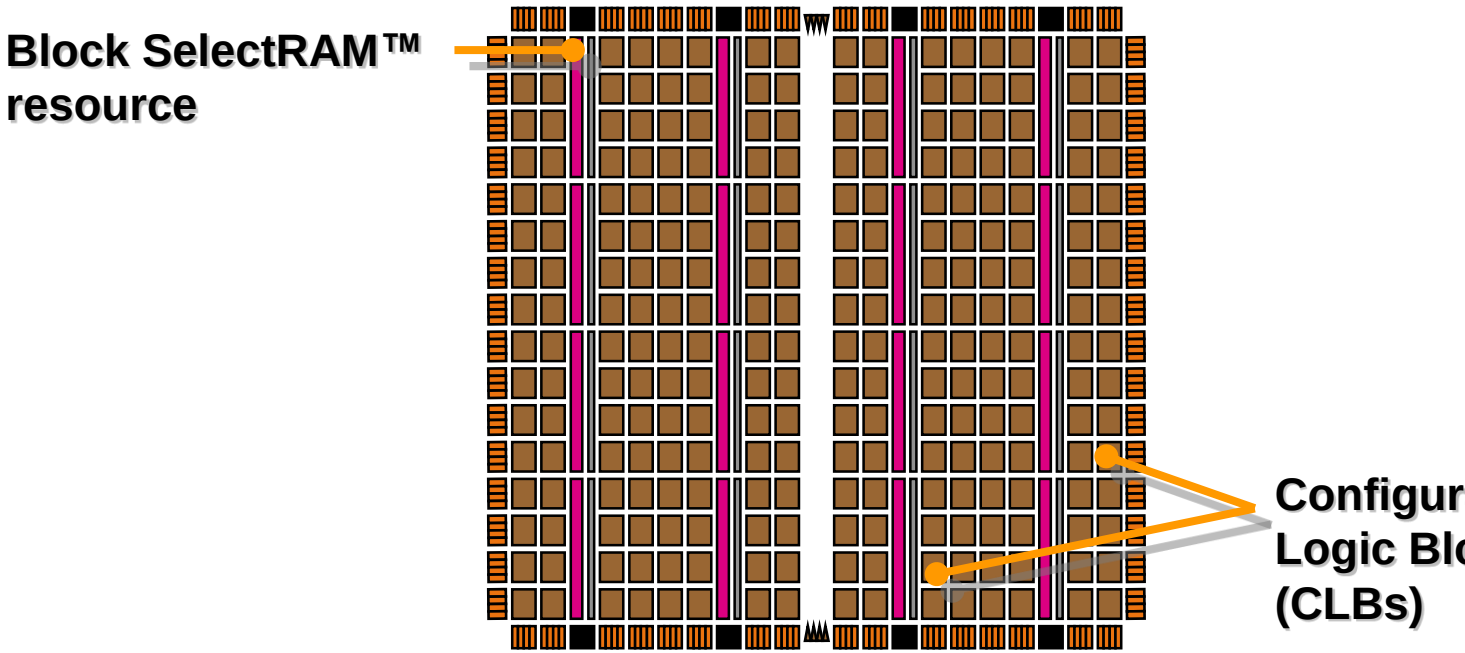
EITF35: Introduction to Structured VLSI Design

Part 3.2.1: Storage Elements

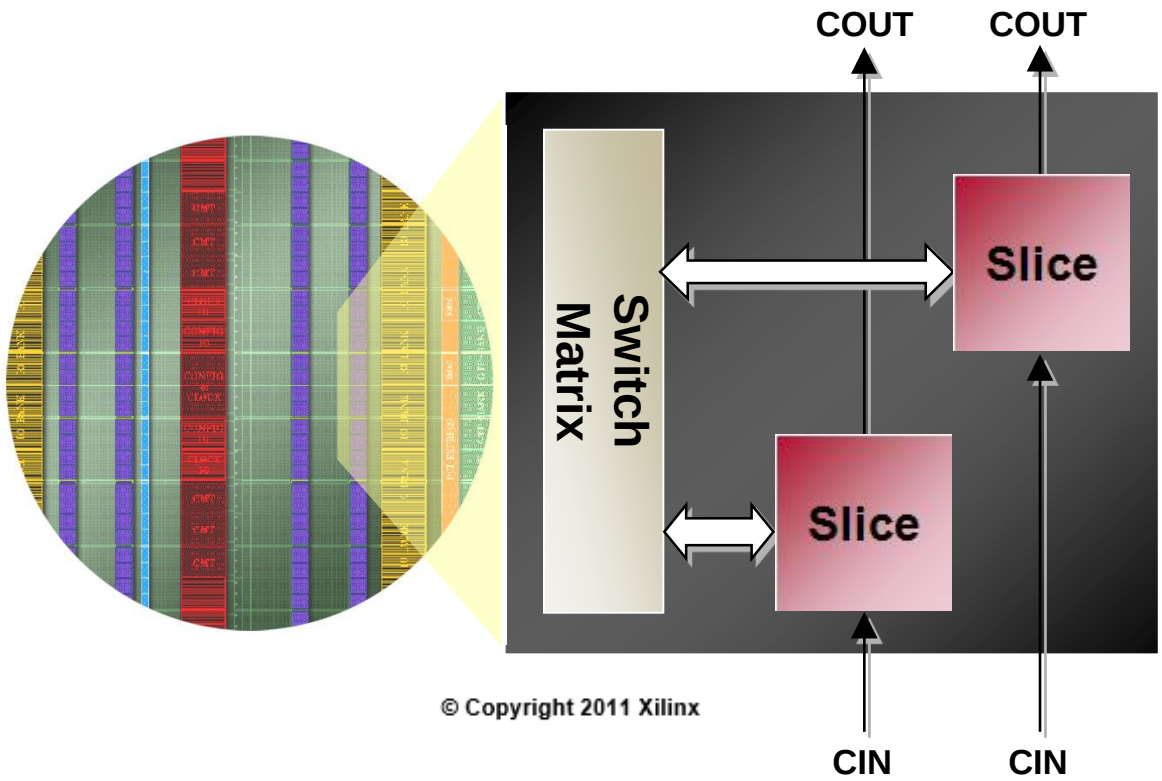
Liang Liu
liang.liu@eit.lth.se

Storage Components in a Xilinx Device

- **Distributed RAM**
  - Fast, localized
  - ideal for small data buffers, FIFOs, or register files
- **Block RAM**
  - For applications requiring large, on-chip memories



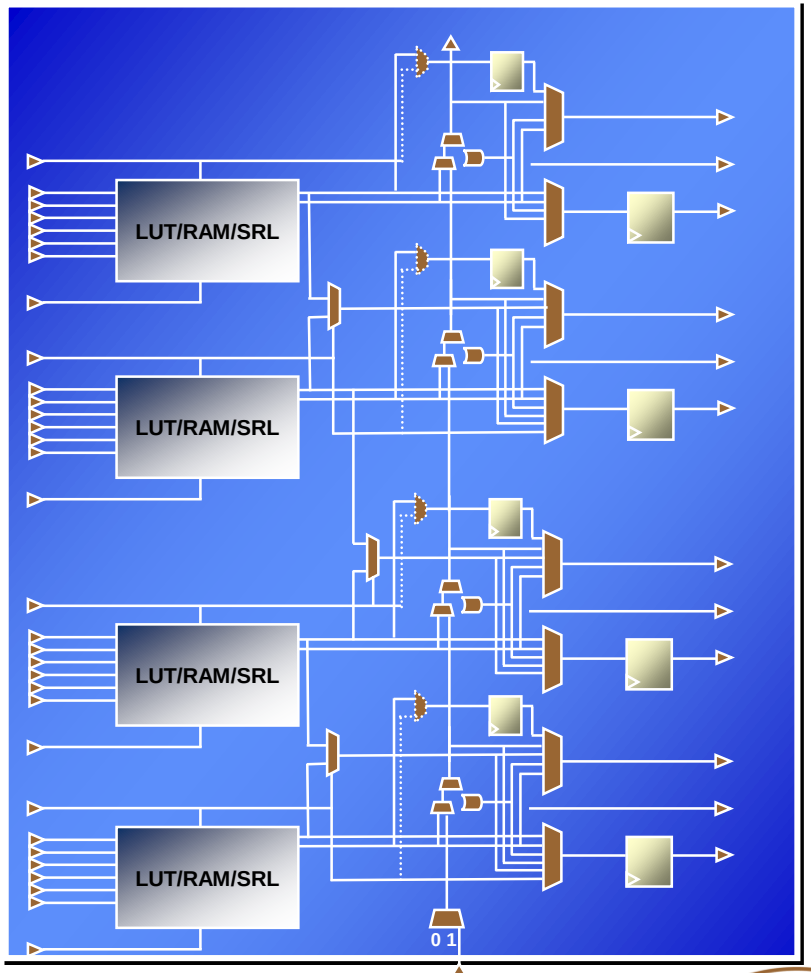
Xilinx CLB



- CLB contains two slices
- Connected to switch matrix for routing to other FPGA resources

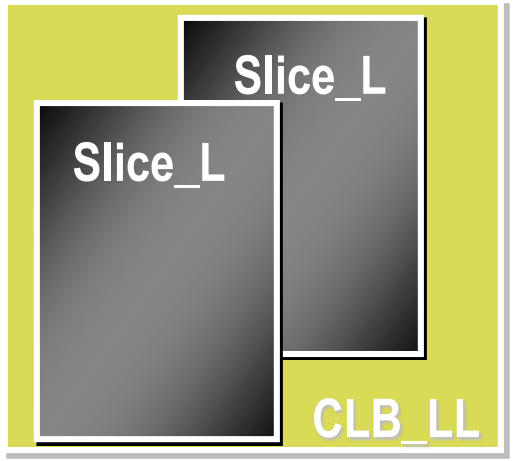
Xilinx Slice

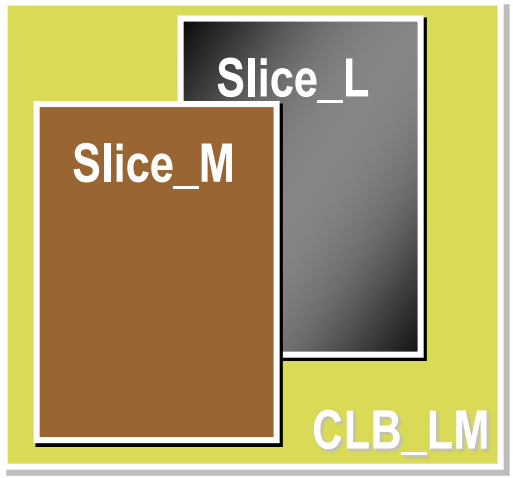
- Four six-input Look Up Tables (LUT)
- Wide multiplexers
- Carry chain
- Four flip-flop/latches
- Four additional flip-flops



Two type of slice

- **Two types of slices**
- **SLICEM: Full slice**
  - LUT can be used for logic and memory/SRL
  - Has wide multiplexers and carry chain
- **SLICEL: Logic and arithmetic only**
  - LUT can only be used for logic (not memory)
  - Has wide multiplexers and carry chain





SLICEM Used as Distributed Memory

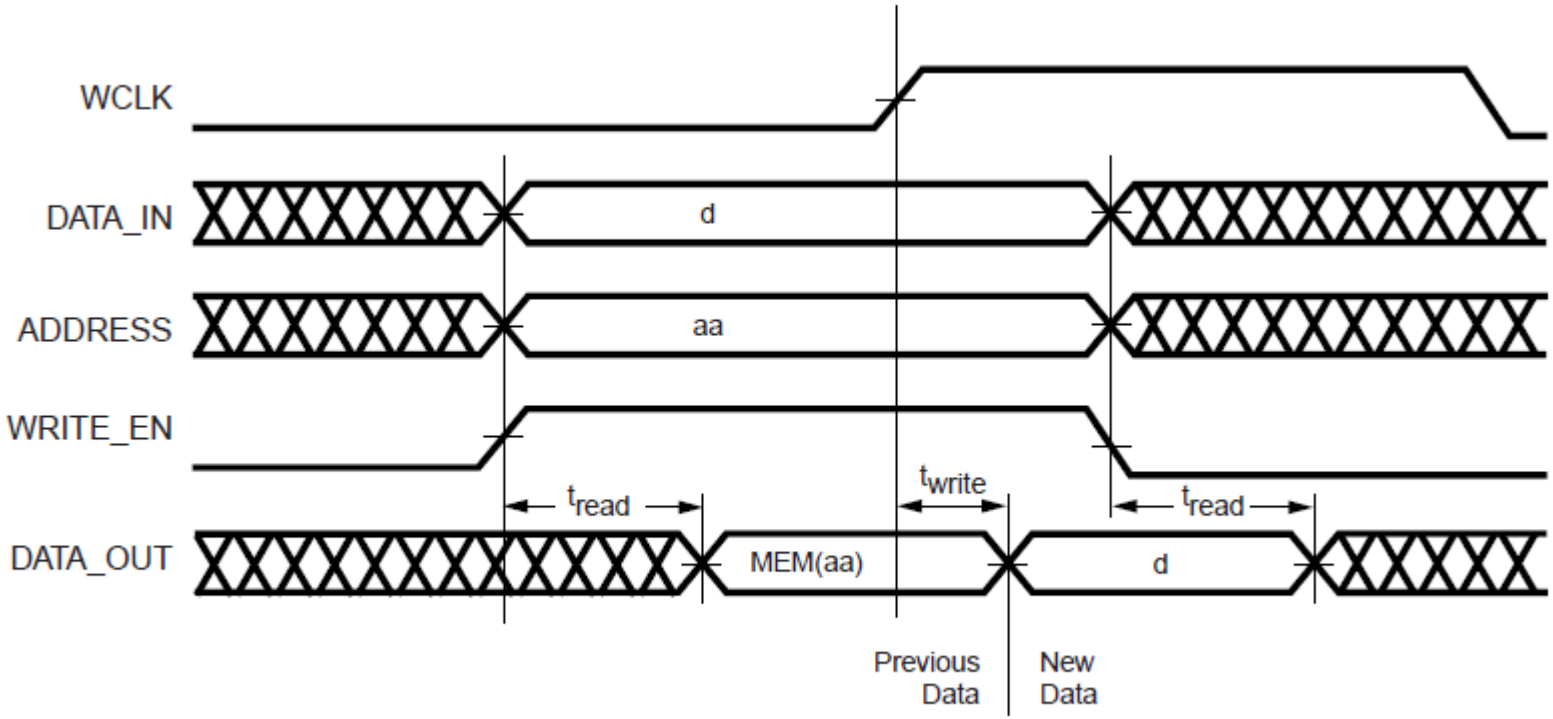
- **Various configurations**
  - Single port
    - One LUT6 = 64x1 or 32x2 RAM
    - Cascadable up to 256x1 RAM
  - Dual port (D)
    - 1 read / write port + 1 read-only port
  - Simple dual port (SDP)
    - 1 write-only port + 1 read-only port
  - Quad-port (Q)
    - 1 read / write port + 3 read-only ports
- **Synchronous write**
- **Asynchronous read**
  - Accompanying flip-flops can be used to create synchronous read

Single Port	Dual Port	Simple Dual Port	Quad Port
32x2	32x2**D**	32x6**SDP**	32x2**Q**
32x4	32x4**D**	64x3**SDP**	64x1**Q**
32x6	64x1**D**		
32x8	64x2**D**		
64x1	128x1**D**		
64x2			
64x3			
64x4			
128x1			
128x2			
256x1			

Xilinx Distributed Memory

Timing

- Synchronous write
- Asynchronous read



x464_02_070303

Artix-7 Block Memory

Logic Fabric
LUT-6 CLB

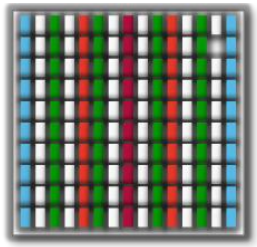
Precise, Low Jitter Clocking
MMCMs

On-Chip Memory
36Kbit/18Kbit Block RAM

Enhanced Connectivity
PCIe® Interface Blocks

DSP Engines
DSP48E1 Slices

Hi-perf. Parallel I/O Connectivity
SelectIO™ Technology

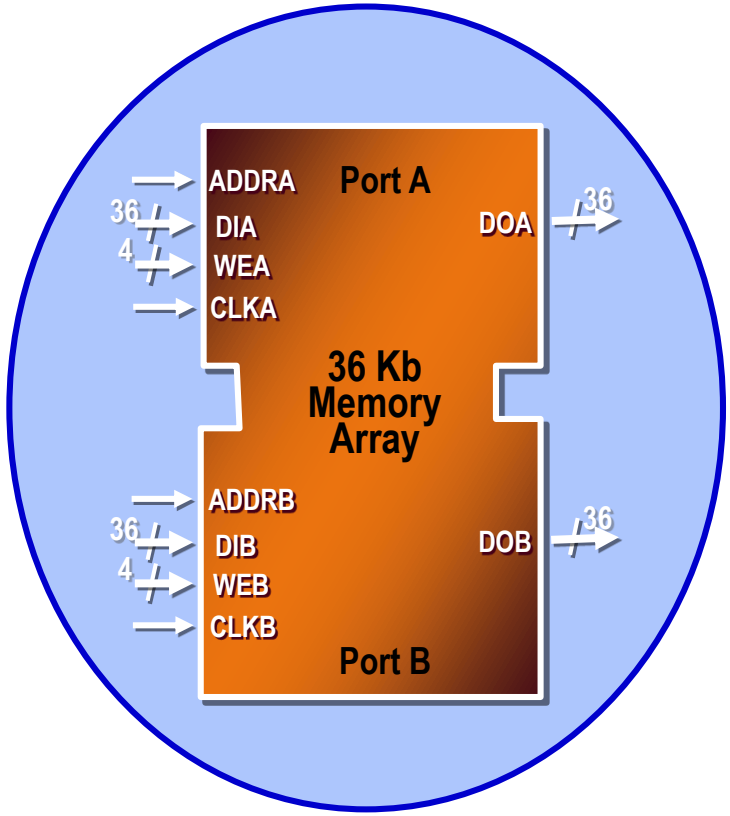


Artix™-7 FPGA

- **Most efficient memory implementation**
  - Dedicated blocks of memory
  - **4,860 Kbits** of fast block RAM for Artix-7 100T
- **Builds both single and true dual-port RAMs**
- **Synchronous write and read (different from distributed RAM)**

Artix-7 Block Memory

- **36K/18K block RAM**
- **Configurations**
  - 32k x 1 to 512 x 72 in one 36K block
  - Simple dual-port and true dual-port configurations
  - Built-in FIFO logic
  - 64-bit error correction coding per 36K block
  - Adjacent blocks combine to 64K x 1 without extra logic



Block RAM Ports

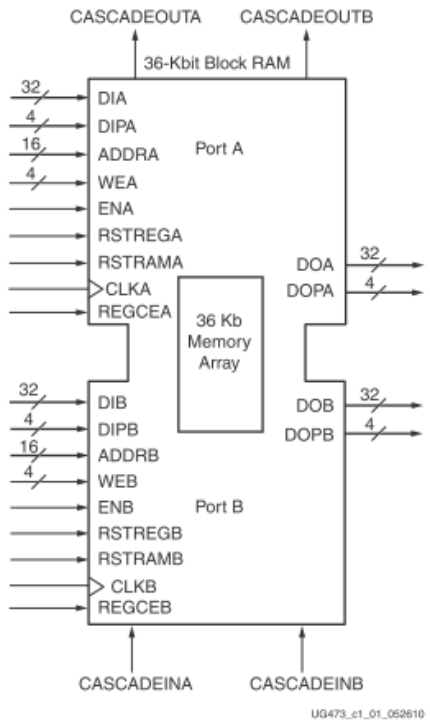


Table 1-3: **True Dual-Port Functions and Descriptions**

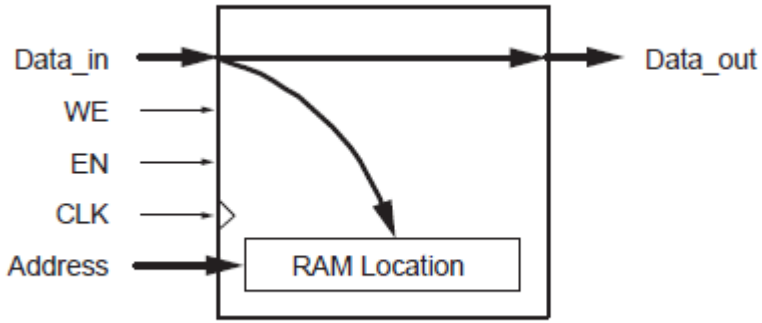
Port Function	Description
DI[A | B]	Data input bus.
DIP[A | B](1)	Data input parity bus. Can be used for additional data inputs.
ADDR[A | B]	Address bus.
WE[A | B]	Byte-wide write enable.
EN[A | B]	When inactive no data is written to the block RAM and the output bus remains in its previous state.
RSTREG[A | B]	Synchronous Set/Reset the output registers (DO_REG = 1). The RSTREG_PRIORITY attribute determines the priority over REGCE.
RSTRAM[A | B]	Synchronous Set/Reset the output data latches.
CLK[A | B]	Clock input.
DO[A | B]	Data output bus.
DOP[A | B](1)	Data output parity bus. Can be used for additional data outputs.
REGCE[A | B]	Output Register clock enable.
CASCADEIN[A | B]	Cascade input for 64K x 1 mode.
CASCADEOUT[A | B]	Cascade output for 64K x 1 mode.

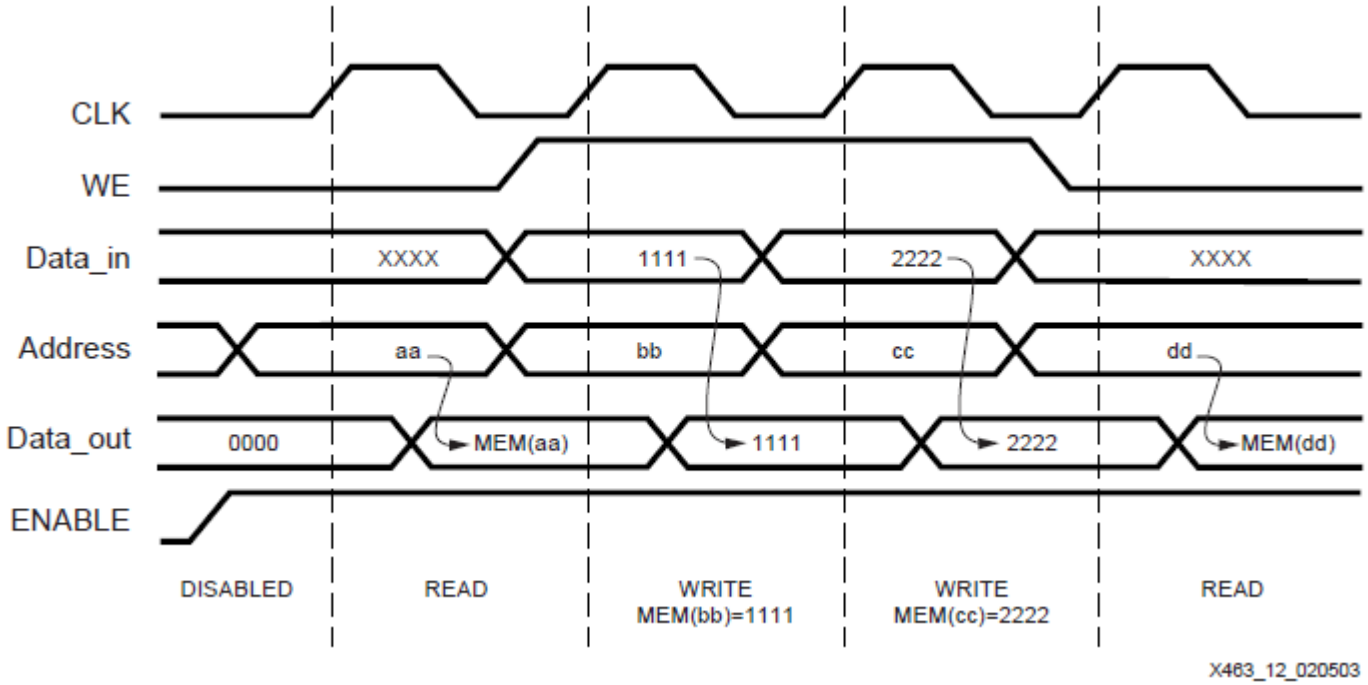
- **$DI_{A,B}$: the data path width at ports A,B.**
- **$ADDR_{A,B}$: the address bus width at ports A, B**
- **The control signals CLK, WE, EN**
- **Reset signal does NOT affect memory cells**

Block RAM: Operation Modes

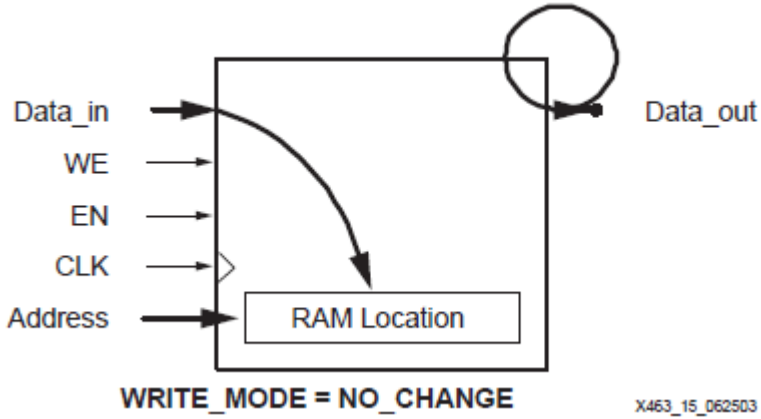
Write Mode	Effect on Same Port	Effect on Opposite Port (dual-port mode only, same address)
WRITE_FIRST Read After Write (Default)	Data on DI, DIP inputs written into specified RAM location and simultaneously appears on DO, DOP outputs.	Invalidates data on DO, DOP outputs.
READ_FIRST Read Before Write (Recommended)	Data from specified RAM location appears on DO, DOP outputs. Data on DI, DIP inputs written into specified location.	Data from specified RAM location appears on DO, DOP outputs.
NO_CHANGE No Read on Write	Data on DO, DOP outputs remains unchanged. Data on DI, DIP inputs written into specified location.	Invalidates data on DO, DOP outputs.

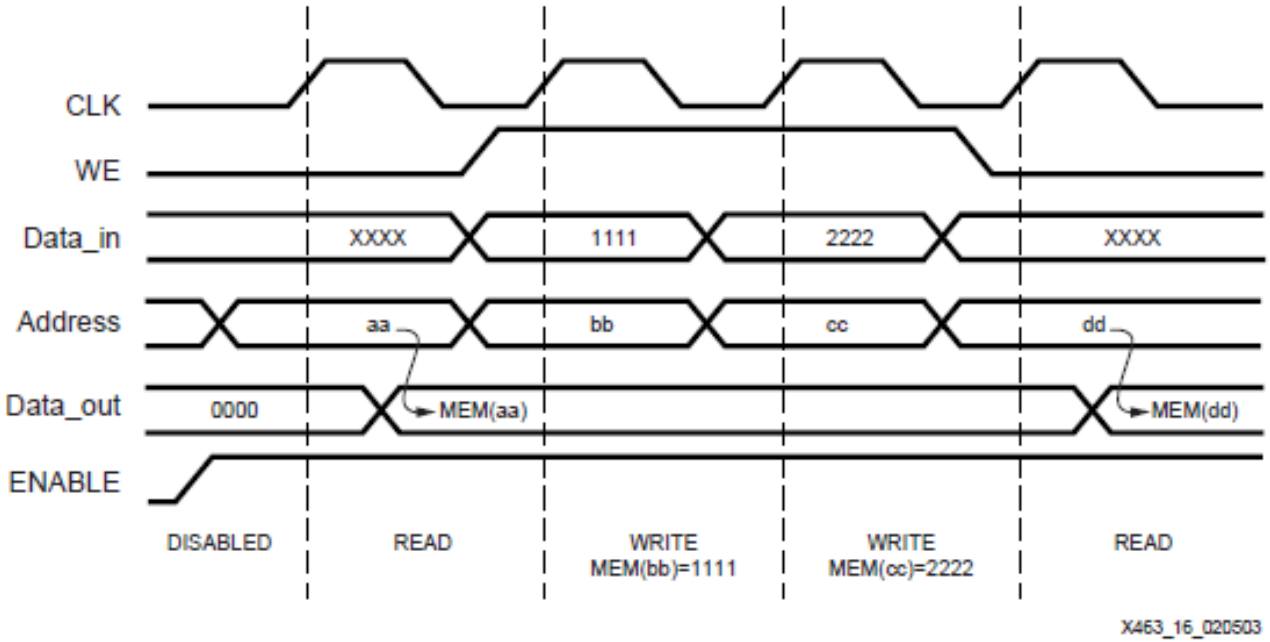
Block RAM: WRITE_FIRST



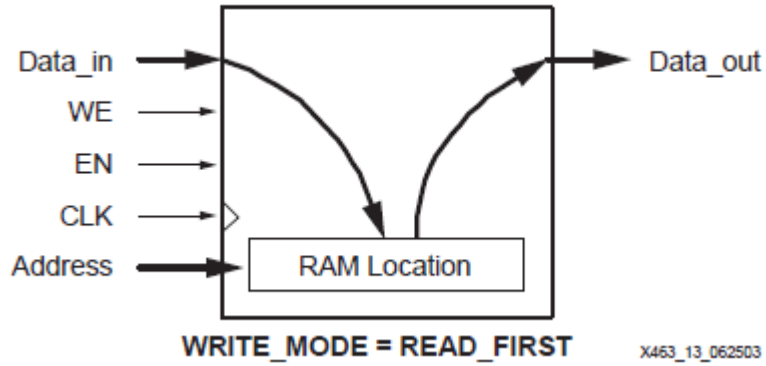


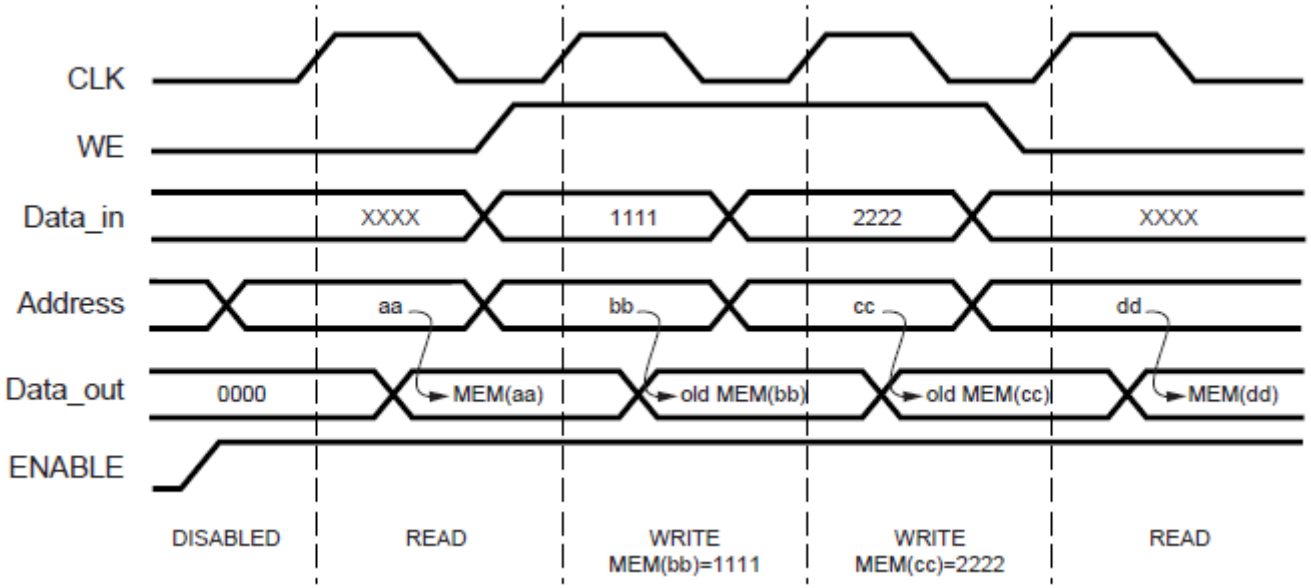
Block RAM: NO_CHANGE





Block RAM: READ_FIRST (Recomm.)





Reading Advice

- RTL Hardware Design Using VHDL: P276-P292
- UG437 7 Series FPGAs Memory Resources
- UG901 Vivado Design Suite User Guide Synthesis