

# EITF35: Introduction to QuestaSim

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# Typical (ASIC/FPGA) Design Flow



- RTL simulation: Proves functionality without timing information.
- GL simulation: Verifies netlist with timing information (slow)
- PL simulation: Verification with parasitics (even slower)



#### **Questasim overview**

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#### **Create new project**



#### **Add VHDL files**



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# **Compiling the project**

Compile →Compile Order



### Simulation

# Right-click on your design (testbench) and select simulate

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#### Waveform viewer



**Different options for zooming** 

Different options to jump with the cursor to falling or rising edges



#### Waveform viewer (cont.)



To change representation style of a bus, right-click on the signal, then Radix



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#### **Errors/warnings in the designs**

