LUND
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EITF35:
Introduction to QuestaSim

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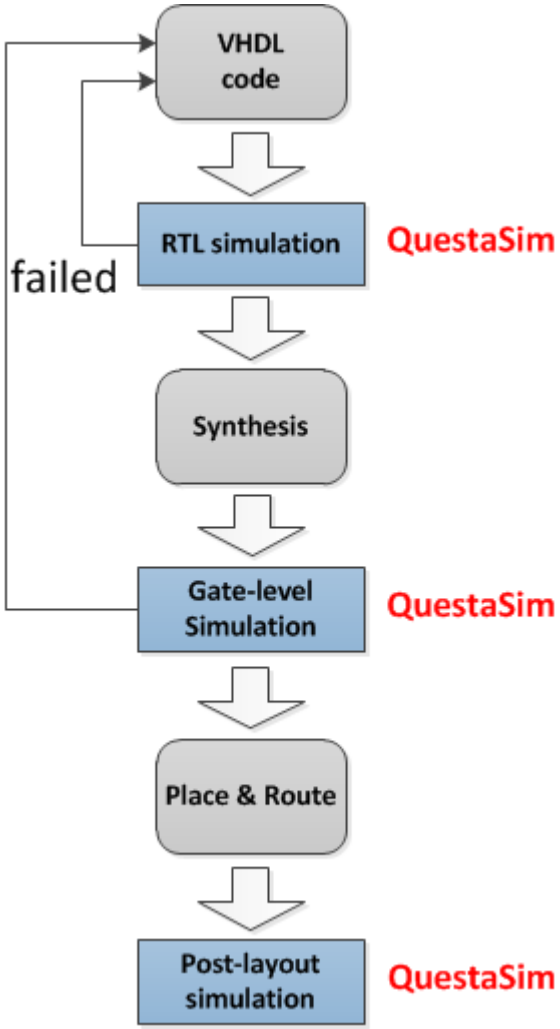
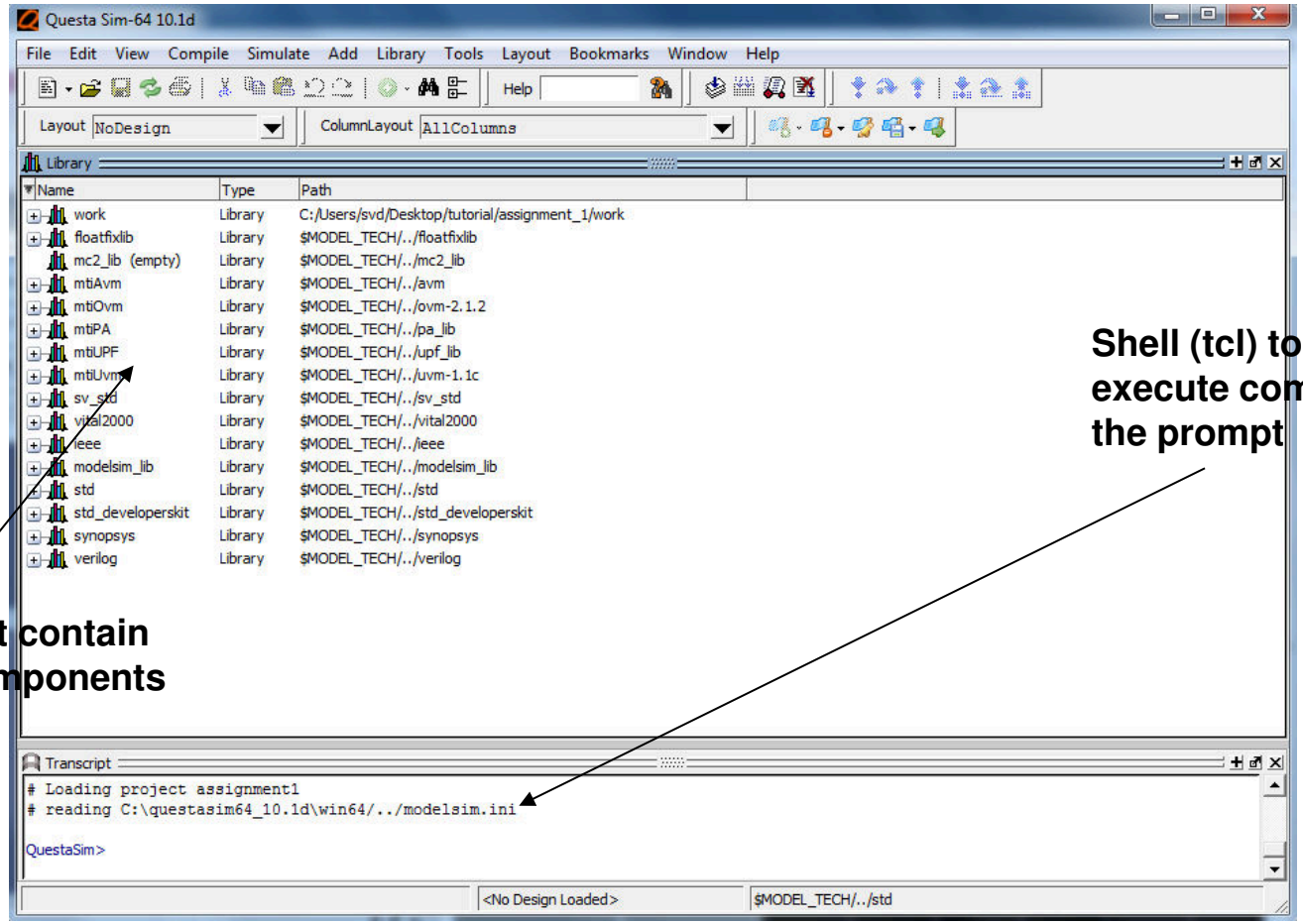
Typical (ASIC/FPGA) Design Flow



- RTL simulation: Proves functionality without timing information.
- GL simulation: Verifies netlist with timing information (slow)
- PL simulation: Verification with parasitics (even slower)

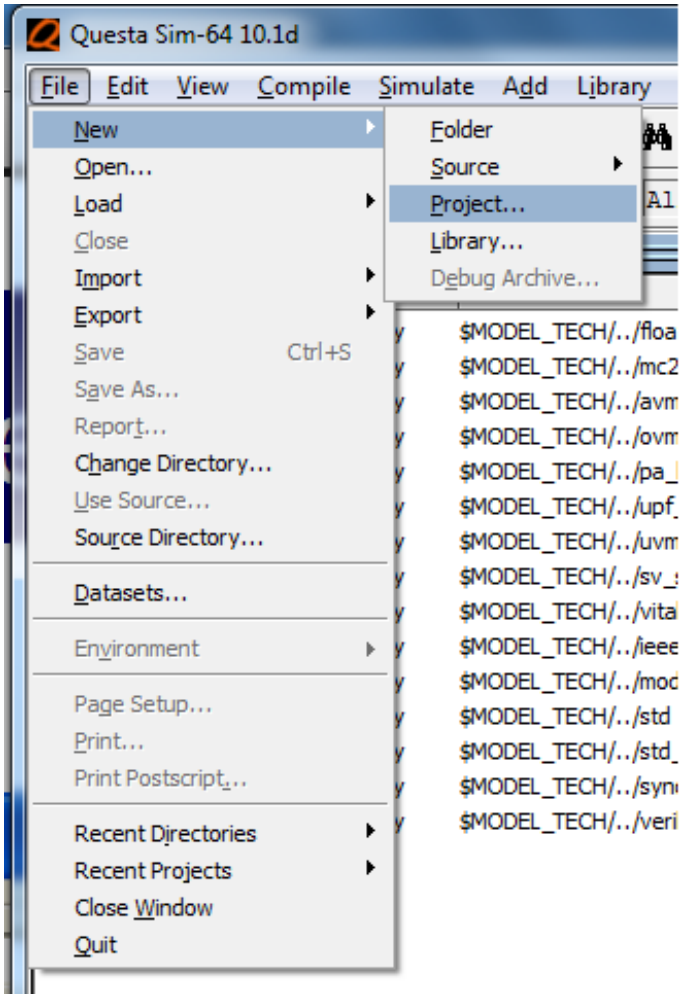
Questasim overview

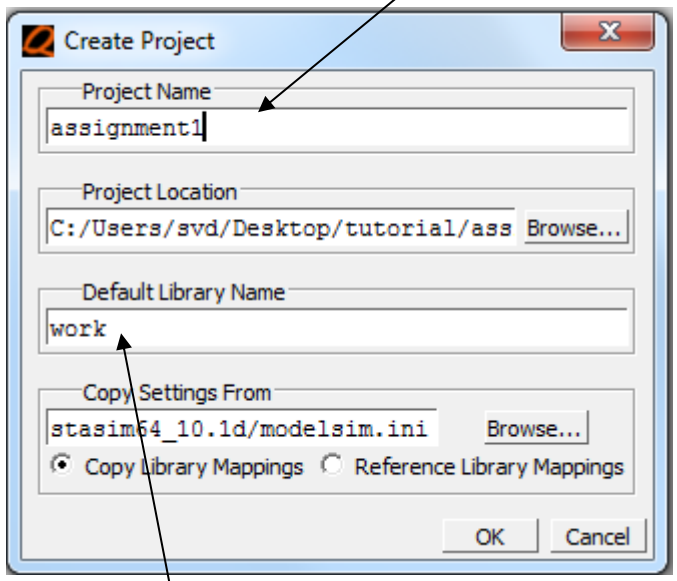


Libraries that contain compiled components

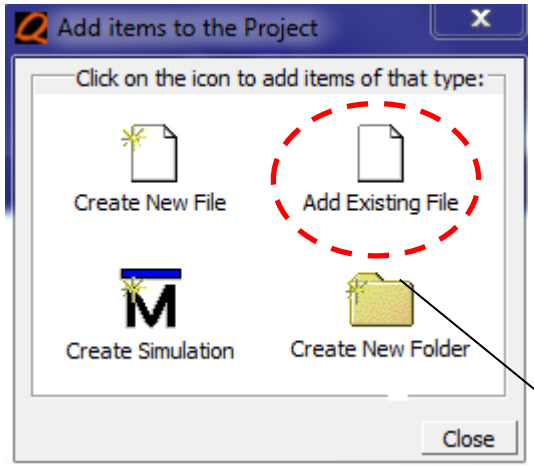
Shell (tcl) to write and execute commands from the prompt

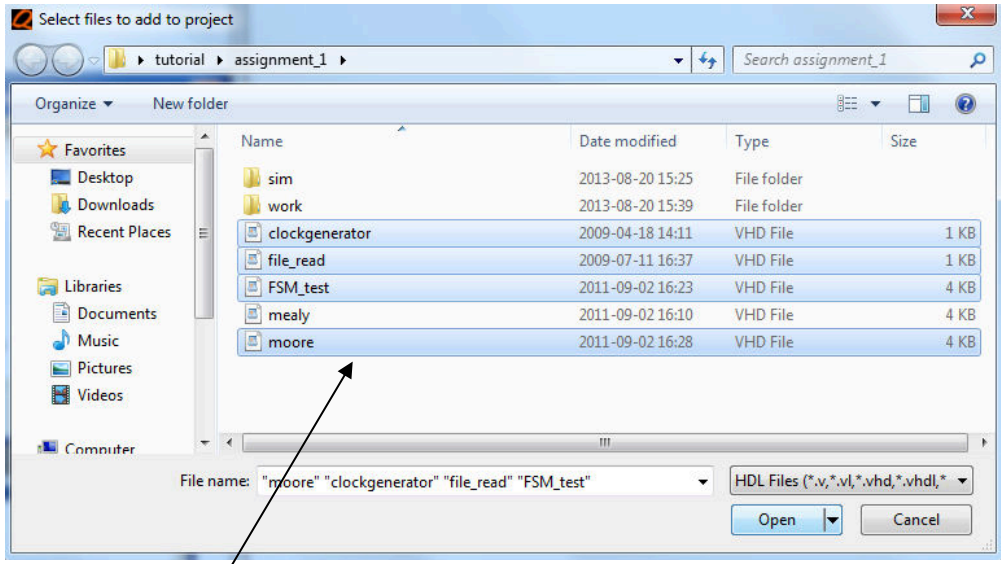
Create new project



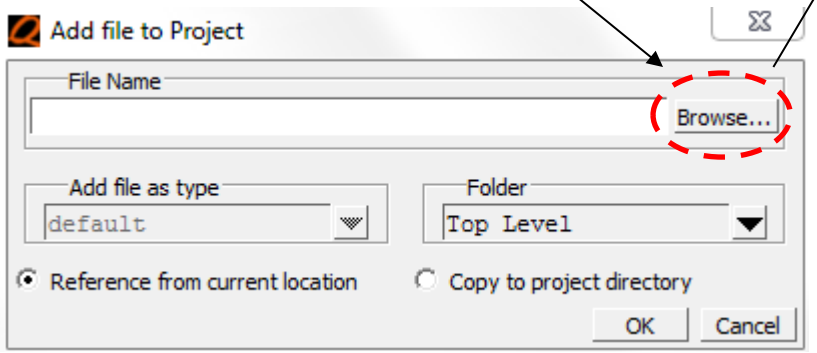


Add VHDL files



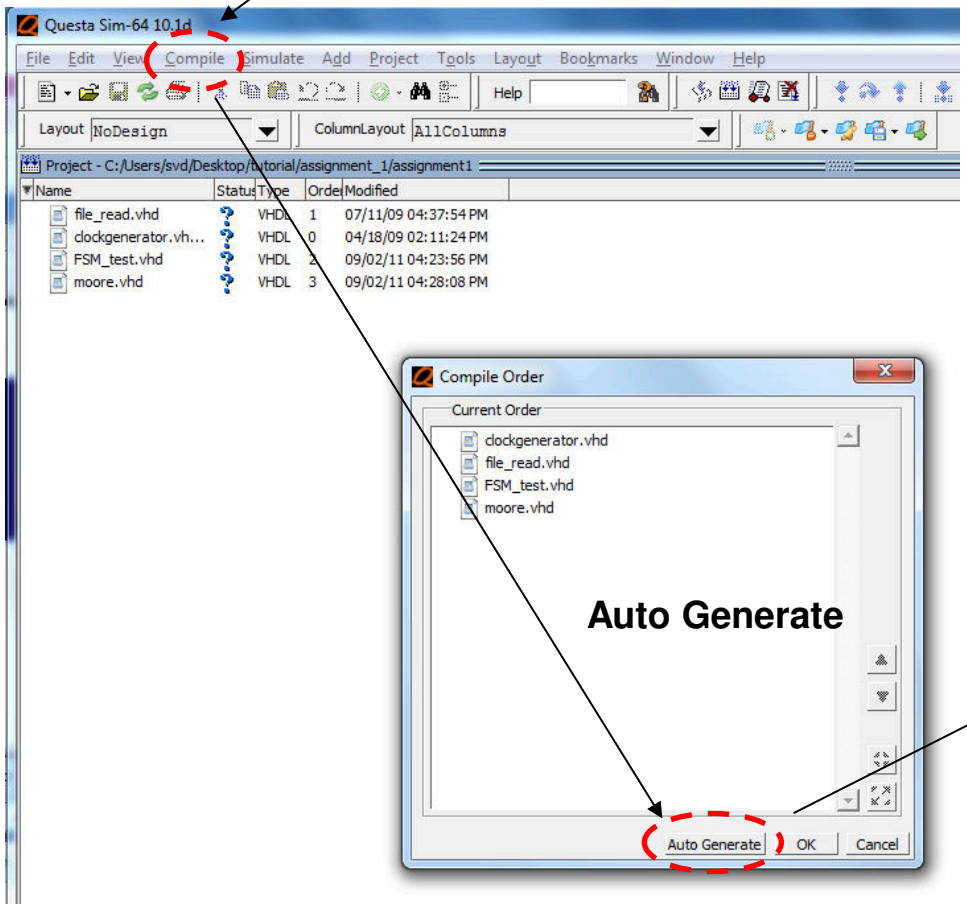


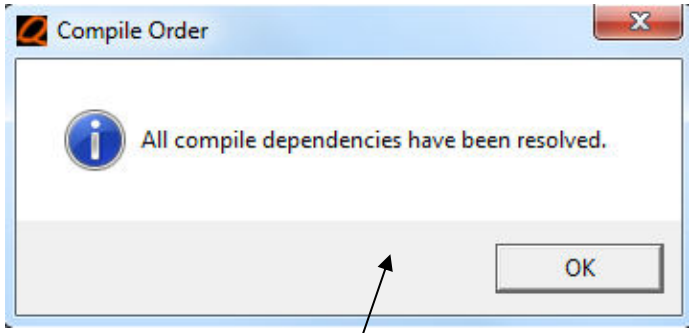
Select files required for simulation

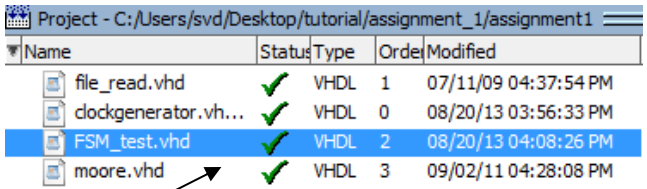


Compiling the project

Compile →Compile Order



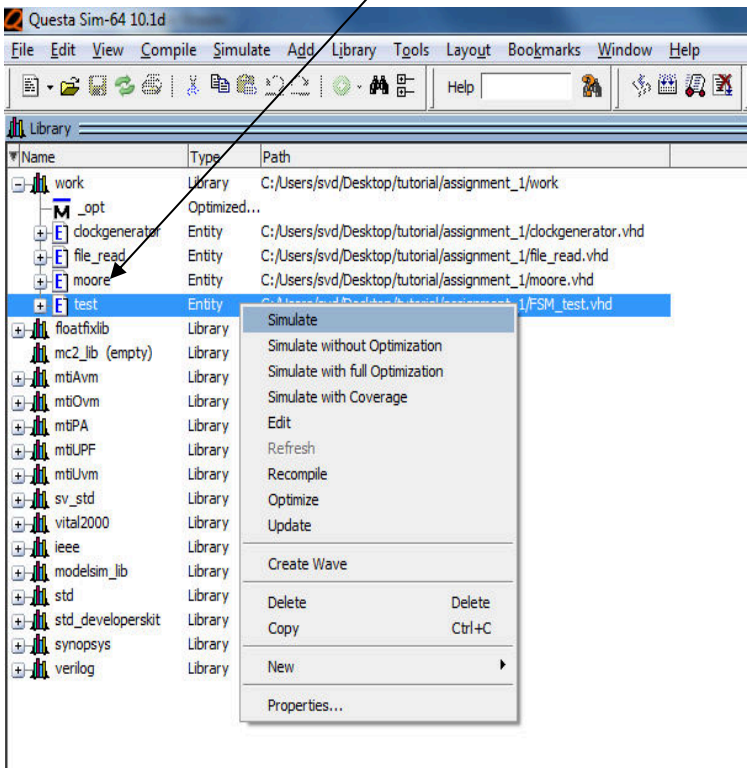


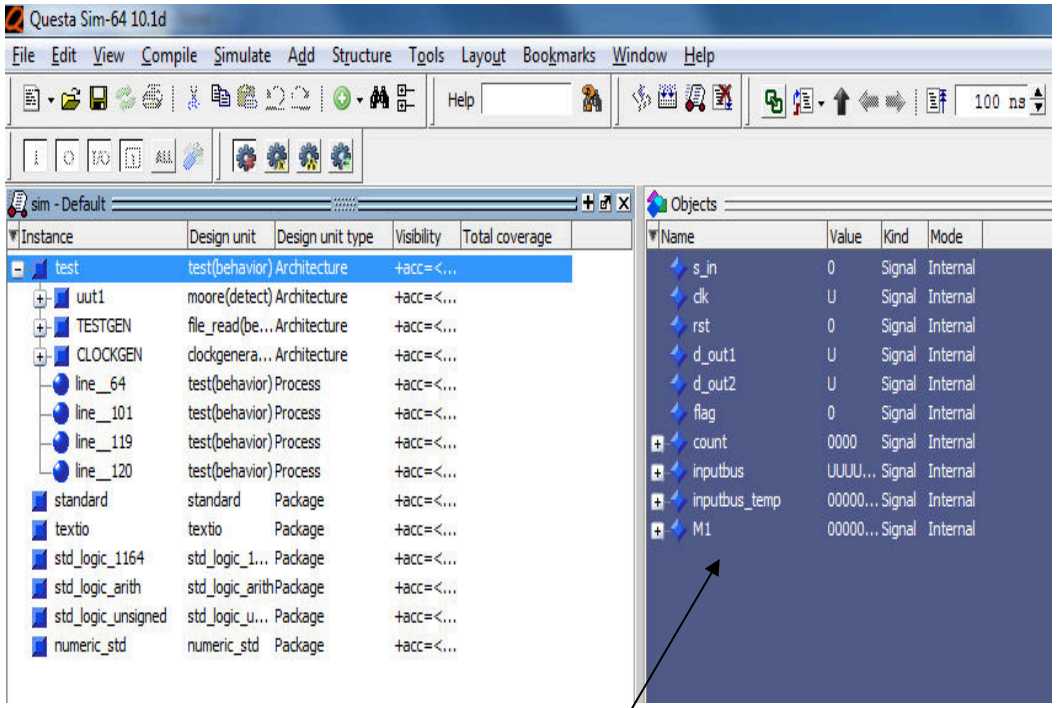


A green check shows for each file if the compilation was successful

Simulation

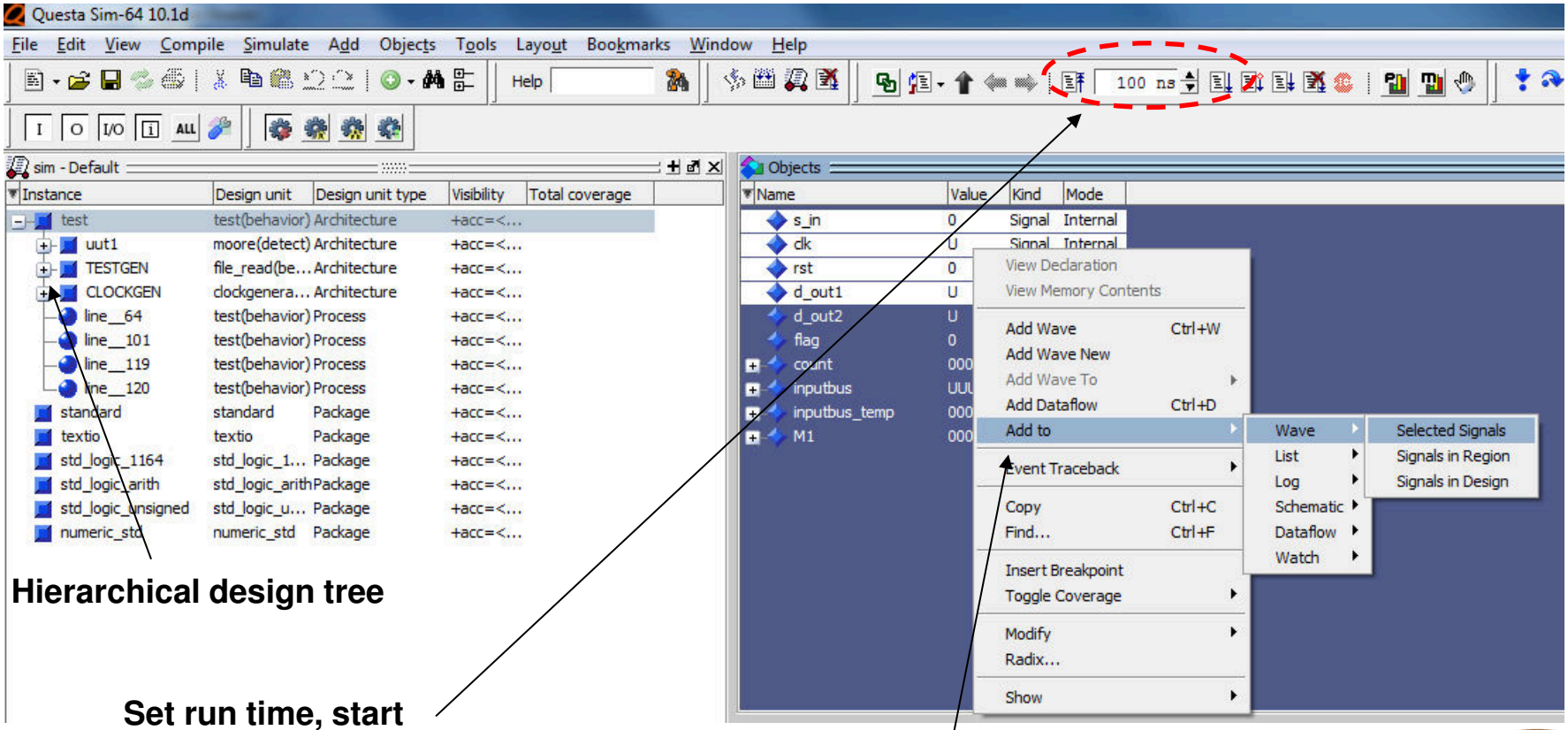
Right-click on your design (testbench) and select simulate





Signals on top level

Adding signals to waveform

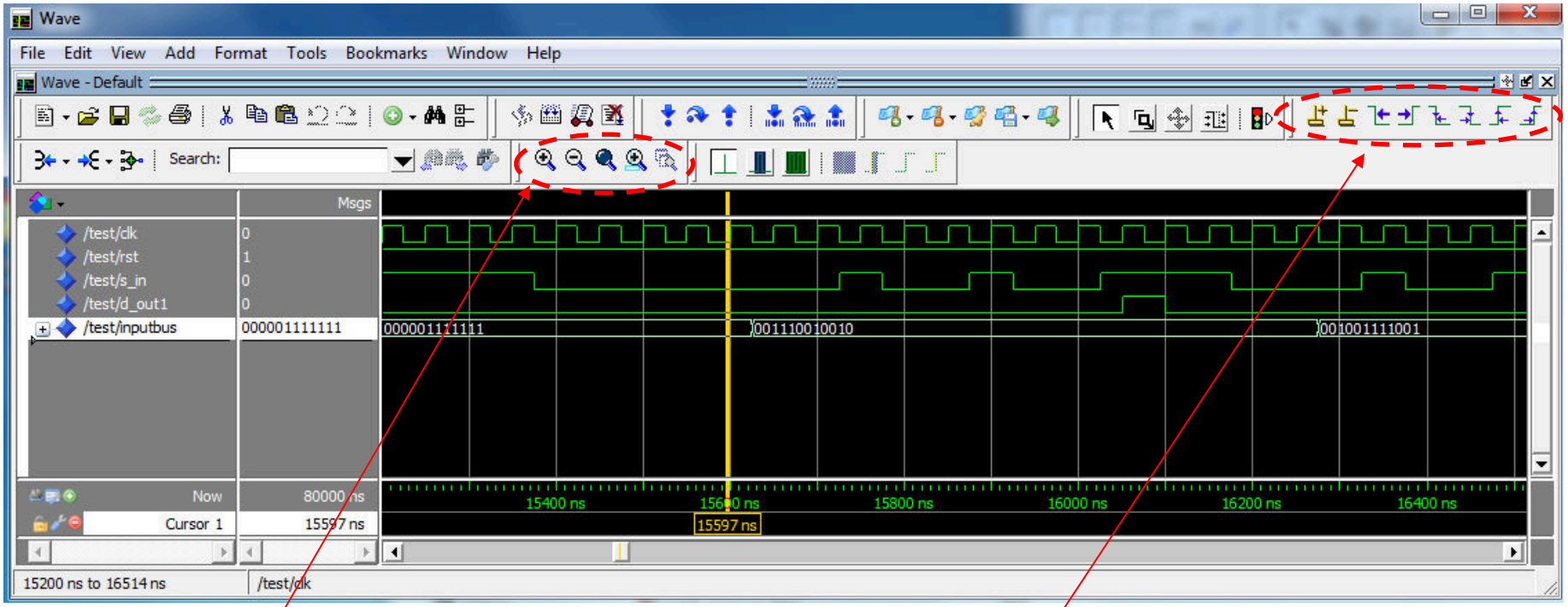


Hierarchical design tree

Set run time, start simulation run or restart simulation after re-compilation

Mark signals to be shown in waveform and click Add to →Wave →Selected Signals

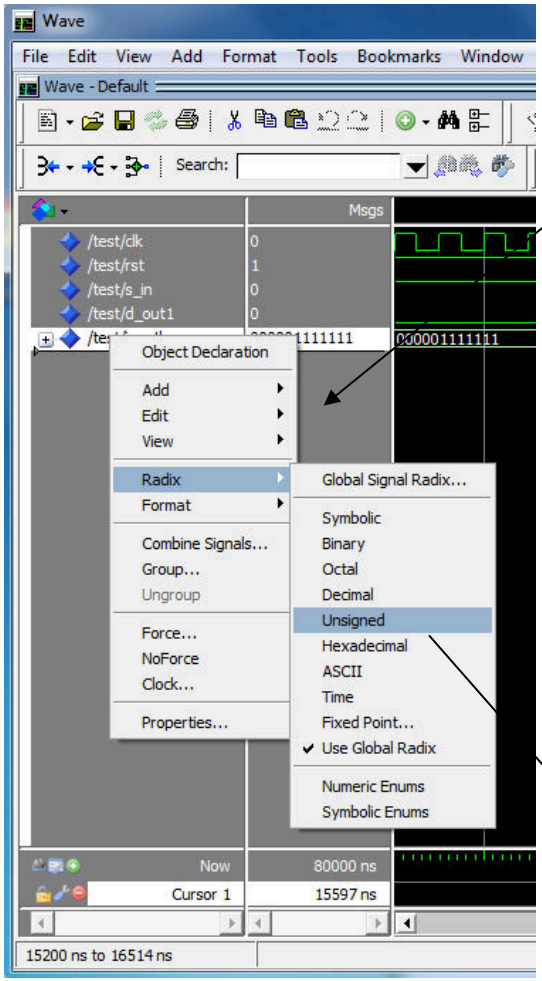
Waveform viewer



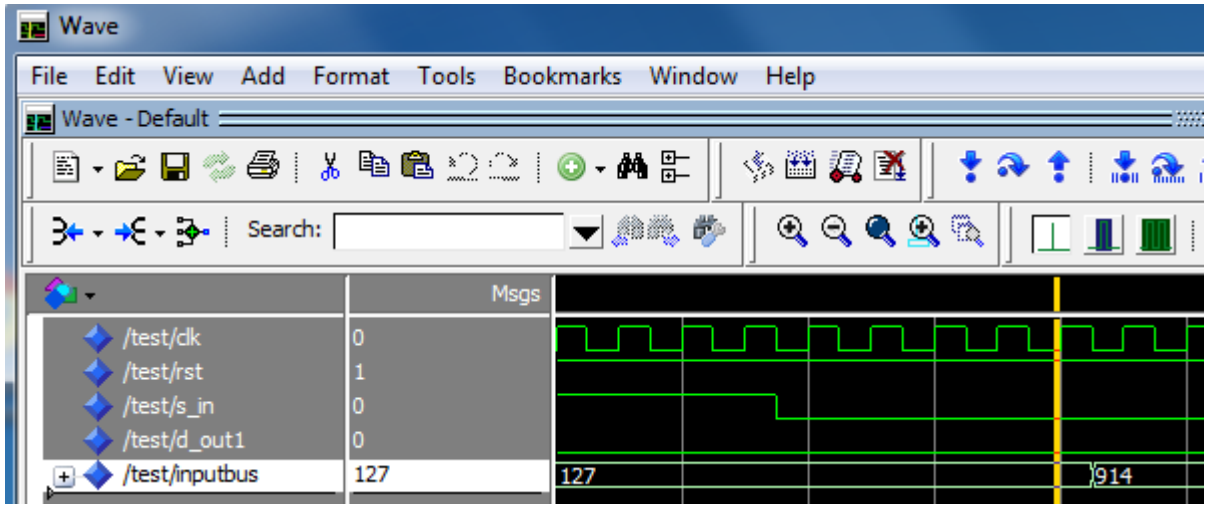
Different options for zooming

Different options to jump with the cursor to falling or rising edges

Waveform viewer (cont.)



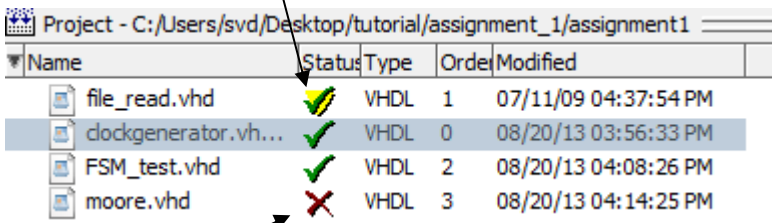
To change representation style of a bus, right-click on the signal, then Radix

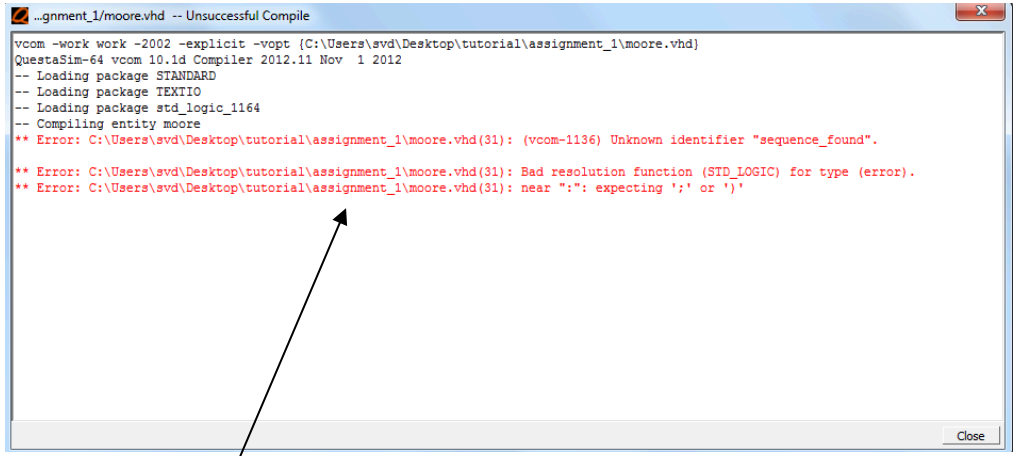


The signal is now shown in an unsigned representation instead of binary

Errors/warnings in the designs

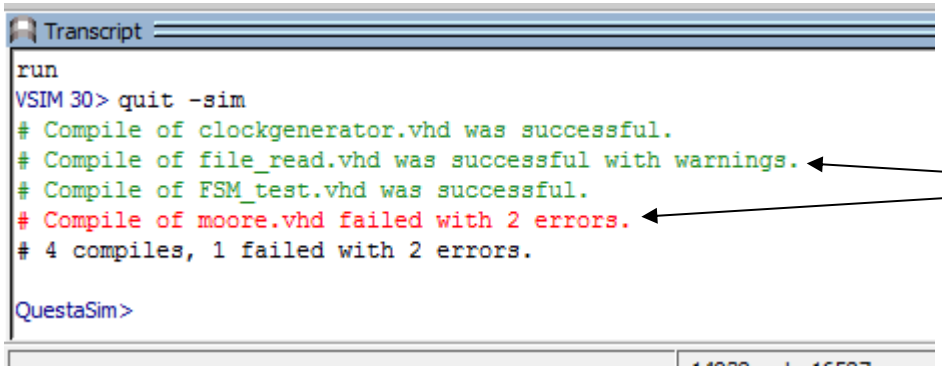
Warning for the design/file





Error in the design/file

A window stating the errors/warnings pops-up



Double-click on the message in the transcript window to get the error/warning messages