



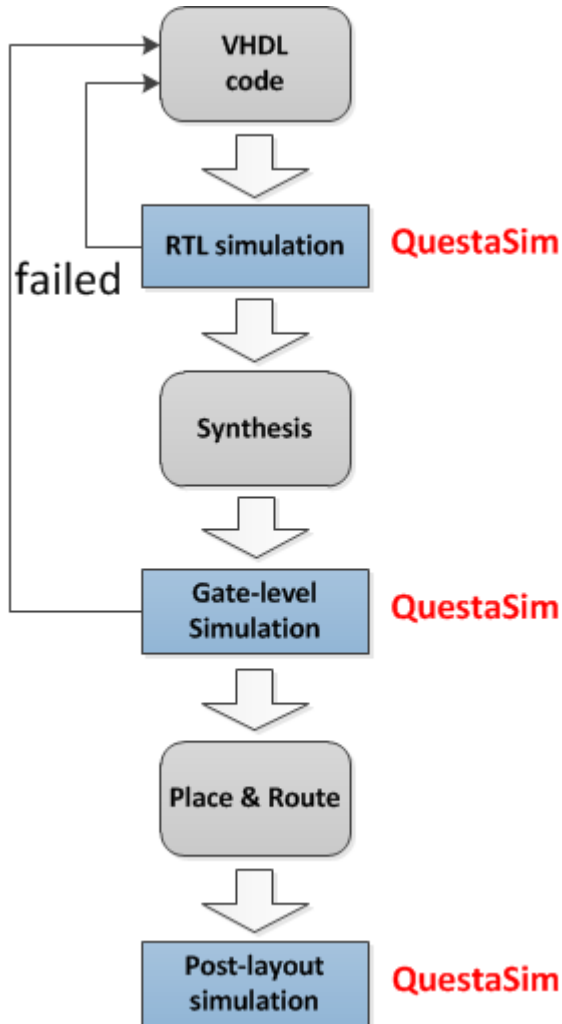
LUND
UNIVERSITY

EITF35: Introduction to QuestaSim

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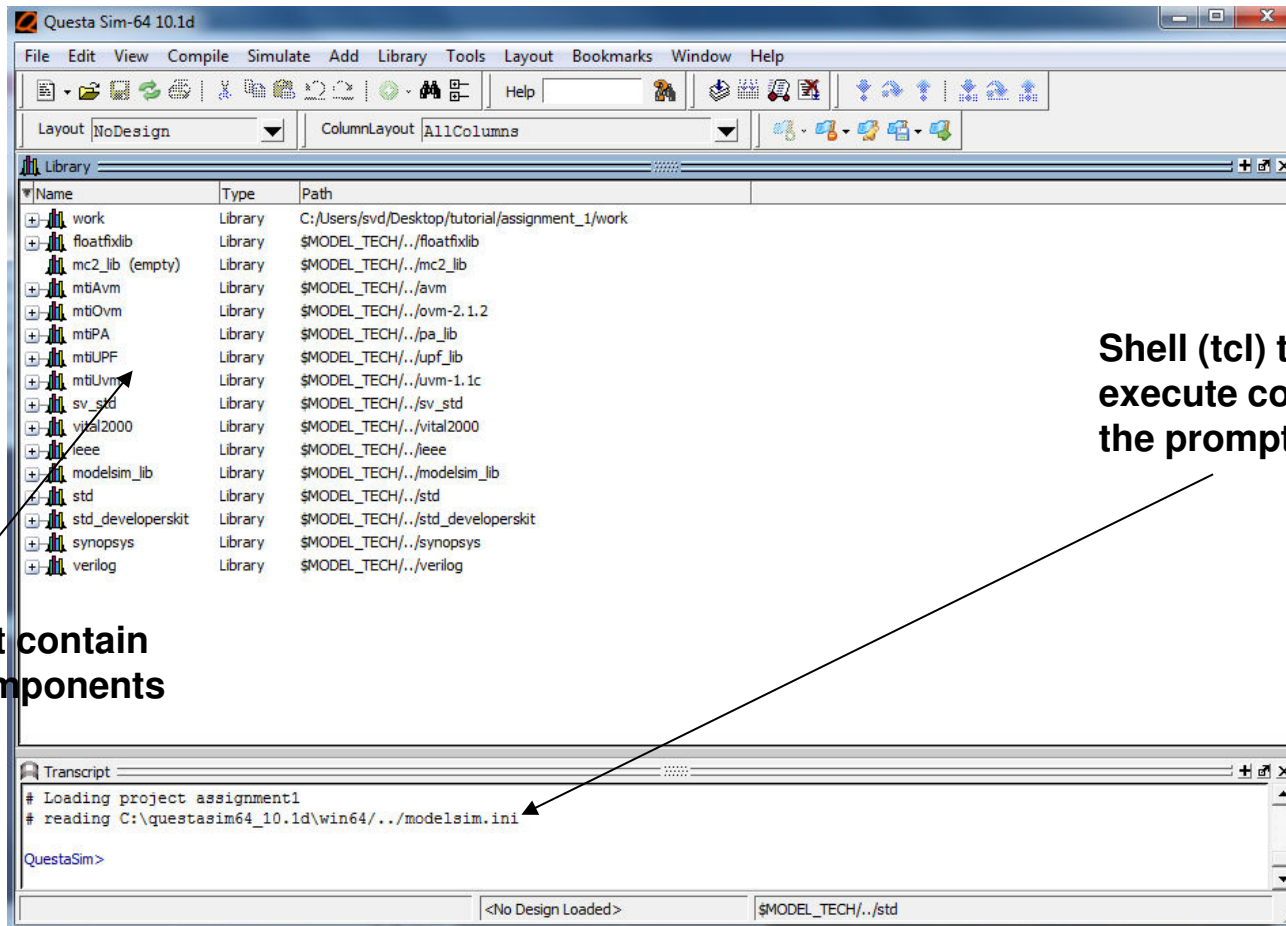
Typical (ASIC/FPGA) Design Flow



- RTL simulation: Proves functionality without timing information.
- GL simulation: Verifies netlist with timing information (slow)
- PL simulation: Verification with parasitics (even slower)



Questasim overview

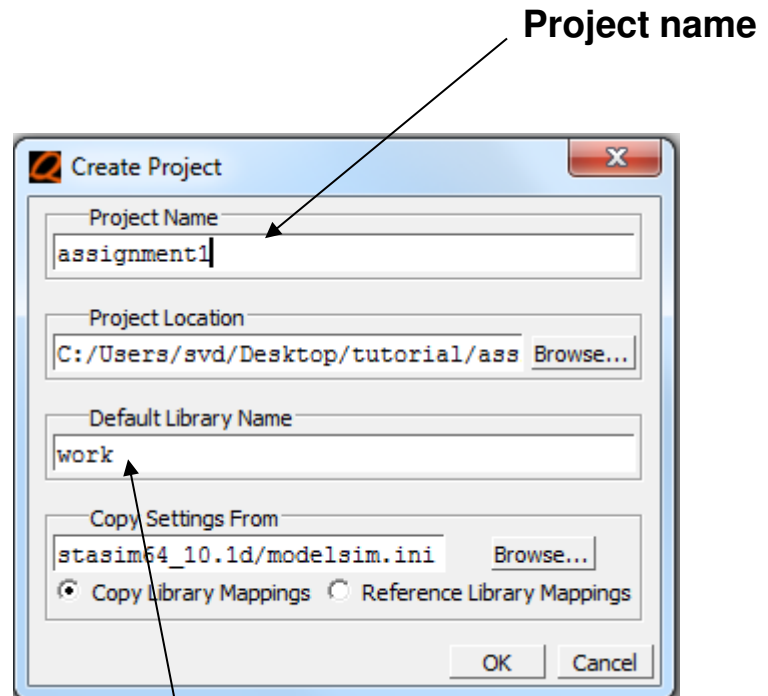
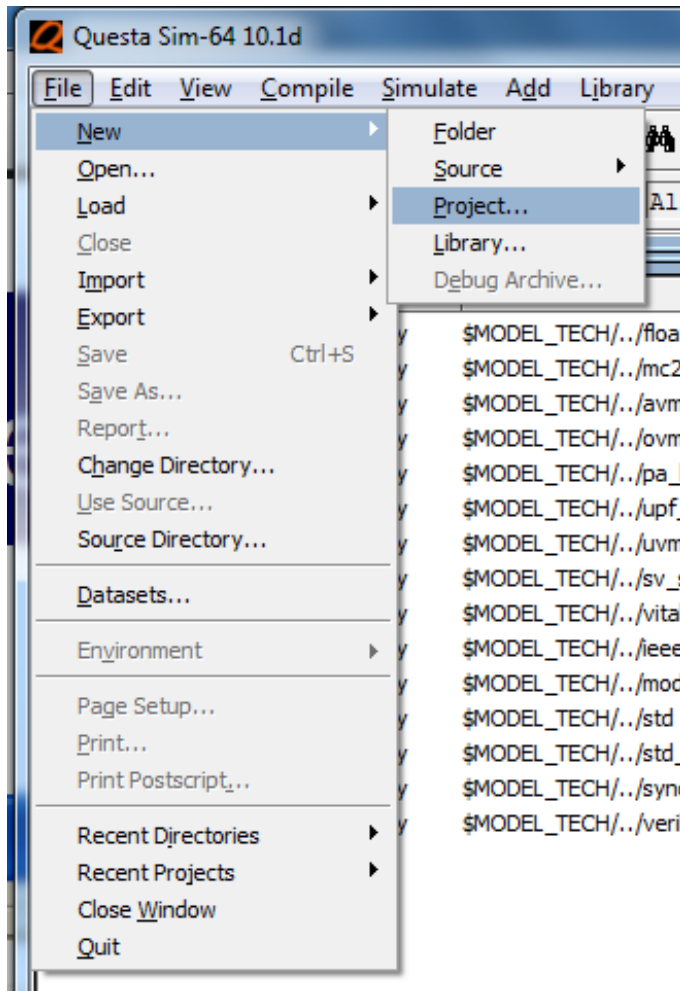


Libraries that contain
compiled components

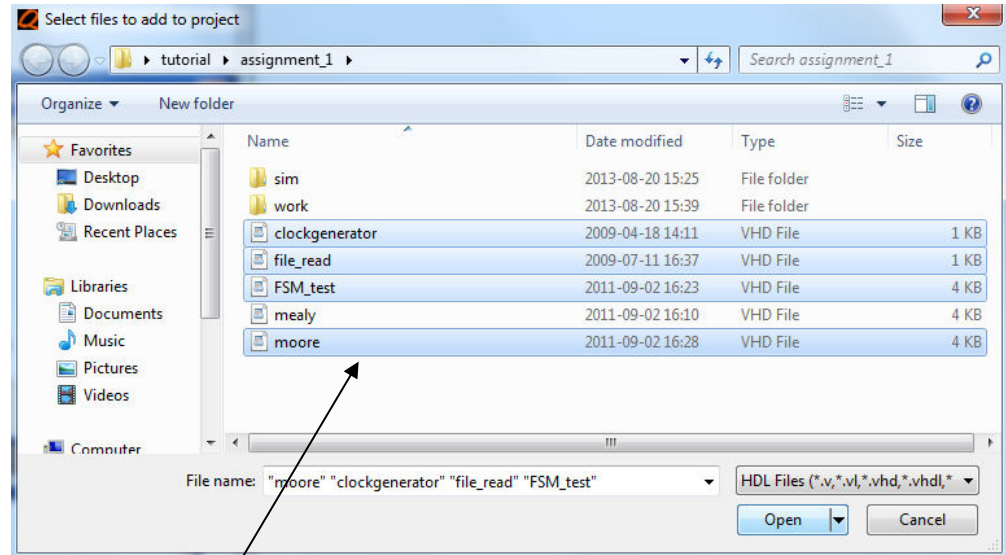
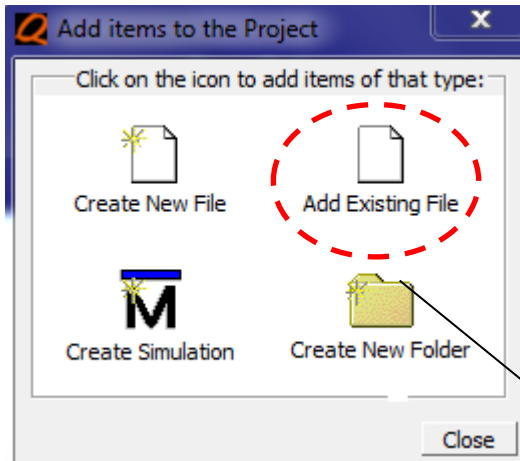
Shell (tcl) to write and
execute commands from
the prompt



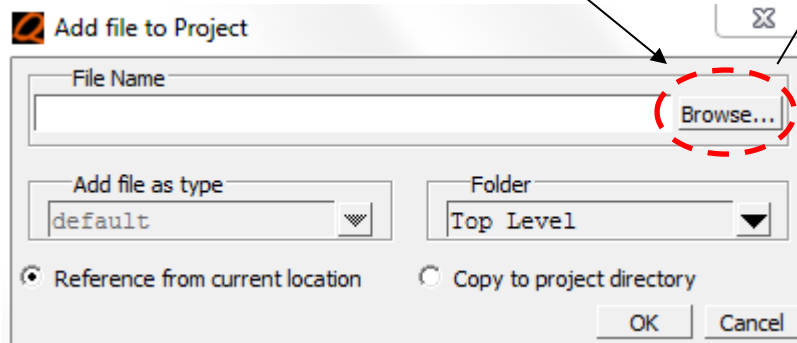
Create new project



Add VHDL files

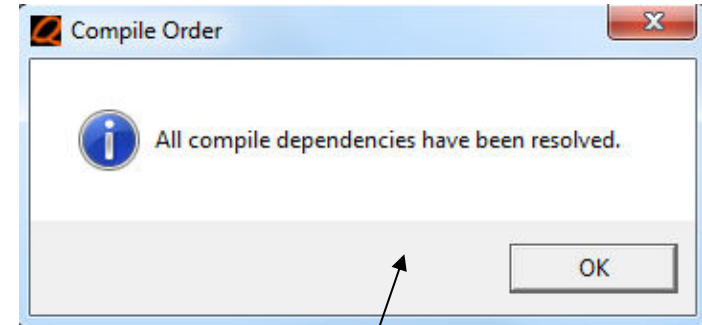
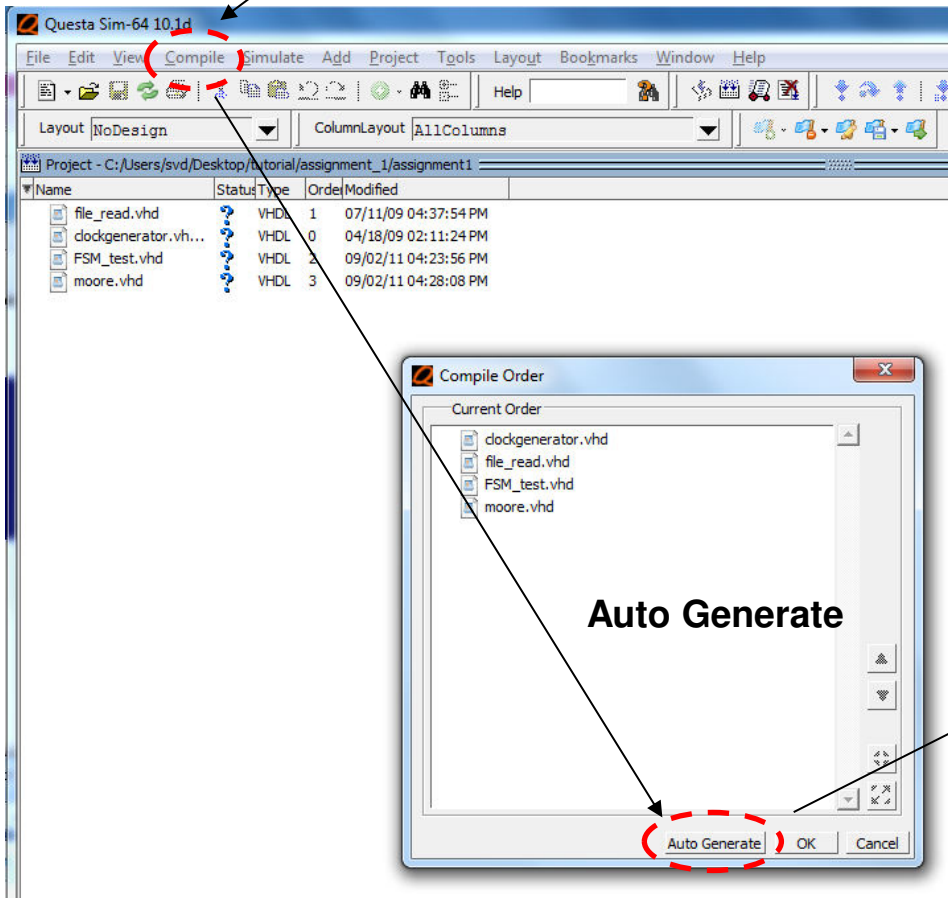


Select files required for simulation



Compiling the project

Compile → Compile Order



Project - C:/Users/svd/Desktop/tutorial/assignment_1/assignment1

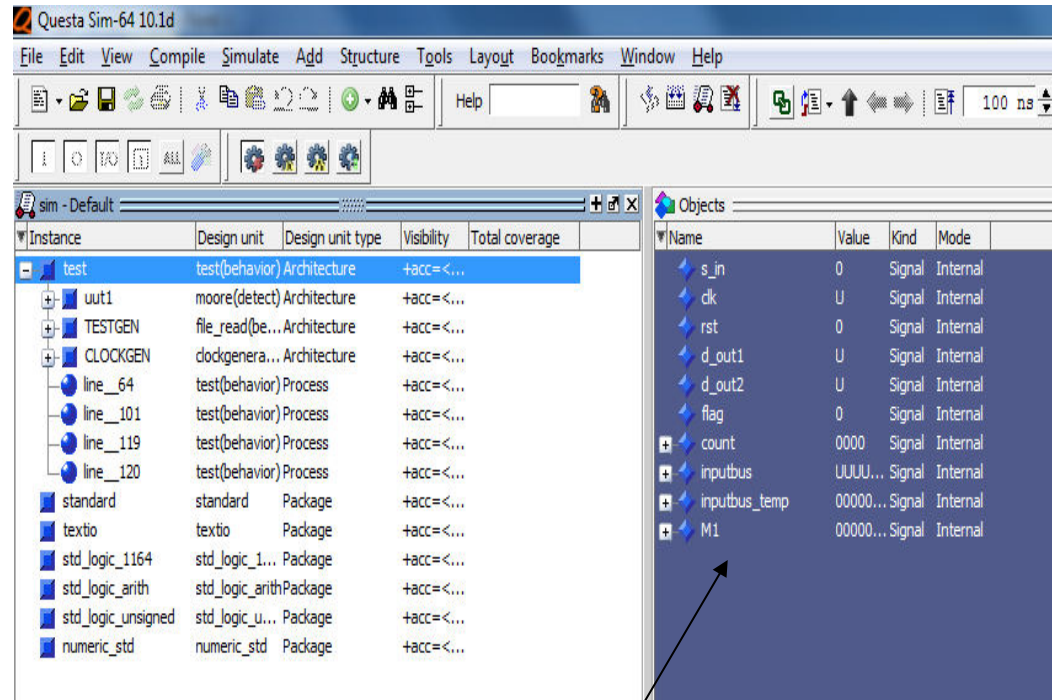
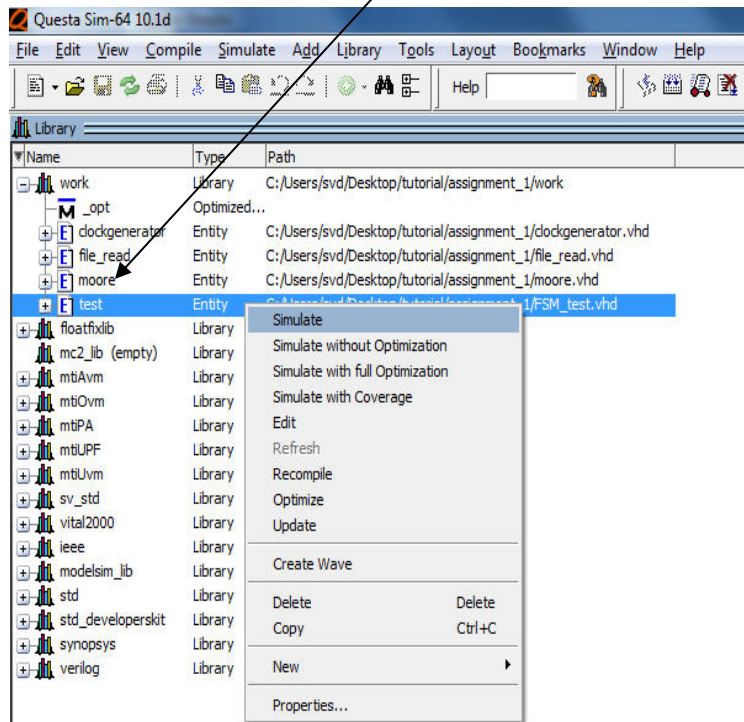
Name	Status	Type	Order	Modified
file_read.vhd	✓	VHDL	1	07/11/09 04:37:54 PM
clockgenerator.vh...	✓	VHDL	0	08/20/13 03:56:33 PM
FSM_test.vhd	✓	VHDL	2	08/20/13 04:08:26 PM
moore.vhd	✓	VHDL	3	09/02/11 04:28:08 PM

A green check shows for each file if the compilation was successful



Simulation

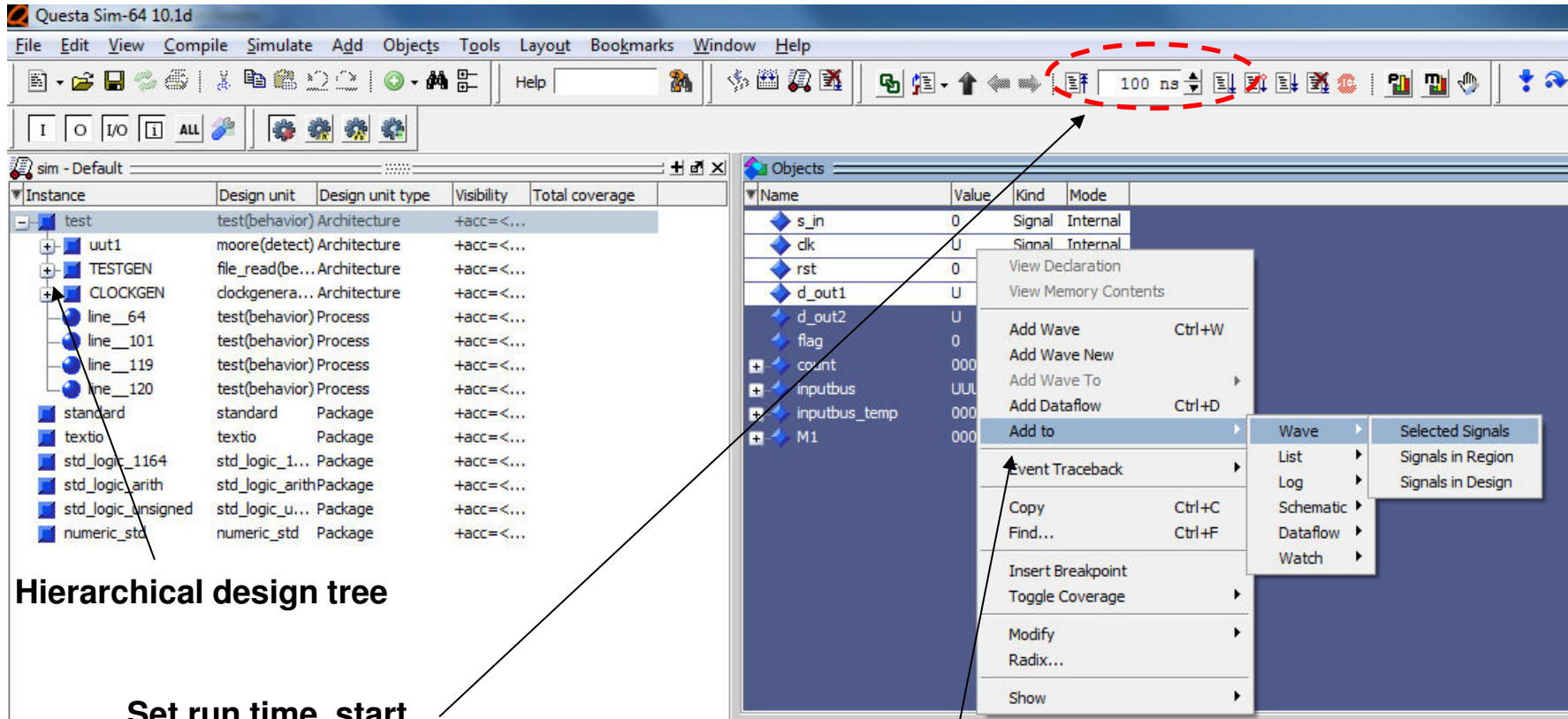
Right-click on your design (testbench) and select simulate



Signals on top level



Adding signals to waveform



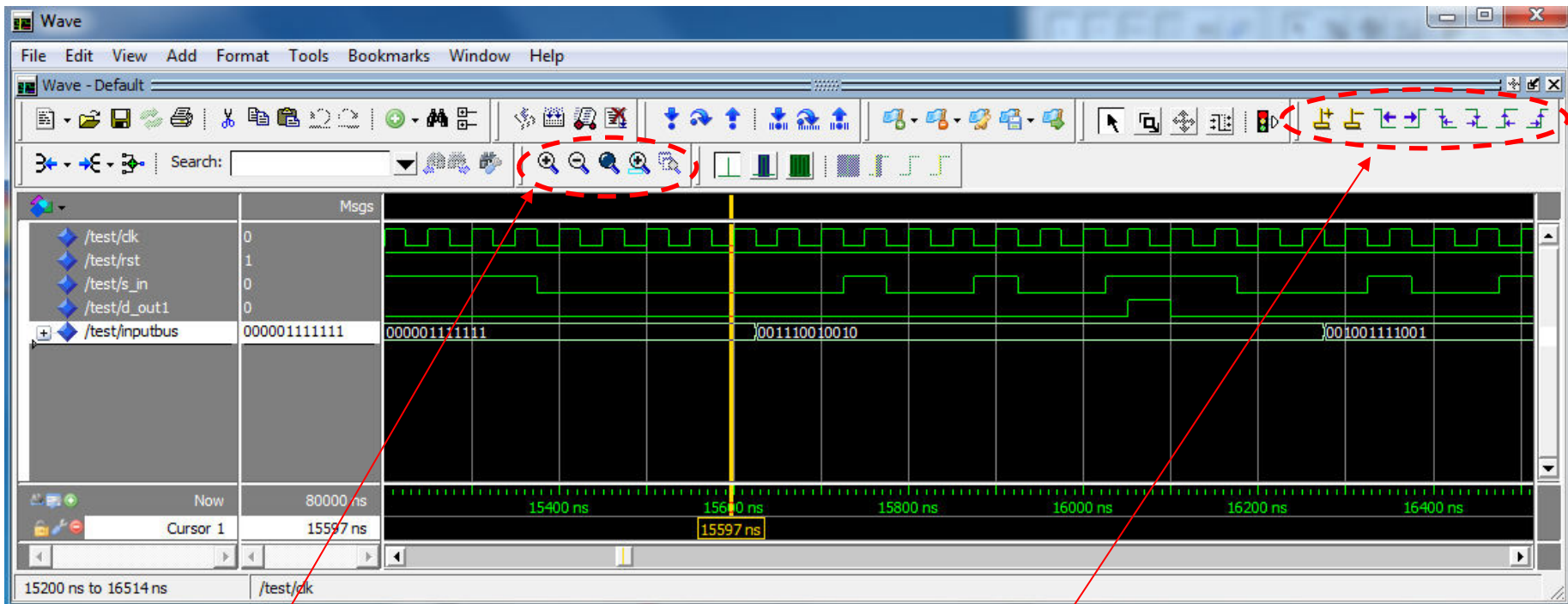
Hierarchical design tree

Set run time, start simulation run or restart simulation after re-compilation

Mark signals to be shown in waveform and click Add to → Wave → Selected Signals



Waveform viewer

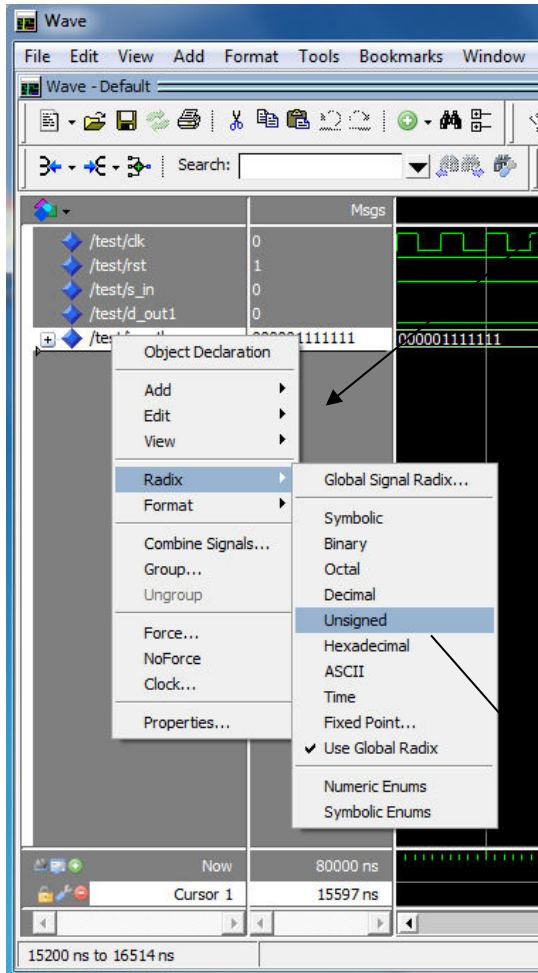


Different options for zooming

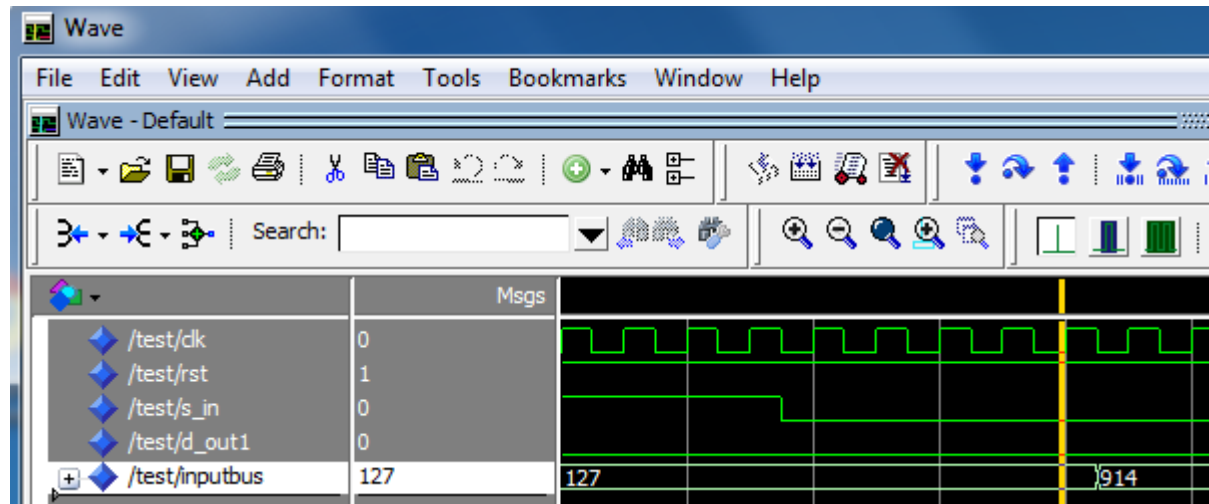
Different options to jump with the cursor to falling or rising edges



Waveform viewer (cont.)



To change representation style of a bus, right-click on the signal, then Radix

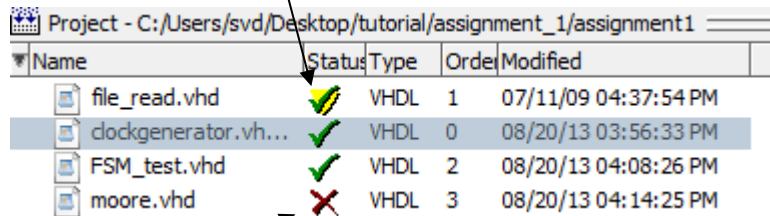


The signal is now shown in an unsigned representation instead of binary



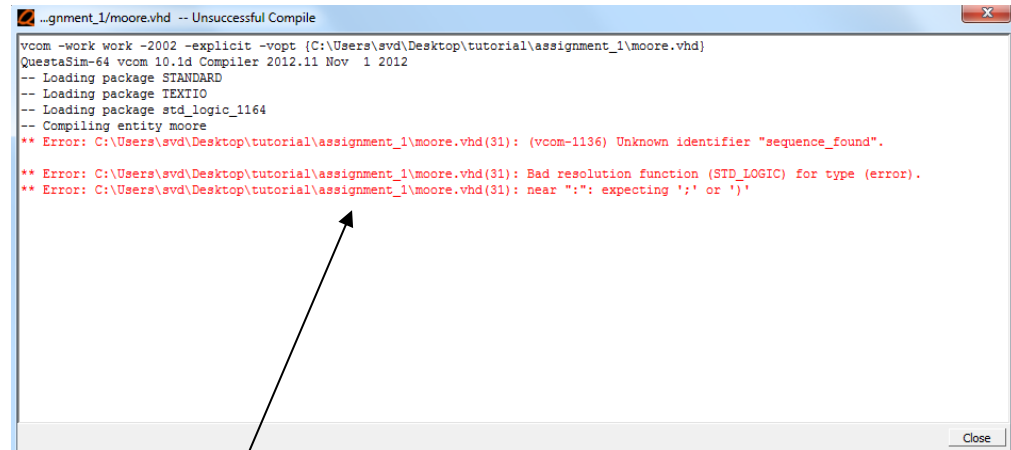
Errors/warnings in the designs

Warning for the design/file



Project - C:/Users/svd/Desktop/tutorial/assignment_1/assignment1

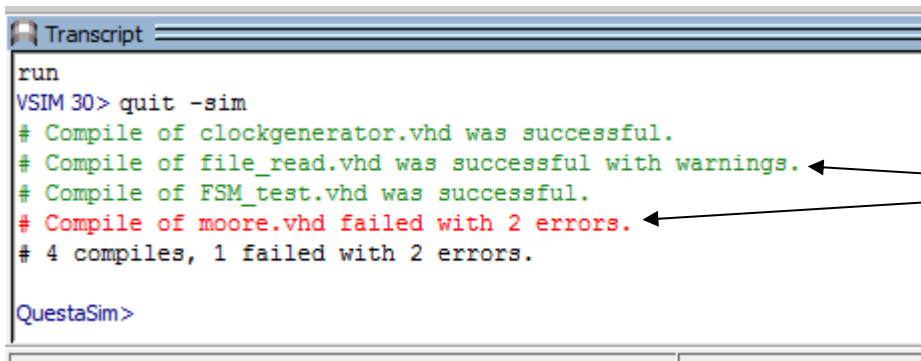
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FSM_test.vhd	✓	VHDL	2	08/20/13 04:08:26 PM
moore.vhd	✗	VHDL	3	08/20/13 04:14:25 PM



```
--gnment_1/moore.vhd -- Unsuccessful Compile
vcom -work work -2002 -explicit -vopt {C:\Users\svd\Desktop\tutorial\assignment_1\moore.vhd}
QuestaSim-64 vcom 10.1d Compiler 2012.11 Nov 1 2012
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity moore
** Error: C:\Users\svd\Desktop\tutorial\assignment_1\moore.vhd(31): (vcom-1136) Unknown identifier "sequence_found".
** Error: C:\Users\svd\Desktop\tutorial\assignment_1\moore.vhd(31): Bad resolution function (STD_LOGIC) for type (error).
** Error: C:\Users\svd\Desktop\tutorial\assignment_1\moore.vhd(31): near "(": expecting ';' or ')'
```

Error in the design/file

A window stating the errors/warnings pops-up



```
Transcript
run
VSIM 30> quit -sim
# Compile of clockgenerator.vhd was successful.
# Compile of file_read.vhd was successful with warnings.
# Compile of FSM_test.vhd was successful.
# Compile of moore.vhd failed with 2 errors.
# 4 compiles, 1 failed with 2 errors.
QuestaSim>
```

Double-click on the message in the transcript window to get the error/warning messages

