Evaluation of Analog Frequency Modulation Performance

Franzén, Björn
2018-03-16
Lund University
Department of Electrical and Information Technology
EITF40, Digital and Analog Projects
Course Coordinator: Lindvall, Bertil

***Abstract*- This project report details the design of an analog frequency modulator and demodulator. The intent was to derive the performance of such a circuit in order to determine the suitability for use in electrical isolation over optical fiber between two systems at different voltage potentials. Several drawbacks in the design was found and while it performs its intended function, it does so with sub-optimal performance. Possibly solutions are presented to be applied to a new iteration of the circuit.**

I. INTRODUCTION

This report is sectioned into five parts. First, an introduction is presented, providing background for the project. Second, schematics with an accompanying discussion, and basis for choice of components, are found. Following that, the reasoning behind the PCB layout is given and the finished board presented. Lastly, measurements are presented and discussed.

A. BACKGROUND AND MOTIVATION

To measure current, a sensing element must be introduced along the wire carrying the current. This sensing element may be placed in series with the wire, i.e. shunt resistor, or around the wire, to measure its magnetic field, i.e. hall sensor or transformer. Regardless of topology, there will be an impedance between the measurement point and the measurement system due to their common impedance e.g. through protective earth or chassis connection in a vehicle.

In high voltage systems, where the measurement node must be electrically isolated from the measurement system, the impedance represents the impedance over the isolation barrier. The impedance is capacitive and thus decreases with frequency. As the impedance decreases, the common mode voltage, in respect to local ground on the isolated part, increases. If the read-out circuitry has insufficient common mode rejection, this voltage will incorrectly be measured. If, however, the impedance is infinite, regardless of frequency, there will be no common mode voltage and therefore no related measurement errors.

In switched motor drives, the common mode voltage is a pulse width modulated signal with typical voltage derivates of 1000V/us i.e. both high voltage and high frequency. If high frequency current needs to be measured in the same frequency range as the common mode voltage, the measurement will be erroneous because amplifiers only has high common mode rejection at lower frequencies.

A. PURPOSE

Given that the isolation impedance is capacitive, and thus a function of distance, the only way to increase the impedance is to increase the separation between the measurement system and its measurement point. For very high isolation, this means either transmission by radio-waves over a non-conducting medium or optical transmission through fiber.

In both transmission mediums, frequency modulation will offer superior noise performance compared to amplitude modulation at the trade-off of lower bandwidth. This project aims to determine what resolution and signal bandwidth may be expected of such modulation.

II. SCHEMATIC

The design consists of two independent parts, a frequency modulator and a frequency demodulator. Input to the modulator is a baseband analog signal, and output is a frequency modulated (FM) version. The output is connected to the input of a frequency demodulator which converts the FM signal back to its original form. The project's main intent is to determine the signal degradation due to this modulating and demodulating process.

B. THE FREQUENCY MODULATOR

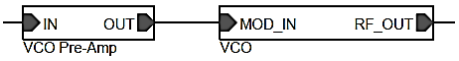

Figure 1 – Block view of the frequency modulator. Input is from the left and output to the right.

The modulator consists of a voltage-controlled oscillator (VCO) with a pre-amplifier attached to the tune input. Input to the amplifier is a baseband signal with bandwidth up to 50 MHz. The main function of the amplifier is to act as an interface between VCO and signal input i.e. to level shift the signal and amplify it appropriately. The result is a 3 GHz FM modulated signal at the output of the VCO.

The key component in modulator performance is the VCO. Choice of VCO have been based on four figures of merit, modulation bandwidth, voltage tuning range, center frequency and phase noise. The bandwidth is not typically listed in datasheets but may be obtained through simulations. Because of the limited time allotted to the project, a product line from analog devices was chosen where the bandwidth had already been determined [1].

The chosen product line has very similar phase noise for all VCOs. Phase noise is measured as the difference in power between carrier and noise, for a fixed frequency from the carrier [2]. Thus, given similar phase noise, higher carrier frequency means better performance. The highest carrier frequency deemed possible was 3GHz, based on the author's limited experience with practical implementation of RF systems.

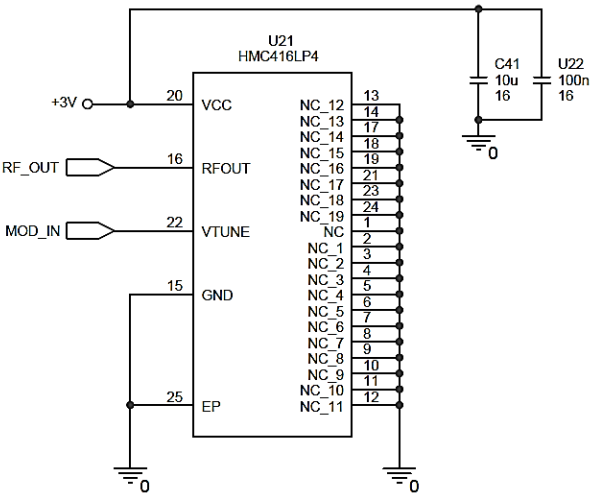

Figure 2 – The Analog Devices HMC416 voltage-controlled oscillator.

Carrier tuning range was considered from the following perspective. The larger frequency deviation for a given input level, the less susceptible the system will be to noise. However, this comes at the cost of linearity. In normal operation as a part of radio transmitter, the VCO operates with input voltage levels around $40mV_{\mathrm{p-p}}$. Here, the signal amplitudes are up to $3V_{p-p}$. Since the voltage to frequency dependency can only be considered linear for very small tuning ranges, the operation will be heavily non-linear. The argument is made that if demodulated by a VCO with the exact same characteristics, the full system will be linear.

As VCO, HMC416 from Analog Devices was chosen. It has a center frequency of 3GHz at 6V bias level in addition to 64.5MHz bandwidth [1]. It also allows easy interfacing as the internal resistance is equal to 50Ω, allowing direct matching to a 50Ω trace. Figure 2 shows the VCO schematic. To comply with the required bias level set for the VCO, 6V, the pre-amplifier must shift the AC input signal by as much. It must further be able to output $3V_{\mathrm{p-p}}$ at a frequency of 50MHz. This puts a limit on the slew rate according to [3],

$$\text{slewrate} > \max\{f\}\,\pi \mathrm{V}_{\mathrm{p-p}} = 471\frac{V}{\mu s} \tag{1}$$

Assuming the same pre-amplifier is used for both the modulator and de-modulator, it is preferable to have as low temperature drift coefficient as possible as they will not be thermally coupled. It should be noted that the rest of the components in the signal path will need to have comparable temperature drift or little is gained.

Gain is also an important figure of merit. Skipping ahead briefly to the demodulator, the required gain is determined by the mixer which is part of the demodulator circuit. By considering the signal chain through the mixer, the available gain can be determined by,

$$\begin{aligned} \mathrm{G} > {} & |mixer\ conversion\ loss| - |mixer\ IP1_{dB}| \\ & + 10\log_{10}\left(\frac{\left[\frac{VCO_{tune}^2}{50\Omega}\right]}{1mW}\right) \\ & = 8dB - 10dBm + 16.5dBm \\ & = 14.5dB \end{aligned} \tag{2}$$

The Analog Devices ADA4895 meets these specifications. It has a slew-rate of 943V/µs, voltage gain greater than 10 and a very low, relative to its frequency range, input temperature drift of 0.15µV/°C. Figure 3 shows the VCO pre-amplifier. The ADR440 is a simple voltage reference to level shift the signal to 6V. Only temperature drift has been accounted for in its choice.

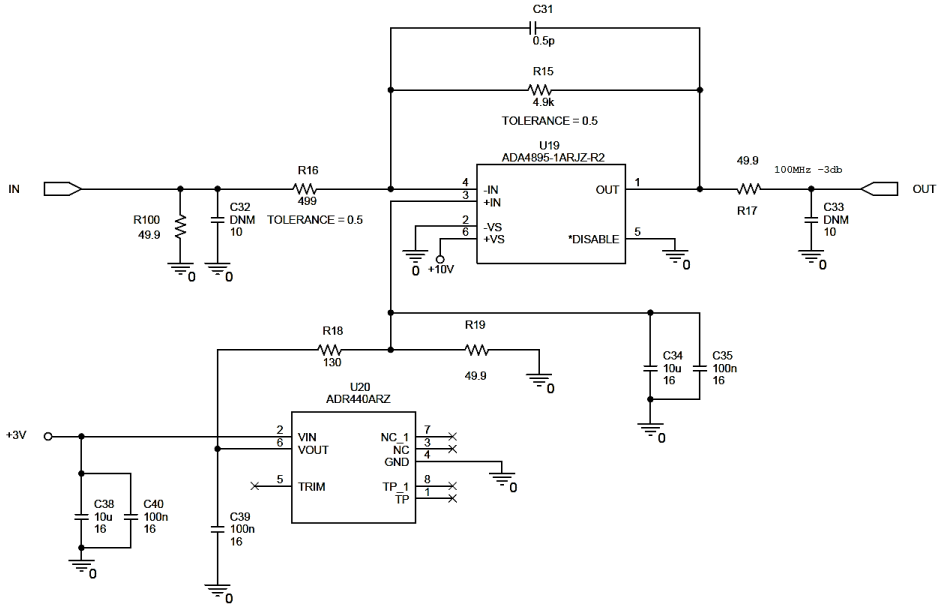

Figure 3 – VCO Pre-Amplifier schematic. Amplifier Analog Devices, ADA4895 with voltage reference Analog Devices ADR440.

C. THE FREQUENCY DEMODULATOR

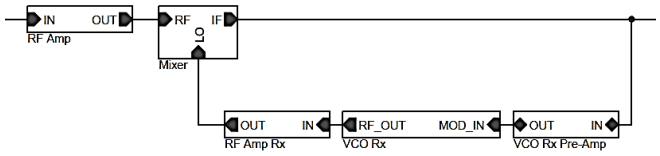

Figure 4 – Block view of the frequency demodulator. The input is to the left and output to the right.

The FM demodulator is a phase locked loop implemented with a balanced passive mixer connected in closed loop with the same VCO and pre-amplifier as used in the modulator. A block view of the demodulator can be seen in Figure 4. The RF amplifiers provides high enough signal to saturate the input of the mixer. By doing so, the IF output of the mixer is a signal with an amplitude independent of input power, but proportional to the difference in phase between RF and LO.

Since the VCO is in closed loop with the mixer, it tracks the input signal. In order to do so, the input to the VCO must be the same signal as used in the modulator. Thus, the original signal is recovered by tapping the input to the VCO or, more precisely, the input to the pre-amplifier.

In selection of mixer, there are several nuances to account for. Most important is to understand that mixer specifications are listed under assumption that it is used as a multiplier, not as a phase detector. The difference is that for phase detector operation, the RF input is saturated to produce an IF output signal independent of input power. This means that parameters specified by the datasheet must be used conservatively. For example, a good rule of thumb is allowing for a maximum operating frequency 30% below rating [4].

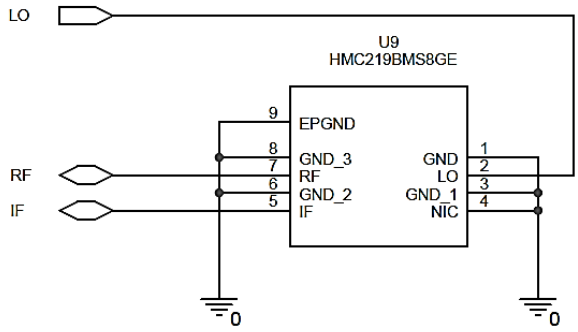

Figure 5 – The Analog Devices HMC219 Double Balanced Mixer.

Another nuance is how outputs and inputs are coupled. At cost of performance, it eases implementation if inputs and outputs are unbalanced. If the inputs (LO, RF) are balanced, they need to be driven either through a balun or through a differential amplifier. If not, a single ended output is sufficient. The IF can be either or as normal operational amplifiers have differential inputs. It is only important that the port may be DC coupled which is commonly not true.

It should also be considered if the mixer should have internal limiting amplifiers attached to the LO port. This would generally be preferred as it decreases emission, increases performance and eases implementation.

Figures of merit to base the decision of mixer can be simplified to the IP3 product. It is a measure of the amplitude of unintentional products stemming from the multiplication of sums of signals with different frequencies. As analog signals are composite signals containing many closely spaces frequencies, the IP3 product is closely related to the noise floor of the system. It should be chosen to be as high as possible.

HMC219 from Analog Devices was deemed suitable. It is a passive balanced mixer with 18dBm IP3 product and all unbalanced input and outputs.

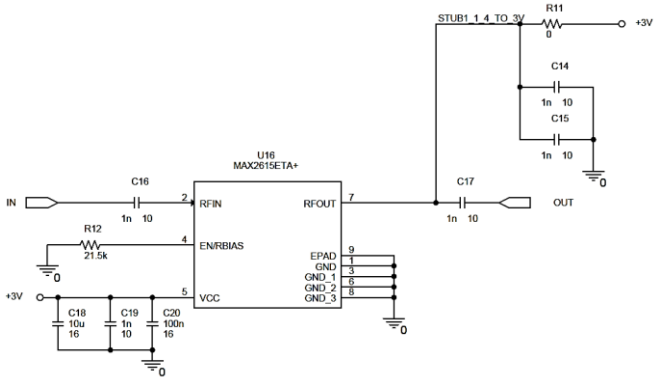

Figure 6 – The Maxim Integrated MAX2616 RF Amplifier

Since a passive mixer without internal limiting amplifiers was chosen, both the RF and LO port needs limiting amplifiers to saturate the inputs. This is done in order to turn on and off the diodes in the double balanced mixer quickly. In contrast to normal mixer operations, where only the LO port is saturated, phase detector operation requires both LO and RF to be saturated. If not, the output will not only be dependent on the difference in phase between LO and RF, but also proportional to their amplitude.

Thus, the mixer inputs are fed by fully saturated RF amplifiers. The output power of these amplifiers are thus equal their output referred compression point, OP1. An amplifier should be chosen were the output compression point OP1 is larger than the input compression point IP1 of the mixer. For the HMC219 mixer, the IP1 product is 10dBm so the amplifiers should be a few dBm greater. MAX2616 from Maxim Integrated has an OP1 of 16.5dBm and is thus suitable.

The MAX2616 amplifier requires bias voltage to be applied to the RF output. The datasheet recommends that a suitable inductor is used to provide 50mA current from the 3V rail. As there are few inductors in the 3GHz range, it is instead implemented by a quarter-wave stub terminated in 3V rail. At the point of contact to rail, the line is heavily decoupled such that RF sees a short-circuit at appropriate distance.

D. THE POWER SUPPLY

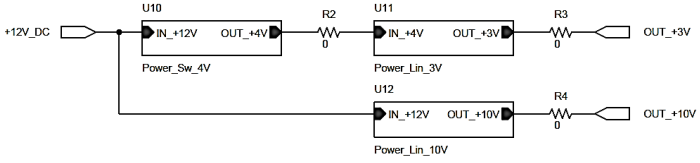

Figure 7 – Block view of the power supply.

There are two required voltages, 3V and 10V. The power requirements are 300mA and 50mA respectively. Since the 3V rail has to supply such high power, it would need a heat

sink if supplied with the same input voltage as the 10V. To get around this, a switched regulator is put in front to get the input voltage down to a manageable 4V. Both the linear regulators are of LDO type. The switched regulator and the 10V linear regulator are both fed by an external 12V DC supply.

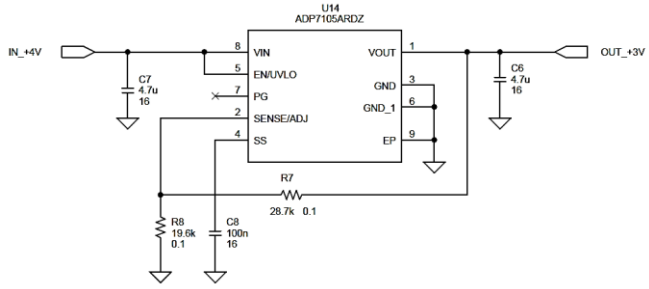

Figure 8 – The linear regulator ADP7105 from Analog Devices.

Figure 8 shows the linear regulators. Both the 3V and 10V rail use the same type of regulator, the ADP7105 from Analog Devices. No real considerations were made in their choice as linear regulators are inherently low noise and offers high power supply rejection if the input voltage is sufficiently high. The output capacitor recommended by the datasheet was used to make sure sufficiently high ESR is presented to the regulating loop to not make the regulator unstable.

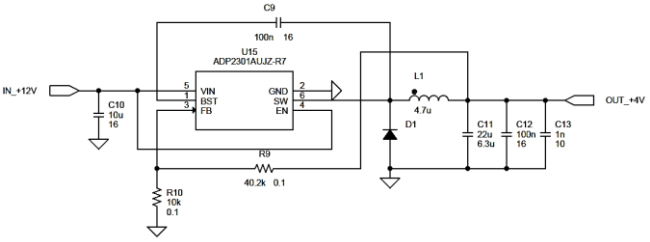

Figure 9 – The switched power supply using ADP2301 from Analog Devices.

The switched regulator is shown in Figure 9. The output filter, consisting of diode, inductor and a large cap must be chosen carefully for switched regulators. Thankfully, the datasheet offers suggestions to suitable components and thus, these have been used without further consideration.

E. CHOICE OF DECOUPLING CAPACITORS

Decoupling supply rails serve two main functions, mitigating emitted noise onto power rails and mitigating the effect of noise already present on the power rails. If emission is mitigated at each IC, then the decoupling of each IC can be considered independently. If not done, every IC would need to have decoupling against every frequency present on the board.

It is important to understand that the distance between power pin and decoupling capacitor adds a certain amount of inductance which will resonate in conjunction with the decoupling capacitor. The decoupling response thus contains several resonances stemming from, for example, capacitor and power pin trace or inductance between two decoupling capacitors and their composite capacitance.

This leads to the following conclusion. Resonances cannot be avoided but can be mitigated by having at least one very lossy (high ESR implies low parallel resistance) capacitor, to bring down the Q value of the resonance. It should typically be a high value tantalum capacitor which also takes care of low frequencies. Furthermore, to be useful at high frequencies, the capacitor value must be small as their resonance frequency is $1/\sqrt{LC}$ and L cannot be decreased further than the size of the package allows for. Even so, it is likely that the decoupling scheme will operate in the inductive region when approaching GHz ranges.

Another aspect to note is that because the inductance is tied to the length of the trace between power-pin and capacitor, and the trace is many times the length of the capacitor pin, there is little benefit in choosing very small packages. As wide traces as possible should also be used to lower the inductance.

By these arguments, the decoupling strategy used for the low frequency VCO pre-amplifier is 100nF//10uF, for the mixer, RF amplifier, and VCO, 1nF/100nF/10uF. The 10uF is ceramic, but a tantalum capacitor should ideally have been used.

III. LAYOUT

The board is double layered FR4 with a dielectric height of 1.5mm. One side of the board was dedicated to ground and components and traces were placed on the opposite side. When signals had to be routed on the ground layer, care was taken to make sure all signal traces had unbroken ground beneath them.

There are only signal lines with 50Ω characteristic impedance on the board. These have been implemented as coplanar waveguides, which are similar to microstrip but are in addition shielded on the same side as the trace. This leads to the fields propagating to greater extent in air than in the board material because of the short distance between trace and top ground plane. This leads to lower permittivity for coplanar than microstrip waveguides. As an effect, RF stubs will have longer length but it is not problematic for the design in question as it does not have any no hard space limitations.

The real benefit comes from the lower losses as more of the fields are propagating through air, which ideally has no loss. In contrast, FR4 material has very high loss and is generally not suited for the frequencies involved on the board. Using coplanar waveguides is a way to work around that.

The waveguide dimensions were calculated with the use of a web-based calculator [5]. Using a board relative permittivity of 4.5 (3 GHz), substrate height of 1.5mm and line to shape spacing 0.1mm, a trace width of 0.8mm was determined. The same spacing was adopted across the board.

Via arrays were placed at the edges of the board, between ground planes and power planes, and along coplanar waveguides. The via spacing was chosen between 6mm and 4mm and equates to less than 1/16 times the smallest wavelength on the board, 3 GHz. It should be sufficient to limit edge radiation from the substrate while at the same time equalizing ground potentials.

Care was taken to provide a large ground-plane around the switched regulator with plenty of vias connecting top ground to bottom ground. The reason was to make sure that stray fields were properly terminated to not affect the analog circuitry. The general layout of the regulator was adopted from the datasheet. Figure 10 shows the component side of the layout in Cadence OrCAD PCB Designer.

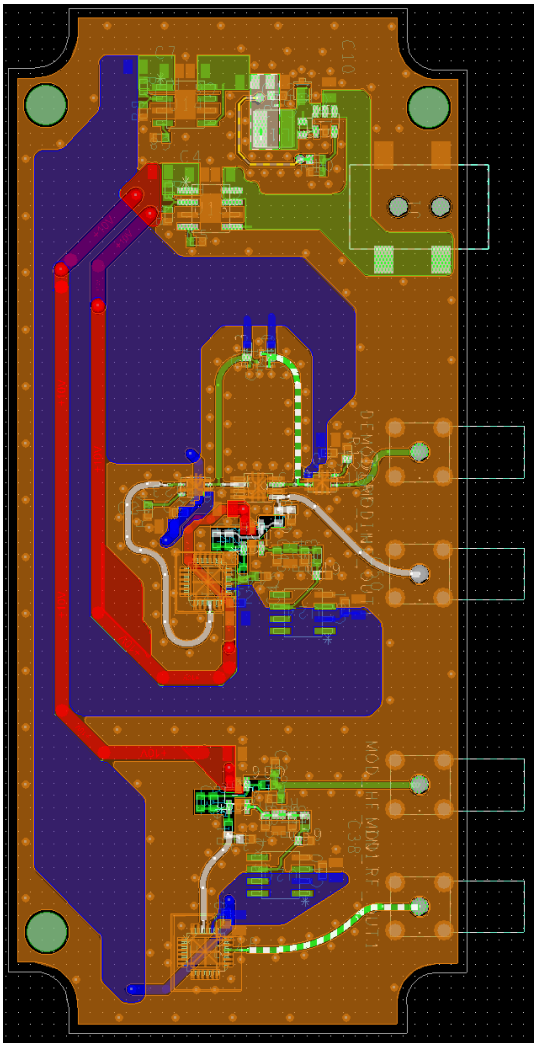

Figure 10 – PCB component side. Brown areas are ground, Red 10V, Blue 3V.

IV. MANUFACTURING

The board was manufactured at Lund University in their CNC milling machine and vias were plated with an electrochemical process. The finished board was coated with a thin layer of tin (SENO321 Glanzzinn).

A few issues were encountered with the PCB layout. To begin with, the VCO had the incorrect footprint attached, even though the model was supplied from the manufacturer, Analog Devices. The symbol had a QFP package attached while only being shipped with QFN packages. Thankfully, these are not so dissimilar. They both have the same size but QFN has no leads attached to it and is entirely connected on the bottom side. A fix was made where the ground plane was cut away under the device such that the pads would not be shorted. The original traces could then be used as the pads were slightly exposed at the edges of the package.

Another model related issue was using the incorrect footprint for all 0603 packages. The intended package was 0603 metric, but footprints for 0603 in imperial units was instead used in the layout. This lead to some passive elements being to small to fit the pads and off the shelf components had to be used in those instances. Those were less ideal than the intended, carefully specified, parts. For example, a few precision resistors were exchanged with standard 1% resistors. This did not pose serious problems as most components were chosen for their temperature coefficient and not their precision rating.

One matter that complicated the soldering process was the very tight spacing chosen, 0.1mm. This would not have been a problem if soldermask has been applied but without, it was very easy to get unintended short circuits. Not necessarily due to packages being skewed and unintentionally soldered to ground, but mostly because excess solder tends to short-circuit lines but with a connection small enough only to be seen in a microscope.

The finished prototype board can be seen in Figure 11 and Figure 12.

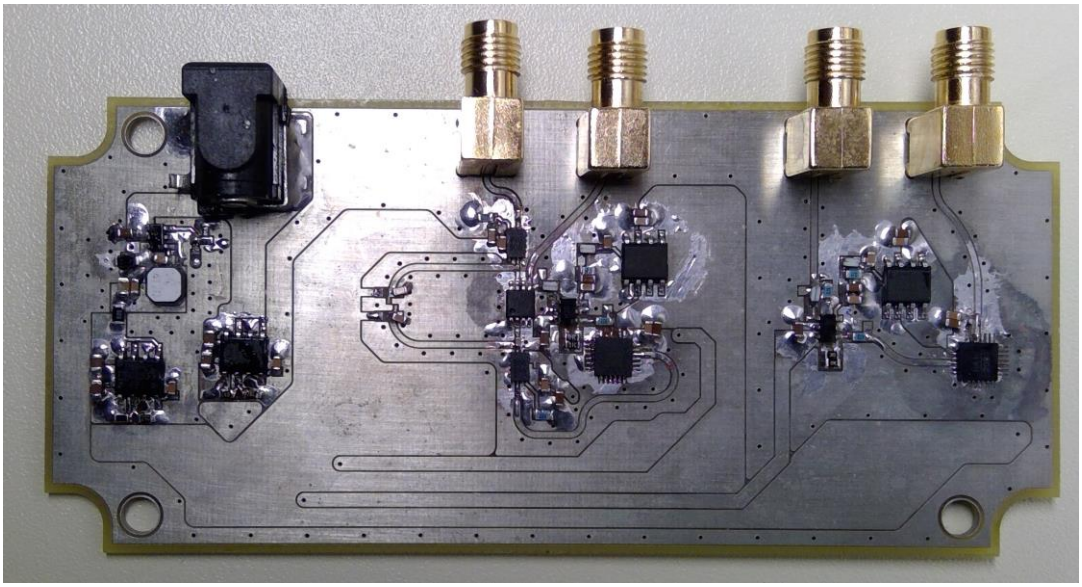

Figure 11 – PCB component side. From right to left, modulator, demodulator and power supply.

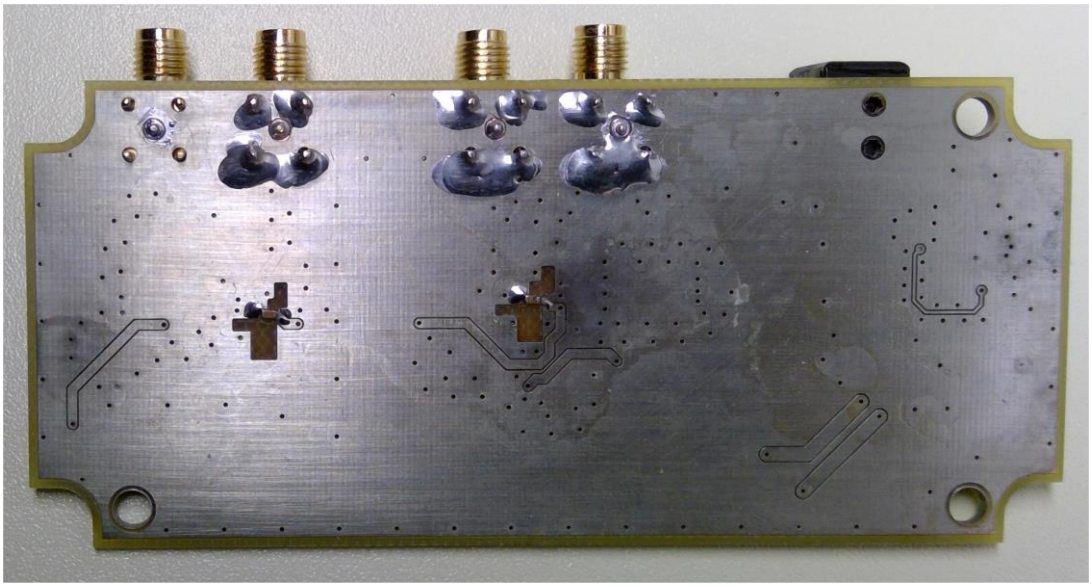

Figure 12 – PCB ground side.

V. RESULTS AND DISCUSSION

A few issues were found in the design which impacted the PLL loop stability. The most critical was the polarity of the phase detector gain. By connecting the signal input to the RF port of the mixer, and the loop input to LO port of the mixer, the output is decreasing for increasing differences in phase. Since the VCO amplifier in the PLL loop has negative gain, the entire loop is unstable. This issue could not have been foreseen as it depends on the internal coupling of the IF port, as the mixer has internal balanced to single-ended conversion. To force the loop stable, the RF and LO ports was swapped. This is possible because when used as a phase detector, the two ports are interchangeable as both have saturated inputs.

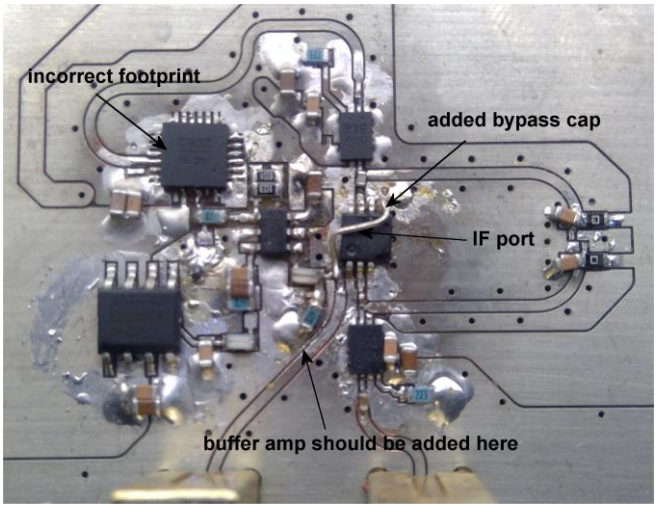

Figure 13 – Corrections made to the PLL loop.

The problem with the fix was that it required the mixer to be flipped 180 degrees, and the IF port run by a small wire across its top surface. This in turn meant that the passive input filter, consisting of the line characteristic impedance and C32 in Figure 3, did not provide low enough impedance at 3 GHz because the filter got placed too far from the mixer output. Thus, the frequency components at 3 GHz, from the mixing process, were not attenuated properly and caused an additional instability in the loop. This was remedied by soldering a 33 pF capacitor between the IF output and an adjacent ground pin. Figure 13 shows the correction.

Having solved the loop instability issues, a 10 MHz sinusoidal was input to the modulator and the output of the demodulator was observed on an oscilloscope. Figure 14 and Figure 15 shows the output for two different input power levels, -20 dBm and -40 dBm. It is easy to assume that Figure 14, with -20 dBm input, shows a well-conditioned signal. However, this is contradicted by the spectrum shown in Figure 15. The signal has substantial harmonics. The difference between first harmonic and fundamental is 27dB (fundamental is at -20dBm even though it is outside the range of the plot).

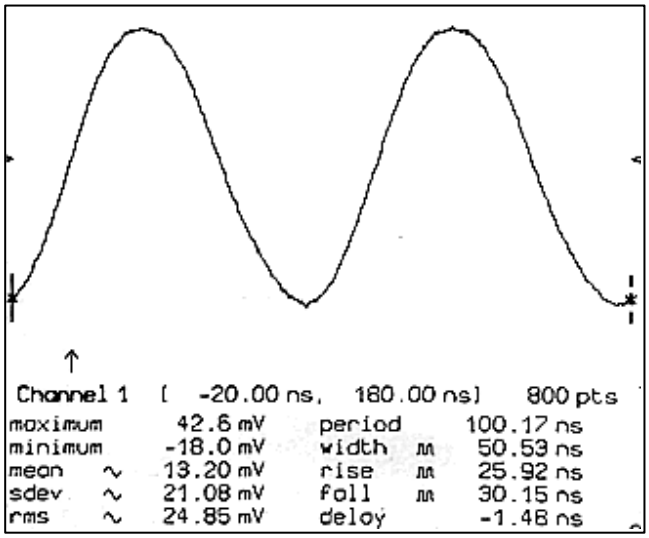

Figure 14 – Output from demodulator. Signal input to modulator is 10 MHz, -20dBm.

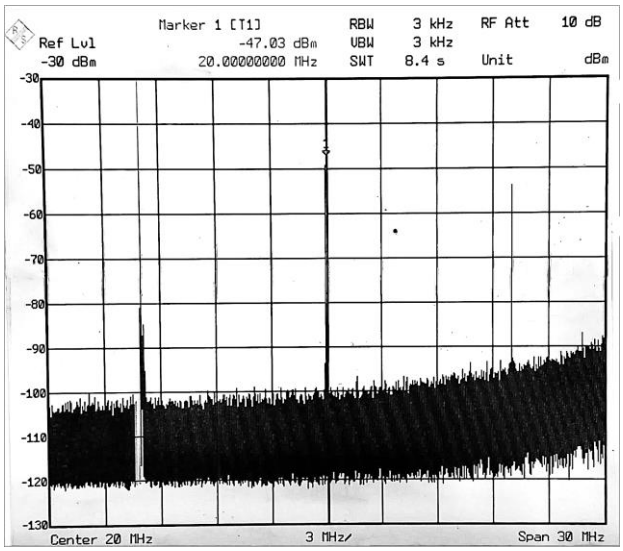

Figure 15 - Output from demodulator. Signal input to modulator is 10 MHz, -20dBm.

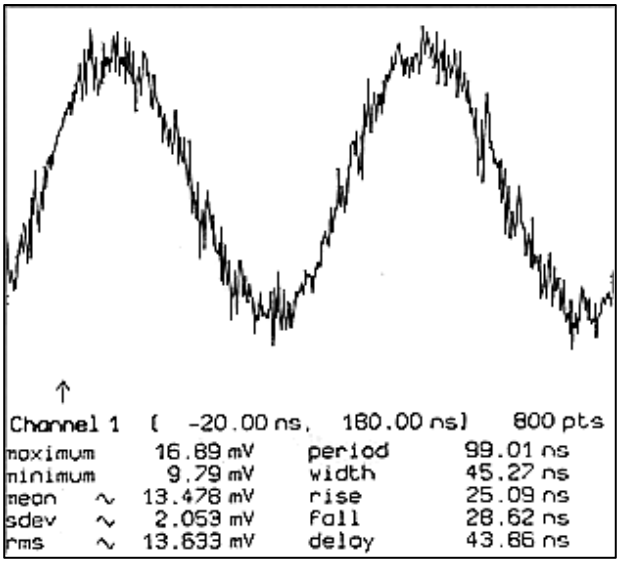

Figure 16 - Output from demodulator. Signal input to modulator is 10 MHz, -40dBm.

Figure 16 shows the demodulator output as the input is lowered 20 dB compared to Figure 17. The signal is seen to have considerate noise yet Figure 17 also shows that it has less distortion. The difference between first harmonic and fundamental is 40dB compared to 27dB for the higher input level of -20 dBm.

Comparing the response to the two different input powers, two things can be noted. Too high input power leads to distortion and conversely, too low input power leads to noise becoming prevalent. Since the VCO in the modulator does not show the same noise for -40 dBm, and when the PLL is locked the VCO in the PLL loop has the same input power (or else it would not be locked), the noise pick-up must be in the PLL. It is likely therefore that the noise is picked up from the measurement unit, which is connected directly at the input to the VCO pre-amplifier without any buffer in between. Thus, a first attempt to noise reduction should include the insertion of such a buffer.

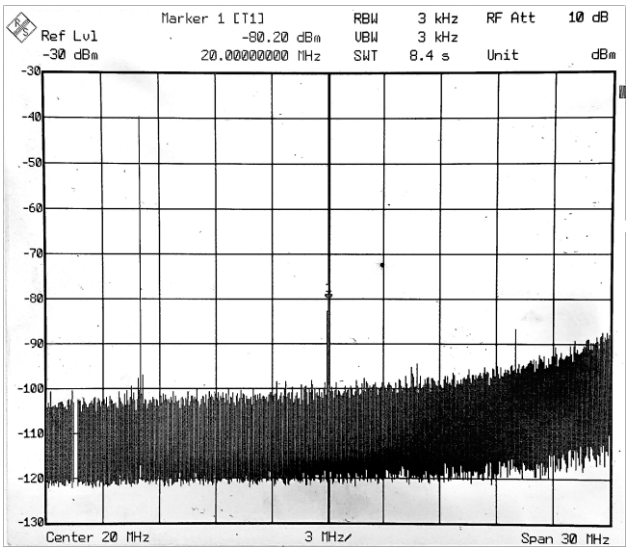

Figure 17 - Output from demodulator. Signal input to modulator is 10 MHz, -40dBm.

As for the increasing distortion at increasing input levels, it may be due to insufficient gain of the VCO pre-amplifier in the PLL loop. It does in fact have less gain than required by the limit given in (2), approximately 8dB less. This is due simulating the tuning input of the VCO incorrectly when the gain was determined. The model given in Figure 18 was used for SPICE simulations in ADIsimPE.

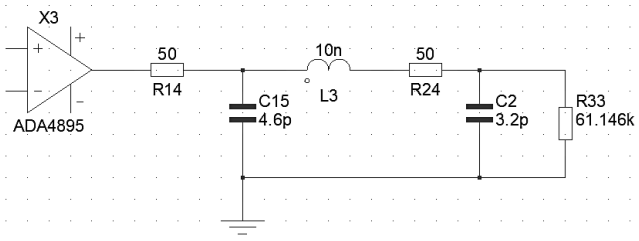

Figure 18 – Circuit used in simulation of the VCO pre-amplifier. Diode incorrectly modelled by a simple capacitance.

C15, L3 are package parasitics, R24 the diode junction resistance, C2 represents the junction capacitance. The values are given in the VCO datasheet. R33 was obtained by optimizing the model in Advanced Design System (ADS) according to [1]. The model is incorrect for SPICE simulations as it does not account for the diode correctly (C2 should be replaced by a diode), which will act as a short when the diode is biased. Thus, a more appropriate model would be to simply short the right side of R24 which leaves approximately a 50Ω input. The consequence of the model is that the load impedance is high and thus there is little voltage drop over R14 and as such, the needed gain is underestimated.

Because of the high load impedance of model used, the effect of the amplifier output impedance was incidentally not considered. At 100 MHz, the output impedance is almost 100 Ω and as such, a 50 Ω series resistance does not provide an accurate match to a 50 Ω line.

Having insufficient gain leaves the mixer (phase detector) inputs unsaturated and thus the IF output will be dependent on the input amplitudes. Arguably, the distortion should then decrease as the input level increase but that is only true if both the VCO in the modulator and the demodulator have the same

bias level and tuning voltage to output frequency relationship. Since the VCOs were re-soldered several times and are generally mounted poorly due to their incorrect footprints, this might not be the case. The increasing distortion could then be because of the PLL not being able to track the low frequency input at its maxima or minima, as either fall outside the maximum or output level the amplifier can achieve.

Regardless of cause, increasing the gain of the pre-amplifier by at least 10dB, such that the mixer inputs are saturated, in addition to using precision resistors at the pre-amplifier, such that the bias level and amplitude are equal at both VCOs, will likely minimize the distortion.

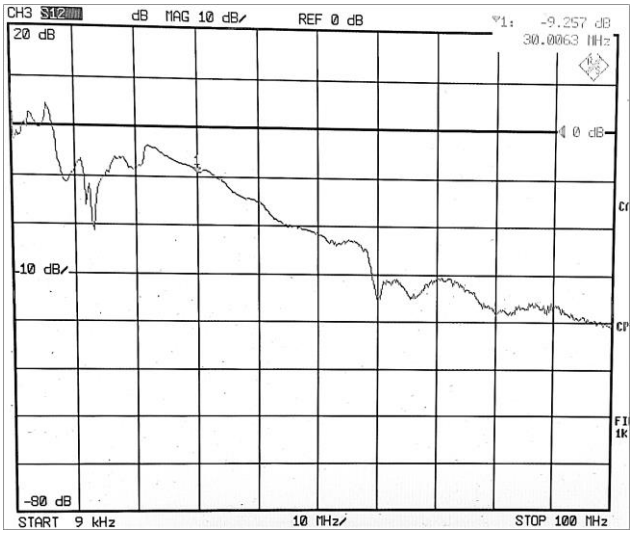

Figure 19 – S12 measurements corresponding to the transfer function from input to output. Input power levels are -25dBm (lowest possible on network analyzer). The non-linear response is most likely due to distortion from too high input level.

Figure 19 shows S12 measurements between modulator input and demodulator output. Because the output power of the network analyzer could not be set lower than -25 dBm, distortion was also measured in addition to the signal. Thus, the input level is too high for an accurate assessment of the frequency response. Even so, the cut-off frequency should be representative, as it is not a function of distortion. The cut-off is seen to be around 20 MHz. This is less than half of the expected, 64 MHz. The reason may be the bandwidth being dependent on the matching of the VCO tuning input [1], and this matching is poor as argued for in the section above.

VI. CONCLUSIONS

The circuit was shown to function correctly (as verified by Figure 14) but at sub-optimal performance. To increase the performance, the following recommendations can be summarized from the result section of the report.

- Increase the pre-amplifier gain by at least 10dB, preferably as much as the mixer can tolerate. Use precision resistors for both the bias level and the gain, such that both VCOs behave the same.
- Insert a buffer amplifier at the demodulator output to prevent noise from coupling into the PLL loop.
- Swap the RF and LO port of the mixer or else the PLL loop does not have negative feedback.
- Use a much sharper filter at the mixer IF output to remove 3 GHz components to avoid loop instability.
- User larger spacing between shapes in the layout to make soldering easier.
- Use correct footprints.

Applying these corrections to the design will probably be sufficient to achieve a representative level of performance to what may be expected of a frequency modulator-demodulator chain. Before the changes are made, there is little reason to make assumptions on performance. As such, the intent of the project, to evaluate performance of such a chain, has not been achieved. The work does however provide a solid base for a new iteration of the same circuit.

REFERENCES

[1] Analog Devices, "Determining the FM Bandwidth of a Wideband Varactor".

[2] Mini-Circuits, "VCO Phase Noise".

[3] Texas Instruments, "SNOA852 Predicting Op Amp Slew," National Semiconductor Corporation, 2002.

[4] Mini-Circuits, "AN-41-001 Frequency asked questions about phase detectors," Mini-Circuits, 2015.

[5] Microwaves101, "Coplanar Waveguide Calculator," [Online]. Available: https://www.microwaves101.com/calculators/864-coplanar-waveguide-calculator. [Accessed 15 02 2018].