EITF40, Digital and Analogue Projects

7-bit 25 ksps Positive Logic Semi-discrete Successive Approximation A/D Converter with built in clock oscillator and Voltage Mode R-2R D/A Converter

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Abstract

An analogue/digital project that set out to construct and implement an analogue to digital and digital to analogue converter "demo" board, using semi-discrete components (ie, no A/D or D/A IC:s) and the archaic wire-wrapping technique. The function of each circuit block is described and the finished circuit presented with complete schematics and pictures. Oscilloscope images of key test points are included and the performance discussed.

Contents

1 Introduction

This project set out to construct an A/D and D/A conversion "demo" board using discrete components. This was successfully accomplished with 74HC logic, linear IC:s, transistors, and thick film resistor networks. The converter can be used in single step mode or run from an internal or external clock and works well at clock speeds up to at least 200 kHz (equalling approximately 25 ksps). The internal clock can be divided up to 11 times, each division chosen by bridging the appropriate pins. Each bit can be switched off at will to evaluate its effect on the conversion. The sample and hold capacitor can be swapped out at one's convenience and the 7-bit word reviewed on the board's LED array which also features a dedicated *end of conversion* indicator. A picture of the circuit board can be found in appendix A.

2 Description

2.1 A brief introduction to A/D and D/A conversion and the implementation chosen

An analogue to digital converter takes an analogue signal at the input and presents a digital representation of that signal at the output. The digital to analogue converter does the same thing in reverse. The method of conversion may differ depending on external demands, eg speed of conversion, accuracy, cost.

In this project a successive approximation A/D converter (SAC) was implemented since it is a relatively simple conversion method. A sample and hold circuit is needed at the input of the A/D converter to keep the input signal constant during conversion and was added to the circuit. For D/A conversion a R-2R resistor ladder converter was chosen by virtue of its simplicity and outstanding performance.

2.2 Successive Approximation A/D conversion

Successive approximation works by testing one bit at a time, comparing the resulting voltage with the input signal, starting with the most significant bit (MSB), and working toward the least significant bit (LSB). The resulting word (7 bits) is then a digital representation of the input voltage. Every SAC contains some kind of control logic, a D/A converter, and a comparator (see figure 1). The SAC D/A converter is identical to the separate D/A converter described in section 2.3.

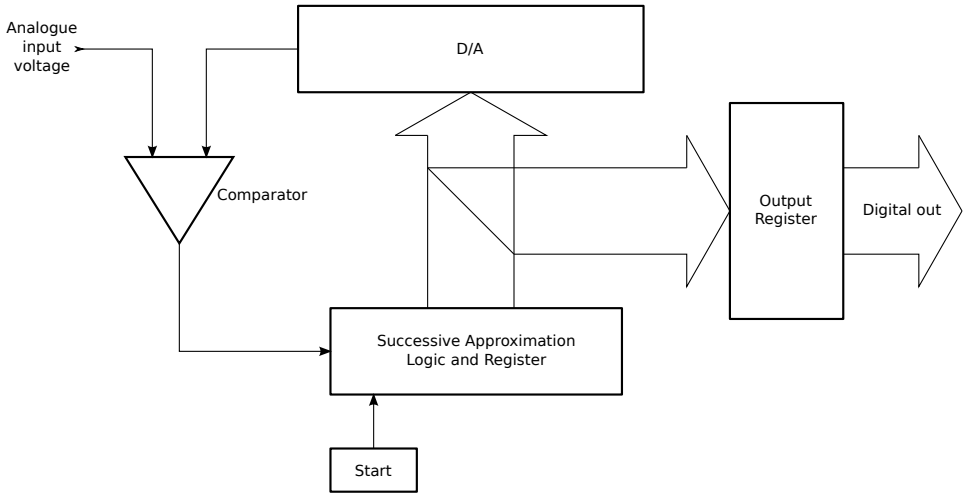


Figure 1: Block diagram of Successive Approximation Converter.

Our implementation works as follows. (Please refer to the schematic in figure 3 and the timing diagram in figure 2.) Upon pressing the start button a *clear* pulse is generated that resets the shift register. When releasing the button a *start* pulse is generated that sets flip-flop 1 (F/F 1) and resets all other flip-flops. This pulse also sets the first shift register output (QA) high. The output from flip-flop 1 activates the most significant bit analogue switch, setting the resistor network output to one half of the full scale voltage (V_{FS}). This voltage (V_{out}) is compared to the input voltage (V_{in}). In this example V_{in} is less than V_{out} resulting in a high output from the comparator. When the clock is high, the comparator output appears at the output of gate 1 (G1), resetting F/F 1, concluding the test of the most significant bit ("0"). Upon the next negative going clock flank, the shift register shifts to the right, setting QB high and simultaneously resetting QA. The comparison is then repeated for the next most significant bit (NMSB), and the result appears at the output of F/F 2 at the beginning of the next clock period. The digital output so far is thus "0100000". After having determined the last bit the complete 7-bit word is saved in the output register and *end of conversion* (EOC) is signalled, the conversion process starting over.

2.2.1 Sample and Hold

The sample and hold (S&H) circuit is needed to keep the input voltage constant during conversion. This is accomplished by charging a capacitor to the input voltage during the "sample" interval and then isolating the capacitor during the conversion to keep the charge constant.

In this implementation the S&H circuit consists of an input buffer, a MOS

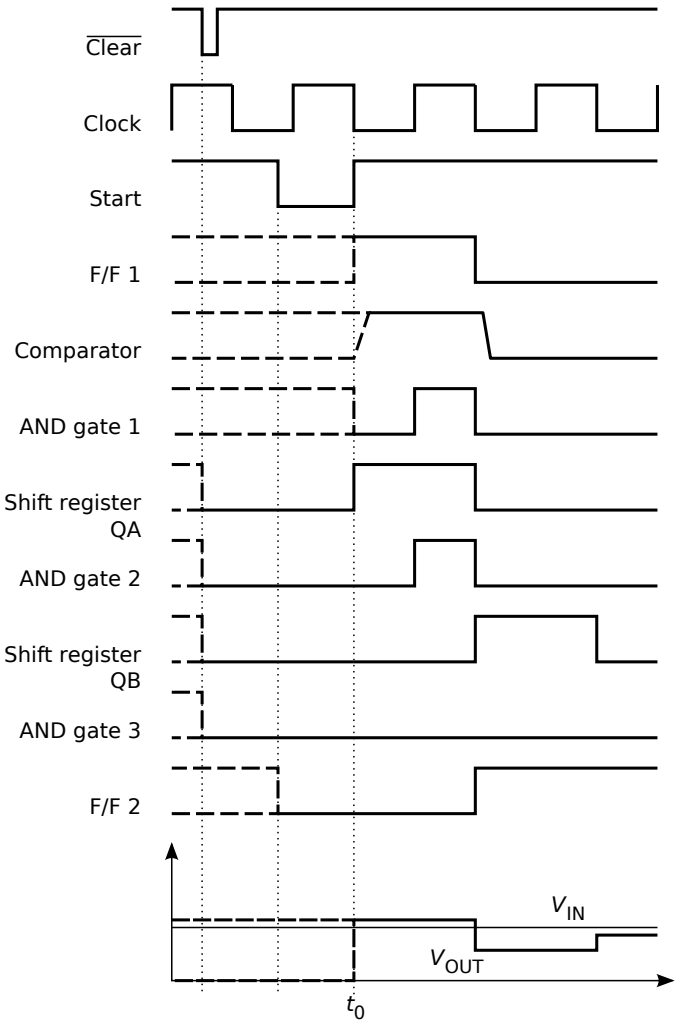


Figure 2: A/D converter timings.

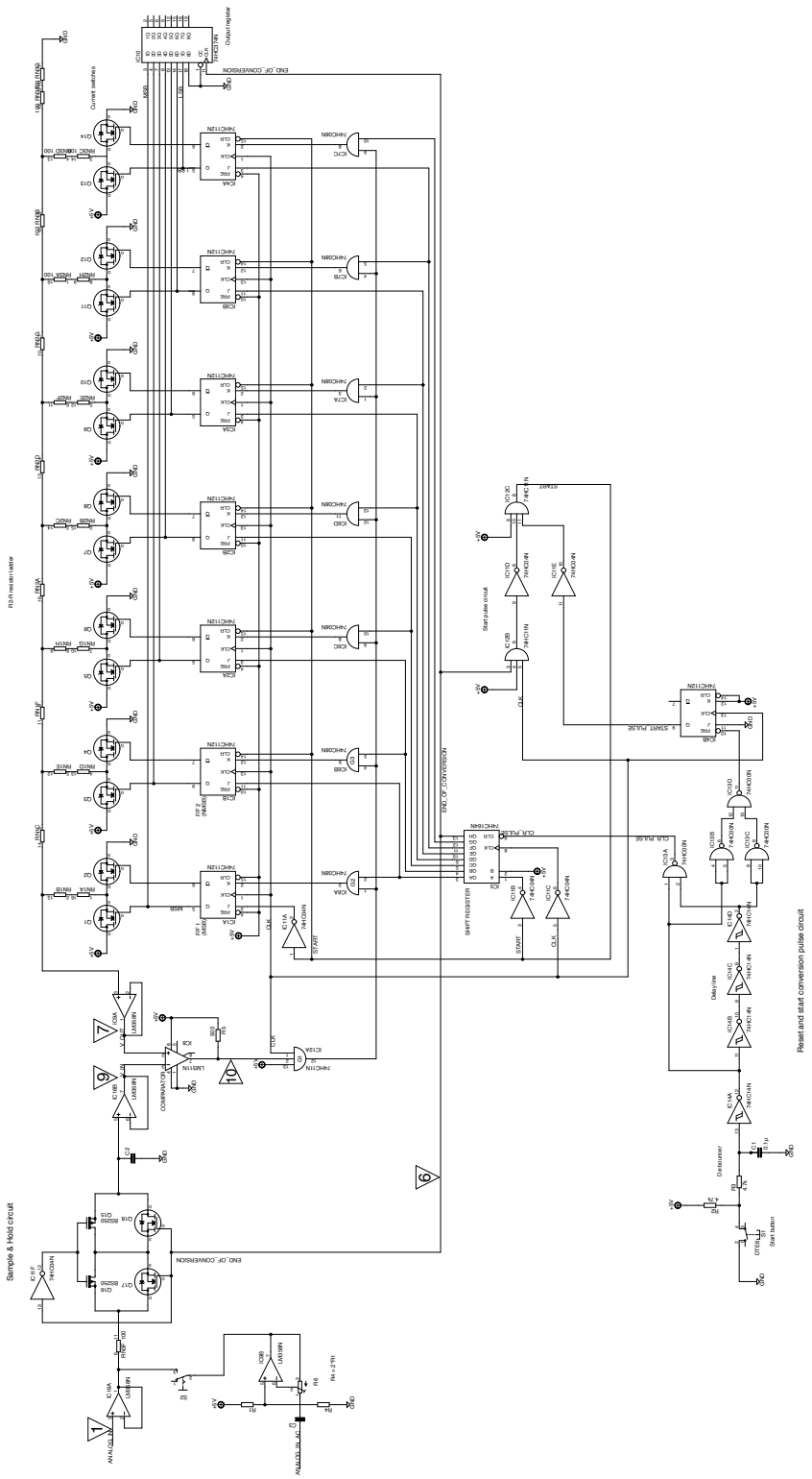


Figure 3: A/D converter schematic.

switch, a sample capacitor, and an output buffer (see schematic in figure 3). At the *end of conversion*-signal, the switch closes, connecting the capacitor to the input buffer. The capacitor is charged to the input voltage, and at the start of the new conversion cycle the switch is opened, the voltage held constant.

2.3 D/A conversion and the R-2R network

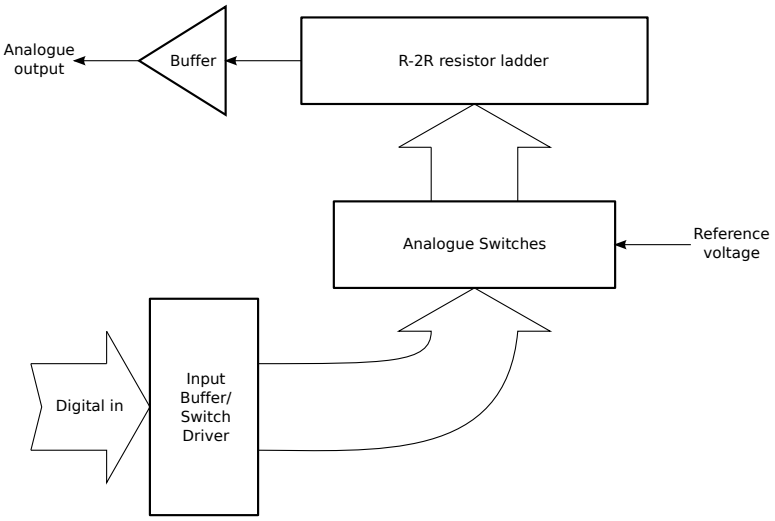


Figure 4: Block diagram of Successive Approximation Converter.

The D/A converter is essentially a switchable voltage divider, see figure 4. A digital word is converted to the corresponding analogue voltage, with respect to an external reference voltage.

In this implementation NMOS FET transistors are used as switches which are controlled by the input buffers, see figure 5. The 7-bit word at the input determines which switches are to be turned on (connected to V_{ref}) and which are to be off (connected to ground). The resulting voltage is the weighted sum of the individual node voltages at each "rung" of the ladder, the MSB contributing $V_{\text{ref}}/2$, the NMSB $V_{\text{ref}}/4$ and so on. The resistor ladder output voltage is buffered and the conversion is complete.

3 Results and discussion

Please see figures 6 and 7 for oscilloscope measurement pictures of key test points, also appearing in the schematics in figures 3 and 5.

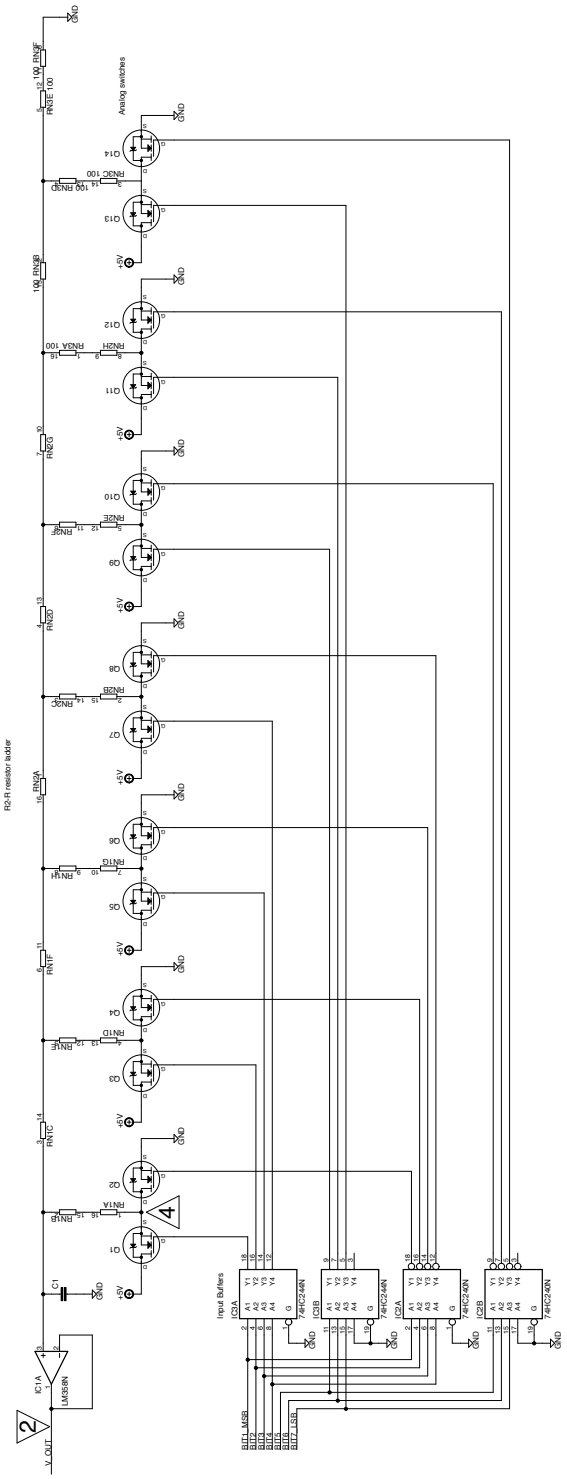
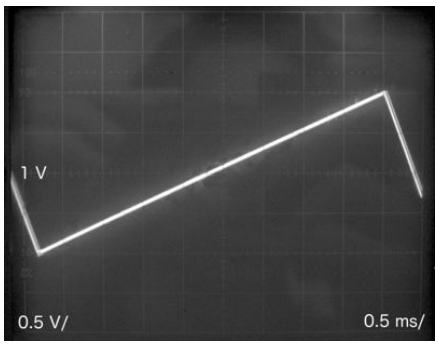
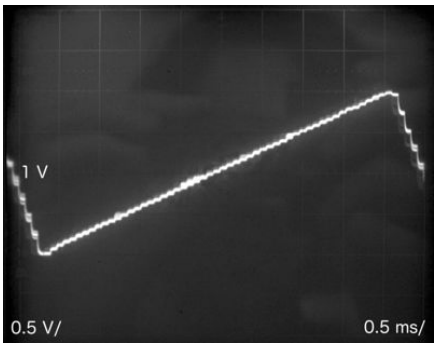


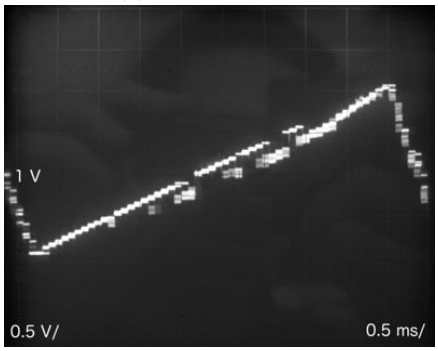
Figure 5: D/A converter schematic.



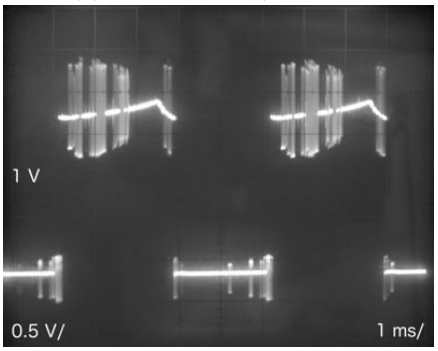
(a) Test point 1: V_{in}



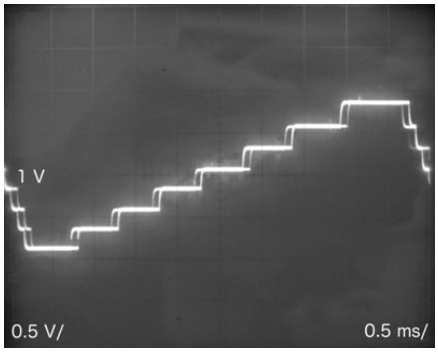
(b) Test point 2: D/A output



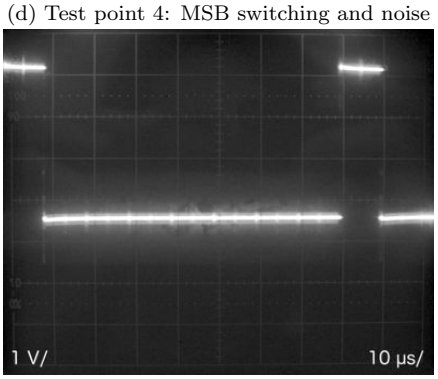
(c) Test point 2: as (6b) without C1



(d) Test point 4: MSB switching and noise

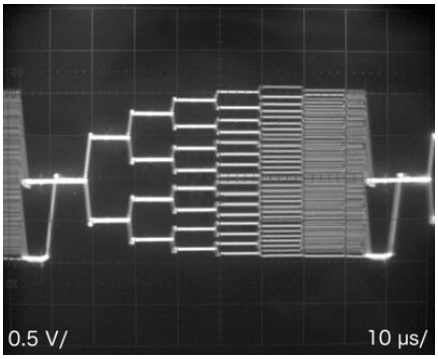


(e) Test point 2: as 6b with 3 bits resolution

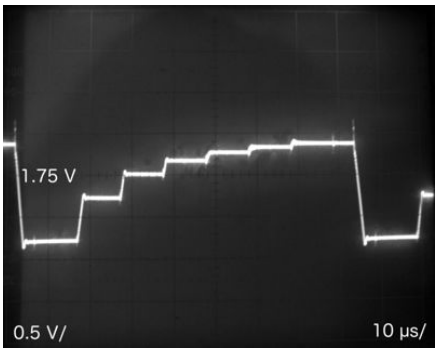


(f) Test point 6: EOC signal

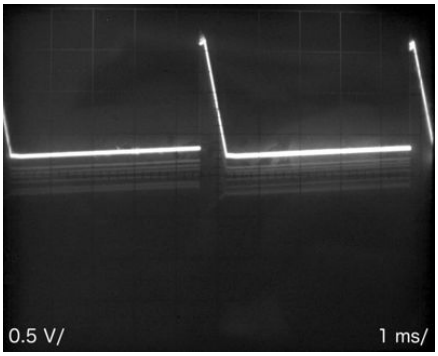
Figure 6: Various test point measurements.



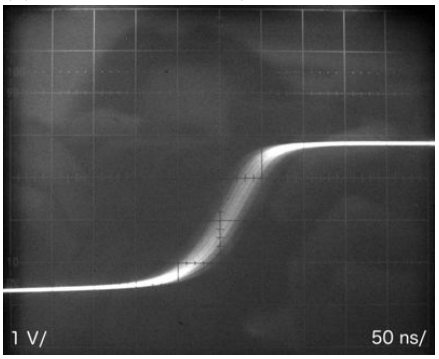
(a) Test point 7: SAC D/A output, ramp input



(b) Test point 7: SAC D/A out, all bits high



(c) Test point 9: S&H output



(d) Test point 10: Comparator rising flank

Figure 7: More measurements.

The circuit performs remarkably well. Several things could be improved, however. First of all a better separation between the digital (logic) and analogue parts would probably have been beneficial since the unshielded construction is very sensitive to noise and coupling issues. For instance, the clock is clearly visible at the analogue input.

The sample and hold circuit would benefit from a better buffer op amp, preferably one with a FET input to limit leakage to or from the S&H capacitor. The circuit works well at higher clock speeds, but when single stepping the converter the S&H capacitor is charged by the op amp input bias current, ruining the sample. This is not really a problem, since most situations will call for a higher sample frequency.

Another issue is that of switching noise in the separate D/A converter. The situation was somewhat remedied by the addition of capacitor "C1" at the ladder output but some noise is still present. It would probably have been a good idea to use som kind of "blanking time circuit" to prevent short circuiting the reference voltage and the creation of voltage spikes. This is not an issue in the SAC D/A since it only ever switches two bits at a time.

4 References

Carlsson, P. & Johansson, S. (1997). *Modern elektronisk mätteknik*. Stockholm: Liber AB.

Ganssle, J.D. (2004). *A Guide to Debouncing*. Baltimore: The Ganssle Group.

Hnatek, E.R. (1976). *A User's Handbook of D/A and A/D Converters*. New York: John Wiley & Sons, Inc.

Sheingold, D.H. (ed.) (1986). *Analog-digital Conversion Handbook*. Englewood Cliffs: Prentice-Hall.

A Circuit board

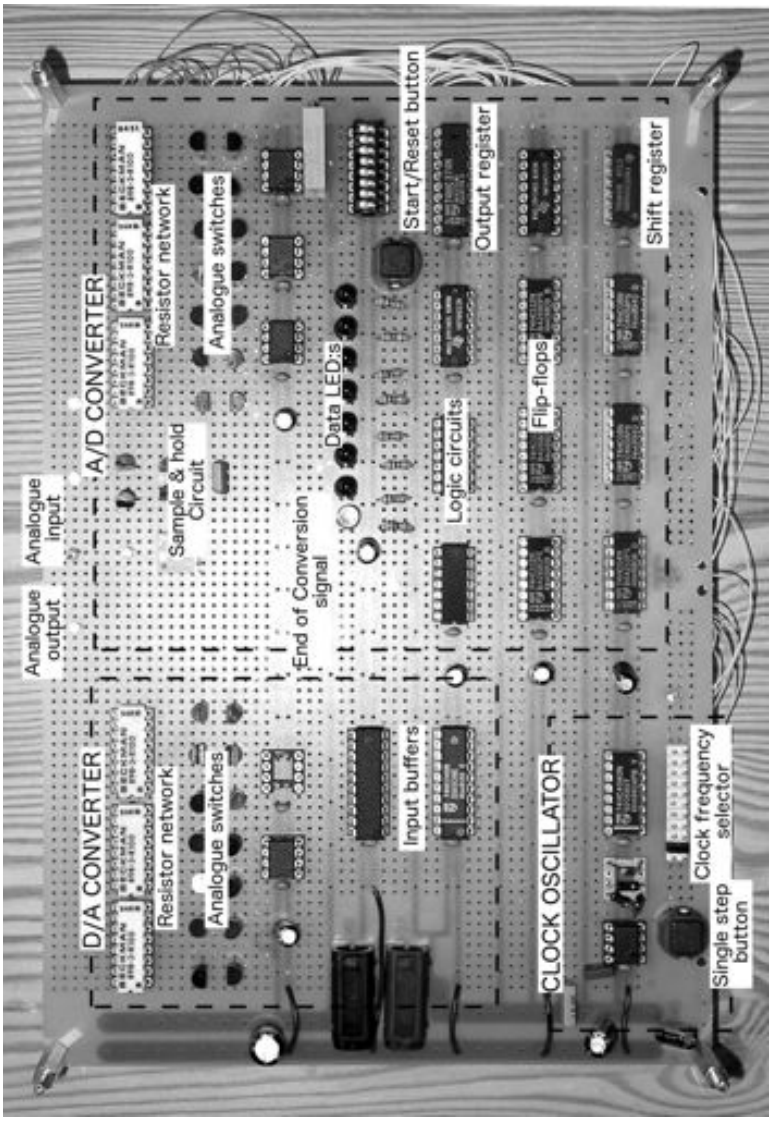


Figure 8: Circuit board.