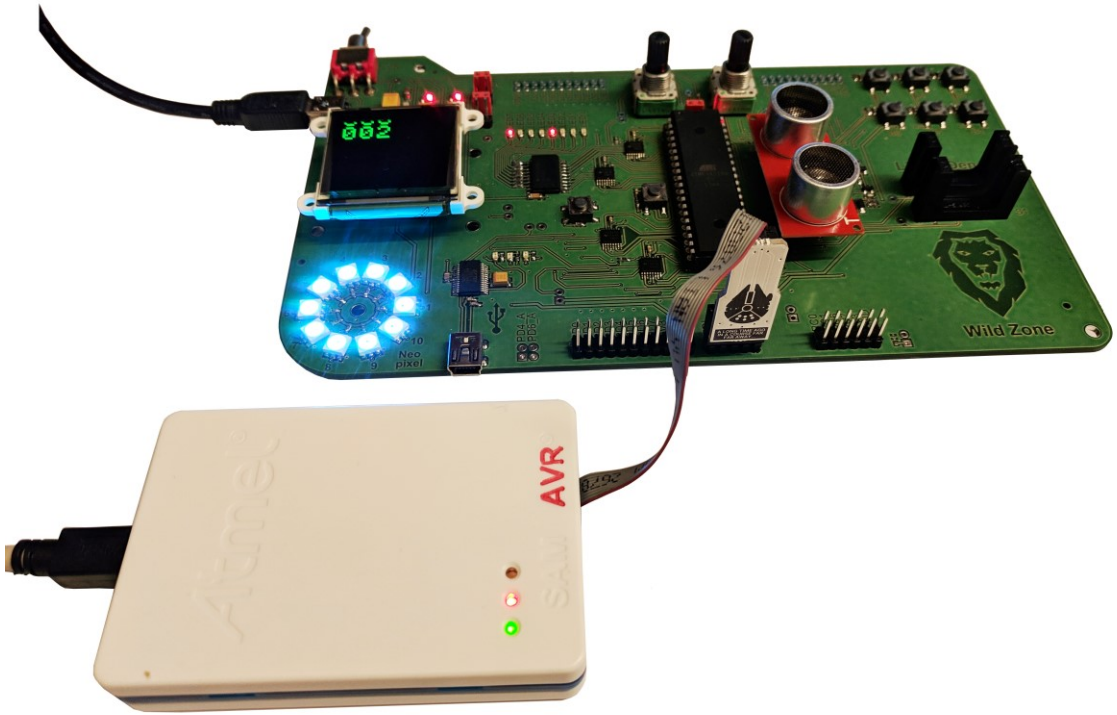
Digitala system EITA15

Elektro- och informationsteknik

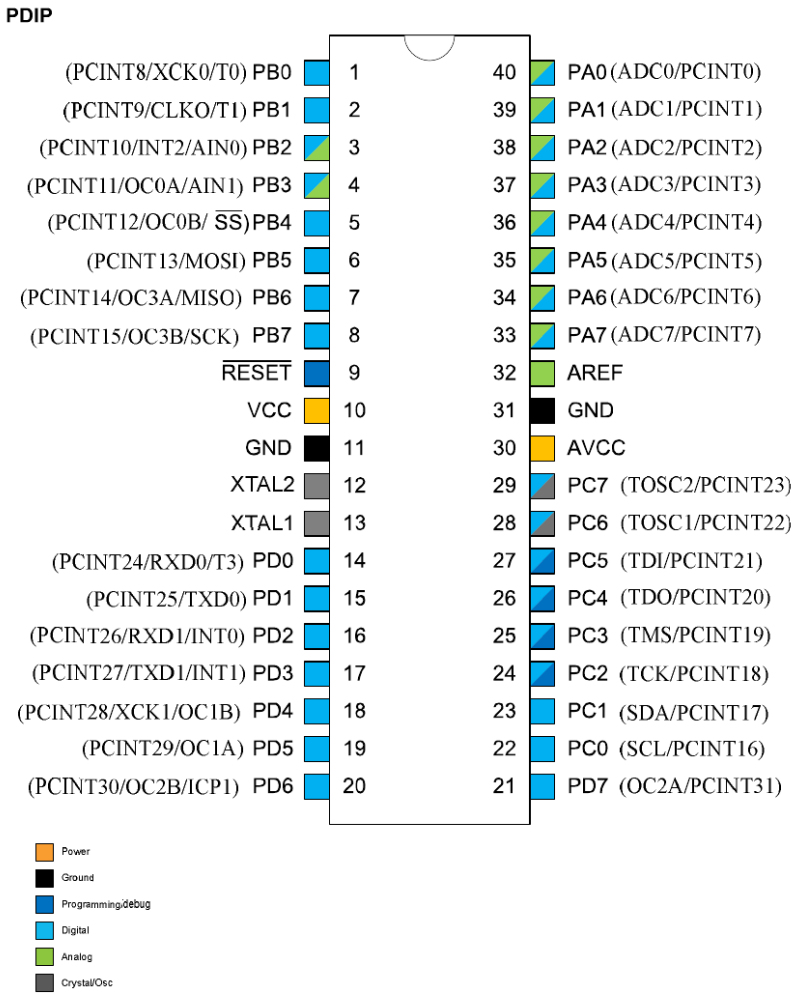
Laboration 1

Labbkort med JTAG debugger

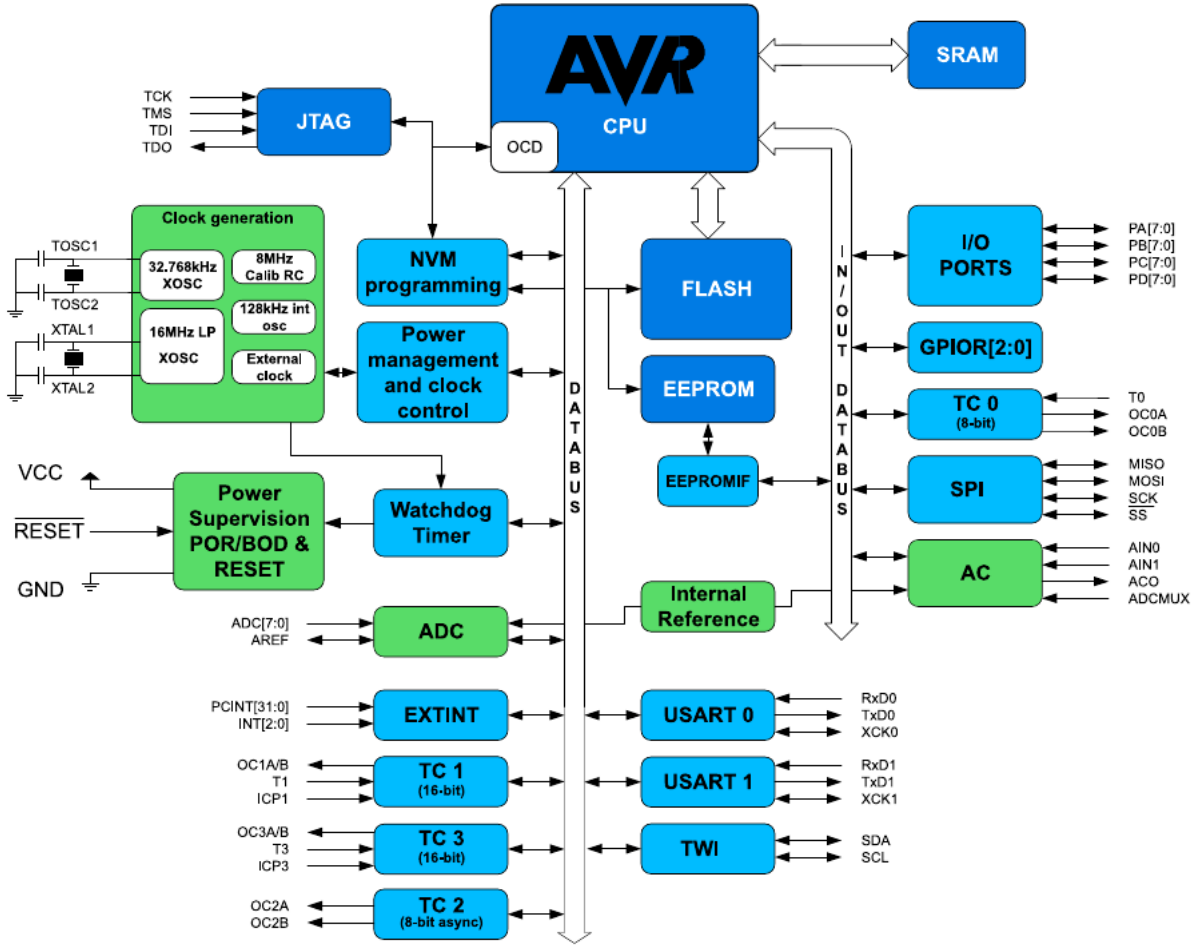


JTAG Ice debugger

40 pin DIP AT1284

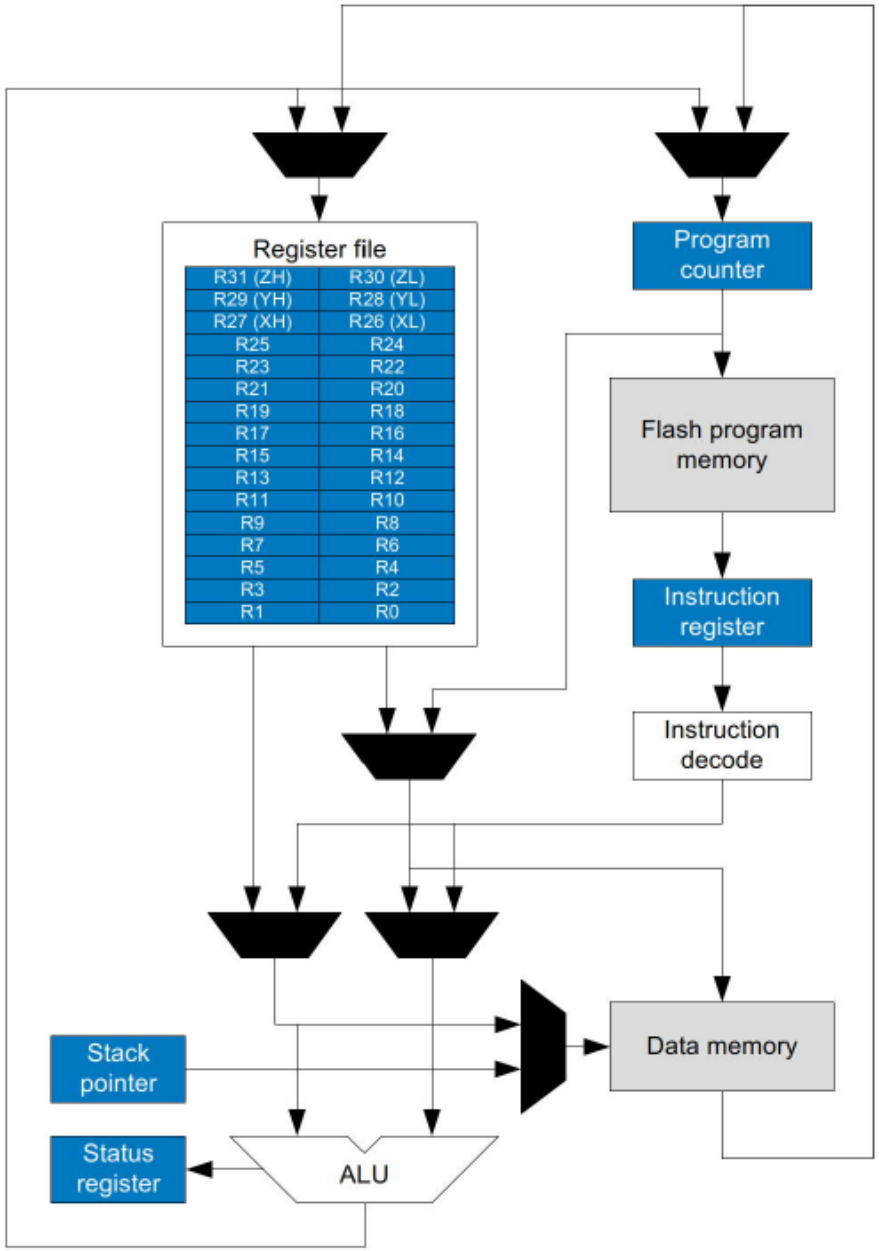


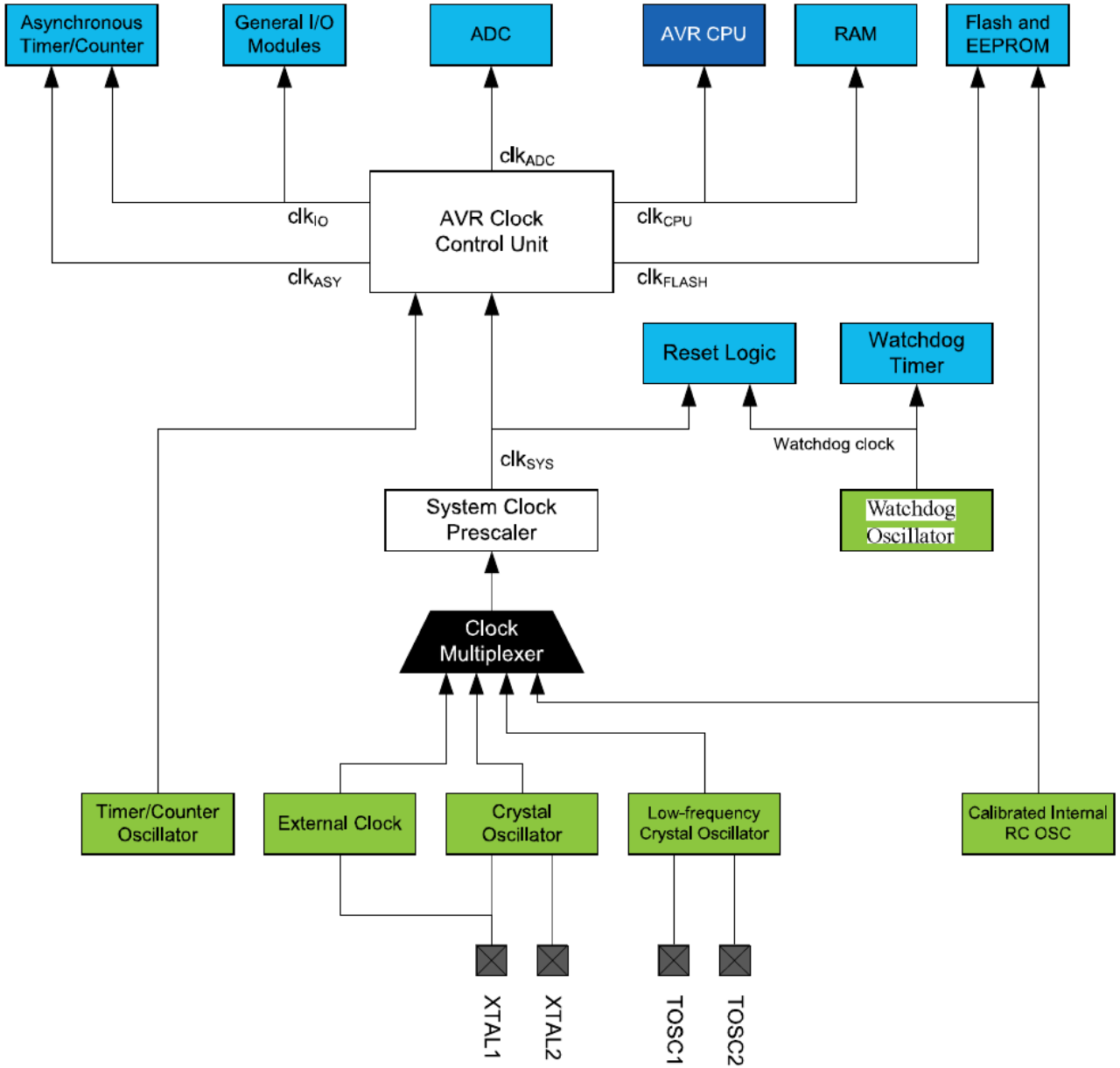
ATmega1284


AVR
CPU
OCD
SRAM
JTAG
TCK
TMS
TDI
TDO
Clock generation
32.768kHz XOSC
8MHz Calib RC
128kHz int osc
16MHz LP XOSC
External clock
TOSC1
TOSC2
XTAL1
XTAL2
NVM programming
Power management and clock control
FLASH
EEPROM
EEPROMIF
DATABUS
I/O PORTS
PA[7:0]
PB[7:0]
PC[7:0]
PD[7:0]
GPIOR[2:0]
TC 0 (8-bit)
T0
OC0A
OC0B
SPI
MISO
MOSI
SCK
SS
AC
AIN0
AIN1
ACO
ADCMUX
I/O DATABUS
VCC
RESET
GND
Power Supervision POR/BOD & RESET
Watchdog Timer
Internal Reference
ADC[7:0]
AREF
ADC
PCINT[31:0]
INT[2:0]
EXTINT
OC1A/B
T1
ICP1
TC 1 (16-bit)
OC3A/B
T3
ICP3
TC 3 (16-bit)
OC2A
OC2B
TC 2 (8-bit async)
USART 0
RxD0
TxD0
XCK0
USART 1
RxD1
TxD1
XCK1
TWI
SDA
SCL

AVR CPU core

R0 –r31 8 bit reg.
R26 –R31 16-bit indirect adr.
SP 16 bit




Asynchronous Timer/Counter
General I/O Modules
ADC
AVR CPU
RAM
Flash and EEPROM
clkADC
clkIO
AVR Clock Control Unit
clkCPU
clkASY
clkFLASH
Reset Logic
Watchdog Timer
Watchdog clock
clkSYS
System Clock Prescaler
Watchdog Oscillator
Clock Multiplexer
Timer/Counter Oscillator
External Clock
Crystal Oscillator
Low-frequency Crystal Oscillator
Calibrated Internal RC OSC
XTAL1
XTAL2
TOSC1
TOSC2

Features	ATmega164A	ATmega324A	ATmega644A	ATmega1284
Pin Count	40/44/49	40/44/49	40/44	40/44
Flash (Bytes)	16K	32K	64K	128K
SRAM (Bytes)	1K	2K	4K	16K
EEPROM (Bytes)	512	1K	2K	4K
General Purpose I/O Lines	32	32	32	32
SPI	1	1	1	1
TWI (I^2C)	1	1	1	1
USART	2	2	2	2
ADC	10-bit 15ksps	10-bit 15ksps	10-bit 15ksps	10-bit 15ksps
ADC Channels	8	8	8	8
Analog Comparator	1	1	1	1
8-bit Timer/ Counters	2	2	2	2
16-bit Timer/ Counters	1	1	1	2
PWM channels	6	6	6	8
Packages	PDIP TQFP VQFN/QFN DRQFN VFBGA	PDIP TQFP VQFN/QFN DRQFN VFBGA	PDIP TQFP VQFN/QFN	PDIP TQFP VQFNQFN

Flash minne

In-System Reprogrammable Flash Program Memory

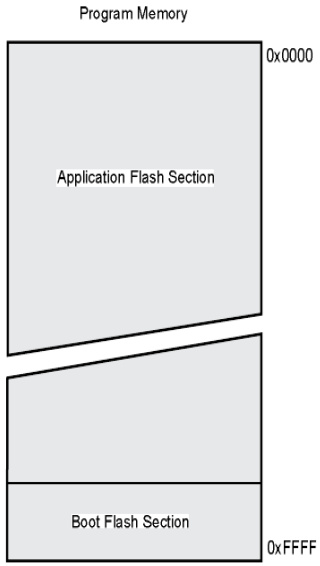
The ATmega1284 contains 128Kbytes On-chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 64 x 16.

The Flash memory has an endurance of at least 10,000 write/erase cycles. The ATmega1284 Program Counter (PC) is 16 bits wide, thus addressing the 64 program memory locations. The operation of Boot Program section and associated Boot Lock bits for software protection are described in detail in *Boot Loader Support – Read-While-Write Self-Programming*. Refer to *Memory Programming* for the description on Flash data serial downloading using the SPI pins or the JTAG interface.

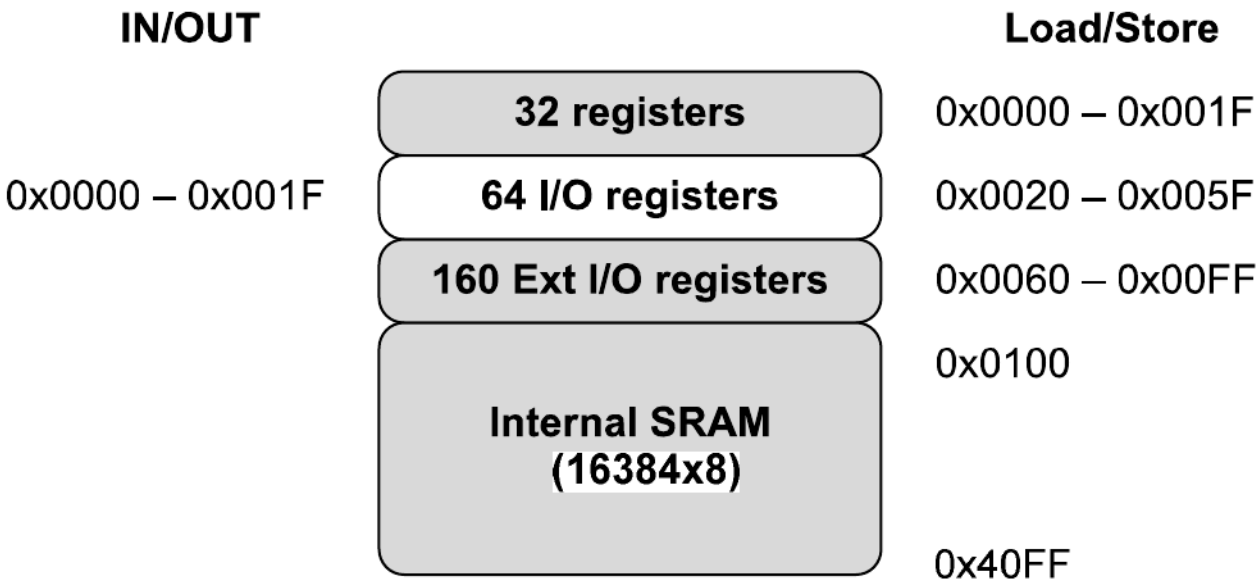
Constant tables can be allocated within the entire program memory address space, using the Load Program Memory (LPM) instruction.

Timing diagrams for instruction fetch and execution are presented in *Instruction Execution Timing*.

Figure 9-1. Program Memory Map ATmega1284



RWM -Minne och register



C-program

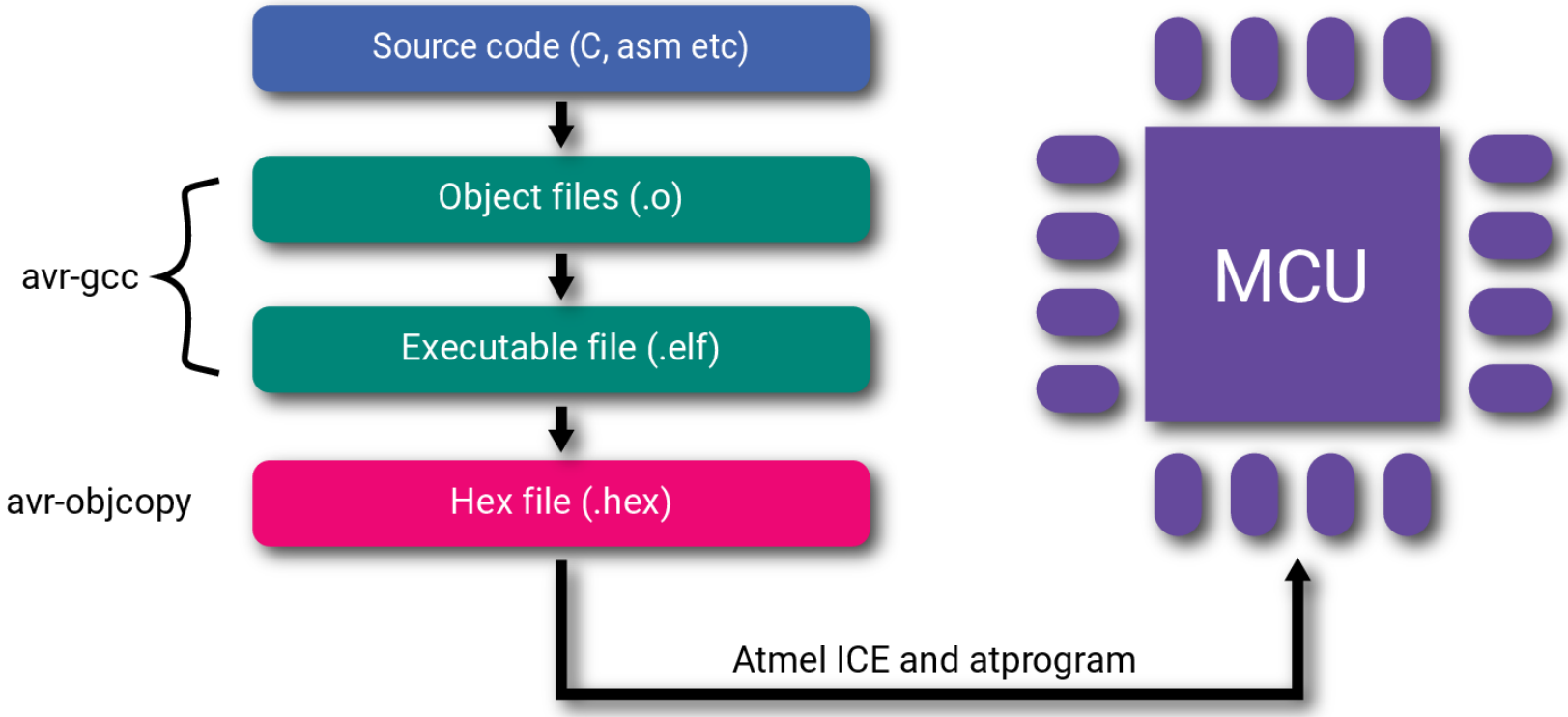
```
#include <avr/io.h>
unsigned char num;  //global variabel

void main(void)
{
int kalle;    //lokal variabel

  DDRA = 0xff; //set PORT A for out
  num = 0;
   while(1)
      {
            PORTA = num;
            num++;
      }
    return;
}
```

Titta på hemsidan "En kort sammanfattning av C"

C till hex


Source code (C, asm etc)
Object files (.o)
avr-gcc
Executable file (.elf)
avr-objcopy
Hex file (.hex)
MCU
Atmel ICE and atprogram

Avr Toolchain command

- **avr-gcc** -mmcu=[*target*] [*Optimization flag*] -g [*source file*] -o [*output .elf-file*]

- **avr-objcopy** -j [*section*] -O [*format*] [*input .elf-file*] [*output .hex-file*]
- **avr-objdump** [*option*] [*input .elf-file*]
- **atprogram.exe** -t [*tool*] -i [*interface*] -d [*device*] program -c -fl --verify -f [*input .hex-file*]

- Sökväg i Windows

- C:\Program Files (x86)\Atmel\Studio\7.0\toolchain\avr8\avr8-gnu-toolchain\bin

Minnets organisation