HARDWARE

Interface Signals

Table 2. Interface Signals

SIGNAL NAME	INPUT/OUTPUT	EXTERNAL CONNECTION	FUNCTION
RS	Input	MPU	Register select signal "0": Instruction register (when writing) Busy flag and address counter (when reading) "1": Data register (when writing and reading)
R/W	Input	MPU	Read/write select signal: "0": Writing; "1": Reading
E	Input	MPU	Operation (data read/write) enable signal
DB_4 - DB_7	Input/Output	MPU	High-order lines of data bus with three-state, bidirctional function for use in data transactions with the MPU. DB_7 may also be used to check the busy flag.
DB_0 - DB_3	Input/Output	MPU	Low-order lines of data bus with three-state, bidirectional function for use in data transactions with the MPU. These lines are not used when interfacing with a 4-bit microprocessor.
V_{DD}, V_{SS}		Power Supply	V_{DD}: +5 V, V_{SS}: GND
V_0		Power Supply	Contrast adjustment voltage

Functional Blocks

Registers

The LCD unit has two 8-bit registers - an instruction register (IR) and a data register (DR). The instruction register stores instruction codes such as "clear display" or "shift cursor", and also stores address information for the display data RAM and character generator RAM. The IR can be accessed by the microprocessor only for writing.

The data register is used for temporarily storing data during data transactions with the microprocessor. When writing data to the LCD unit, the data is initially stored in the data register, and is then automatically written into either the display data RAM or character generator RAM, as determined by the current operation. The data register is also used as a temporary storage area when reading data from the display data RAM or character generator RAM. When address information is written into the instruction register, the corresponding data from the display data RAM or character generator RAM is moved to the data register. Data transfer is completed when the microprocessor reads the contents of the data register by the next instruction. After the transfer is completed, data from the next address position of the appropriate RAM is moved to the data register, in preparation for subsequent reading operations by the microprocessor. One of the two registers is selected by the register select (RS) signal.

Table 3. Register Selection

RS	R/W	OPERATION
0	0	Write to instruction register, and execute internal operation (clear display, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 - DB_6)
1	0	Write to data register, and execute internal operation (DR → DD RAM or DR → CG RAM)
1	1	Read data register and execute internal operation (DD RAM → DR or CG RAM → DR)

Busy Flag (BF)

When the busy flag is set at a logical "1", the LCD unit is executing an internal operation, and no instruction will be accepted. The state of the busy flag is output on data line DB_7 in response to the register selection signals RS = 0, R/W= 1 as shown in Table 3. The next instruction may be entered after the busy flag is reset to logical "0".

Address Counter (AC)

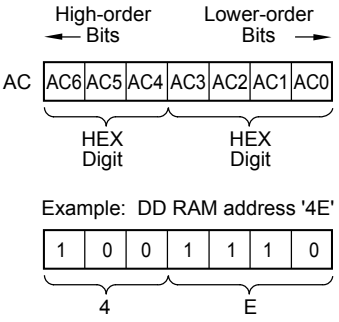
The address counter generates the address for the display data RAM and character generator RAM. When the address set instruction is written into the instruction register, the address information is sent to the address counter. The same instruciton also determines which of the two RAM's is to be selected.

After data has been written to or read from the display data RAM or character generator RAM, the address counter is automatically incremented or decremented by one. The contents of the address counter are output on data lines DB_0 - DB_6 in response to the register selection signals RS = 0, R/W = 1 as shown in Table 3.

Display Data RAM (DD RAM)

This 80 x 8 bit RAM stores up to 80 8-bit character codes as display data. The unused area of the RAM may be used by the microprocessor as a general purpose RAM area.

The display data RAM address, set in the address counter, is expressed in hexadecimal (HEX) numbers as follows:



The address of the display data RAM corresponds to the display position on the LCD panel as follows:

a. Address type a . . . .For dual-line display

	Digit 1	2	3	4	5	6	7	8	9		39	40
Line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	· · ·	26_H	27_H
Line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	· · ·	66_H	67_H

Display Position

DD RAM Address (HEX)

When a display shift takes place, the addresses shift is as follows:

Left Shift	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	09_H	· · ·	27_H	00_H
	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	49_H	· · ·	67_H	40_H

Right Shift	27_H	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	· · ·	25_H	26_H
	67_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	· · ·	65_H	66_H

The addresses for the second line are not continuous to the addresses for the first line. A 40-character RAM area is assigned to each of the two line as follows:

line 1: 00_H - 27_H

line 2: 40_H - 67_H

For an LCD unit with a display capacity of less than 40 characters per line, characters equal in number to the display capacity, as counted from display position 1, are displayed.

b. Address type b . . . .For single-line display with logically dual-line addressing

	Digit 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H

Display Position

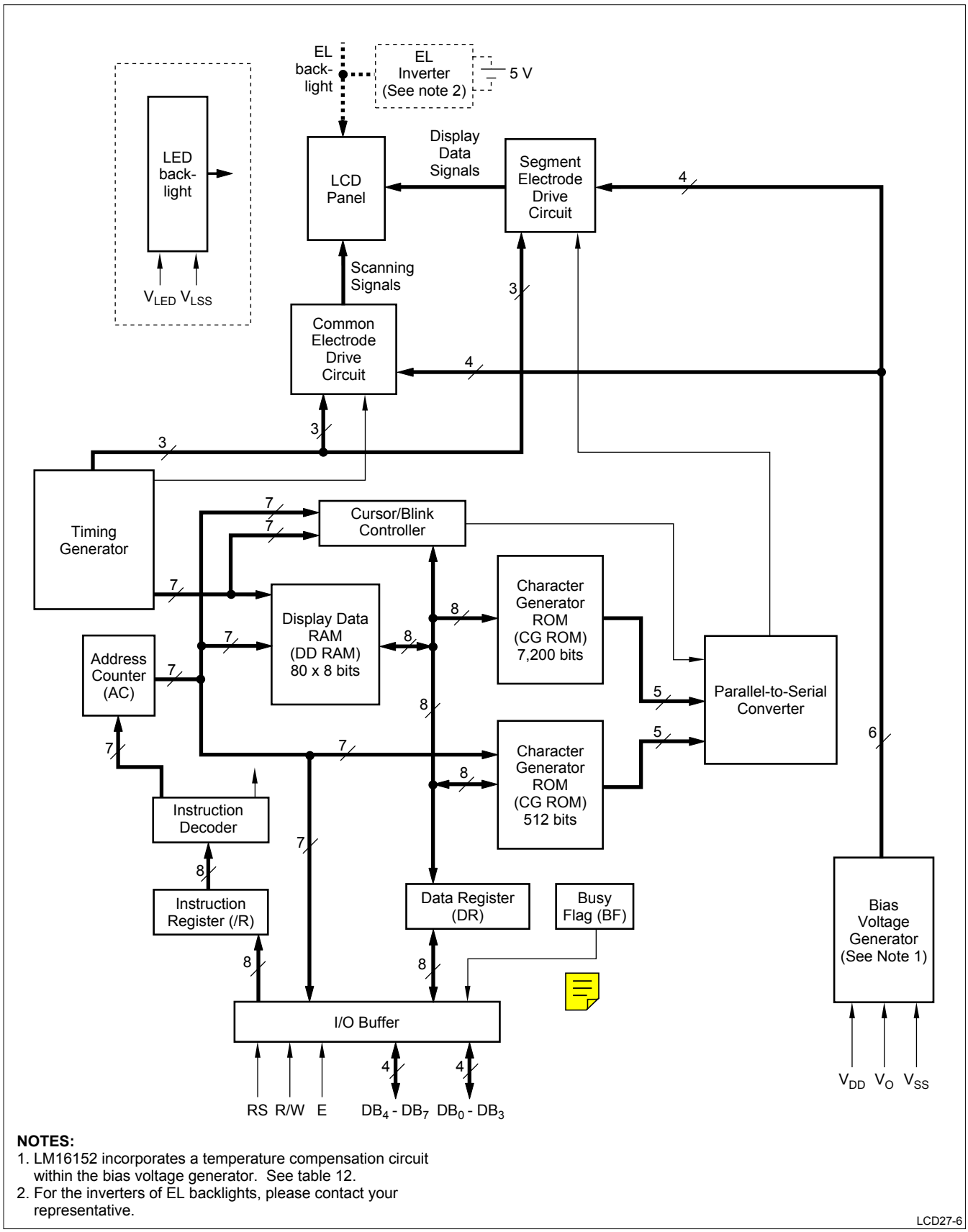
DD RAM Address (HEX)

When a display shift takes place, the addresses shift as follows:

Left Shift	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H

Right Shift	27_H	00_H	01_H	02_H	03_H	04_H	05_H	06_H	67_H	40_H	41_H	42_H	43_H	44_H	45_H	46_H

The right-hand eight characters, for the purposes of addressing and shifting, may be considered to constitute a second display line. For the address type of each model, see Table 12.



NOTES:
1. LM16152 incorporates a temperature compensation circuit within the bias voltage generator. See table 12.
2. For the inverters of EL backlights, please contact your representative.

Figure 1. Functional Block Diagram

Table 4. Character Codes

HIGH-ORDER 4 BIT / LOW-ORDER 4 BIT	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxx0101	(6)												
xxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

NOTES:
1. The CG RAM generates character patterns in accordance with the user's program.
2. Shaded areas indicate 5 x 10 dot character patterns.

4-Bit Interface

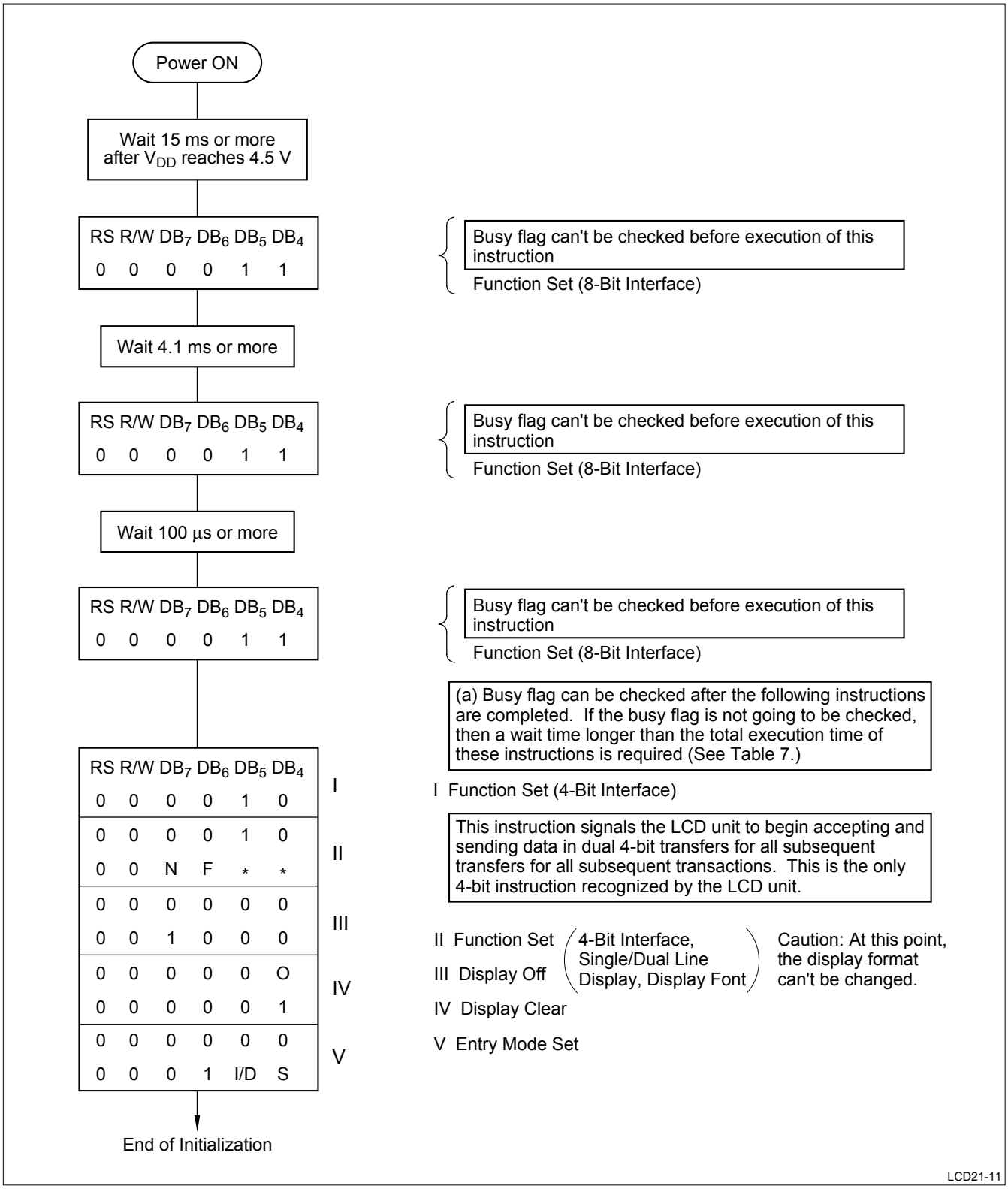


Figure 4. 4-Bit Interface

Table 7. Instruction Set

INSTRUCTION	CODE										FUNCTION	EXECUTION TIME (max) (f_{CP} or f_{OSC} = 250 kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear enter display area, restore display from shift, and load address counter with DD RAM address 00_H.	1.64 ms
Display/Cursor Home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00_H.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.	40 µs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D), cursor (C), and blinking of character at cursor position (B).	40 µs
Display/Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.	40 µs
Function Set	0	0	0	0	1	DL	N	0	*	*	Set interface data length (DL) and number of display lines (N).	40 µs
CG RAM Address Set	0	0	0	1	A_{CG}						Load the address counter with a CG RAM address. Subsequent data is CG RAM data.	40 µs
DD RAM Address Set	0	0	1	A_{DD}							Load the address counter with a DD RAM address. Subsequent data is DD RAM data.	40 µs
Busy Flag/Address Counter Read	0	1	BF	AC							Read busy flag (BF) and contents of address counter (AC).	0 µs
CG RAM/DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM.	40 µs
CG RAM/DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM.	40 µs
	I/D = 1: Increment, I/D = 0: Decrement S = 1: Display Shift On S/C = 1: Shift Display, S/C = 0: Move Cursor R/L = 1: Shift Right, R/L = 0: Shift Left DL = 1: 8-Bit, DL = 0: 4-Bit N = 1: Dual Line, N = 0: Single Line BF = 1: Internal Operation, BF = 0: Ready for Instruction										DD RAM: Display Data RAM CG RAM: Character Generator RAM A_{CG}: Character Generator RAM Address A_{DD}: Display Data RAM Address AC: Address Counter	

NOTES:

1. Symbol "*" signifies a "don't care" bit.
2. Correct input value for "N" is predetermined for each model (see Table 12).

ELECTRICAL CHARACTERISTICS

Absolue Maximum Ratings

See the device specifications for each LCD unit model.

Electrical Characteristics

See the device specificiations for each LCD unit model. Some of the currently available specifications do not describe the test conditions for the high-level and low-level output voltages. These conditions are as follows:

Table 8.

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Output Voltage	H	V_{OH}	$-I_{OH}$ = 0.205 mA	2.4	—	V
	L	V_{OL}	I_{OL} = 1.2 mA	—	0.4	V

Timing Characteristics

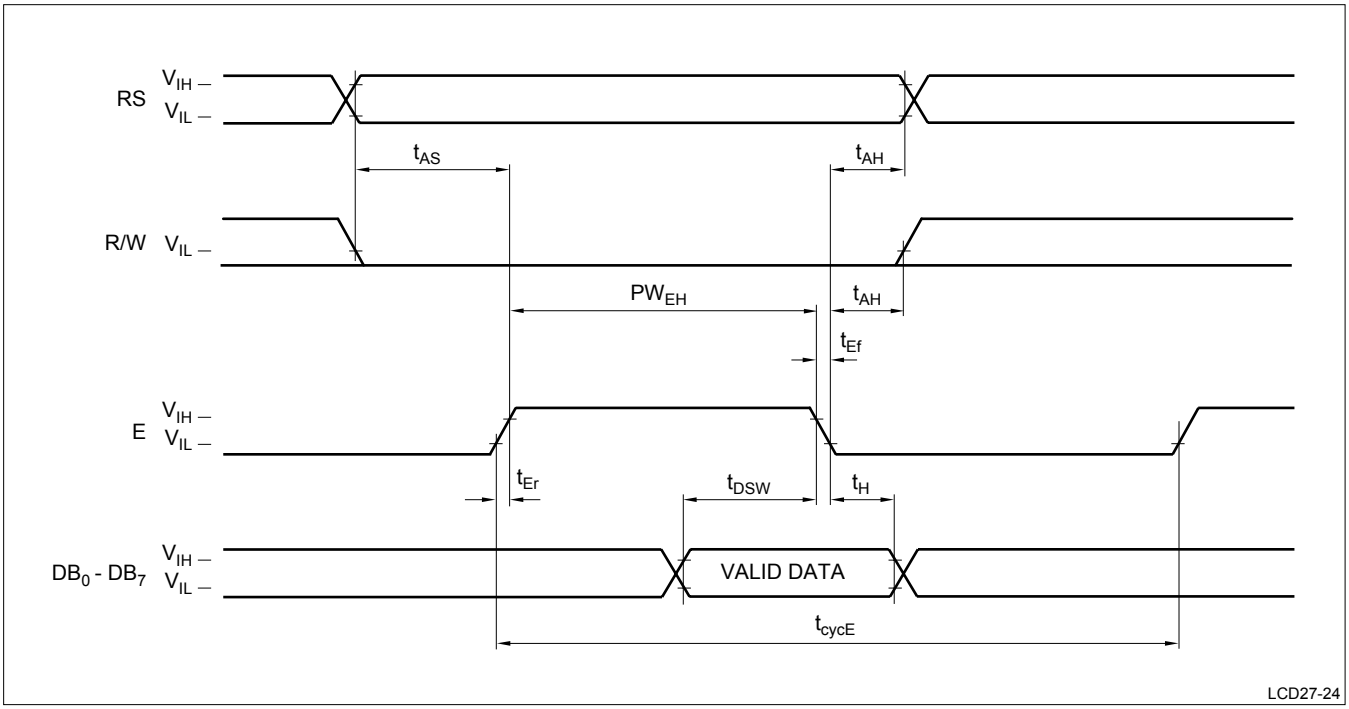


Figure 5. Write Operation Timing Diagram
(For data sent from the external microprocessor to the LCD unit)

Table 9. Write Operation Timing Characteristics
(V_{DD} = 5.0 ± 5%, V_{SS} = 0 V, T_A = 0 ~ 50°C)

PARAMETER		SYMBOL	VALUE		UNIT
			MIN.	MAX.	
Enable Cycle Time		$t_{CYC}E$	1000	—	ns
Enable Pulse Width	"High" Level	PW_{EH}	450	—	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns
Setup Time	RS, R/W-E	t_{AS}	140	—	ns
Address Hold Time		t_{AH}	10	—	ns
Data Setup Time		t_{DSW}	195	—	ns
Data Hold Time		t_H	10	—	ns

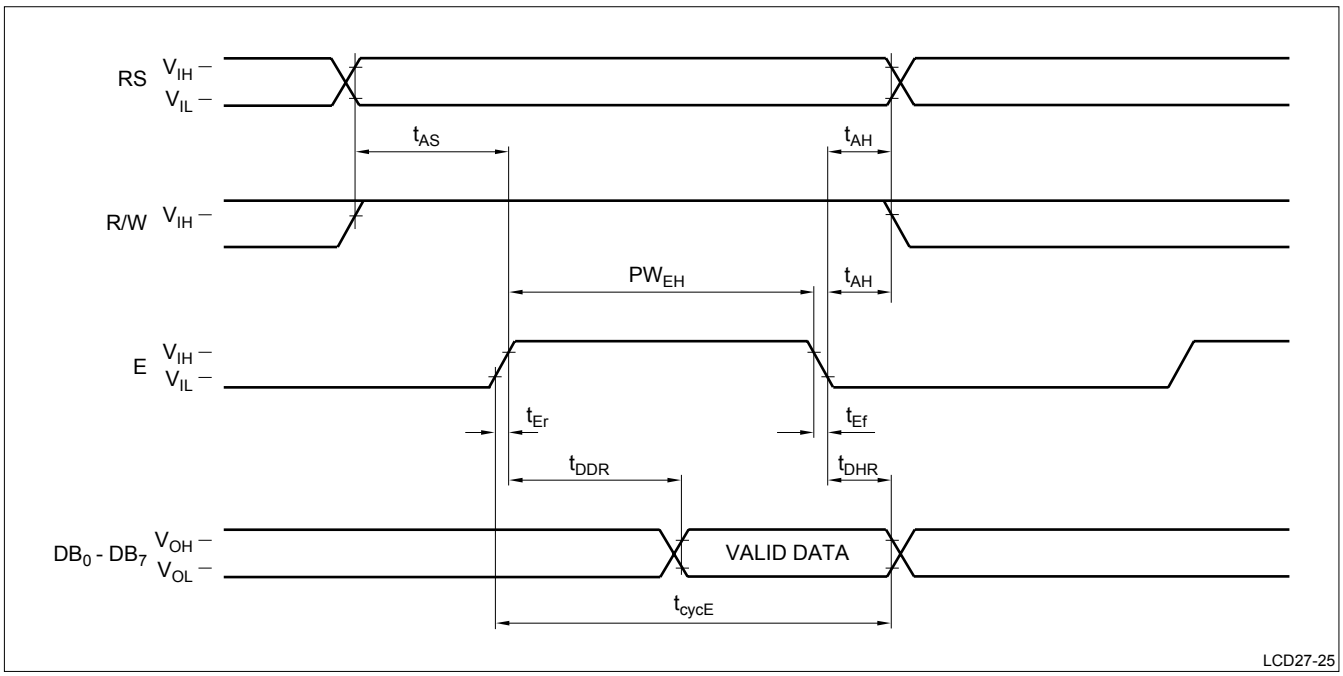


Figure 6. Read Operation Timing Diagram
(For data sent from the LCD unit to the external microprocessor)

Table 10. Read Operation Timing Characteristics
(V_{DD} = 5.0 ± 5%, V_{SS} = 0 V, Ta = 0 ~ 50°C)

PARAMETER		SYMBOL	VALUE		UNIT
			MIN.	MAX.	
Enable Cycle Time		$t_{cyc}E$	1000	—	ns
Enable Pulse Width	"High" Level	PW_{EH}	450	—	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns
Setup Time	RS, R/W-E	t_{AS}	140	—	ns
Address Hold Time		t_{AH}	10	—	ns
Data Delay Time		t_{DDR}	—	320	ns
Data Hold Time		t_{OHR}	20	—	ns

Table 11. Power Conditions for Internal Reset

PARAMETER	SYMBOL	VALUE			UNIT
		MIN.	TYP.	MAX.	
Voltage Build-Up Time	t_{rcc}	0.1	—	10	ms
Power-Off Period	t_{OFF}	1	—	—	ms

If the above conditions are not satisfied, the internal reset circuit will not operate normally. In such a case, the LCD unit must be initialized by executing a series of instructions (see the Execution by Instructions section).

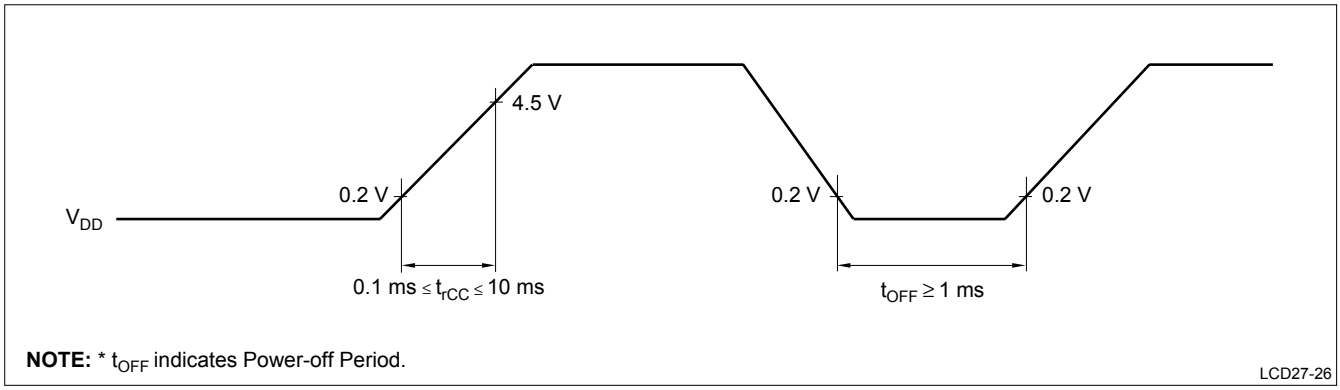


Figure 7.

2. 4-Bit Data Transfer with a Single-Line, 16-Character Display (Using Internal Reset). Table 14 shows a sample operating procedure for an LCD unit in this mode. After power has been turned on, the 8-bit data transfer mode is in effect, and the first write operation is assumed to be an 8-bit data transfer.

   Since the data lines DB_0 - DB_3 are not connected, this data is not accepted and must be written again (i.e. the function set instruction must be written twice). Subsequent data transfers are completed in two 4-bit transfer operations (see Table 14).

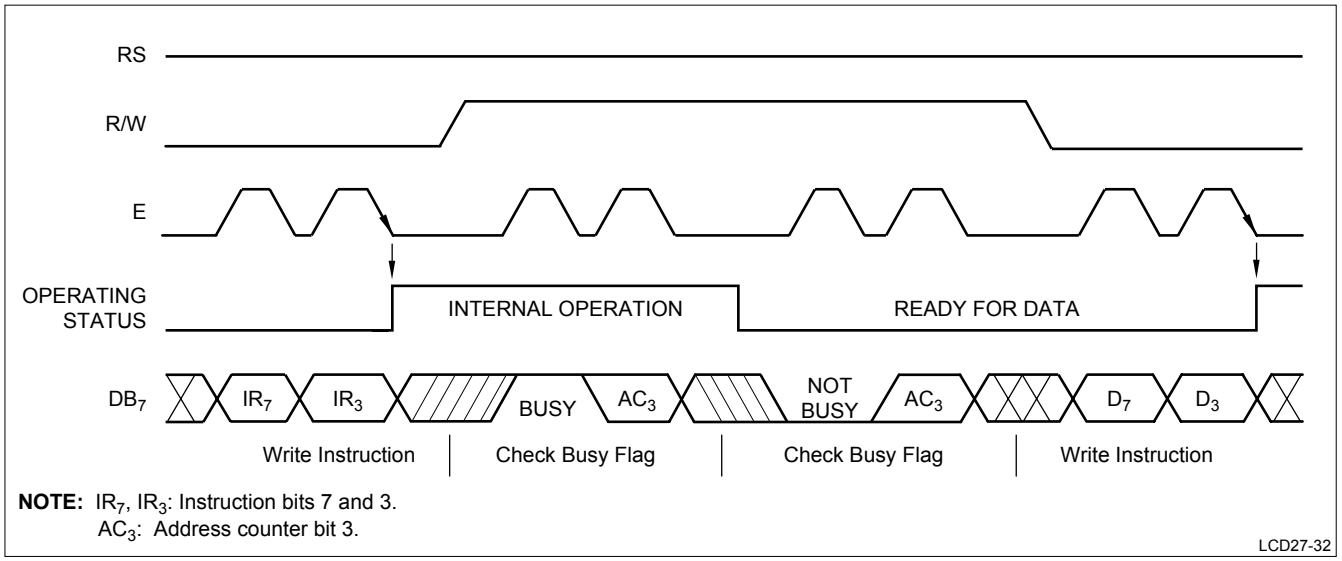


Figure 9. 4-Bit Interface Timing (Example)

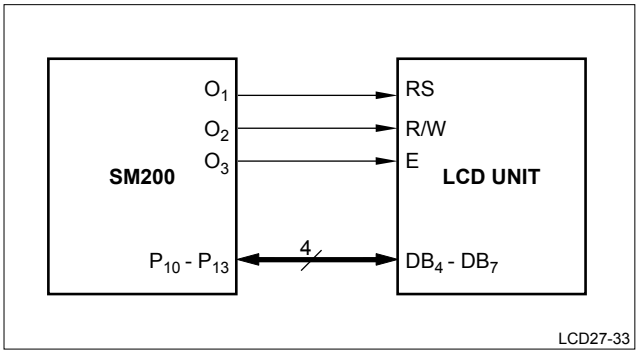


Figure 10. Connection to SM200