TL7702A, TL7705A, TL7709A, TL7712A, TL7715A
TL7702AY, TL7705AY, TL7709AY, TL7712AY, TL7715AY
SUPPLY VOLTAGE SUPERVISORS

SLVS028D – APRIL 1983 – REVISED JANUARY 1999
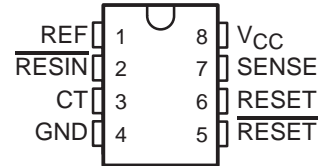
- **Power-On Reset Generator**

- **Automatic Reset Generation After Voltage Drop**

- **Wide Supply Voltage Range**

- **Precision Voltage Sensor**

- **Temperature-Compensated Voltage Reference**

- **True and Complement Reset Outputs**

- **Externally Adjustable Pulse Duration**

D, JG, OR P PACKAGE
(TOP VIEW)

REF	1	8 V_{CC}
$\overline{\text{RESIN}}$	2	7 SENSE
CT	3	6 RESET
GND	4	5 $\overline{\text{RESET}}$

FK PACKAGE
(TOP VIEW)

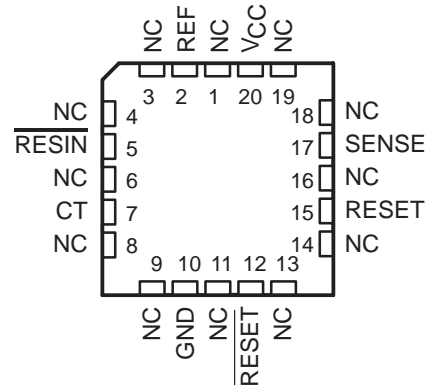NC – No internal connection

description

The TL77xxA family of monolithic integrated circuit supply voltage supervisors is specifically designed for use as reset controllers in micro-computer and microprocessor systems. The supply voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down (assuming that SENSE is below V_{IT-}), the outputs remain active until the V_{CC} falls below a maximum of 2 V. After this, the outputs are undefined.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	TL7702ACD – TL7715ACD			TL7702ACP – TL7715ACP	TL7702ACY – TL7715ACY
−40°C to 85°C	TL7702AID – TL7715AID			TL7702AIP – TL7715AIP	
−55°C to 125°C		TL7702AMFK TL7705AMFK	TL7702AMJG TL7705AMJG		

TEXAS INSTRUMENTS

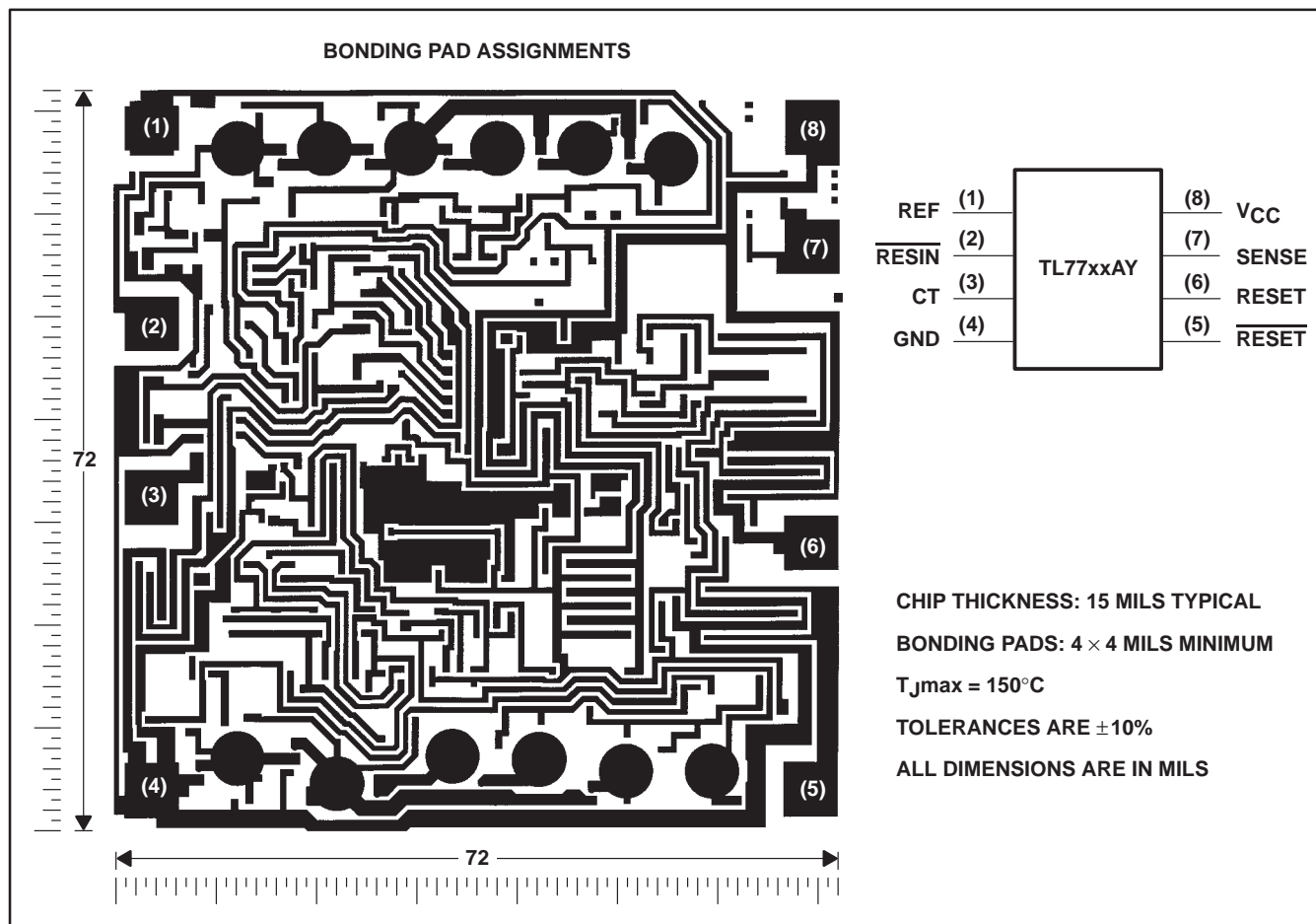POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

description (continued)

An external capacitor (typically 0.1 μF for the TL77xxAC and TL77xxAI and typically 0.02 μF for the TL77xxAM) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77xxAC series are characterized for operation from 0°C to 70°C. The TL77xxAI series are characterized for operation from −40°C to 85°C. The TL7702AM and TL7705AM are characterized for operation over the full military range of −55°C to 125°C.

TL77xxAY chip information

This chip, when properly assembled, displays characteristics similar to the TL77xxAC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4×4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE $\pm$10%

ALL DIMENSIONS ARE IN MILS

functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense comparator trip point.
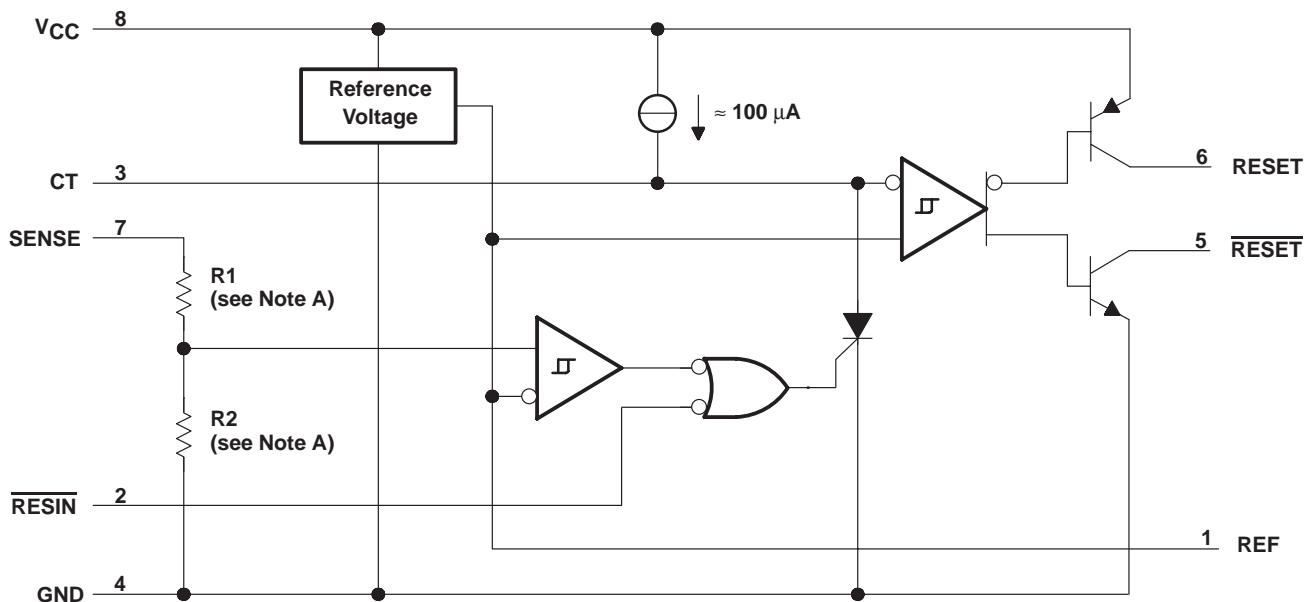
NOTES: A.   TL7702A: R1 = 0 Ω, R2 = open
               TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
               TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
               TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
               TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
      B.   Terminal numbers shown are for the D, JG, or P package.
      C.   Resistor values shown are nominal.

timing diagram
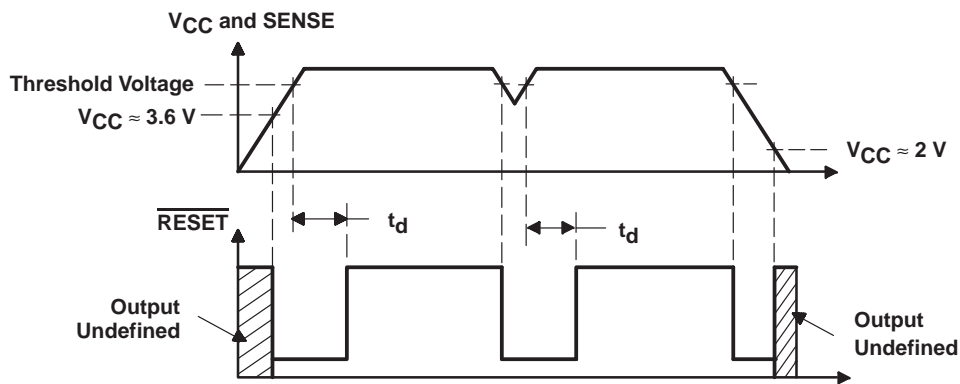
absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	20 V
Input voltage range, V_I, $\overline{RESIN}$	−0.3 V to 20 V
Input voltage range, V_I, SENSE: TL7702A (see Note 2)	−0.3 V to 6 V
TL7705A	−0.3 V to 20 V
TL7709A	−0.3 V to 20 V
TL7712A, TL7715A	−0.3 V to 20 V
High-level output current, I_{OH}, $\overline{RESET}$	−30 mA
Low-level output current, I_{OL}, $\overline{RESET}$	30 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxAC	0°C to 70°C
TL77xxAI	−40°C to 85°C
TL7702AM, TL7705AM	−55°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		TL77xxAC, TL77xxAI		TL77xxAM		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		3.5	18	3.6	10	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2		2		V
Low-level input voltage at $\overline{RESIN}$, V_{IL}			0.6		0.6	V
Input voltage, SENSE, V_I	TL7702A	0	See Note 2	0	See Note 2	V
	TL7705A	0	10	0	10	
	TL7709A	0	15			
	TL7712A	0	20			
	TL7715A	0	20			
High-level output current, $\overline{RESET}$, I_{OH}			−16		−16	mA
Low-level output current, $\overline{RESET}$, I_{OL}			16		16	mA
Timing capacitor, C_T			10		10	µF
Operating free-air temperature range, T_A	TL77xxAC	0	70			°C
	TL77xxAI	−40	85			
	TL7702AM, TL7705AM			−55	125	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} −1 V or 6 V, whichever is less.

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TEXAS
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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL77xxAC, TL77xxAI			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET	I_{OH} = −16 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$	I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage	T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A — T_A = 25°C	2.48	2.53	2.58	V
		TL7705A	4.5	4.55	4.6	
		TL7709A	7.5	7.6	7.7	
		TL7712A	10.6	10.8	11	
		TL7715A	13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE (V_{IT+} − V_{IT-})	TL7702A — T_A = 25°C		10		mV
		TL7705A		15		
		TL7709A		20		
		TL7712A		35		
		TL7715A		45		
I_I	Input current, $\overline{\text{RESIN}}$	V_I = 2.4 V to V_{CC}			20	µA
		V_I = 0.4 V			−100	
I_I	Input current, SENSE	TL7702A — $V_{ref} < V_I < V_{CC}$ − 1.5 V		0.5	2	µA
I_{OH}	High-level output current, $\overline{\text{RESET}}$	V_O = 18 V			50	µA
I_{OL}	Low-level output current, RESET	V_O = 0			−50	µA
I_{CC}	Supply current	All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	TL77xxAC, TL77xxAI			UNIT
			MIN	TYP	MAX	
	Output pulse duration	C_T = 0.1 µF	0.65	1.2	2.6	µs
	Input pulse duration at $\overline{\text{RESIN}}$		0.4			µs
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs	$V_{IH} = V_{IT-} + 200$ mV, $V_{IL} = V_{IT-} − 200$ mV	2			µs
t_{pd}	Propagation delay time from $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	V_{CC} = 5 V			1	µs
t_r	RESET	V_{CC} = 5 V, See Note 3			0.2	µs
	$\overline{\text{RESET}}$				3.5	
t_f	RESET				3.5	µs
	$\overline{\text{RESET}}$				0.2	

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.
NOTE 3:   The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

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TL7702A, TL7705A, TL7709A, TL7712A, TL7715A
TL7702AY, TL7705AY, TL7709AY, TL7712AY, TL7715AY
SUPPLY VOLTAGE SUPERVISORS

SLVS028D – APRIL 1983 – REVISED JANUARY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS†	TL7702AM, TL7705AM			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		$I_{OH} = -16$ mA	$V_{CC}-1.5$			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		$I_{OL} = 16$ mA			0.4	V
V_{ref}	Reference voltage			2.38	2.53	2.63	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702AM	$V_{CC} = 3.6$ V to 10 V	2.38	2.53	2.63	V
		TL7705AM		4.25	4.55	4.7	
V_{hys}	Hysteresis SENSE ($V_{IT+} - V_{IT-}$)	TL7702AM	$V_{CC} = 3.6$ V to 10 V		10		mV
		TL7705AM			15		
I_I	Input current, $\overline{\text{RESIN}}$		$V_I = 2.4$ V to V_{CC}			20	µA
			$V_I = 0.4$ V			−100	
I_I	Input current, SENSE	TL7702AM	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5	2	µA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		$V_O = 10$ V			50	µA
I_{OL}	Low-level output current, RESET		$V_O = 0$			−50	µA
I_{CC}	Supply current	TL7702AM	All inputs and outputs open		1.8	3	mA
		TL7705AM	VSENSE = 10 V, $\overline{\text{RESIN}} \geq 2$ V				

† All electrical characteristics are measured with 0.02-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS‡	TL7702AM, TL7705AM			UNIT
			MIN	TYP	MAX	
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs	$V_{IH} = V_{IT-} + 200$ mV, $V_{IL} = V_{IT-} - 200$ mV	2*			µs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	$V_{CC} = 5$ V		1.5		µs
t_r	RESET	$V_{CC} = 5$ V, See Note 3			0.2*	µs
	$\overline{\text{RESET}}$				3.5*	
t_f	RESET				3.5*	µs
	$\overline{\text{RESET}}$				0.2*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
‡ All switching characteristics are measured with 0.02-µF capacitors connected at REF and V_{CC} to GND.
NOTE 3:   The rise and fall times are measured with a 4.7-kΩ load resistor at $\overline{\text{RESET}}$ and RESET.

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electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL77xxAY			UNIT
			MIN	TYP	MAX	
V_{ref}	Reference voltage			2.53		V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A		2.53		V
		TL7705A		4.55		
		TL7709A		7.6		
		TL7712A		10.8		
		TL7715A		13.5		
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702A		10		mV
		TL7705A		15		
		TL7709A		20		
		TL7712A		35		
		TL7715A		45		
I_I	Input current, SENSE	TL7702A	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5		µA
I_{CC}	Supply current		All inputs and outputs open		1.8		mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL77xxAY			UNIT
		MIN	TYP	MAX	
Output pulse duration	$C_T = 0.1$ µF		1.2		µs

‡ All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.
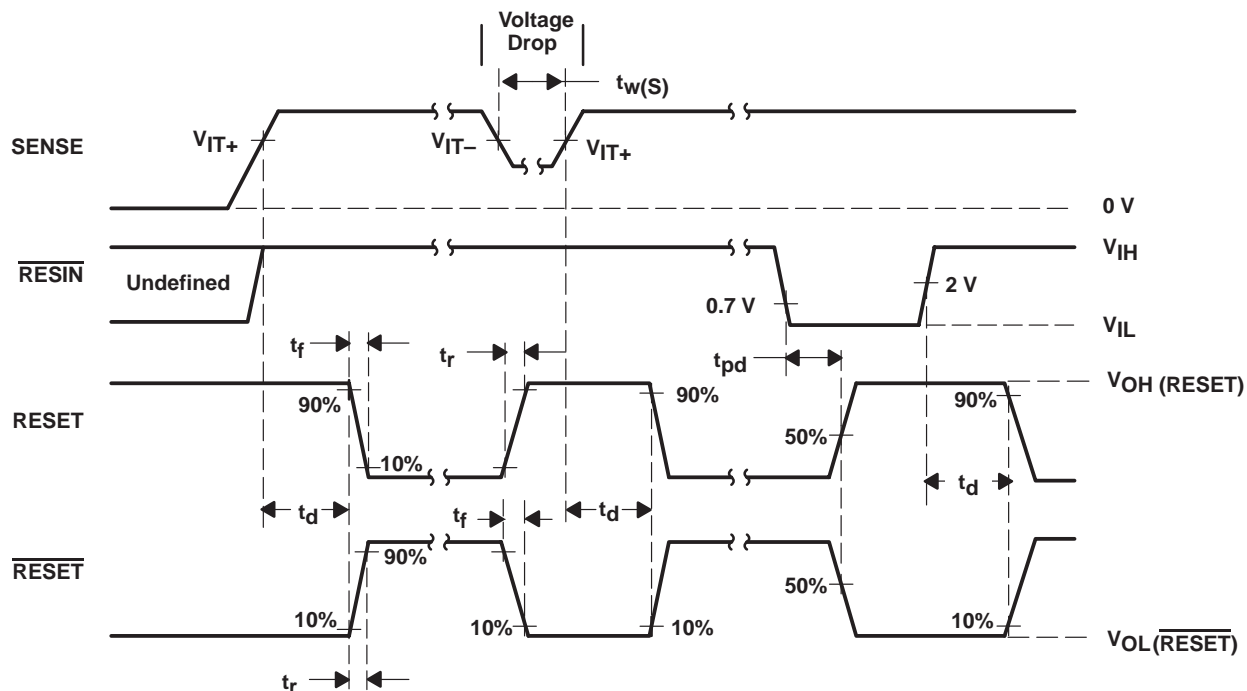
PARAMETER MEASUREMENT INFORMATION

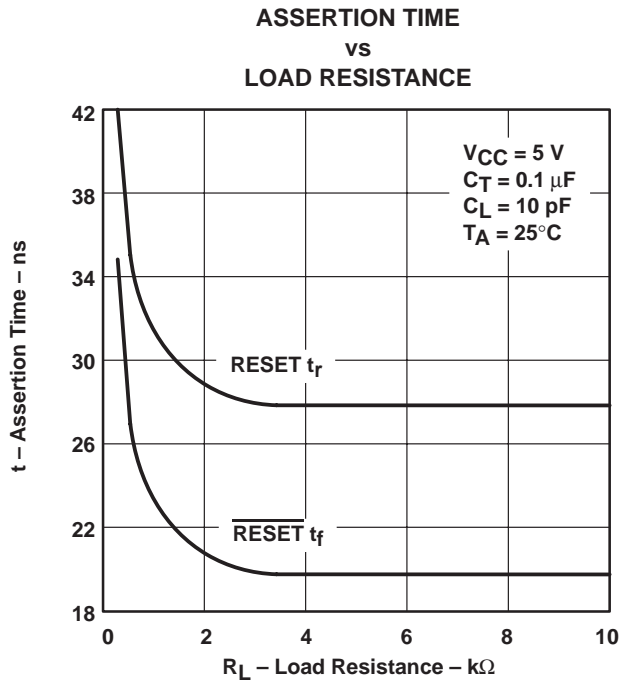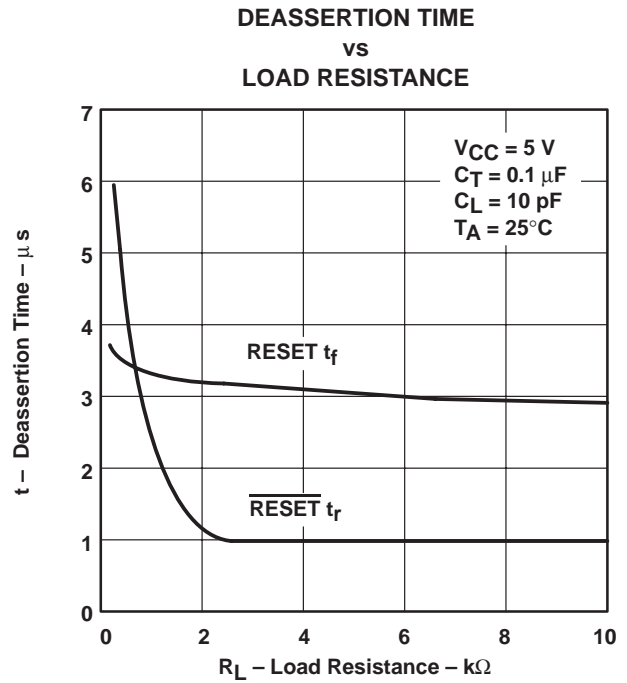**Figure 1. Voltage Waveforms**

TYPICAL CHARACTERISTICS†

ASSERTION TIME vs LOAD RESISTANCE

Figure 2

DEASSERTION TIME vs LOAD RESISTANCE

Figure 3

ASSERTION TIME vs LOAD CAPACITANCE
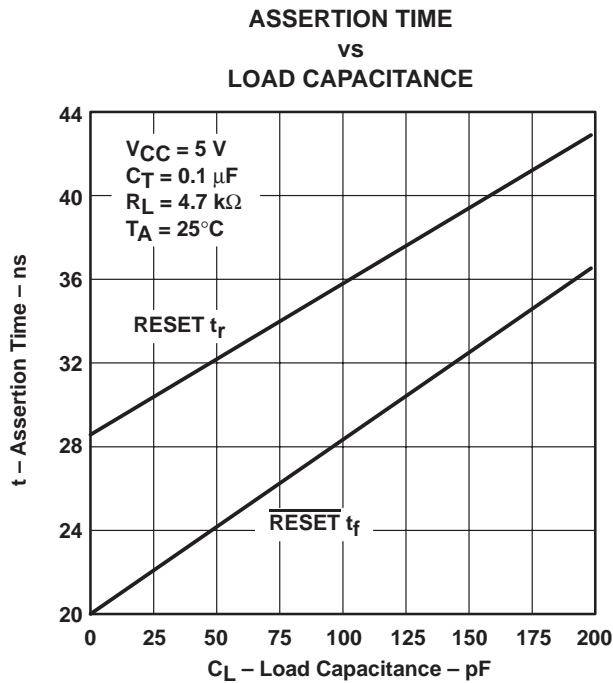

Figure 4

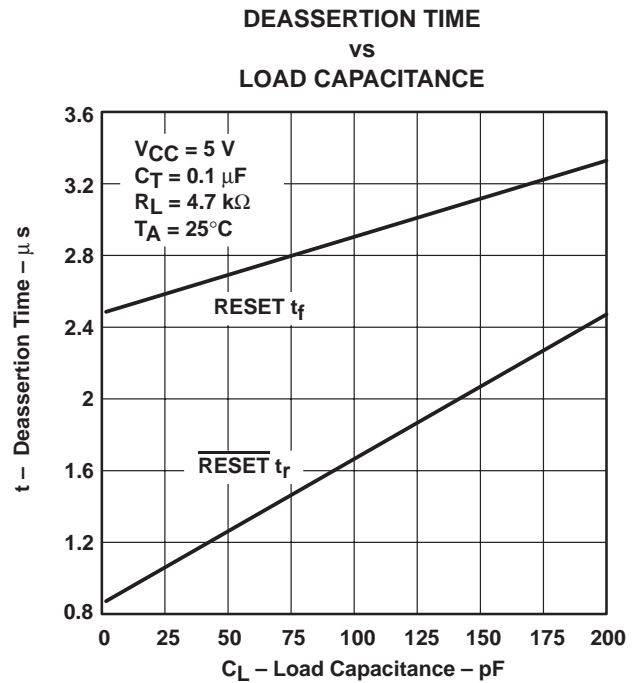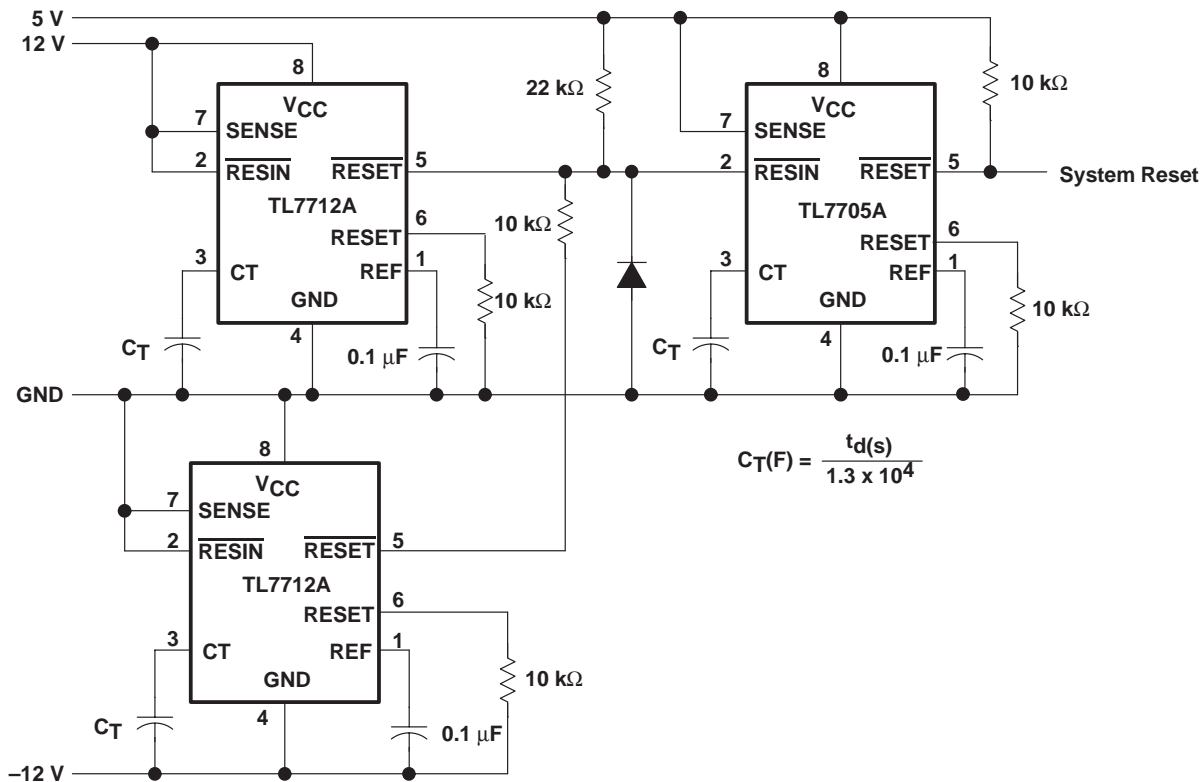### DEASSERTION TIME vs LOAD CAPACITANCE

Figure 5

† For proper operation both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

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APPLICATION INFORMATION

Figure 6. Multiple Power Supply System Reset Generation
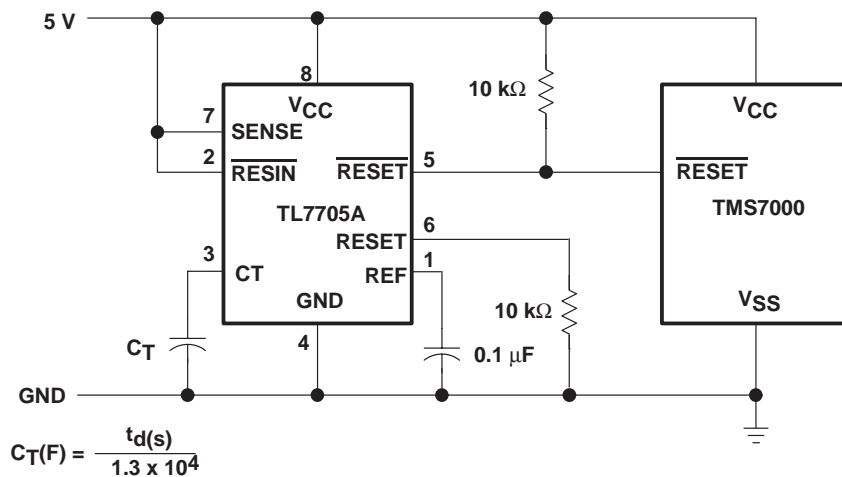
$$C_T(F) = \frac{t_{d(s)}}{1.3 \times 10^4}$$

Figure 7. Reset Controller for TMS7000 System

$$C_T(F) = \frac{t_{d(s)}}{1.3 \times 10^4}$$

Terminal numbers shown are for the D, JG, and P packages.

APPLICATION INFORMATION

Figure 8. Eliminating Undefined States Using a P-Channel JFET

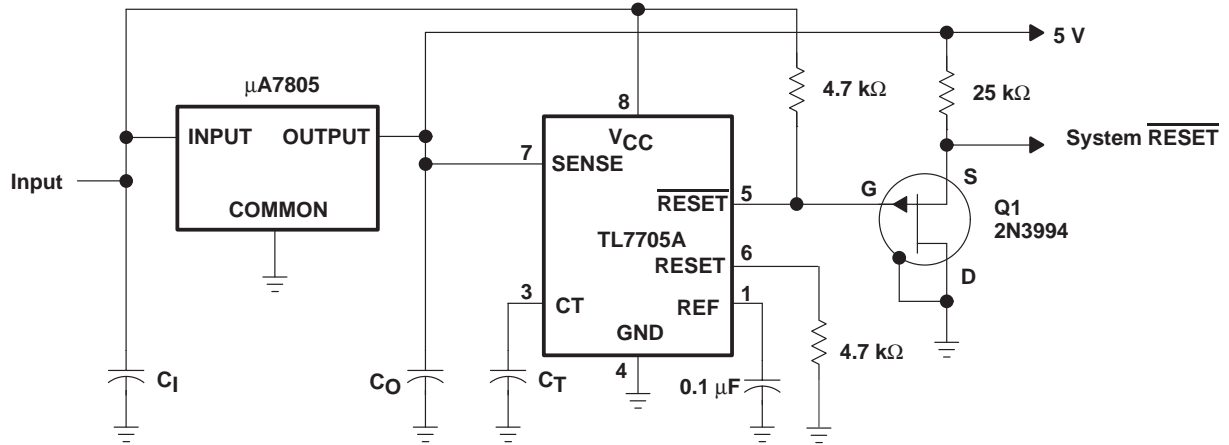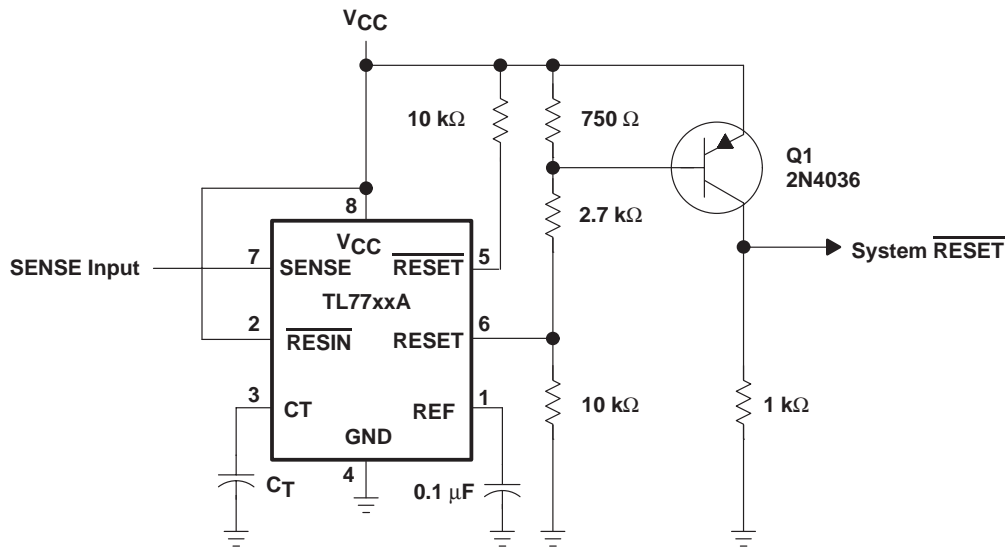**Figure 9. Eliminating Undefined States Using a pnp Transistor**

Terminal numbers shown are for the D, JG, and P packages.

MECHANICAL DATA

D (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN
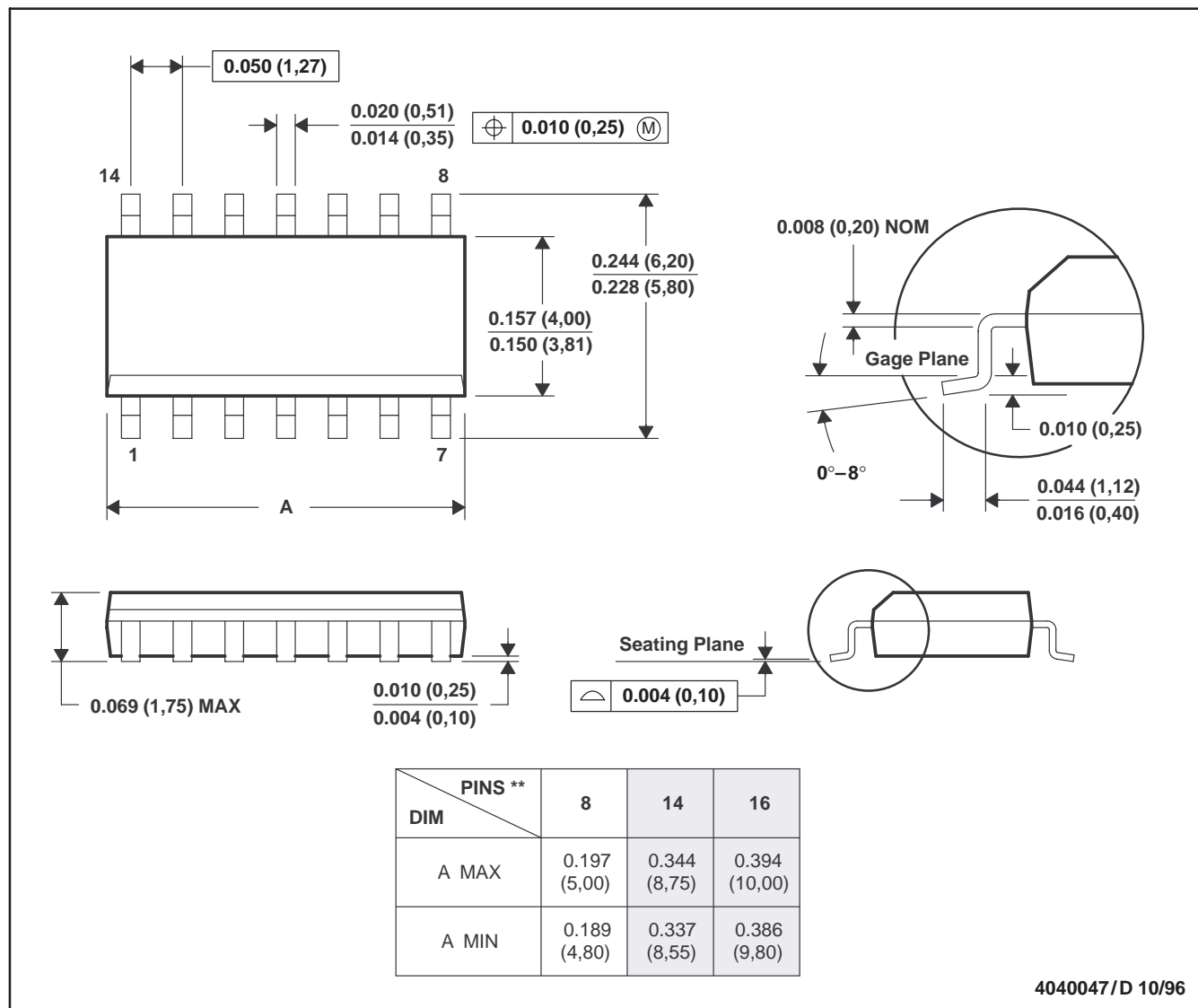
	PINS **	8	14	16
DIM				
A MAX		0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN		0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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MECHANICAL DATA

FK (S-CQCC-N)**   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

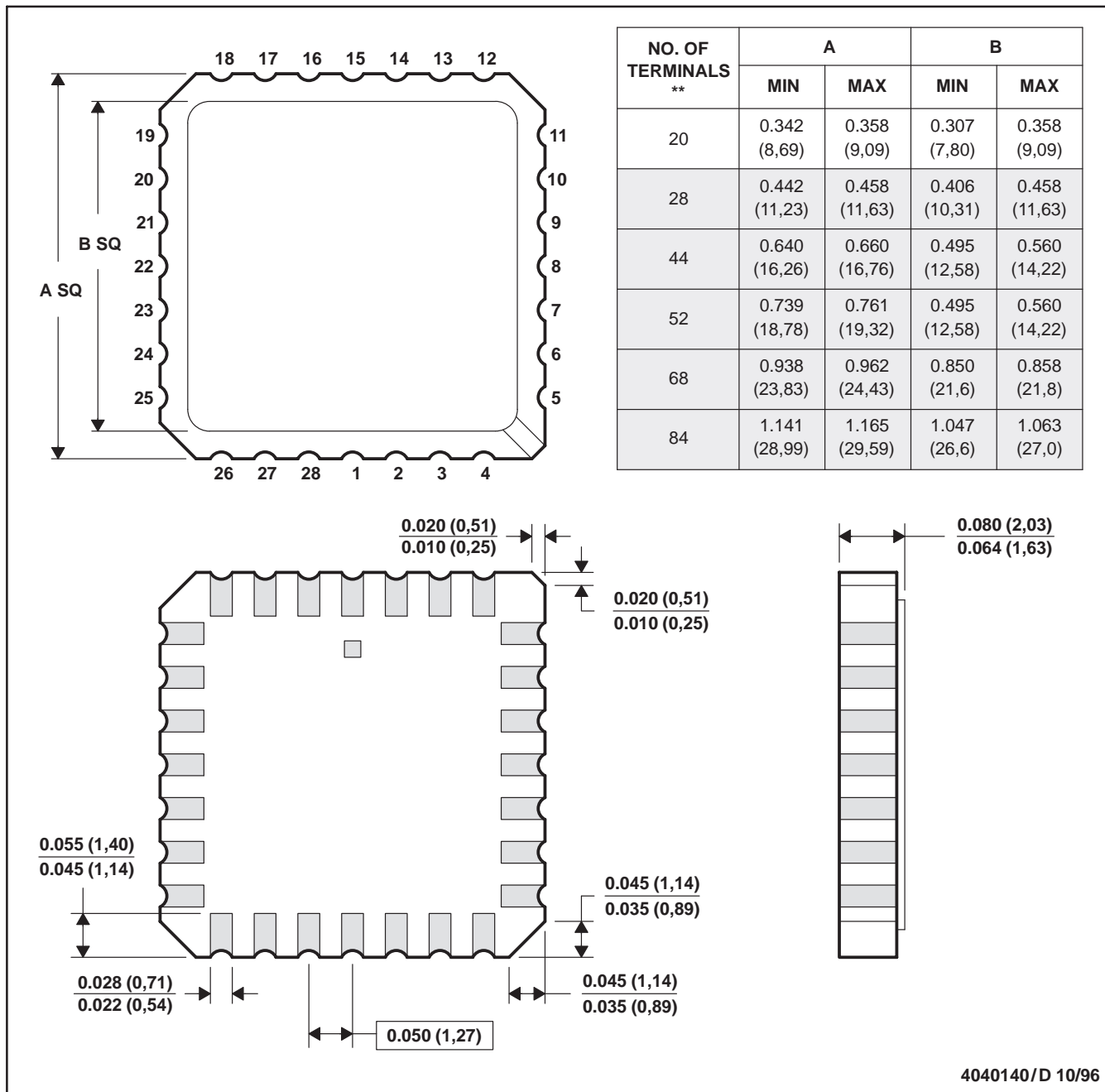| NO. OF TERMINALS **	A		B	
	MIN	**MAX**	**MIN**	**MAX**
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
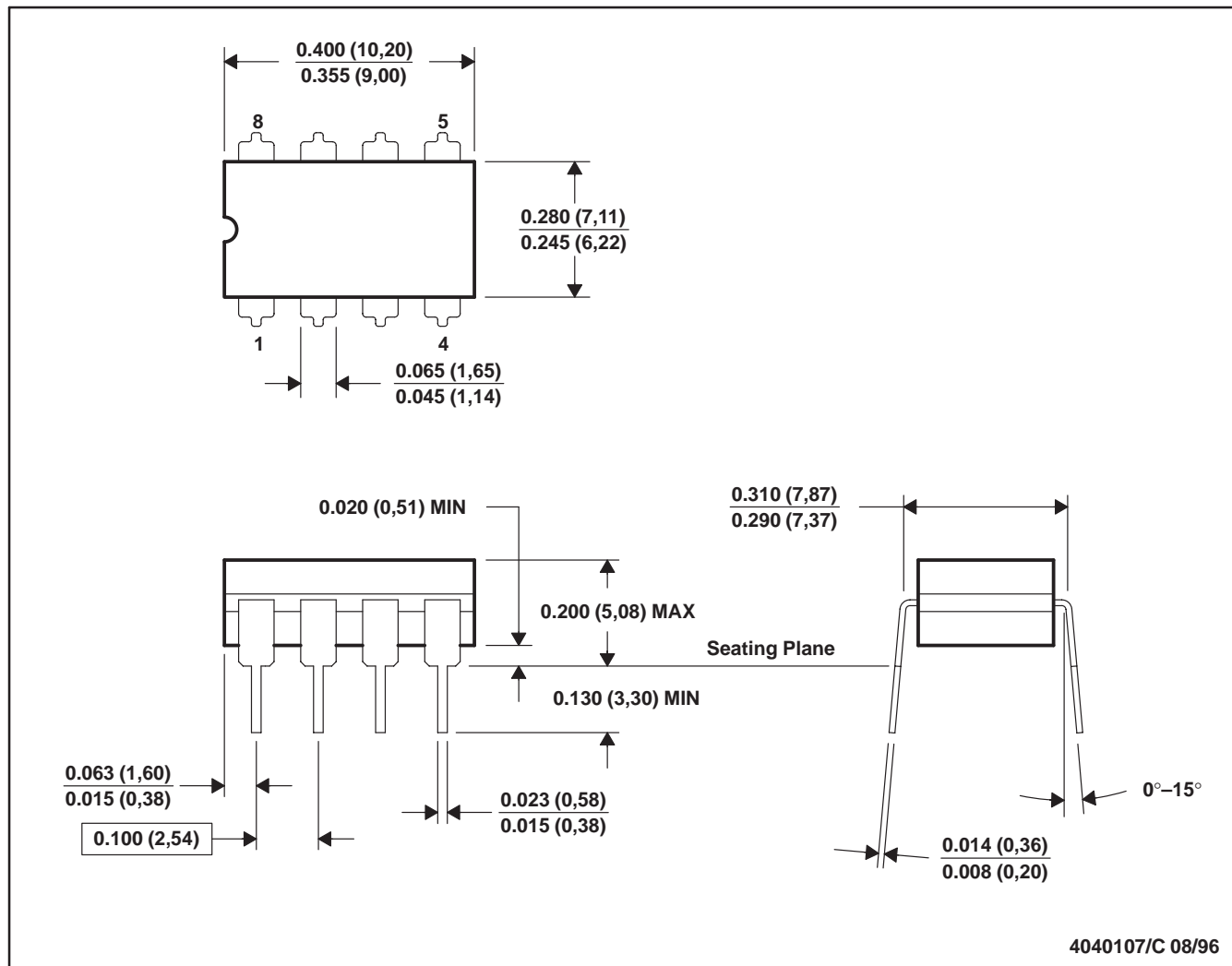E. Falls within JEDEC MS-004

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MECHANICAL DATA

JG (R-GDIP-T8)   **CERAMIC DUAL-IN-LINE PACKAGE**

$$\frac{0.400\ (10,20)}{0.355\ (9,00)}$$

8   5

$$\frac{0.280\ (7,11)}{0.245\ (6,22)}$$

1   4

$$\frac{0.065\ (1,65)}{0.045\ (1,14)}$$

0.020 (0,51) MIN

0.200 (5,08) MAX

$$\frac{0.310\ (7,87)}{0.290\ (7,37)}$$

Seating Plane

0.130 (3,30) MIN

$$\frac{0.063\ (1,60)}{0.015\ (0,38)}$$

$$\frac{0.023\ (0,58)}{0.015\ (0,38)}$$

0.100 (2,54)

$$\frac{0.014\ (0,36)}{0.008\ (0,20)}$$

0°–15°

4040107/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
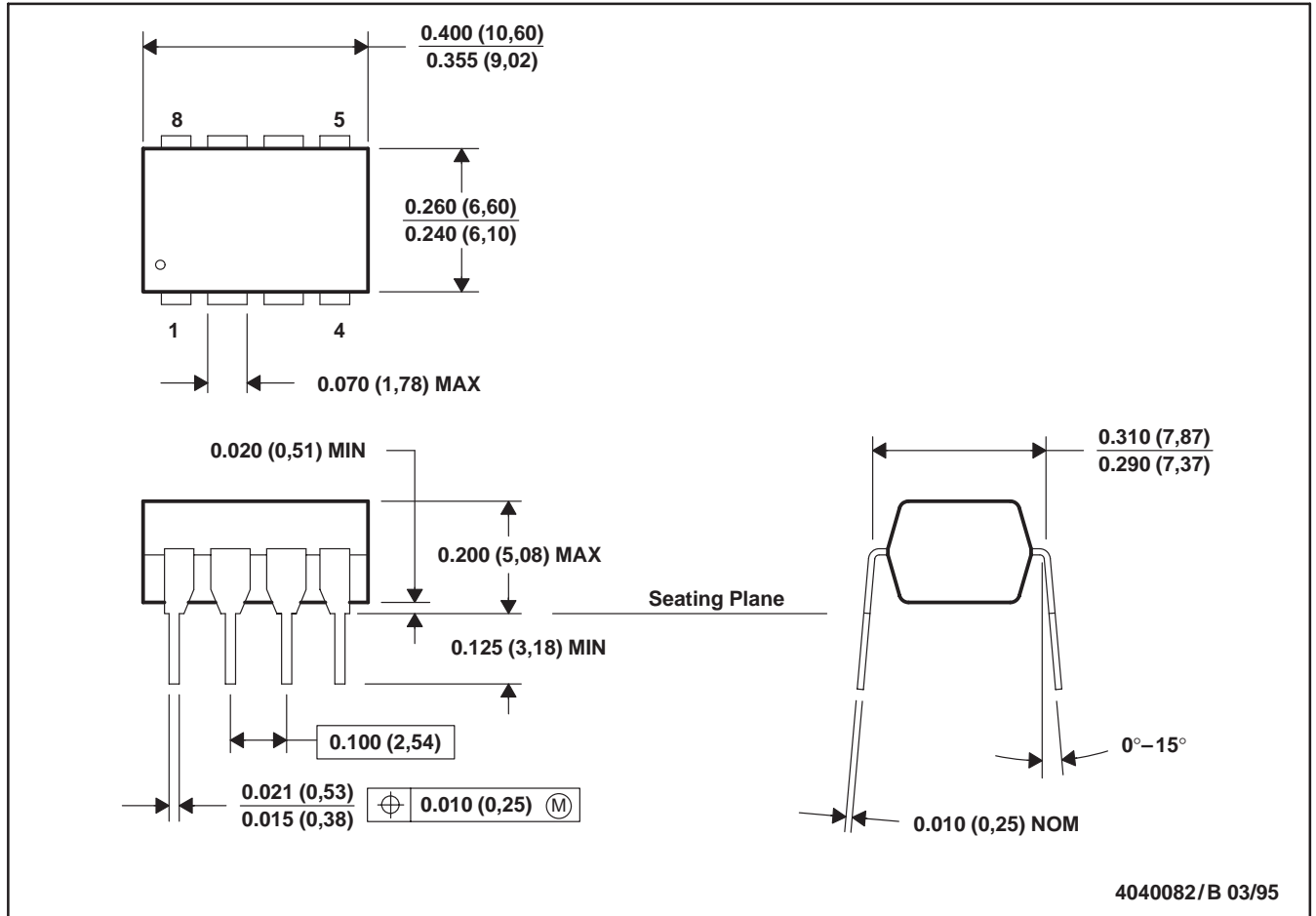   E. Falls within MIL-STD-1835 GDIP1-T8

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MECHANICAL DATA

P (R-PDIP-T8)   **PLASTIC DUAL-IN-LINE PACKAGE**

$$\frac{0.400\ (10,60)}{0.355\ (9,02)}$$

$$\frac{0.260\ (6,60)}{0.240\ (6,10)}$$

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$$\frac{0.021\ (0,53)}{0.015\ (0,38)}$$ ⊕ | 0.010 (0,25) Ⓜ

$$\frac{0.310\ (7,87)}{0.290\ (7,37)}$$

0°−15°

0.010 (0,25) NOM

4040082 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS-001

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