Lattice® Semiconductor Corporation

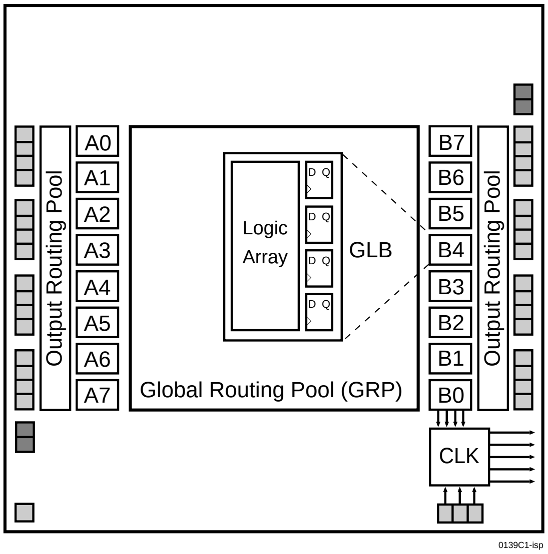
ispLSI® and pLSI® 1016E

High-Density Programmable Logic

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **2000 PLD Gates**
  - **32 I/O Pins, Four Dedicated Inputs**
  - **96 Registers**
  - **High-Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
- **HIGH-PERFORMANCE E^{2}CMOS® TECHNOLOGY**
  - **f_{max} = 125 MHz Maximum Operating Frequency**
  - **t_{pd} = 7.5 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **In-System Programmable (ISP™) 5-Volt Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Device for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **Superior Quality of Results**
  - **Tightly Integrated with Leading CAE Vendor Tools**
  - **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI and pLSI 1016E are High-Density Programmable Logic Devices containing 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins, one Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1016E features 5-Volt in-system programming and in-system diagnostic capabilities. The ispLSI 1016E offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1016E device, but multiplexes four input pins to control in-system programming. A functional superset of the ispLSI and pLSI 1016 architecture, the ispLSI and pLSI 1016E devices add a new global output enable pin.

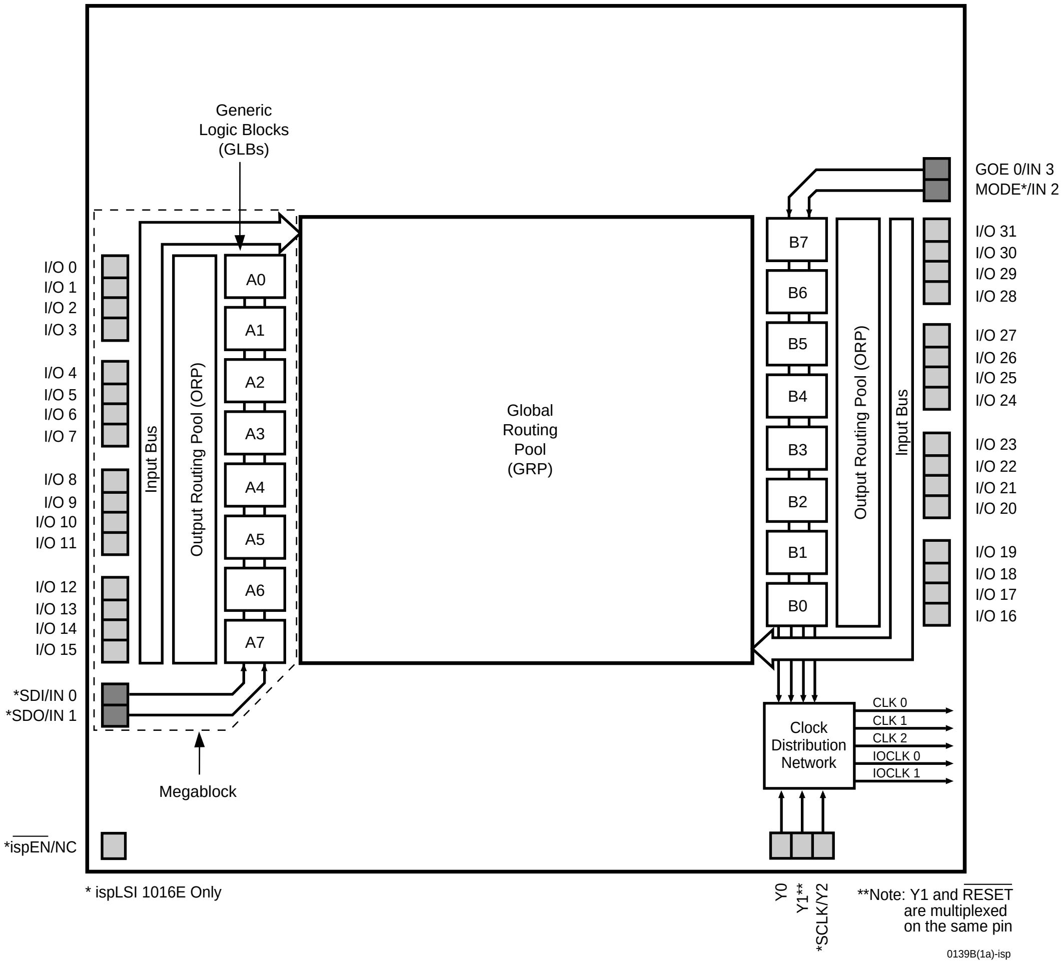
The basic unit of logic on the ispLSI and pLSI 1016E devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1...B7 (see Figure 1). There are a total of 16 GLBs in the ispLSI and pLSI 1016E devices. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

October 1998

Functional Block Diagram

Figure 1. ispLSI and pLSI 1016E Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI and pLSI 1016E device contains two Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1016E devices are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the ispLSI and pLSI 1016E devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} .... -0.5 to +7.0V

Input Voltage Applied........................ -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature................................ -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{cc}+1	V

Table 2-0005/1016E

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance (Commercial/Industrial)	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	12	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

Table 2-0006/1016E

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008/1016E

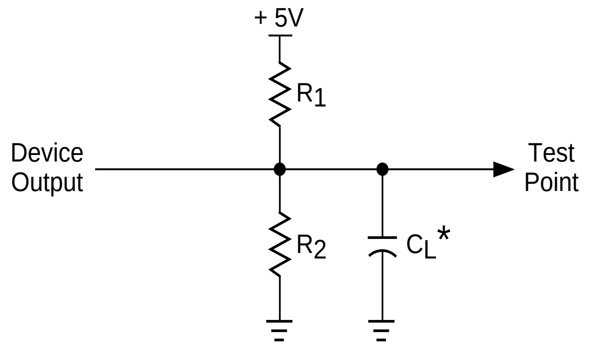
Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	-100, -80	≤ 3 ns
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See Figure 2	

Table 2-0003/1016E

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*CL includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004/1016E

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{\text{ispEN}}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	90	–	mA
		f_{CLOCK} = 1 MHz	Industrial	–	90	–	mA

Table 2-0007/1016E

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC}= 5V and T_A= 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC} .

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-125		-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Prop. Delay, Worst Case Path	–	10.0	–	13.0	–	18.5	ns
f_{max}	A	3	Clk. Frequency with Int. Feedback[3]	125	–	100	–	84.0	–	MHz
f_{max} (Ext.)	–	4	Clk. Frequency with Ext. Feedback$\left(\frac{1}{t_{su2} + t_{co1}}\right)$	100	–	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clk. Frequency, Max. Toggle$\left(\frac{1}{t_{wh} + t_{w1}}\right)$	167	–	125	–	100	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clk., 4 PT Bypass	5.0	–	7.0	–	8.5	–	ns
t_{co1}	A	7	GLB Reg. Clk. to Output Delay, ORP Bypass	–	4.5	–	5.0	–	8.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clk., 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clk.	5.5	–	8.0	–	9.5	–	ns
t_{co2}	–	10	GLB Reg. Clk. to Output Delay	–	5.5	–	6.0	–	9.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clk.	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	12.0	–	15.0	–	20.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	12.0	–	15.0	–	20.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	9.0	–	10.5	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	9.0	–	10.5	ns
t_{wh}	–	18	Ext. Sync. Clk. Pulse Duration, High	3.0	–	4.0	–	5.0	–	ns
t_{wl}	–	19	Ext. Sync. Clk. Pulse Duration, Low	3.0	–	4.0	–	5.0	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync. Clk. (Y2, Y3)	3.0	–	3.5	–	4.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clk. (Y2, Y3)	0.0	–	0.0	–	0.0	–	ns

Table 2-0030-16/125,100, 80

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-125		-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	22	I/O Register Bypass	–	0.3	–	0.4	–	0.6	ns
t_{iolat}	23	I/O Latch Delay	–	1.8	–	2.4	–	3.6	ns
t_{iosu}	24	I/O Register Setup Time before Clock	3.0	–	3.5	–	4.5	–	ns
t_{ioh}	25	I/O Register Hold Time after Clock	-0.3	–	-0.4	–	-0.6	–	ns
t_{ioco}	26	I/O Register Clock to Out Delay	–	4.0	–	5.0	–	7.5	ns
t_{ior}	27	I/O Register Reset to Out Delay	–	4.0	–	5.0	–	7.5	ns
t_{din}	28	Dedicated Input Delay	–	2.2	–	2.6	–	3.9	ns
GRP									
t_{grp1}	29	GRP Delay, 1 GLB Load	–	1.8	–	1.9	–	2.9	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	–	1.9	–	2.2	–	3.3	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	–	2.1	–	2.5	–	3.8	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	–	2.4	–	3.1	–	4.7	ns
GLB									
t_{4ptbpc}	34	4 Product Term Bypass Path Delay (Combinatorial)	–	3.9	–	5.7	–	8.1	ns
t_{4ptbpr}	35	4 Product Term Bypass Path Delay (Registered)	–	3.9	–	5.6	–	7.3	ns
t_{1ptxor}	36	1 Product Term/XOR Path Delay	–	4.4	–	6.1	–	7.1	ns
$t_{20ptxor}$	37	20 Product Term/XOR Path Delay	–	4.4	–	6.1	–	8.2	ns
t_{xoradj}	38	XOR Adjacent Path Delay[3]	–	4.4	–	6.6	–	8.3	ns
t_{gbp}	39	GLB Register Bypass Delay	–	1.0	–	1.6	–	1.9	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.2	–	0.2	–	-0.6	–	ns
t_{gh}	41	GLB Register Hold Time after Clock	1.5	–	2.5	–	4.3	–	ns
t_{gco}	42	GLB Register Clock to Output Delay	–	1.8	–	1.9	–	2.9	ns
t_{gro}	43	GLB Register Reset to Output Delay	–	4.4	–	6.3	–	7.0	ns
t_{ptre}	44	GLB Product Term Reset to Register Delay	–	3.5	–	5.1	–	7.2	ns
t_{ptoe}	45	GLB Product Term Output Enable to I/O Cell Delay	–	5.5	–	7.1	–	9.7	ns
t_{ptck}	46	GLB Product Term Clock Delay	3.2	3.5	4.8	5.3	6.8	7.5	ns
ORP									
t_{orp}	47	ORP Delay	–	1.0	–	1.0	–	1.5	ns
t_{orpbp}	48	ORP Bypass Delay	–	0.0	–	0.0	–	0.0	ns

Table 2-0036-16/125,100, 80

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice hard macros.

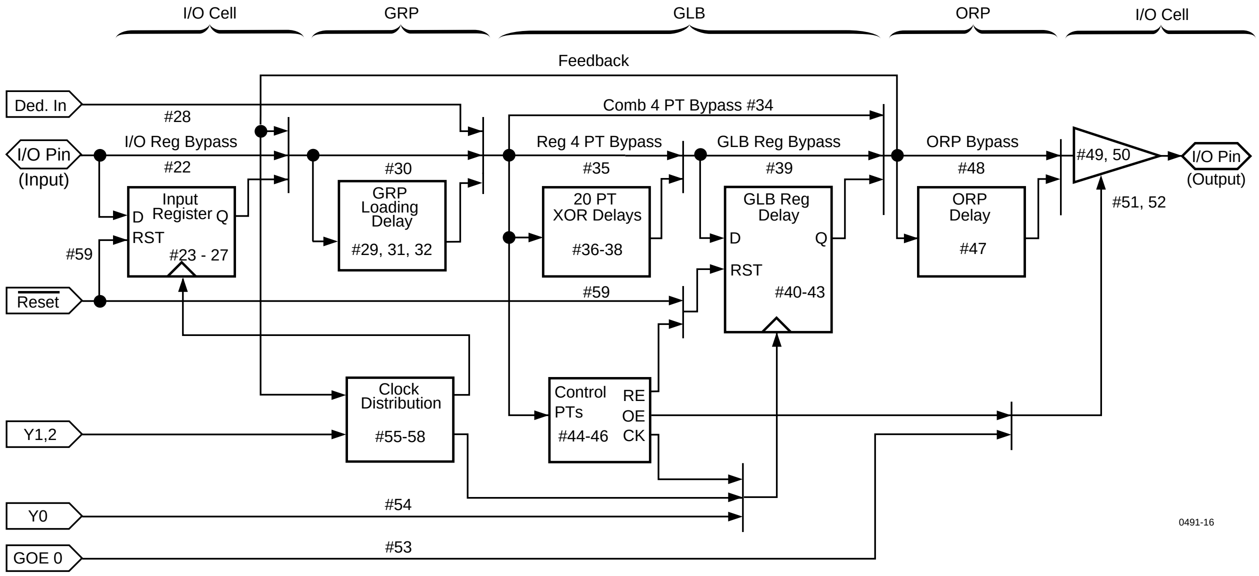
Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-125		-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	49	Output Buffer Delay	–	1.4	–	1.7	–	3.0	ns
t_{sl}	50	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	10.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	4.3	–	5.3	–	6.4	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	4.3	–	5.3	–	6.4	ns
t_{goe}	53	Global Output Enable	–	2.7	–	3.7	–	4.1	ns
Clocks									
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.3	1.3	1.4	1.4	2.1	2.1	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.7	2.4	2.9	3.6	4.4	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	1.2	2.7	ns
$t_{ioy1/2}$	57	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	0.0	0.3	0.0	0.4	0.0	0.6	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	1.8	0.8	1.8	1.2	2.7	ns
Global Reset									
t_{gr}	59	Global Reset to GLB and I/O Registers	–	3.2	–	4.5	–	5.5	ns

Table 2-0037-16/125,100,80

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1016E Timing Model



Derivations of **t**su, **t**h and **t**co from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp4 + **t**ptck(min))
= (#22 + #30 + #37) + (#40) - (#22 + #30 + #46)
1.4 ns = (0.3 + 1.9 + 4.4) + (0.2) - (0.3 + 1.9 + 3.2)

th = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
0.6 ns = (0.3 + 1.9 + 3.5) + (1.5) - (0.3 + 1.9 + 4.4)

tco = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#22 + #30 + #46) + (#42) + (#47 + #49)
9.9 ns = (0.3 + 1.9 + 3.5) + (1.8) + (1.0 + 1.4)

Derivations of **t**su, **t**h and **t**co from the Clock GLB[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**gy0(min) + **t**gco + **t**gcp(min))
= (#22 + #30 + #37) + (#40) - (#54 + #42 + #56)
2.9 ns = (0.3 + 1.9 + 4.4) + (0.2) - (1.3 + 1.8 + 0.8)

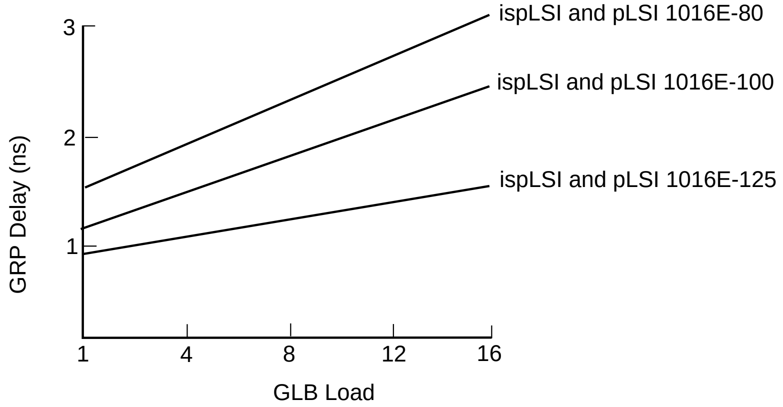
th = Clock (max) + Reg h - Logic
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
= (#54 + #42 + #56) + (#41) - (#22 + #30 + #37)
-0.2 ns = (1.3 + 1.8 + 1.8) + (1.5) - (0.3 + 1.9 + 4.4)

tco = Clock (max) + Reg co + Output
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#54 + #42 + #56) + (#42) + (#47 + #49)
9.1 ns = (1.3 + 1.8 + 1.8) + (1.8) + (1.0 + 1.4)

Table 2-0042-16

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1016E-125

Maximum GRP Delay vs GLB Loads

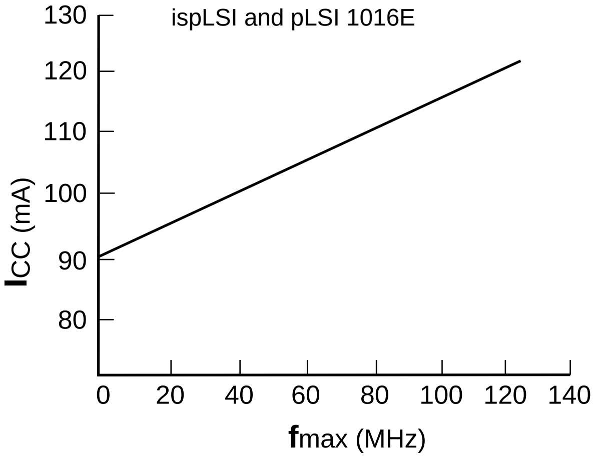


16E GRP/GLB.eps

Power Consumption

Power Consumption in the ispLSI and pLSI 1016E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of four 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1016E using the following equation:

I_{CC}(mA) = 23 + (# of PTs * 0.52) + (# of nets * max freq * 0.004)

Where:
- # of PTs = Number of product terms used in design
- # of nets = Number of signals used in device
- Max freq = Highest clock frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of four GLB loads on average exists and the device is filled with four 16-bit counters. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127B-16-80-isp/1016

Pin Description

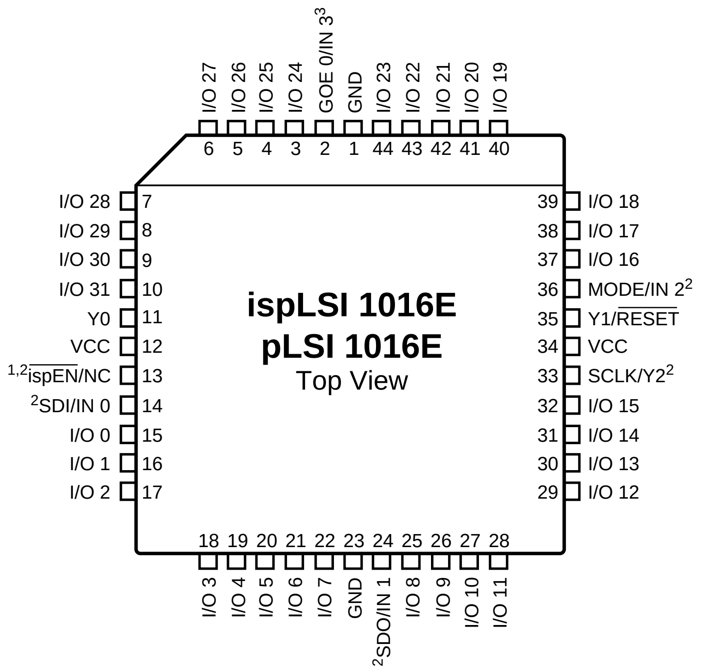
NAME	PLCC PIN NUMBERS	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0/IN 3[3]	2	40	This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin.
$\overline{\text{ispEN}}$/NC[1,2]	13	7	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI/IN 0[2]	14	8	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.SDI/IN0 also is used as one of the two control pins for the isp state machine.
MODE/IN 2[2]	36	30	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SDO/IN 1[2]	24	18	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SCLK/Y2[2]	33	27	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
Y0	11	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35	29	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND	1, 23	17, 39	Ground (GND)
VCC	12, 34	6, 28	Vcc

Table 2-0002C-16-isp

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability for ispLSI 1016E only.
3. Pins have dual function capability which is software selectable.

Pin Configurations

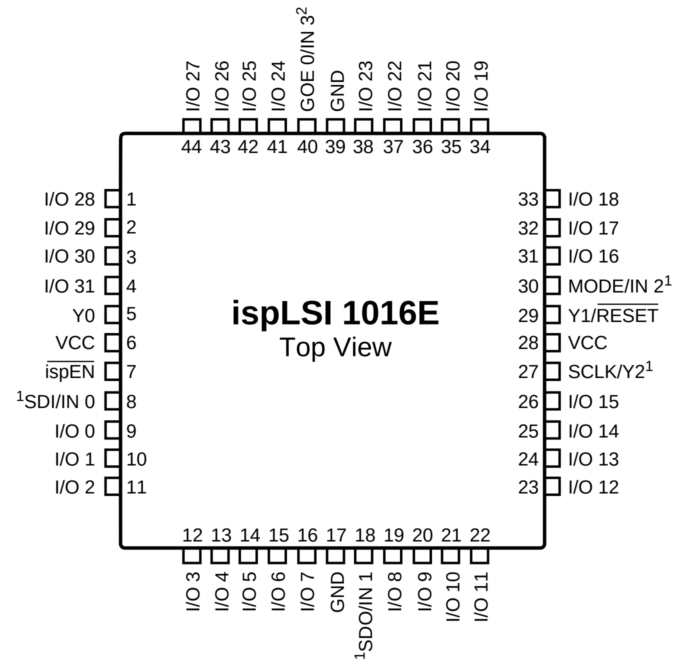
ispLSI and pLSI 1016E 44-Pin PLCC Pinout Diagram



1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability for ispLSI 1016E only (except pin 13, which is ispEN only).
3. Pins have dual function capability which is software selectable.

0123A-isp1016

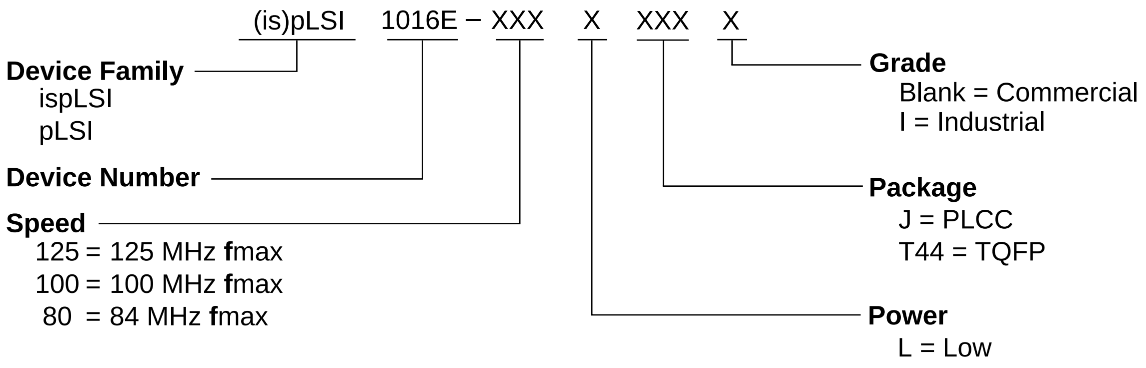
ispLSI 1016E 44-Pin TQFP Pinout Diagram



1. Pins have dual function capability.
2. Pins have dual function capability which is software selectable.

0851-16E/TQFP

Part Number Description



Device Family
ispLSI
pLSI

Device Number

Speed
125 = 125 MHz **f**max
100 = 100 MHz **f**max
80 = 84 MHz **f**max

Grade
Blank = Commercial
I = Industrial

Package
J = PLCC
T44 = TQFP

Power
L = Low

0212/1016E

ispLSI and pLSI 1016E Ordering Information

COMMERCIAL

FAMILY	**f**max (MHz)	**t**pd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 1016E-125LJ	44-Pin PLCC
	125	7.5	ispLSI 1016E-125LT44	44-Pin TQFP
	100	10	ispLSI 1016E-100LJ	44-Pin PLCC
	100	10	ispLSI 1016E-100LT44	44-Pin TQFP
	84	15	ispLSI 1016E-80LJ	44-Pin PLCC
	84	15	ispLSI 1016E-80LT44	44-Pin TQFP
pLSI	125	7.5	pLSI 1016E-125LJ	44-Pin PLCC
	100	10	pLSI 1016E-100LJ	44-Pin PLCC
	84	15	pLSI 1016E-80LJ	44-Pin PLCC

Table 2-0041A/1016E

INDUSTRIAL

FAMILY	**f**max (MHz)	**t**pd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	84	15	ispLSI 1016E-80LJI	44-Pin PLCC
	84	15	ispLSI 1016E-80LT44I	44-Pin TQFP

Table 2-0041B/1016E