1000EA Family Architectural Description

Introduction

The ispLSI® 1000EA Family of High Density Programmable Logic devices includes the 1016EA, 1024EA, 1032EA and 1048EA. Each member of the family offers internal registers, input registers, Universal I/O pins, dedicated input pins, dedicated clock inputs and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1000EA Family of devices feature 5 volt JTAG In-System Programming (ISP™) and in-system diagnostic capabilities via the IEEE 1149.1 Test Access Port. The ispLSI 1000EA Family offer non-volatile re-programmability of the logic as well as the interconnects to provide truly reconfigurable systems. Each output pin has optional slow slew and open-drain configurations.

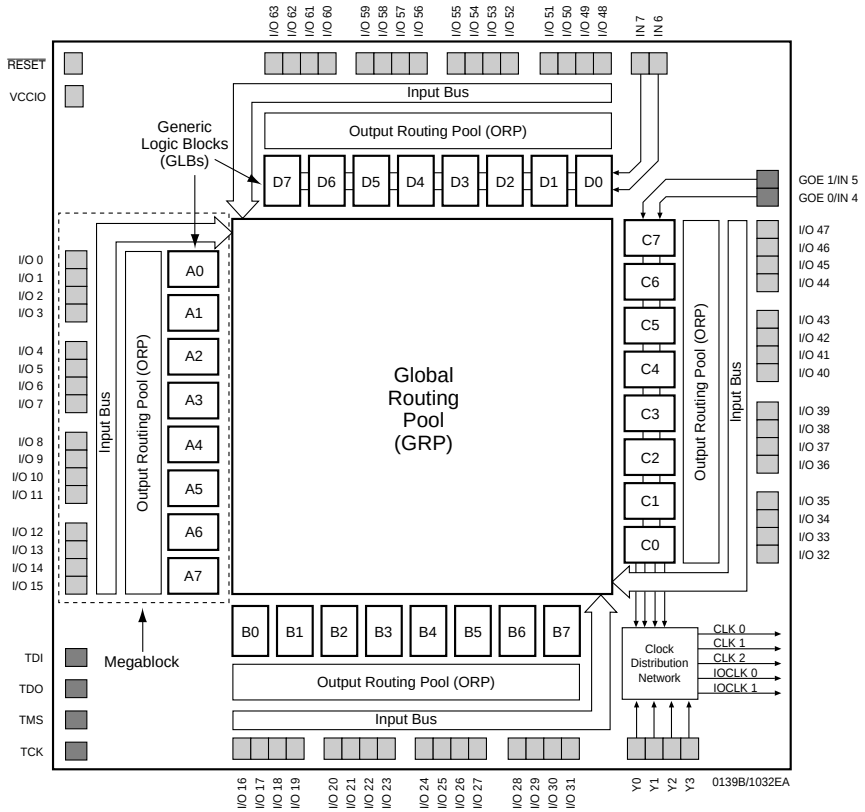
The basic unit of logic for the ispLSI families is the Generic Logic Block (GLB). Figure 1 illustrates the ispLSI 1032EA with its 32 GLBs labeled A0, A1 .. D7. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs, which can be configured to be either combinatorial or registered. Inputs to the GLB come from the Global Routing Pool (GRP) and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

As an example, the ispLSI 1032EA has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bidirectional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages.

The I/O cells are grouped into sets of 16 as shown in Figure 1. Each of these I/O groups is associated with a Megablock through the use of the Output Routing Pool (ORP).

Eight GLBs, 16 I/O cells, one ORP and two dedicated inputs are connected together to make a Megablock. The

Figure 1. ispLSI 1032EA Functional Block Diagram



outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each Megablock can generate one common Product Term Output Enable (PTOE) signal. The ispLSI 1032EA device, shown in Figure 1, contains four Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the devices are selected using the Clock Distribution Network. The dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five outputs (CLK 0, CLK1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special GLB (C0 on the ispLSI 1032EA devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

All ispLSI 1000EA family members are 100% IEEE 1149.1 Boundary Scan Testable through the Boundary Scan Test Access Port (TAP).

Generic Logic Block

The Generic Logic Block (GLB) is the standard logic block of Lattice's high density ispLSI devices. A GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections: the AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions (see Figure 2). The AND array consists of 20 product terms, which can produce the logical product of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the GLBs or inputs from the external I/O cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes Boolean logic reduction more efficient.

The PTSA takes the 20 product terms and routes them to the four GLB outputs. There are four OR gates, with four, four, five and seven product terms each (see Figure 2). The output of any of these OR gates can be routed to any of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. In

Figure 2. GLB: Product Term Sharing Array Example

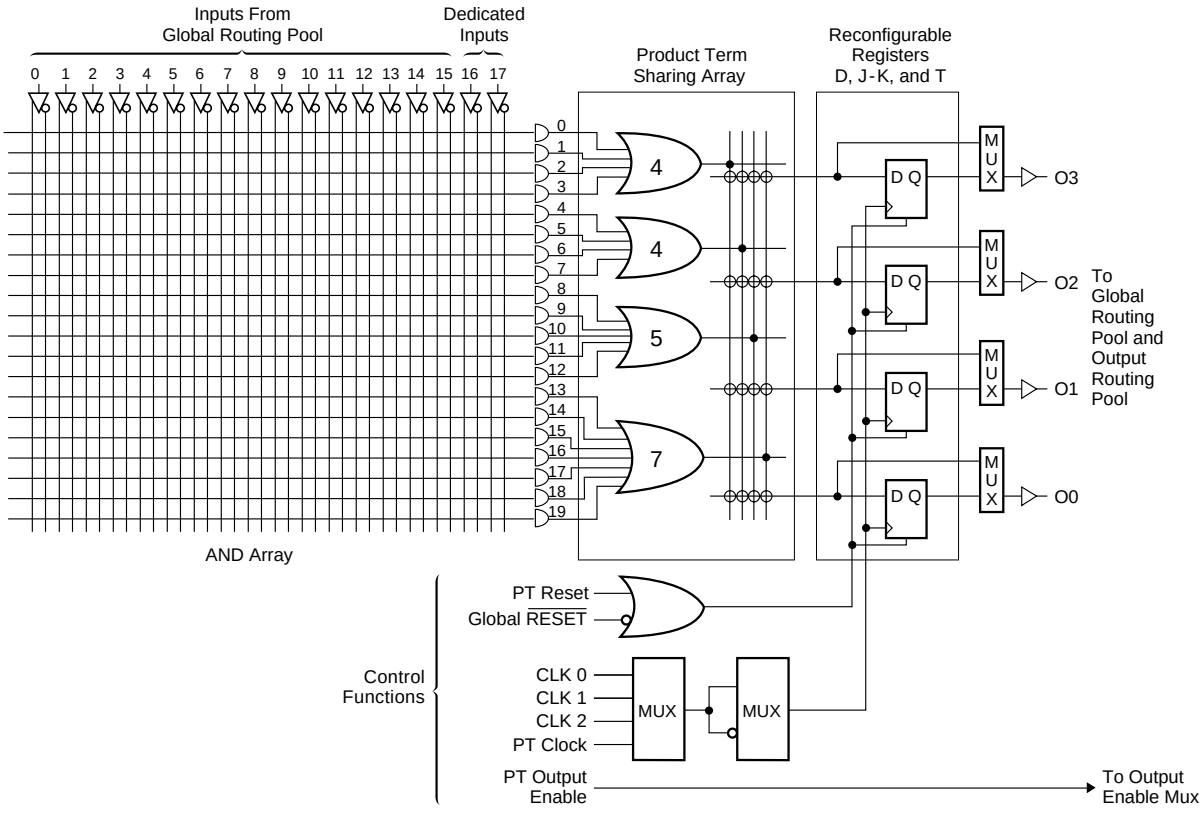


Figure 3. GLB: Four Product Term Bypass Example

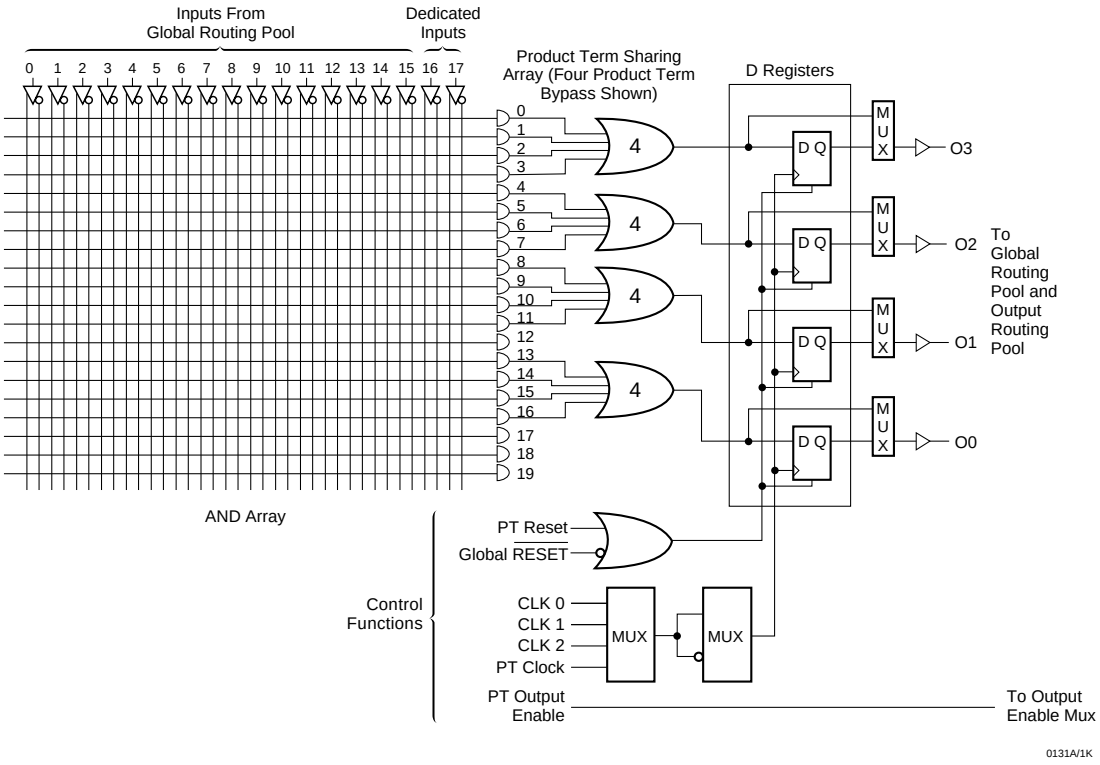
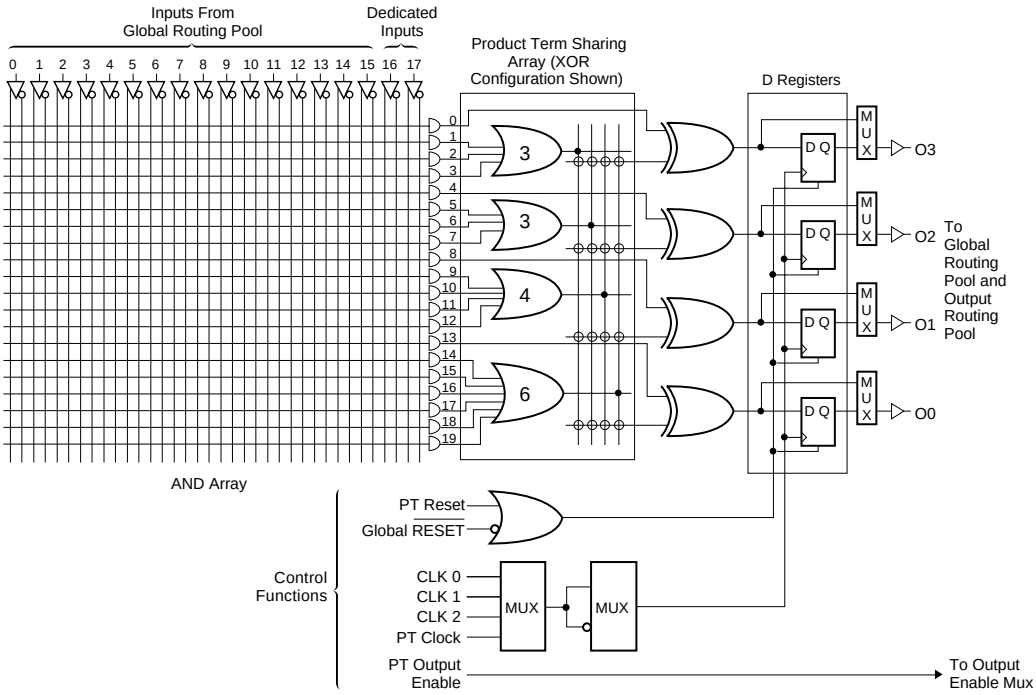


Figure 4. GLB: XOR Gate Example



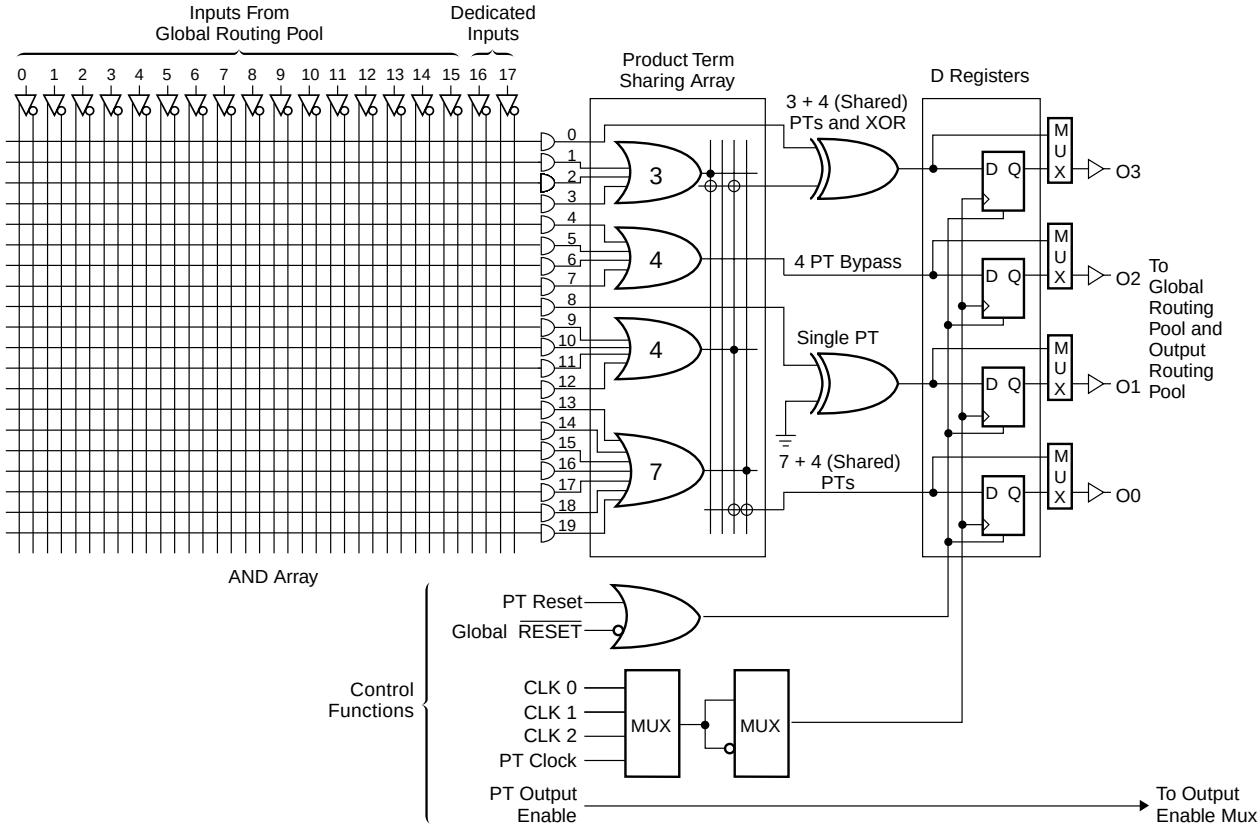
addition, the PTSA can share product terms similar to an FPLA device. If the user's main concern is speed, the PTSA can use a bypass circuit which provides four product terms to each output, to increase the performance of the cell (see Figure 3). This can be done to any or all of the four outputs from the GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop (see Figure 4). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used.

The PTSA is flexible enough to allow these features to be used in virtually any combination that the user desires. In the GLB shown in Figure 5, Output Three (O3) is configured using the XOR gate while Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of 11 (7+4).

Various signals that control the operation of the GLB outputs are driven from the Control Functions (see Figure 5). The clock for the registers can come from any of three sources developed in the Clock Distribution Network (see Clock Distribution Network section) or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin ($\overline{\text{RESET}}$) or from a product term within the GLB. The global reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to a logic 0 state. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block. Use of a product term for

Figure 5. GLB: Mixed Mode Configuration Example



a control function makes that product term unavailable for use as a logic term. Refer to the Product Term Sharing Matrix (Table 1) to determine which logic functions are affected.

There are many additional features in a GLB that allow implementation of logic intensive functions. These features are accessible using the Hard Macros from the software and require no intervention on the part of the user.

Product Term Sharing Matrix

This matrix describes how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four product term bypass mode. When GLB output one is used in the XOR mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

The Megablock

A Megablock consists of eight GLBs, an ORP, 16 I/O cells, two dedicated inputs and a common product term OE. These elements are coupled together as shown in Figure 6. The various members of the ispLSI 1000EA family combine from one to six Megablocks on a single device (see Table 2).

For the ispLSI 1000EA family, the eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. The pins are dedicated (non-registered) inputs only. The product term OE signal is generated within the Megablock. The OE signal can be generated using a product term (PT19) in any of eight GLBs within the Megablock. See Output Enable Control section for further details.

Because of the shared logic within the Megablock, signals that share a common function (counters, busses, etc.) should be grouped within a Megablock. This will allow the user to obtain the best utilization of the logic within the device and eliminate routing bottlenecks.

Table 1. Product Term Sharing Matrix

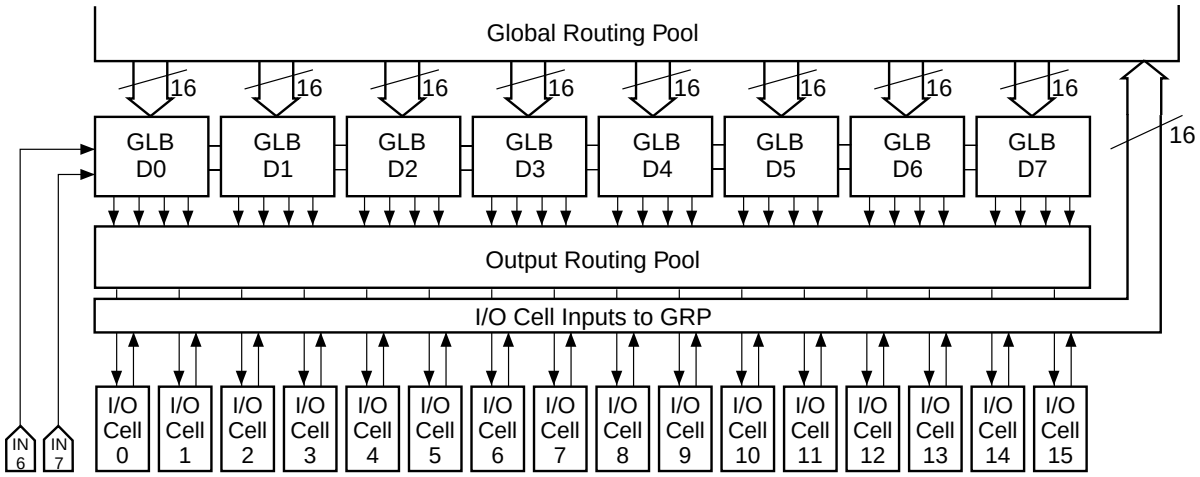
Product Term #	Standard Configuration Output Number				Four Product Term Bypass Output Number				Single Product Term Output Number				XOR Function Output Number								Alternate Function
	3	2	1	0	3	2	1	0	3	2	1	0	3	3	2	2	1	1	0	0	
0	■	■	■	■	■				■				■								
1	■	■	■	■	■									■							
2	■	■	■	■	■									■							
3	■	■	■	■	■									■							
4	■	■	■	■		■				■					■						
5	■	■	■	■		■										■					
6	■	■	■	■		■										■					
7	■	■	■	■		■										■					
8	■	■	■	■			■				■						■				
9	■	■	■	■			■											■			
10	■	■	■	■			■											■			
11	■	■	■	■			■											■			
12	■	■	■	■														■			■CLK/Reset
13	■	■	■	■				■				■							■		
14	■	■	■	■				■												■	
15	■	■	■	■				■												■	
16	■	■	■	■				■												■	
17	■	■	■	■																■	
18	■	■	■	■																■	
19	■	■	■	■																■	■ OE/Reset

Table 2. Device Resources

ispLSI Device	Megablocks	GLBs	I/O Cells	Dedicated Inputs
1016EA	2	16	32	1
1024EA	3	24	48	2
1032EA	4	32	64	4
1048EA	6	48	96	8

Table 2-0051/1K

Figure 6. The Megablock Block Diagram



Input Routing

Signal inputs are handled in two ways within the device. First, each I/O cell within the device has its input routed directly to the GRP. This gives every GLB within the device access to each I/O cell input. Second, each Megablock has two dedicated inputs which are directly routed to the eight GLBs within the Megablock. Both input paths are shown in Figure 6.

The Output Routing Pool

The ORP routes signals from the GLB outputs to I/O cells configured as outputs or bidirectional pins (see Figure 7). The purpose of the ORP is to allow greater flexibility when assigning I/O pins. It also simplifies the job for the routing software which results in a higher degree of utilization.

By examining the ORP in Figure 7, it can be seen that a GLB output can be connected to one of four I/O cells. Further flexibility is provided by using the PTSA (Figures 2 through 5) which makes the GLB outputs completely interchangeable. This allows the routing program to freely interchange the outputs to achieve the best routability. This is an automatic process and requires no intervention on the part of the user.

The ORP bypass connections (see Figure 8) further increase the flexibility of the device. The ORP bypass connects specific GLB outputs to specific I/O cells at a faster speed. The bypass path tends to restrict the routability of the device and should only be used for critical signals.

I/O Cell

The I/O cell (see Figure 9) is used to route input, output or bidirectional signals connected to the I/O pin. One logic input comes from the ORP, and the other comes from the faster ORP bypass (see Figure 9). A pair of multiplexers select which signal will be used, and its polarity.

The Output Enable can be set to a logic high (enabled) when an output pin is desired, or logic low (disabled) when an input pin is needed. The Global Reset ($\overline{\text{RESET}}$) signal is driven by the active low chip reset pin. The Global Reset pin is always connected to all GLB and I/O registers. Each I/O cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). The clock signals are generated by the Clock Distribution Network.

Figure 7. Output Routing Pool

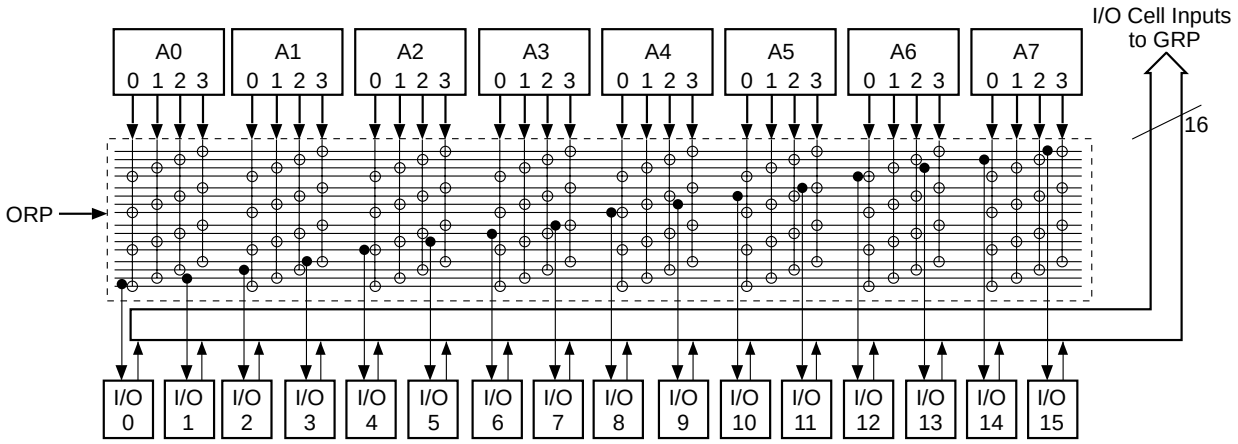
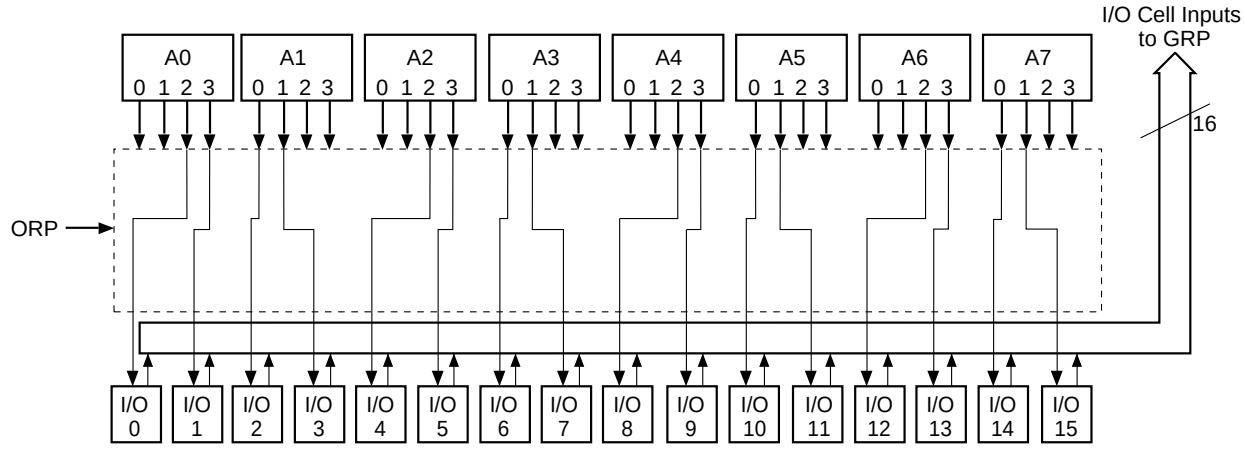


Figure 8. Output Routing Pool Showing Bypass



Using the multiplexers, the I/O cell can be configured as an input, an output, a 3-stated output or a bidirectional I/O. The D-type register can be configured as a level sensitive transparent latch or an edge triggered flip-flop to store the incoming data. Figure 10 illustrates some of the various I/O cell configurations possible.

In addition to the standard totem-pole output configuration, each output can be programmed as an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up resistance. The default configuration for the output driver is the totem-pole configuration.

Each output can be programmed independently with a slow or fast slew rate. In order to minimize output switching noise, the slow slew option should be used. The default slew rate for all output pins is fast slew.

A VCCIO pin is available which must be connected to a common 5 or 3.3 volt power supply so the output levels can be matched to 5 or 3.3 compatible voltages. VCCIO is common to all the I/O cells and the user applied VCCIO voltage on the pin determines the I/O voltage reference for the entire device. When VCCIO is set to 3.3 volts, the output can source 2 mA and sink 8 mA. When VCCIO is set to 5 volts the outputs can source 4 mA and sink 8 mA.

Figure 9. I/O Cell Architecture

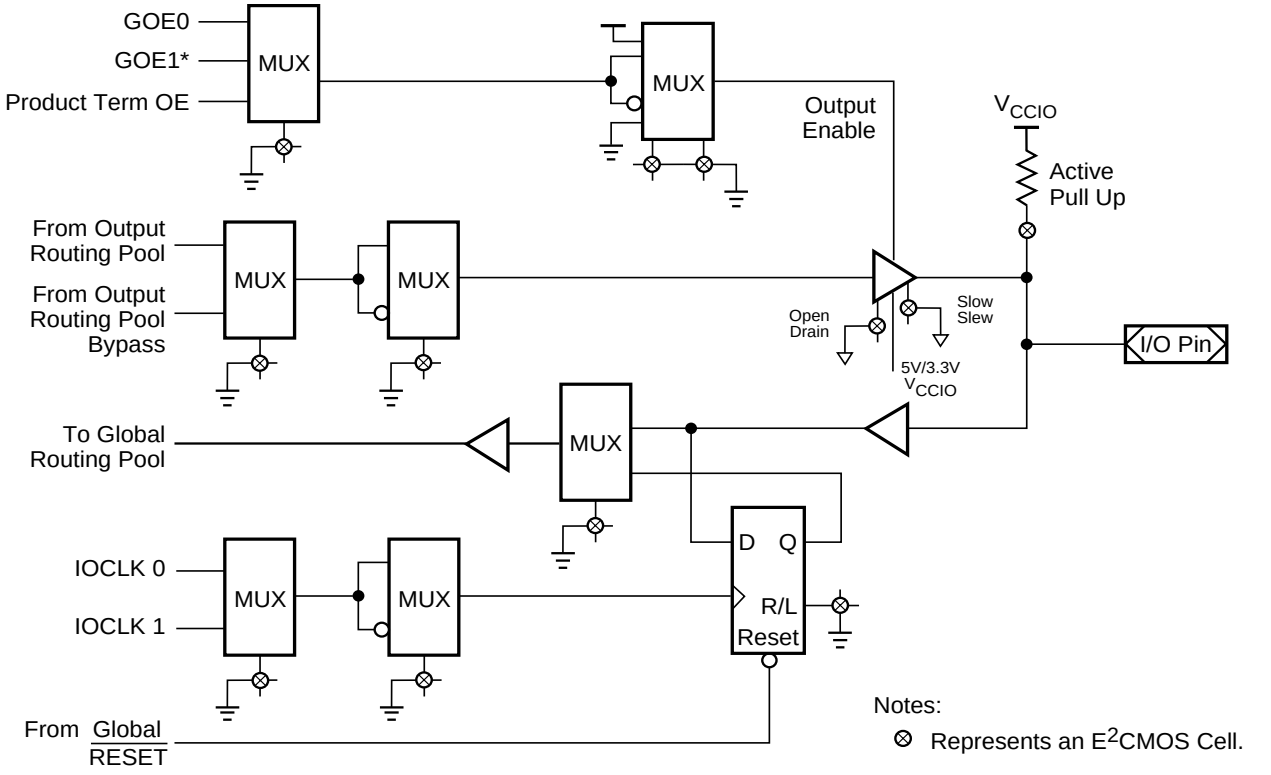
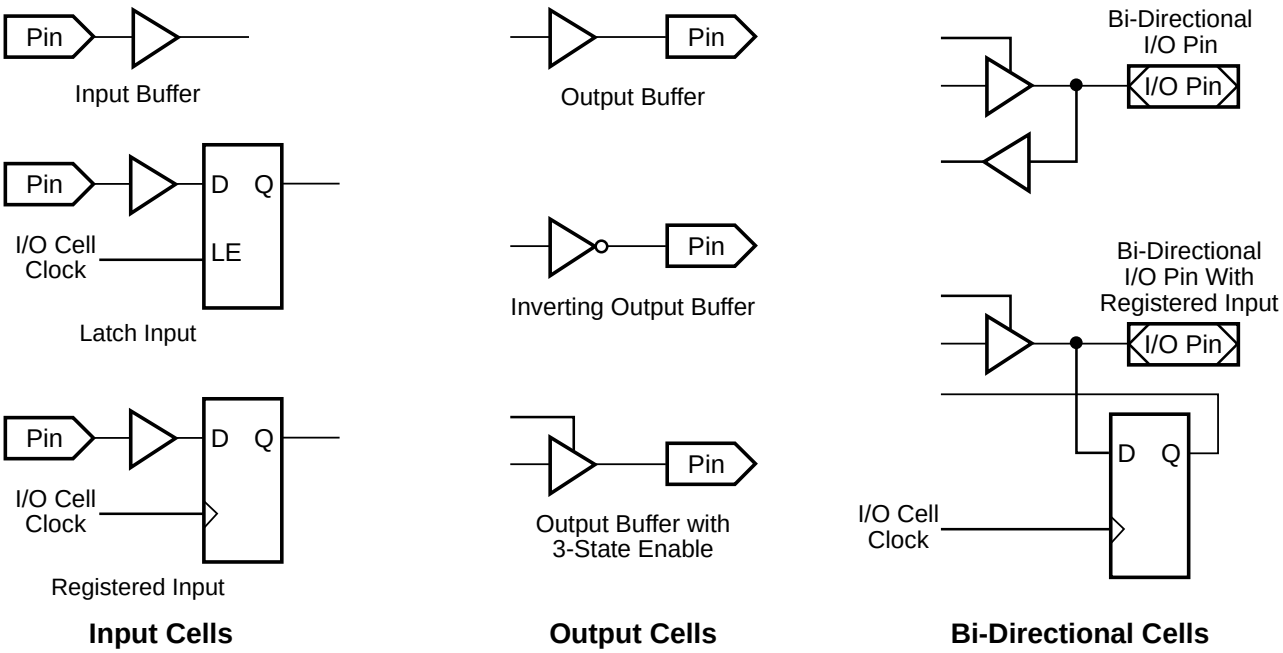


Figure 10. Examples of I/O Cell Configurations



An active pull-up resistor is available on all the I/O pins connected to VCCIO. If an I/O pin is not being used in a functional design, the pull-up will automatically be used in order to hold the I/O cell at VCCIO. Noise immunity can be improved by having all the active pull-ups on the I/O pins being programmed on. Each I/O pin that is used functionally in the design can be configured with the pull-up on or off.

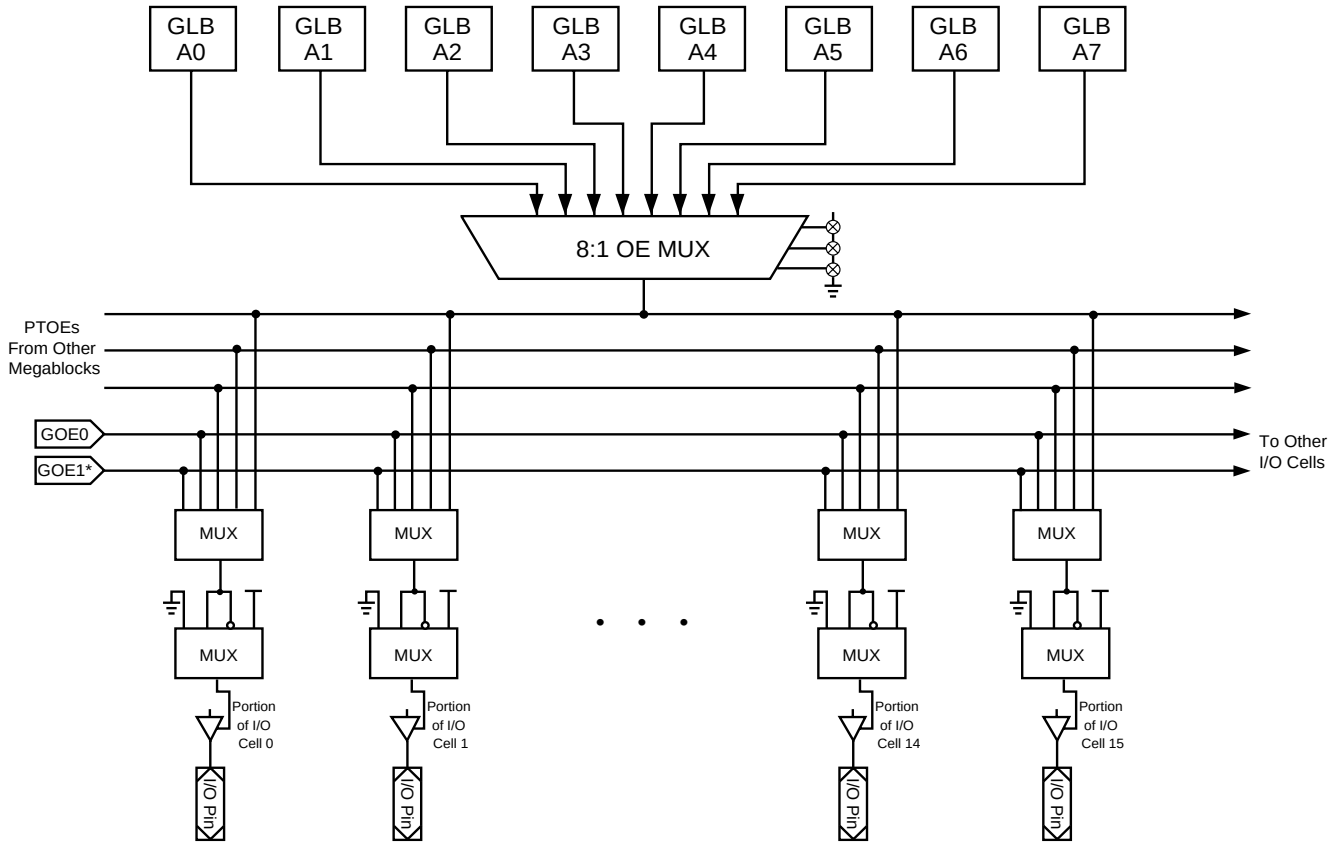
The Output Enable Control

The product term OE signal produced in each Megablock is available to all I/O cells in the Megablock that produced the signal. This product term OE bus allows more flexibility for bi-directional or tri-state control. An optional Global Output Enable (GOE) is provided on each of the 1000EA devices. The GOE provides minimum delay output enable control and additional OE signal choices to the OE MUX. On the 1016EA and 1032EA devices, the GOE is multiplexed with dedicated inputs.

Global Routing Pool

The GRP is a proprietary interconnect structure that offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available as an input to all of the GLBs. Because of the uniform architecture of the ispLSI devices, the delays through the GRP

Figure 11. Output Enable Control for a Megablock



*Not available on ispLSI 1016E.

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are both consistent and predictable. However, they are slightly affected by GLB loading. See the individual ispLSI 1000EA device data sheet for specific GLB loading delays. Delays through the GRP have been equalized to minimize timing skew.

Clock Distribution Network

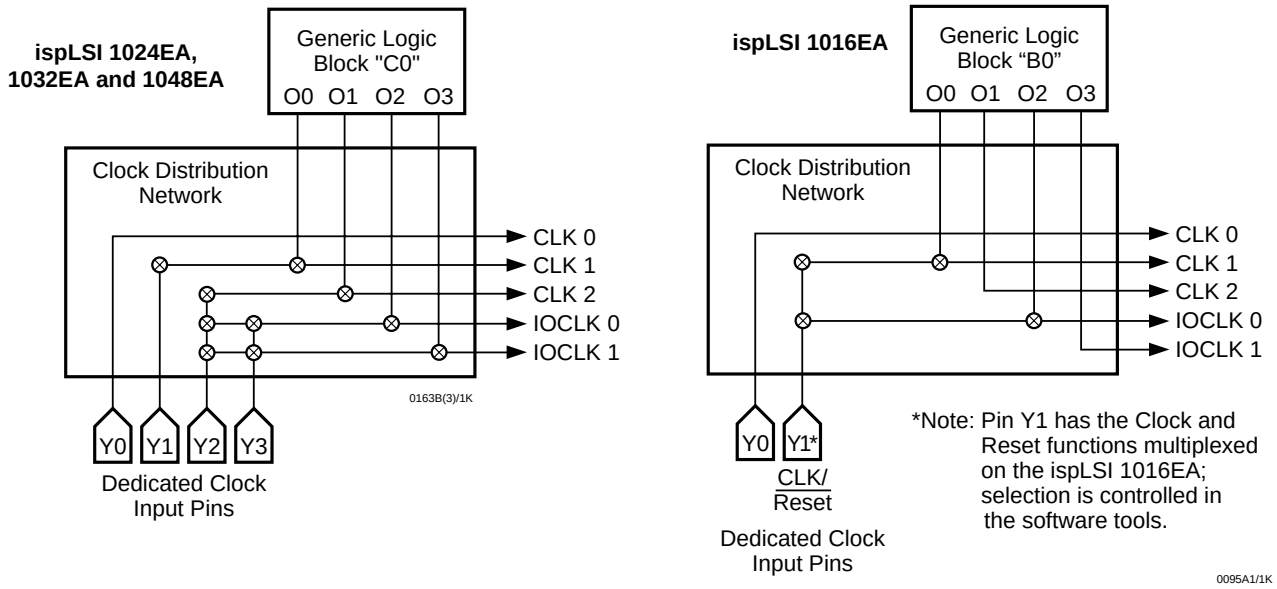
The Clock Distribution Networks are shown in Figure 13. They generate five global clock signals CLK 0, CLK 1, CLK 2 , IOCLK 0 and IOCLK 1. The first three, CLK 0, CLK 1 and CLK 2 may be used for clocking all the GLBs in the device. Similarly, IOCLK 0 and IOCLK 1 signals are used for clocking all of the I/O cells in the device. There are four dedicated system clock pins (Y0, Y1, Y2, Y3) (two for the ispLSI 1016EA (Y0, Y1)), which can be directed to any GLB or any I/O cell using the Clock Distribution Network. The other inputs to the Clock Distribution Network are the four outputs of a dedicated clock GLB ("C0" for the ispLSI 1032EA is shown in Figure 1). These clock GLB outputs can be used to create a user-defined internal clocking scheme.

For example, the clock GLB can be clocked using the external main clock pin Y0 connected to global clock signal CLK 0. The outputs of the clock GLB in turn can generate a "divide by" signal of the CLK 0 which can be connected to the CLK 1, CLK 2, IOCLK 0 or IOCLK 1 global clock lines.

All GLBs have the capability of generating their own asynchronous clocks using the clock Product Term (PT12). CLK 0, CLK 1 and CLK 2 feed to their corresponding clock MUX inputs on all the GLBs (see Figure 2).

The two I/O clocks generated in the Clock Distribution Network IOCLK 0 and IOCLK 1, are brought to all the I/O cells and the user programs the I/O cell to use one of the two.

Figure 12. Clock Distribution Networks



Boundary Scan and ISP

ISP programming of the device is performed via IEEE1149.1 compliant JTAG state machine. The programming signals are driven on the standard Test Access Port (TAP) interface. The four wire interface includes Test Data In (TDI), Test Clock (TCK), Test Mode Select (TMS), and Test Data Out (TDO). ISP program enable and disable is controlled by the private programming instruction set.

In addition to ISP programming, the JTAG state machine also provides standard boundary scan test capability. Standard boundary scan instructions supported are Sample/Preload, Extest, Bypass and High-Z instructions. The boundary scan test registers associated with each of the I/O pins control the state of the I/O pin when the device is not in normal functional mode. This feature allows users to define the state of the I/O pins during test and ISP programming modes.

Figure 13. Boundary Scan Register for I/O Pins

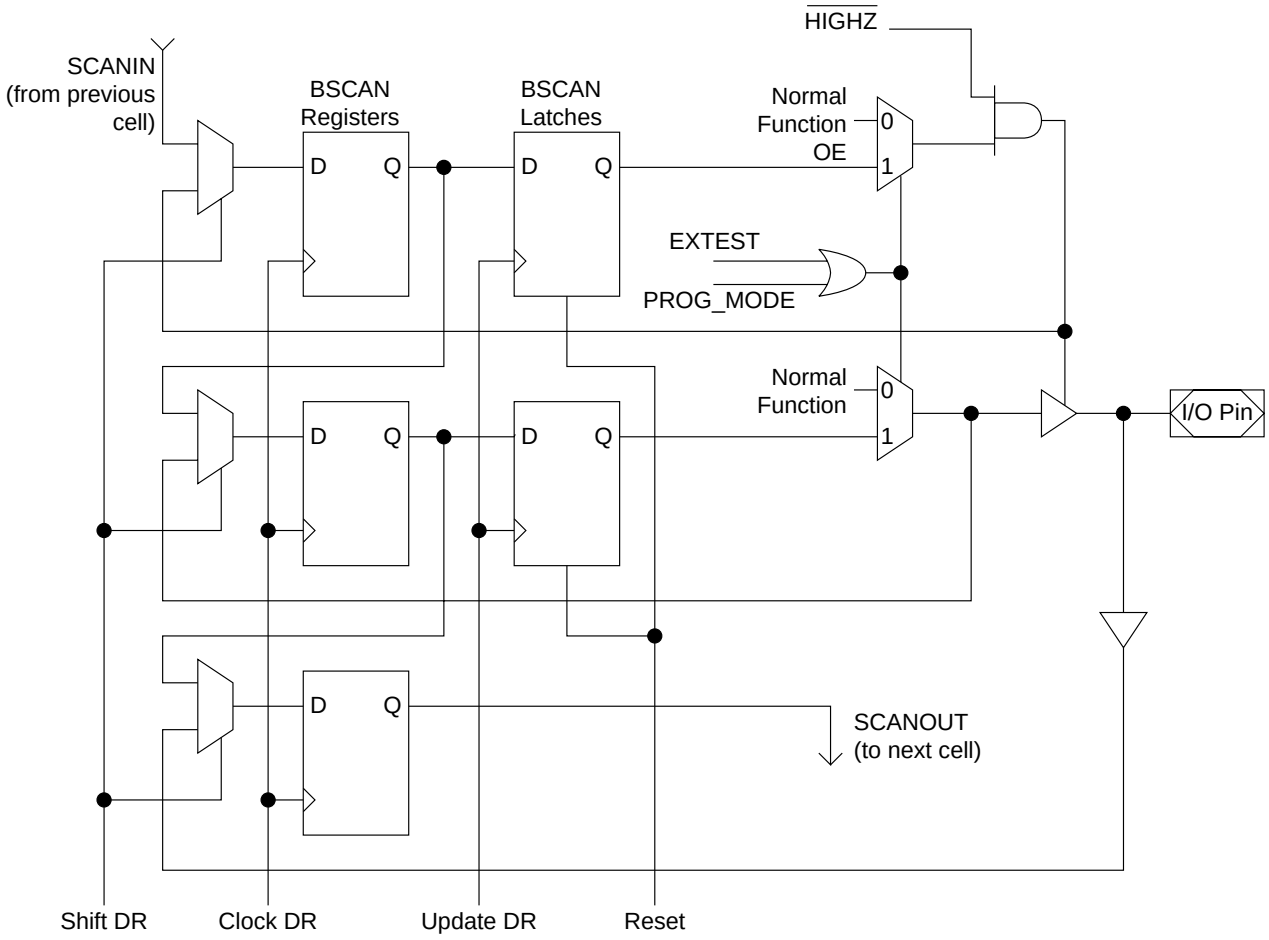
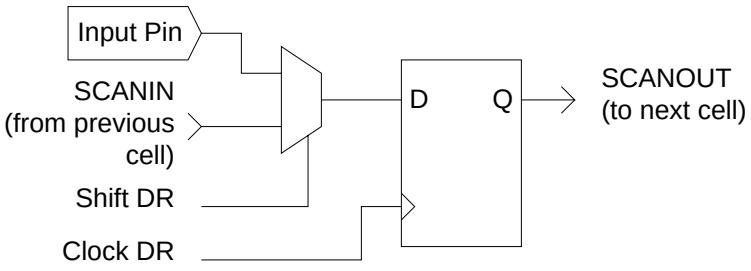


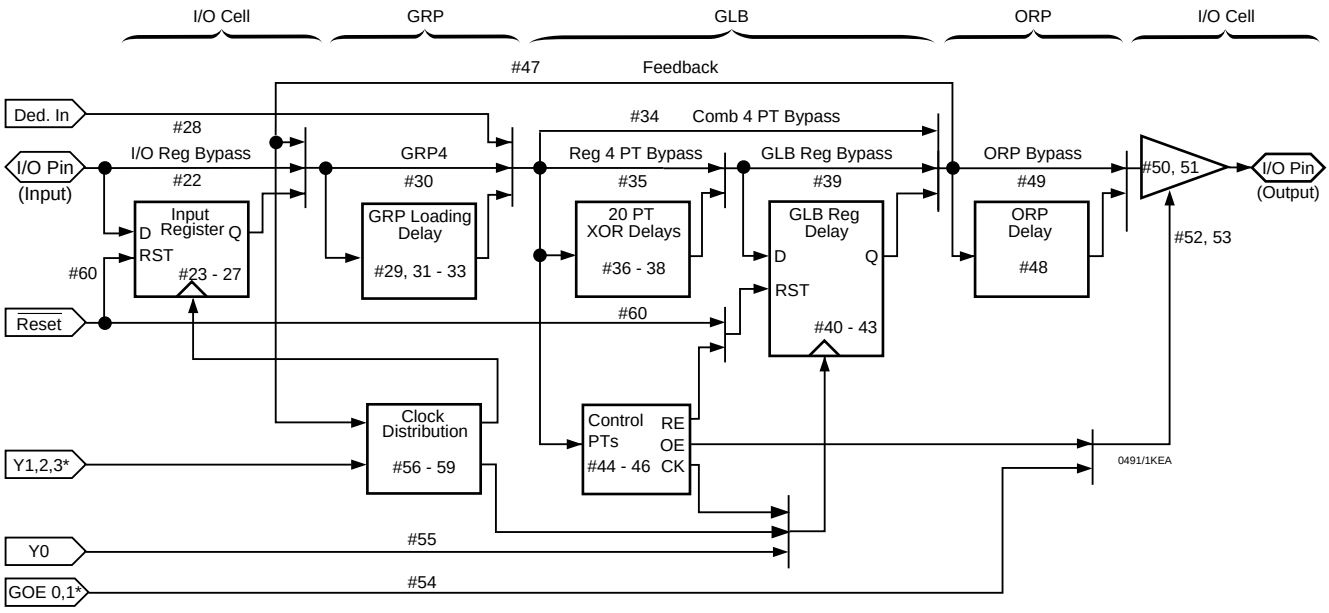
Figure 14. Boundary Scan Register for Dedicated Input Pins



Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in Figure 15. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (Figure 16). Critical timing paths are shown in Figure 16, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 15. ispLSI 1000EA Timing Model



*Note: Y1,Y2 and GOE0 only for the ispLSI 1016EA.

Figure 16. ispLSI Timing Model Examples[1]

Combinatorial Paths

t_{pd1}	=	t_{iobp}	+	t_{grp4}	+	t_{4ptbp}	+	$t_{20ptxor}$	+	t_{orpbp}	+	t_{ob}
#1	=	#22	+	#30	+	#35	+	#39	+	#49	+	#50,51
t_{pd2}	=	t_{iobp}	+	t_{grp4}	+	t_{xoradj}	+	$t_{20ptxor}$	+	t_{orp}	+	t_{ob}
#2	=	#22	+	#30	+	#38	+	#39	+	#48	+	#50,51

Registered Paths

General Form:

t_{su}	=	Logic	+	Regsu	-	Clock(min)
t_{h}	=	Clock(max)	+	Regh	-	Logic
t_{co}	=	Clock(max)	+	Regco	+	Output

Specific Examples:

t_{su1}	=	(t_{iobp}	+	t_{grp4}	+	t_{4ptbp})	+	t_{gsu}	-	$t_{gy0(min)}$		
#6	=	#22	+	#30	+	#35	+	#40	+	#55		
t_{h1}	=	$t_{gy0(max)}$	+	t_{gh}	-	(t_{iobp}	+	t_{grp4}	+	t_{4ptbp})		
#8	=	#55	+	#41	+	#22	+	#30	+	#35		
t_{co1}	=	$t_{gy0(max)}$	+	t_{gco}	+	(t_{orpbp}	+	t_{ob})				
#7	=	#55	+	#42	+	#49	+	#50				
t_{su2}	=	(t_{iobp}	+	t_{grp4}	+	t_{xoradj})	+	t_{gsu}	+	$t_{gy0(min)}$		
#9	=	#22	+	#30	+	#38	+	#40	+	#55		
t_{h2}	=	$t_{gy0(max)}$	+	t_{gh}	-	(t_{iobp}	+	t_{grp4}	+	t_{xoradj})		
#11	=	#55	+	#41	+	#22	+	#30	+	#38		
t_{co2}	=	$t_{gy0(max)}$	+	t_{gco}	+	(t_{orp}	+	t_{ob})				
#10	=	#55	+	#42	+	#48	+	#50,51				

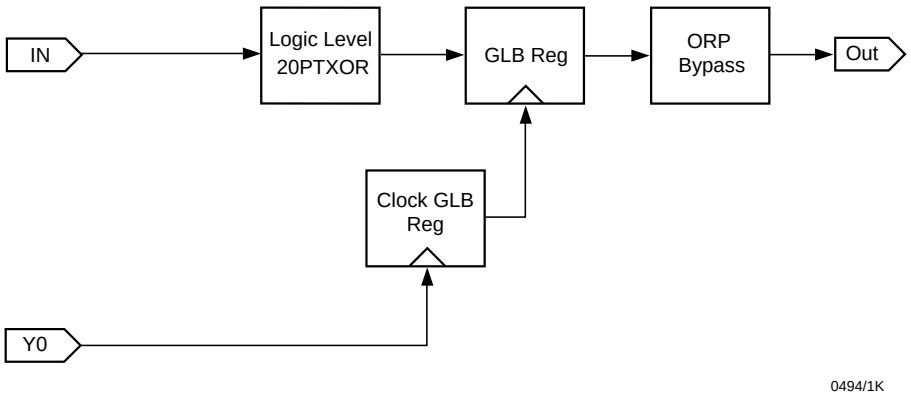
Table 2-0016/1kea.eps

1. The timing parameter reference numbers refer to the Internal Timing Parameters contained in the individual data sheets.

Circuit Timing Example

A design requires one logic level (using the 20PTXOR path). The design then uses a GLB register before exiting the device using the ORP bypass. Calculate **t**su, **t**h and **t**co.

Figure 15. Timing Calculation Example



tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) – (**t**gy0(min) + **t**gco + **t**gcp(min))
	=	(#22 + #30 + #37) + (#40) – (#54 + #42 + #57)
0.8 ns	=	(0.3 + 1.5 + 1.9) + (0.2) – (0.9 + 1.4 + 0.8)
th	=	Clock (max) + Reg h - Logic
	=	(**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) – (**t**iobp + **t**grp4 + **t**20ptxor)
	=	(#55 + #42 + #57) + (#41) – (#22 + #30 + #37)
1.4 ns	=	(0.9 + 1.4 + 1.8) + (1.0) – (0.3 + 1.5 + 1.9)
tco	=	Clock (max) + Reg co + Output
	=	(**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#55 + #42 + #57) + (#42) + (#48 + #50)
7.2 ns	=	(0.9 + 1.4 + 1.8) + (1.4) + (0.8 + 0.9)

Table 2-0042a-32ea

1. Calculations are based upon timing specifications for the ispLSI 1032EA-200 device.