

### CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V<sub>P-P</sub> can be achieved by digital signal amplitudes of 4.5V to 20V (if V<sub>DD</sub>-V<sub>SS</sub> = 3V, a V<sub>DD</sub>-V<sub>EE</sub> of up to 13V can be controlled; for V<sub>DD</sub>-V<sub>EE</sub> level differences above 13V, a V<sub>DD</sub>-V<sub>SS</sub> of at least 4.5V is required). For example, if V<sub>DD</sub> = +4.5V, V<sub>SS</sub> = 0V, and V<sub>EE</sub> = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V<sub>DD</sub>-V<sub>SS</sub> and V<sub>DD</sub>-V<sub>EE</sub> supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERDIP	F16.3
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP	E16.3
CD4051BM	-55 to 125	16 Ld SOIC	M16.15

### Features

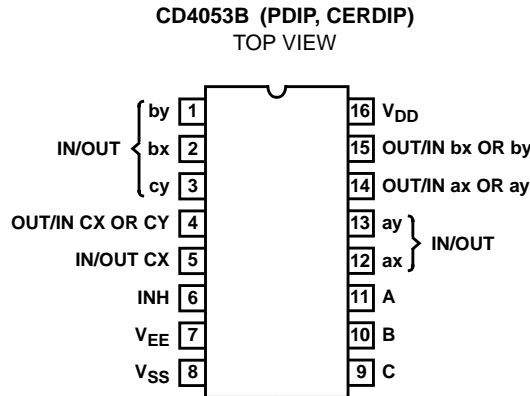
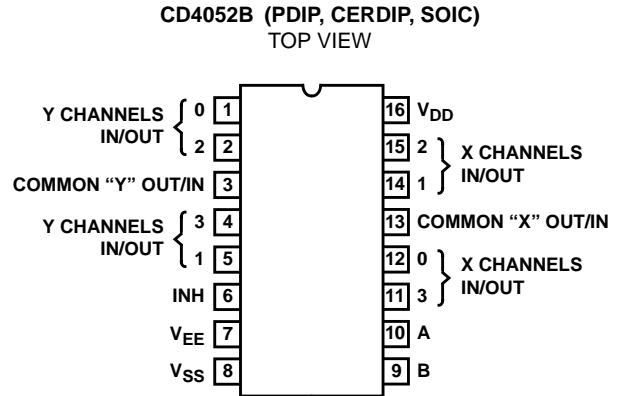
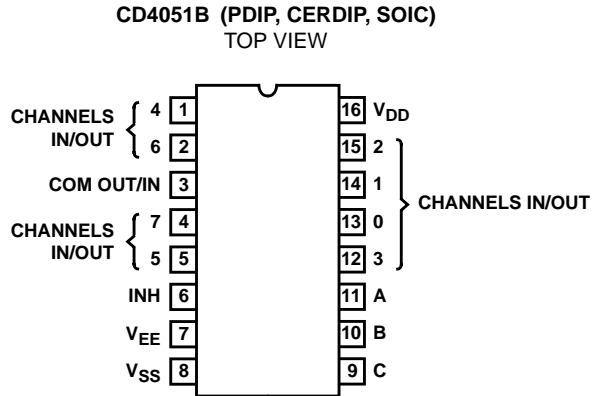
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog . . . . . ≤20V<sub>P-P</sub>
- Low ON Resistance, 125Ω (Typ) Over 15V<sub>P-P</sub> Signal Input Range for V<sub>DD</sub>-V<sub>EE</sub> = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V<sub>DD</sub>-V<sub>EE</sub> = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V<sub>DD</sub>-V<sub>SS</sub> = 3V to 20V) to Switch Analog Signals to 20V<sub>P-P</sub> (V<sub>DD</sub>-V<sub>EE</sub> = 20V)
- Matched Switch Characteristics, r<sub>ON</sub> = 5Ω (Typ) for V<sub>DD</sub>-V<sub>EE</sub> = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V<sub>DD</sub>-V<sub>SS</sub> = V<sub>DD</sub>-V<sub>EE</sub> = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

### Applications

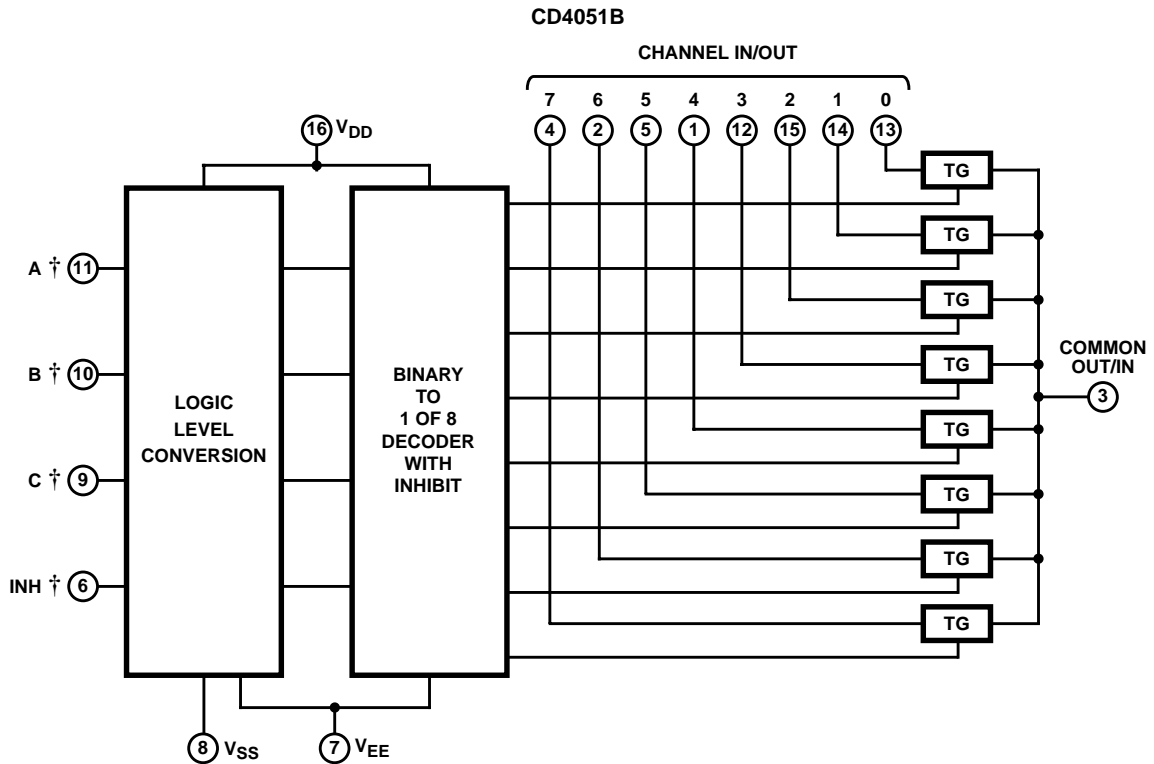
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

# CD4051B, CD4052B, CD4053B

## Pinouts



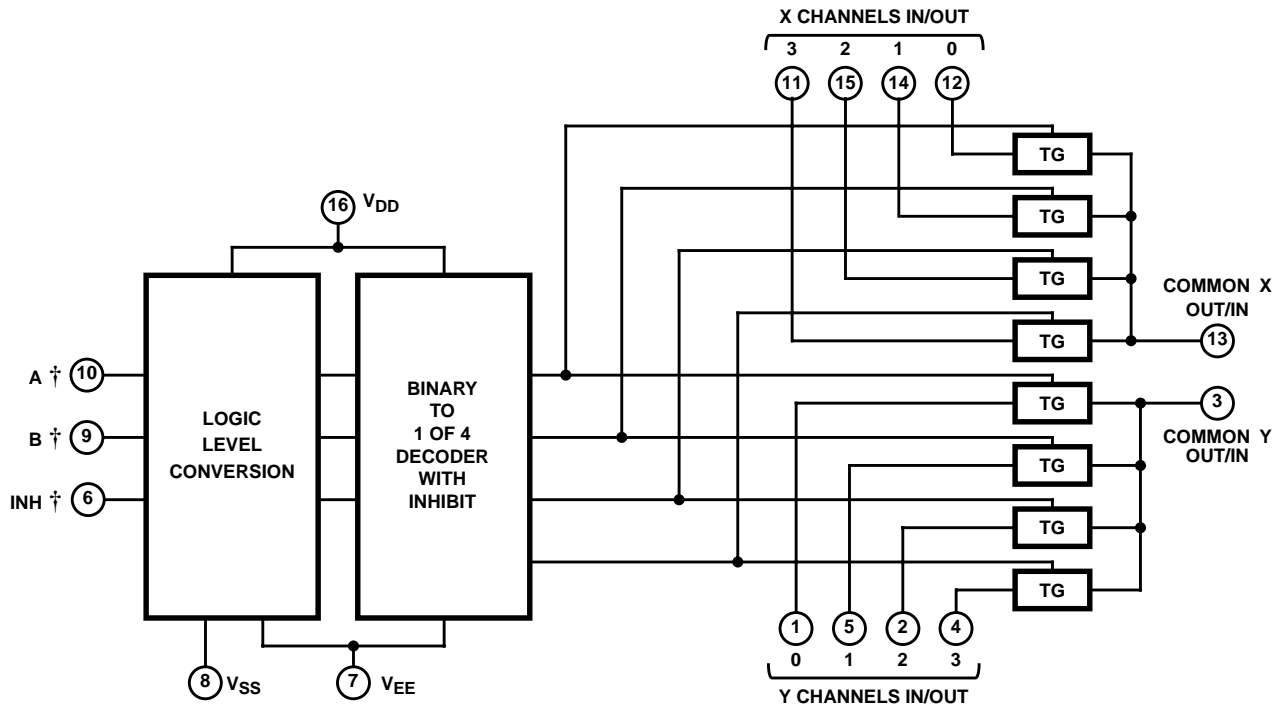
## Functional Block Diagrams



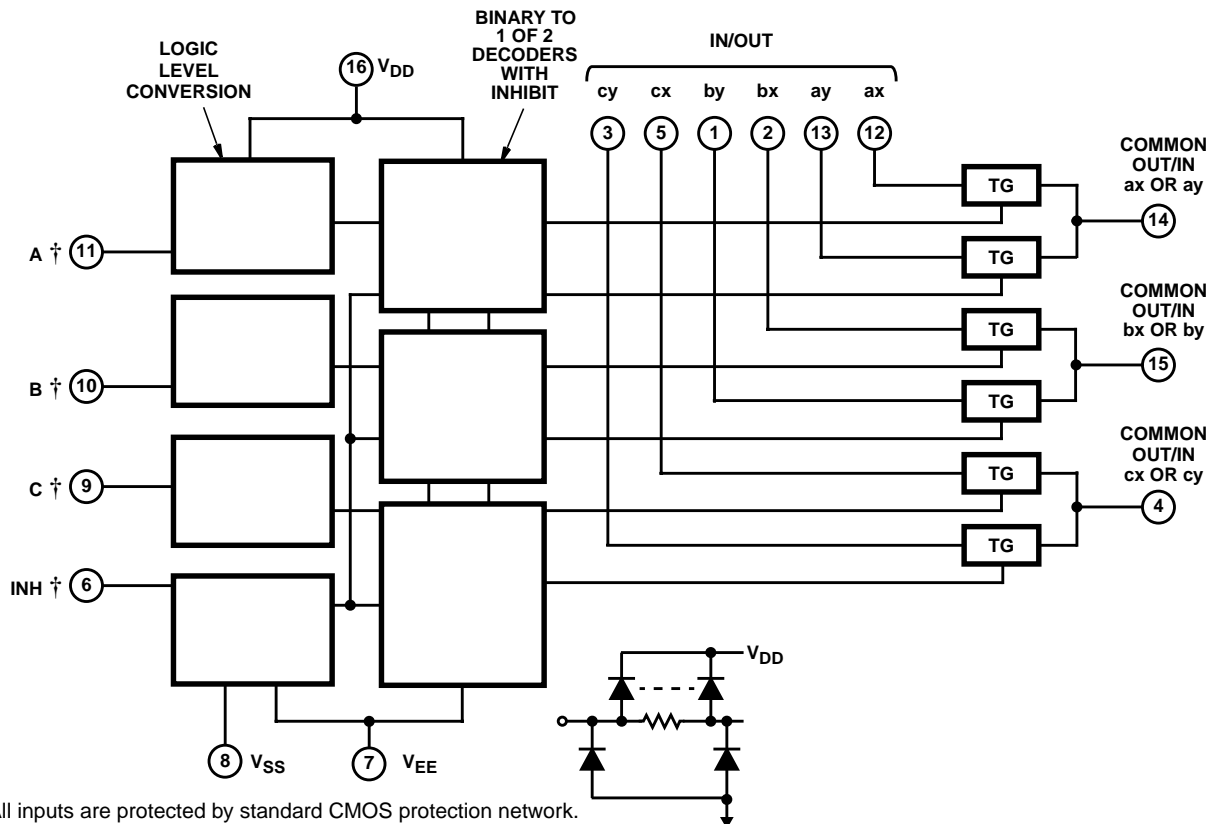
† All inputs are protected by standard CMOS protection network.

Functional Block Diagrams (Continued)

CD4052B



CD4053B



† All inputs are protected by standard CMOS protection network.

**CD4051B, CD4052B, CD4053B**

**TRUTH TABLES**

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
<b>CD4051B</b>				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
<b>CD4052B</b>				
INHIBIT	B		A	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
<b>CD4053B</b>				
INHIBIT	A OR B OR C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

X = Don't Care

# CD4051B, CD4052B, CD4053B

## Absolute Maximum Ratings

Supply Voltage (V+ to V-)  
 Voltages Referenced to V<sub>SS</sub> Terminal . . . . . -0.5V to 20V  
 DC Input Voltage Range . . . . . -0.5V to V<sub>DD</sub> +0.5V  
 DC Input Current, Any One Input. . . . . ±10mA

## Operating Conditions

Temperature Range . . . . . -55°C to 125°C

## Thermal Information

Thermal Resistance (Typical, Note 1)     $\theta_{JA}$  (°C/W)     $\theta_{JC}$  (°C/W)  
 PDIP Package . . . . . 78    N/A  
 CERDIP Package . . . . . 115    45  
 SOIC Package . . . . . 113    N/A  
 Maximum Junction Temperature (Ceramic Package) . . . . . 175°C  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 265°C  
 (SOIC - Lead Tips Only)


**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

Common Conditions Here: If Whole Table is For the Full Temp. Range, V<sub>SUPPLY</sub> = ±5V, A<sub>V</sub> = +1, R<sub>L</sub> = 100Ω, Unless Otherwise Specified (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	-55	-40	85	125	25			
									MIN	TYP	MAX	
<b>SIGNAL INPUTS (V<sub>IS</sub>) AND OUTPUTS (V<sub>OS</sub>)</b>												
Quiescent Device Current, I <sub>DD</sub> Max	-	-	-	5	5	5	150	150	-	0.04	5	μA
	-	-	-	10	10	10	300	300	-	0.04	10	μA
	-	-	-	15	20	20	600	600	-	0.04	20	μA
	-	-	-	20	100	100	3000	3000	-	0.08	100	μA
Drain to Source ON Resistance r <sub>ON</sub> Max 0 ≤ V <sub>IS</sub> ≤ V <sub>DD</sub>	-	0	0	5	800	850	1200	1300	-	470	1050	Ω
	-	0	0	10	310	330	520	550	-	180	400	Ω
	-	0	0	15	200	210	300	320	-	125	240	Ω
Change in ON Resistance (Between Any Two Channels), Δr <sub>ON</sub>	-	0	0	5	-	-	-	-	-	15	-	Ω
	-	0	0	10	-	-	-	-	-	10	-	Ω
	-	0	0	15	-	-	-	-	-	5	-	Ω
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)	-	0	0	18	±100 (Note 2)		±1000 (Note 2)		-	±0.01	±100 (Note 2)	μA
Capacitance:	-	-5	5-	5	-	-	-	-	-	5	-	pF
Input, C <sub>IS</sub>												
Output, C <sub>OS</sub>												
CD4051										30	-	pF
CD4052										18	-	pF
CD4053										9	-	pF
Feedthrough C <sub>IOS</sub>										0.2	-	pF
Propagation Delay Time (Signal Input to Output)		V <sub>DD</sub>	R <sub>L</sub> = 200kΩ, C <sub>L</sub> = 50pF, t <sub>r</sub> , t <sub>f</sub> = 20ns	5	-	-	-	-	-	30	60	ns
				10	-	-	-	-	-	15	30	ns
				15	-	-	-	-	-	10	20	ns

## CD4051B, CD4052B, CD4053B

**Electrical Specifications** Common Conditions Here: If Whole Table is For the Full Temp. Range,  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_L = 100\Omega$ , Unless Otherwise Specified **(Continued)** (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	-55	-40	85	125	25			
									MIN	TYP	MAX	
<b>CONTROL (ADDRESS OR INHIBIT), <math>V_C</math></b>												
Input Low Voltage, $V_{IL}$ , Max	$V_{IL} = V_{DD}$ through 1k $\Omega$ ; $V_{IH} = V_{DD}$ through 1k $\Omega$	$V_{EE} = V_{SS}$ , $R_L = 1k\Omega$ to $V_{SS}$ , $I_{IS} < 2\mu A$ on All OFF Channels	5	1.5	1.5	1.5	1.5	-	-	1.5	V	
			10	3	3	3	3	-	-	3	V	
			15	4	4	4	4	-	-	4	V	
Input High Voltage, $V_{IH}$ , Min	$V_{IL} = V_{DD}$ through 1k $\Omega$ ; $V_{IH} = V_{DD}$ through 1k $\Omega$	$V_{EE} = V_{SS}$ , $R_L = 1k\Omega$ to $V_{SS}$ , $I_{IS} < 2\mu A$ on All OFF Channels	5	3.5	3.5	3.5	3.5	3.5	-	-	V	
			10	7	7	7	7	7	-	-	V	
			15	11	11	11	11	11	-	-	V	
Input Current, $I_{IN}$ (Max)	$V_{IN} = 0, 18$		18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$	
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figures 10, 11, 14	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	450	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-5	0	5	-	-	-	-	-	225	450	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 1k\Omega$	0	0	5	-	-	-	-	-	400	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-10	0	5	-	-	-	-	-	200	400	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	200	450	ns
		0	0	10	-	-	-	-	-	90	210	ns
		0	0	15	-	-	-	-	-	70	160	ns
		-10	0	5	-	-	-	-	-	130	300	ns
Input Capacitance, $C_{IN}$ (Any Address or Inhibit Input)				-	-	-	-	-	5	7.5	pF	

NOTE:

- Determined by minimum feasible leakage measurement for automatic testing.

### Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS		UNITS	
	$V_{IS}$ (V)	$V_{DD}$ (V)	$R_L$ (k $\Omega$ )	TYP			
Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)	5 (Note 3)	10	1	$V_{OS}$ at Common OUT/IN	CD4053	30	MHz
					CD4052	25	MHz
					CD4051	20	MHz
				$V_{EE} = V_{SS}$ , $20\text{Log} \frac{V_{OS}}{V_{IS}} = -3\text{dB}$	$V_{OS}$ at Any Channel	60	MHz

Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS			
	V <sub>IS</sub> (V)	V <sub>DD</sub> (V)	R <sub>L</sub> (kΩ)	TYP	UNITS		
Total Harmonic Distortion, THD	2 (Note 3)	5	10	0.3	%		
	3 (Note 3)	10		0.2	%		
	5 (Note 3)	15		0.12	%		
	V <sub>EE</sub> = V <sub>SS</sub> , f <sub>IS</sub> = 1kHz Sine Wave				%		
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V <sub>OS</sub> at Common OUT/IN	CD4053	8	MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$				CD4052	10	MHz
					CD4051	12	MHz
				V <sub>OS</sub> at Any Channel	8	MHz	
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels		3	MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$			Between Sections, CD4052 Only	Measured on Common	6	MHz
					Measured on Any Channel	10	MHz
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	MHz
					In Pin 15, Out Pin 14	6	MHz
Address-or-Inhibit-to-Signal Crosstalk	-	10	10 (Note 4)			65	mV <sub>PEAK</sub>
	V <sub>EE</sub> = 0, V <sub>SS</sub> = 0, t <sub>r</sub> , t <sub>f</sub> = 20ns, V <sub>CC</sub> = V <sub>DD</sub> - V <sub>SS</sub> (Square Wave)					65	mV <sub>PEAK</sub>

NOTES:

- Peak-to-Peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$
- Both ends of channel.

Typical Performance Curves

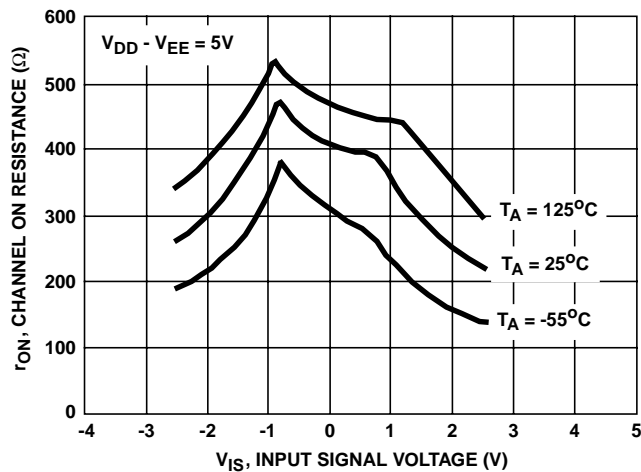


FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

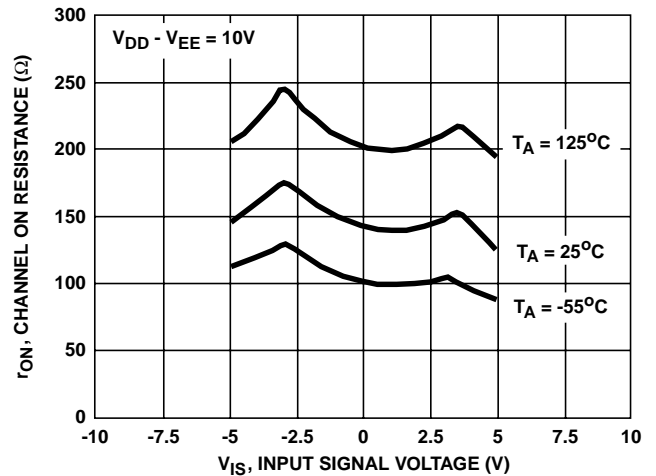


FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Curves (Continued)

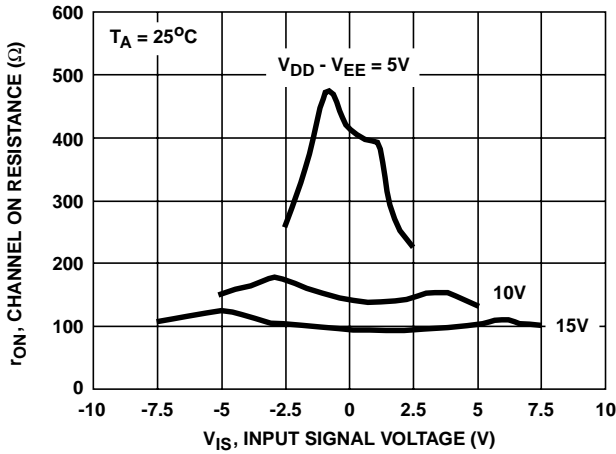


FIGURE 3. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)



FIGURE 4. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

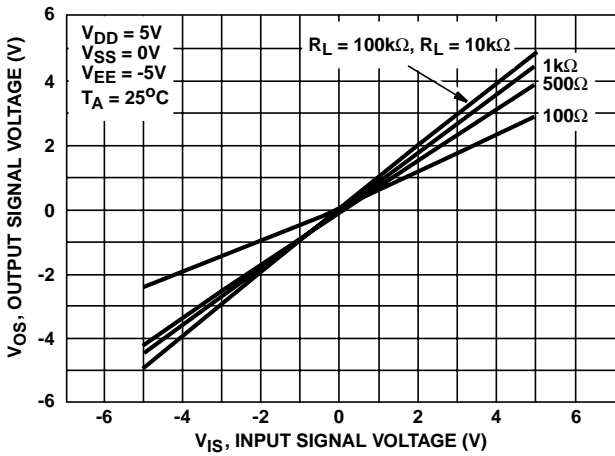


FIGURE 5. ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051B)

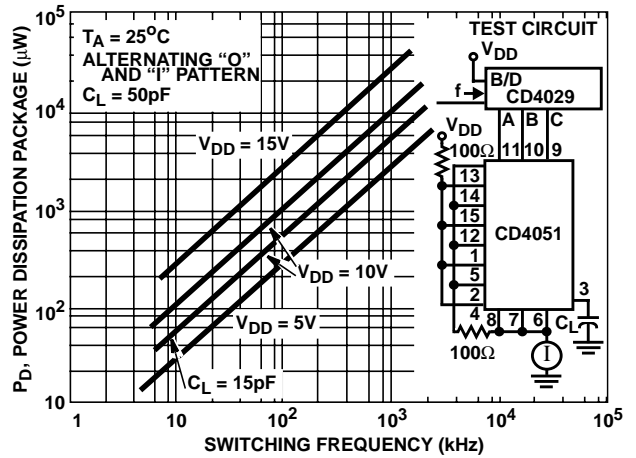


FIGURE 6. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051B)



FIGURE 7. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052B)

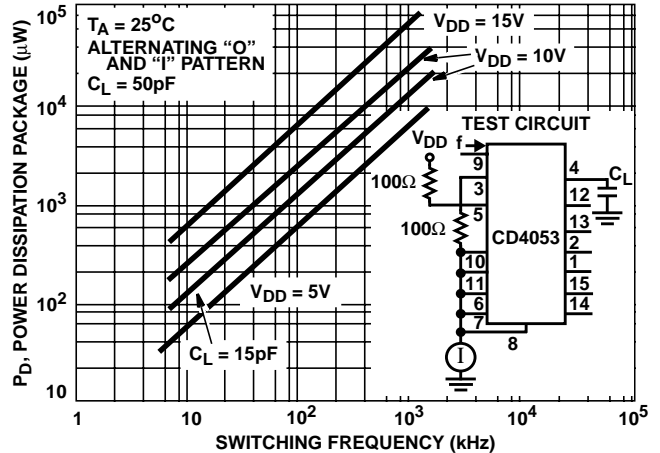


FIGURE 8. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053B)



Test Circuits and Waveforms



NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" =  $V_{SS}$  and "1" =  $V_{DD}$ . The analog signal (through the TG) may swing from  $V_{EE}$  to  $V_{DD}$ .

FIGURE 9. TYPICAL BIAS VOLTAGES



FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON ( $R_L = 1k\Omega$ )



FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF ( $R_L = 1k\Omega$ )



FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

Test Circuits and Waveforms (Continued)



FIGURE 13. OFF CHANNEL LEAKAGE CURRENT - ALL CHANNELS OFF

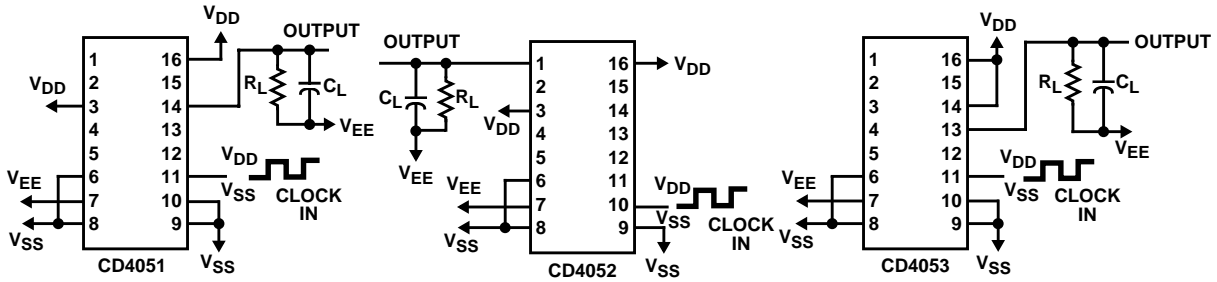


FIGURE 14. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

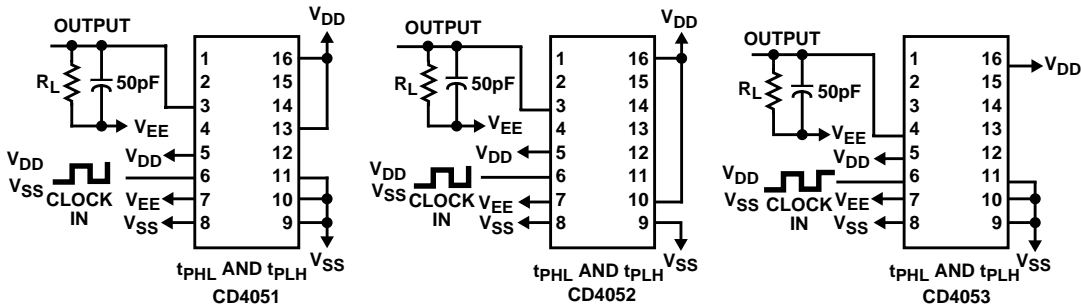
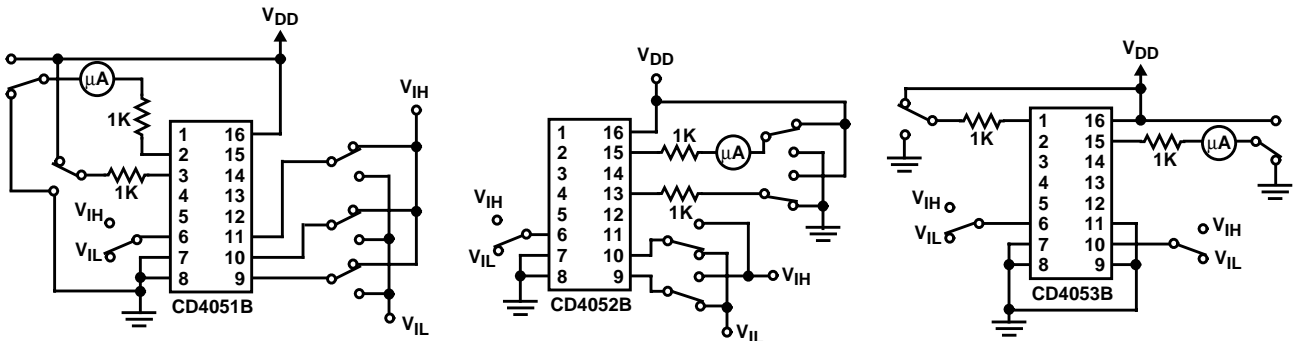


FIGURE 15. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT



MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 6)

MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 2x)

MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL by)

FIGURE 16. INPUT VOLTAGE TEST CIRCUITS (NOISE IMMUNITY)

Test Circuits and Waveforms (Continued)



FIGURE 17. QUIESCENT DEVICE CURRENT



FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT



FIGURE 19. INPUT CURRENT



FIGURE 20. FEEDTHROUGH (ALL TYPES)

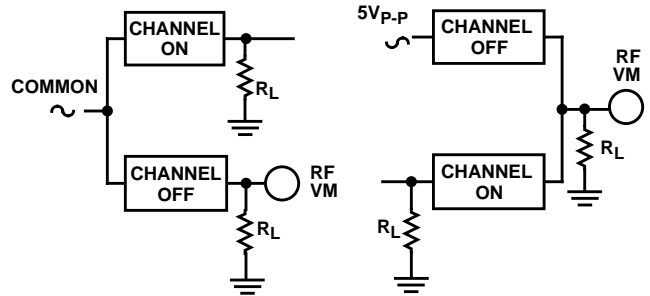


FIGURE 21. CROSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)

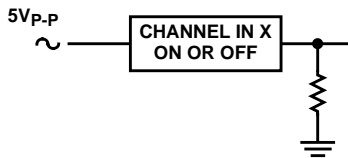


FIGURE 22. CROSTALK BETWEEN DUALS OR TRIPLETS (CD4052B, CD4053B)

Test Circuits and Waveforms (Continued)



FIGURE 23. TYPICAL TIME-DIVISION APPLICATION OF THE CD4052B

**Special Considerations**

In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

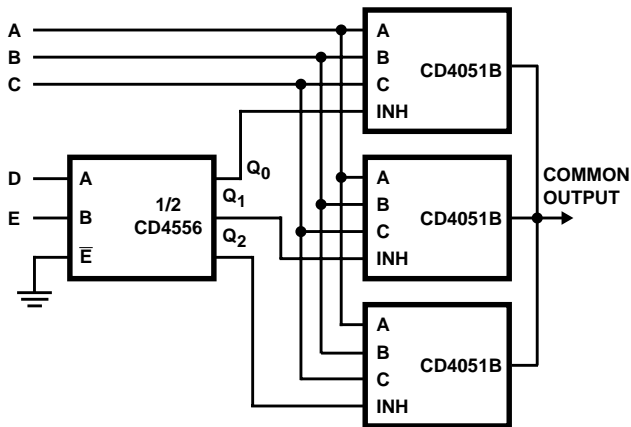


FIGURE 24. 24-TO-1 MUX ADDRESSING

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.