# SN54LS668, SN54LS669, SN74LS668, SN74LS669
# SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

D2351, APRIL 1977 — REVISED MARCH 1988

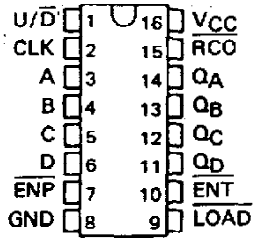
## 'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
## 'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

**Programmable Look-Ahead Up/Down Binary/Decade Counters**

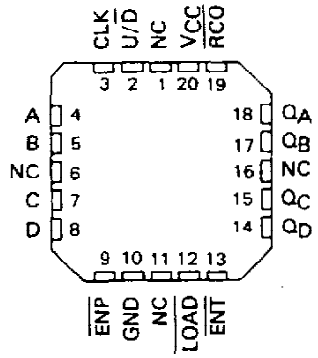
- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Buffered Outputs**

| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY | | TYPICAL POWER DISSIPATION |
|---|---|---|---|
| | COUNTING UP | COUNTING DOWN | |
| 'LS668, 'LS669 | 32 MHz | 32 MHz | 100 mW |

SN54LS668, SN54LS669 . . . J OR W PACKAGE
SN74LS668, SN74LS669 . . . D OR N PACKAGE
(TOP VIEW)




SN54LS668, SN54LS669 . . . FK PACKAGE
(TOP VIEW)




NC – No internal connection

### description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

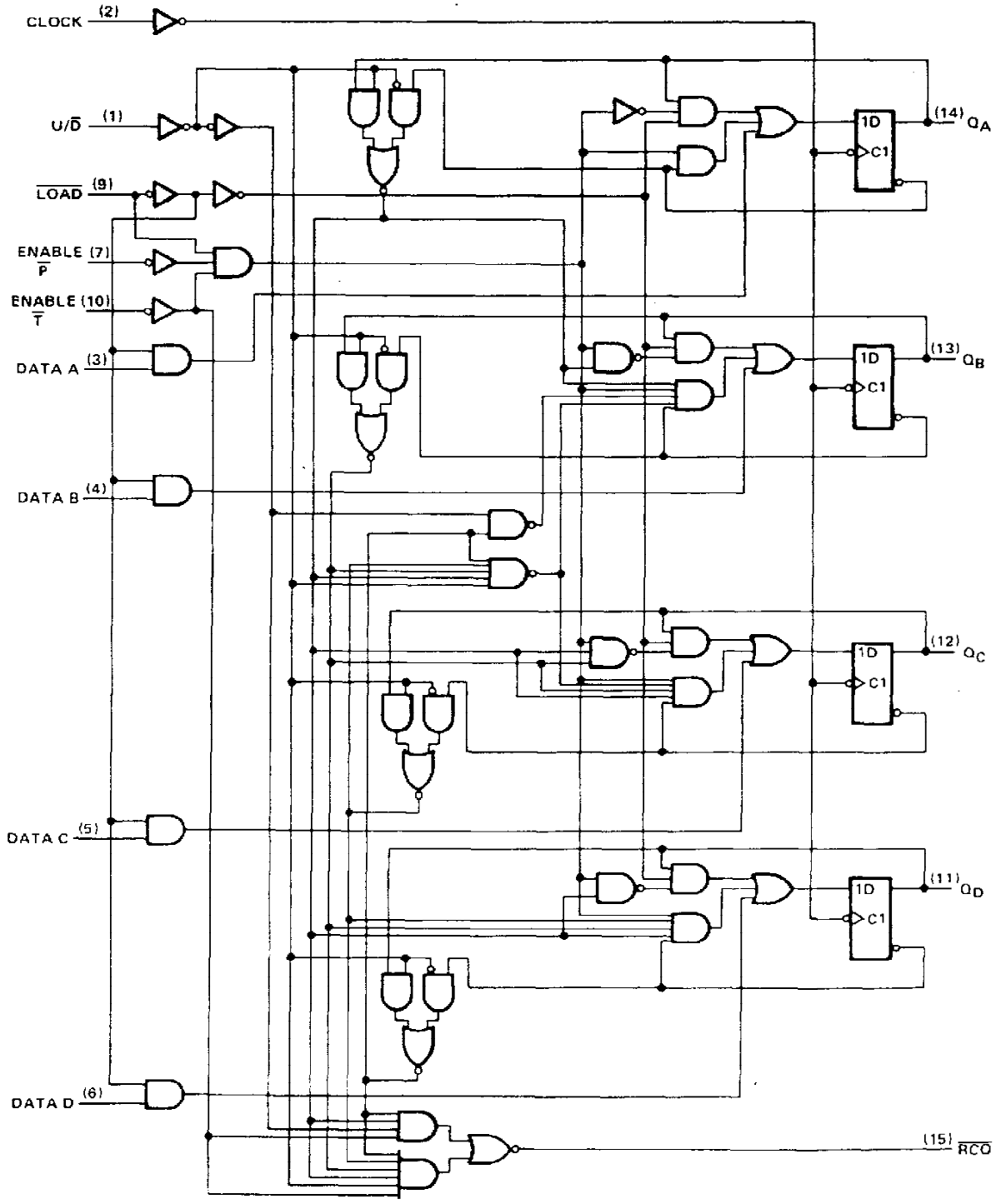
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse when the count is maximum counting up or zero counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents $I_{IH}$ and $I_{IL}$, and all buffered outputs.

**logic diagram (positive logic)**

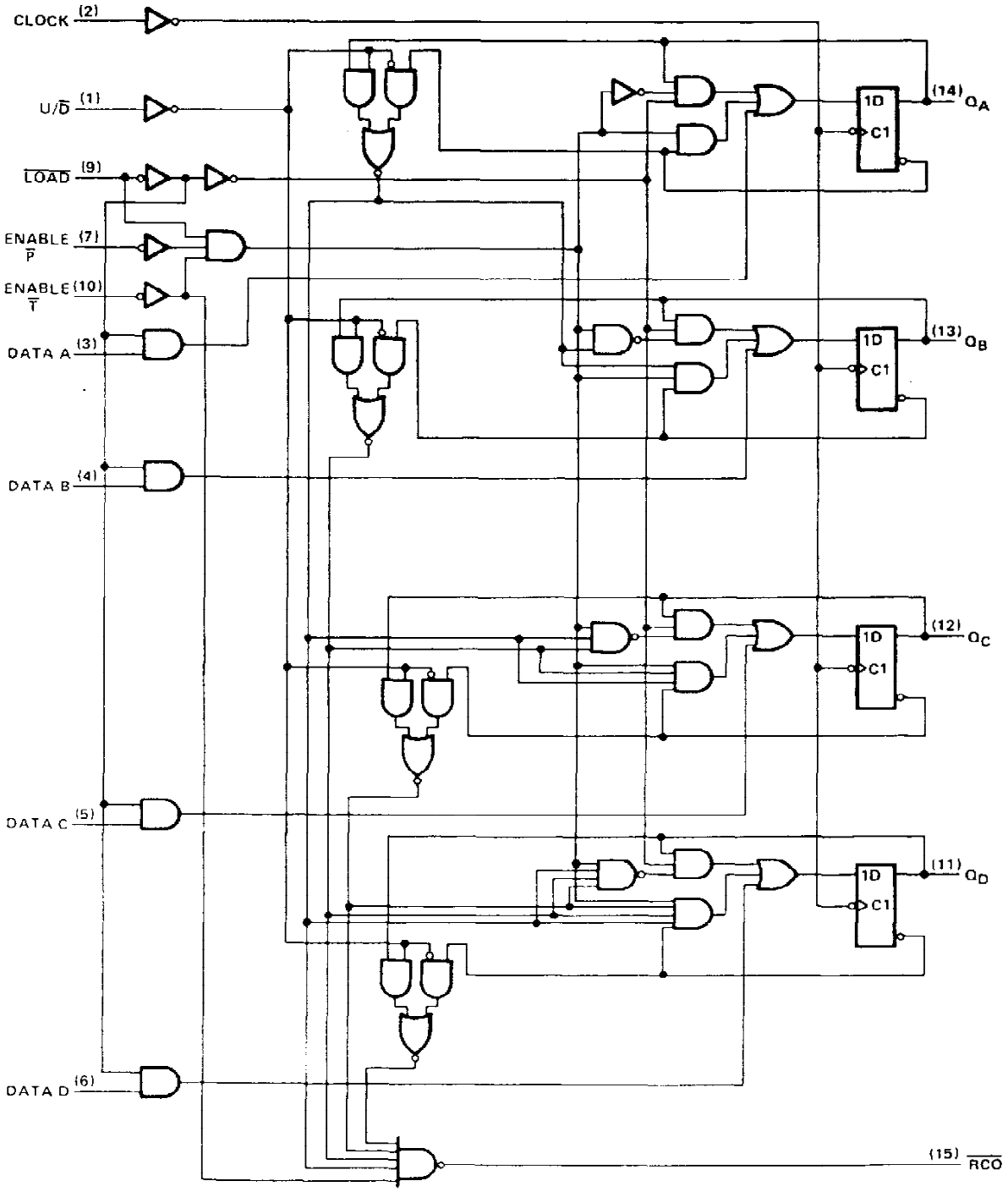
SN54LS668, SN74LS668, DECADE COUNTERS




Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic) (continued)

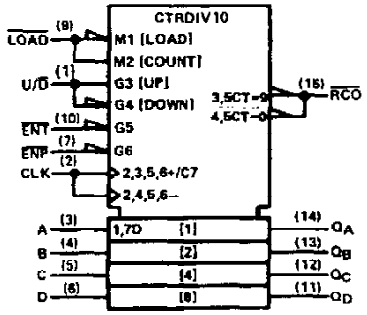
SN54LS669, SN74LS669, BINARY COUNTERS




Pin numbers shown are for D, J, N, and W packages.

## 'LS668 DECADE COUNTERS

### logic symbol†

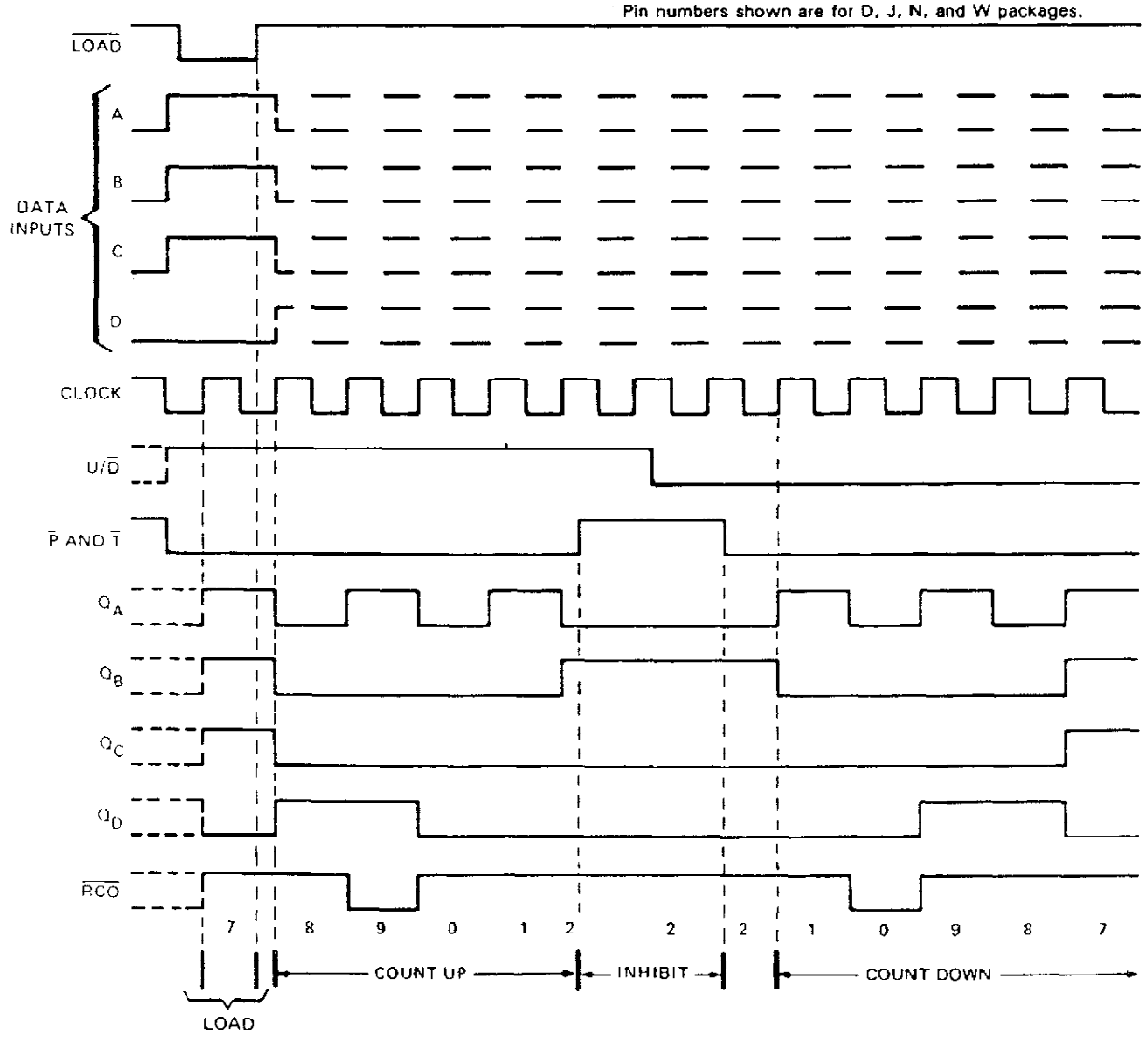



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

### typical load, count, and inhibit sequences

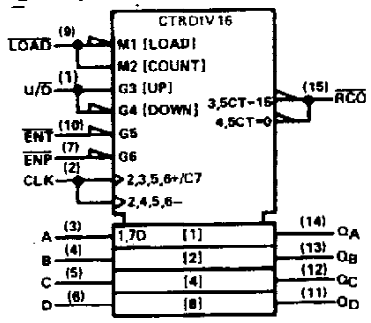
Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



## 'LS669 BINARY COUNTERS

### logic symbol†

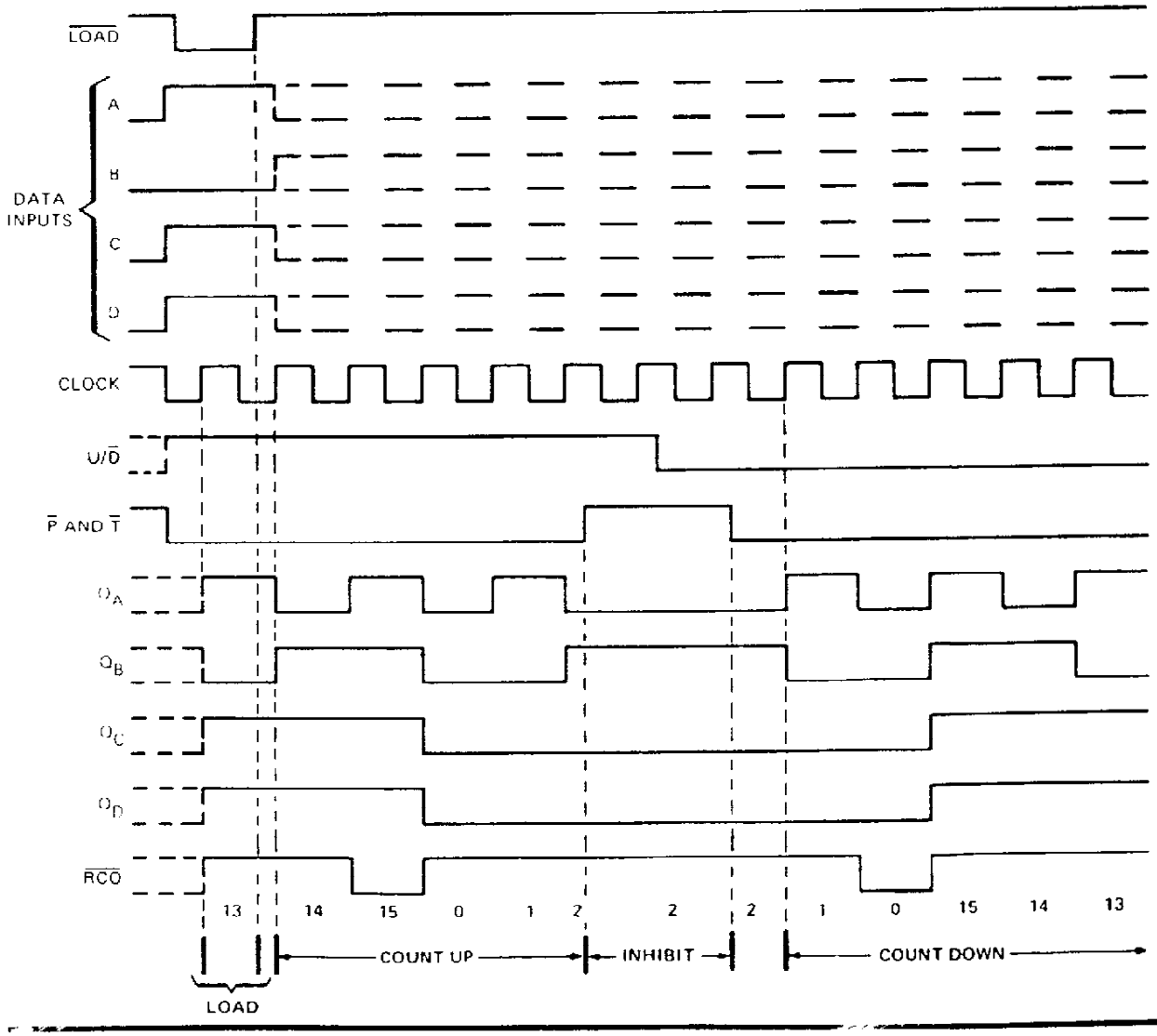



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

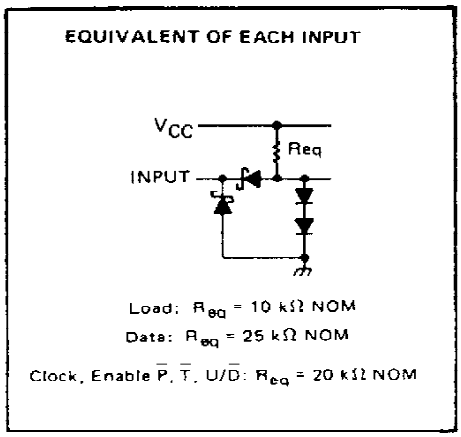
### typical load, count, and inhibit sequences

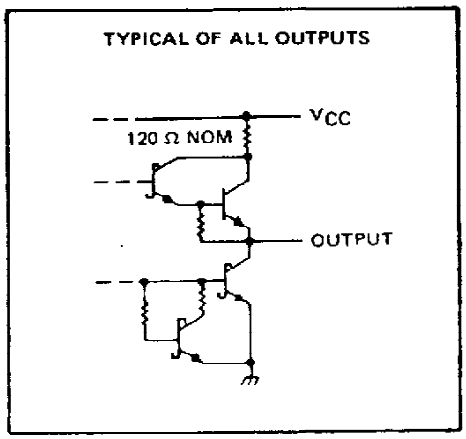
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS668, SN54LS669 . . . . . −55°C to 125°C
SN74LS668, SN74LS669 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | SN54LS668 SN54LS669 | | | SN74LS668 SN74LS669 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | | 4 | | | 8 | mA |
| Clock frequency, $f_{clock}$ | | 0 | | 25 | 0 | | 25 | MHz |
| Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1) | | 20 | | | 20 | | | ns |
| Setup time, $t_{su}$ (see Figure 1) | Data inputs A, B, C, D | 25 | | | 25 | | | ns |
| | $\overline{ENP}$ or $\overline{ENT}$ | 40 | | | 40 | | | |
| | $\overline{LOAD}$ | 30 | | | 30 | | | |
| | $U/\overline{D}$ | 45 | | | 45 | | | |
| Hold time at any input with respect to clock, $t_h$ (see Figure 1) | | 0 | | | 0 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | SN54LS668 SN54LS669 | | | SN74LS668 SN74LS669 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | | Clock, $\overline{T}$ | | | | | 0.1 | | | 0.1 | |
| | | $\overline{LOAD}$ | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | High-level input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| | | Clock, $\overline{T}$ | | | | | 20 | | | 20 | |
| | | $\overline{LOAD}$ | | | | | 40 | | | 40 | |
| $I_{IL}$ | Low-level input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| | | Clock, $\overline{T}$ | | | | | −0.4 | | | −0.4 | |
| | | $\overline{LOAD}$ | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 2 | | 20 | 34 | | 20 | 34 | mA |

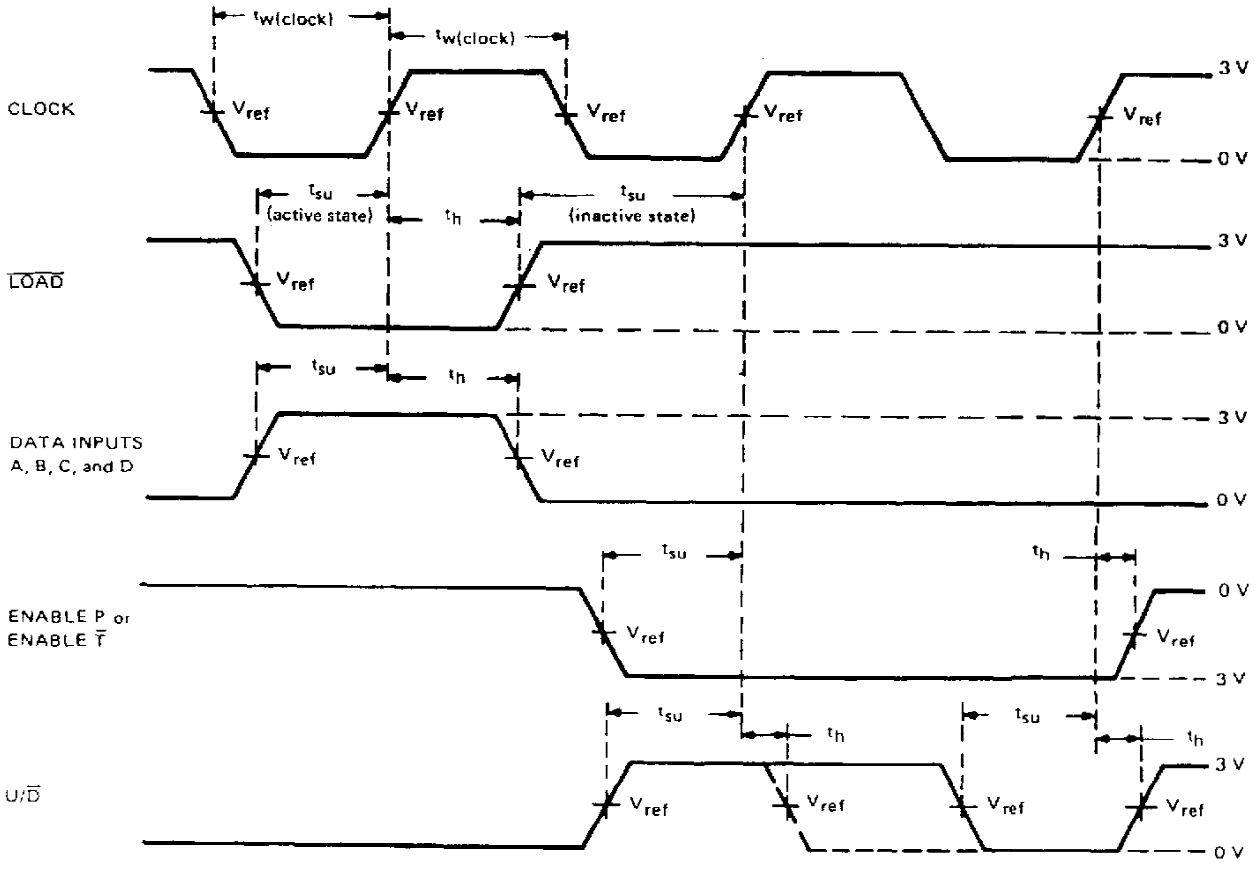
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Figures 2 and 3 | 25 | 32 | | MHz |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | | | 26 | 40 | ns |
| $t_{PHL}$ | | | | | 40 | 60 | |
| $t_{PLH}$ | CLK | Any Q | | | 18 | 27 | ns |
| $t_{PHL}$ | | | | | 18 | 27 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | | 29 | 45 | |
| $t_{PLH}$# | U/$\overline{D}$ | $\overline{RCO}$ | | | 22 | 35 | ns |
| $t_{PHL}$# | | | | | 26 | 40 | |

¶ $f_{max}$ = Maximum clock frequency.
$t_{PLH}$ = propagation delay time, low-to-high-level output.
$t_{PHL}$ = propagation delay time, high-to-low-level output.
# Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.

## PARAMETER MEASUREMENT INFORMATION

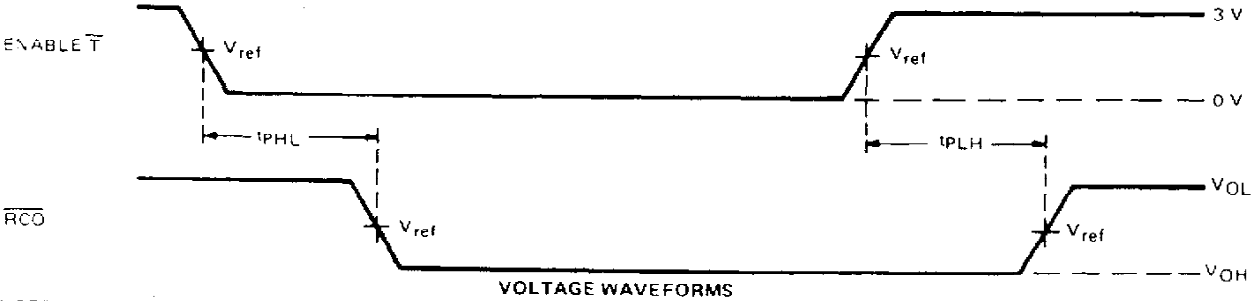



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. $V_{ref} = 1.3$ V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES




VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

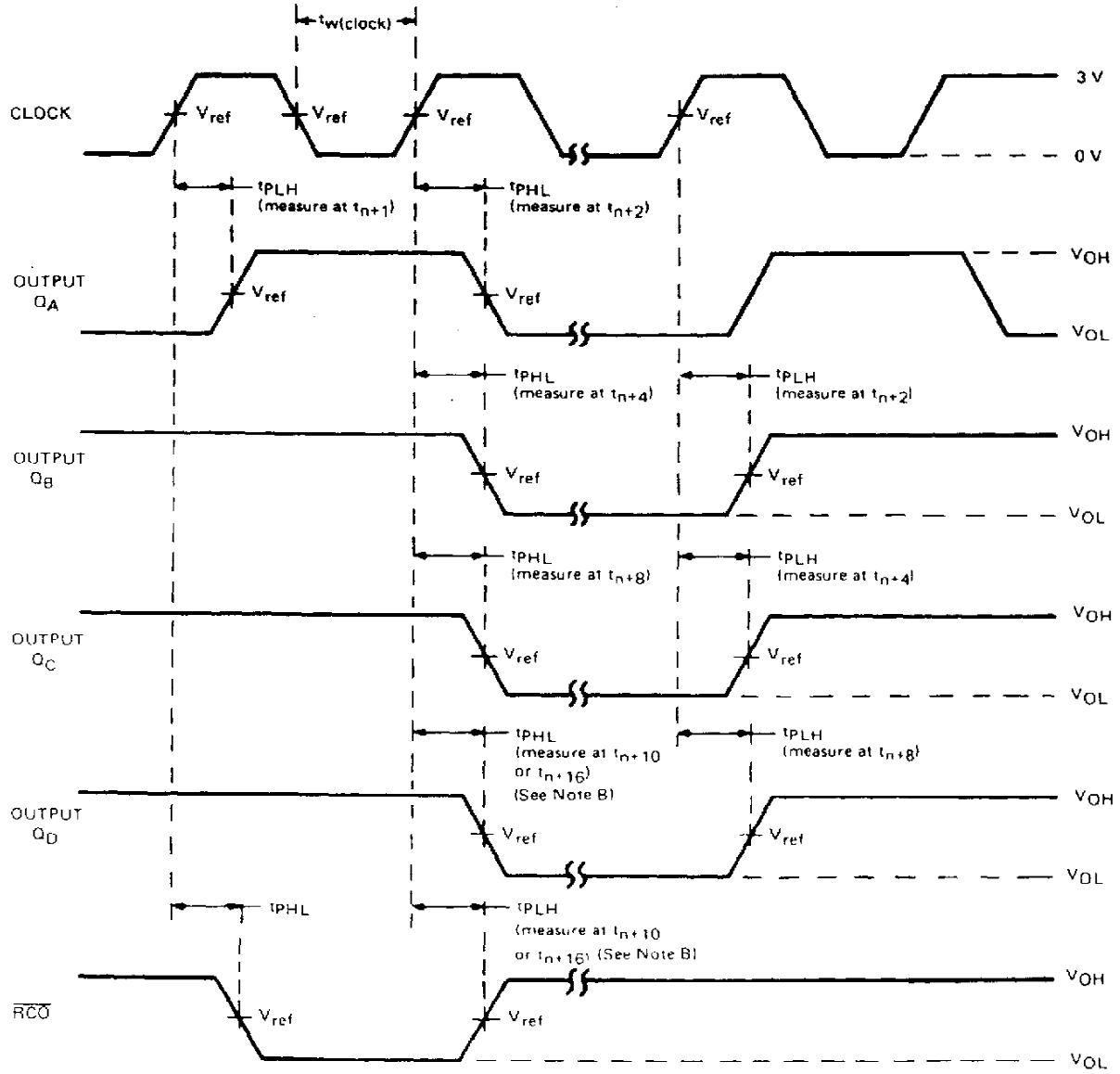
B. $t_{PLH}$ and $t_{PHL}$ from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count ($Q_A$ and $Q_D$ high for 'LS668, all Q outputs high for 'LS669).

C. $V_{ref} = 1.3$ V.

D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

## PARAMETER MEASUREMENT INFORMATION




UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $Z_{out}$ = 50 Ω, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure $f_{max}$.

B. Outputs $Q_D$ and carry are tested at $t_{n+10}$ for the 'LS668, and at $t_{n+16}$ for the 'LS669, where $t_n$ is the bit-time when all outputs are low.

C. $V_{ref}$ = 1.3 V.

FIGURE 3 PROPAGATION DELAY TIMES FROM CLOCK

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.