

**SN54LS377, SN54LS378, SN54LS379,
SN74LS377, SN74LS378, SN74LS379**
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE
SDLS167

OCTOBER 1976 — REVISED MARCH 1988

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
 Buffer/Storage Registers
 Shift Registers
 Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

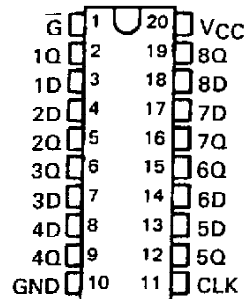
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input \bar{G} is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the \bar{G} input.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

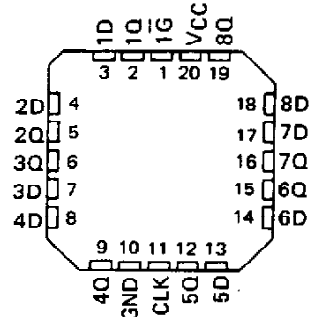
**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS			OUTPUTS	
\bar{G}	CLOCK	DATA	Q	\bar{Q}
H	X	X	Q_0	\bar{Q}_0
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	\bar{Q}_0

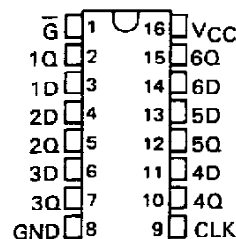
**SN54LS377 . . . J PACKAGE
SN74LS377 . . . DW OR N PACKAGE
(TOP VIEW)**



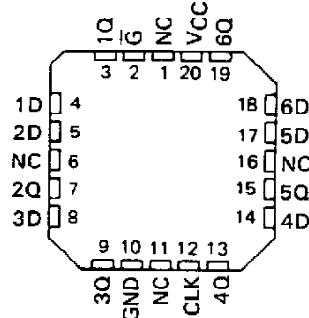
**SN54LS377 . . . FK PACKAGE
(TOP VIEW)**



**SN54LS378 . . . J OR W PACKAGE
SN74LS378 . . . D OR N PACKAGE
(TOP VIEW)**



**SN54LS378 . . . FK PACKAGE
(TOP VIEW)**



NC - No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

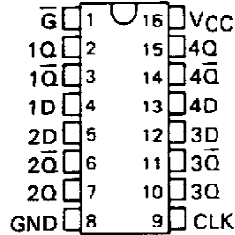


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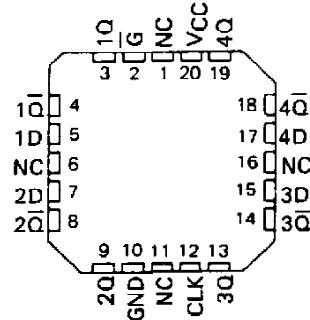
SN54LS379 . . . J OR W PACKAGE
SN74LS379 . . . D OR N PACKAGE

(TOP VIEW)



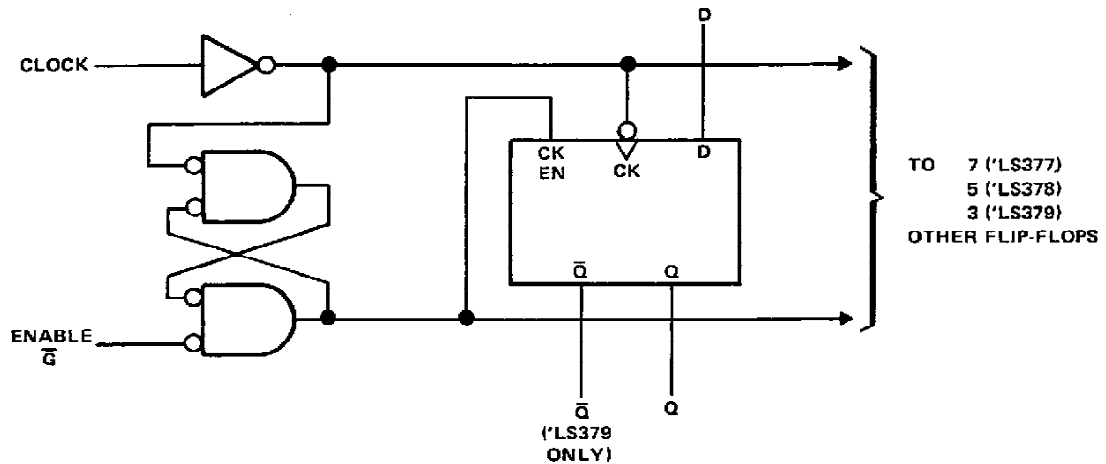
SN54LS379 . . . FK PACKAGE

(TOP VIEW)

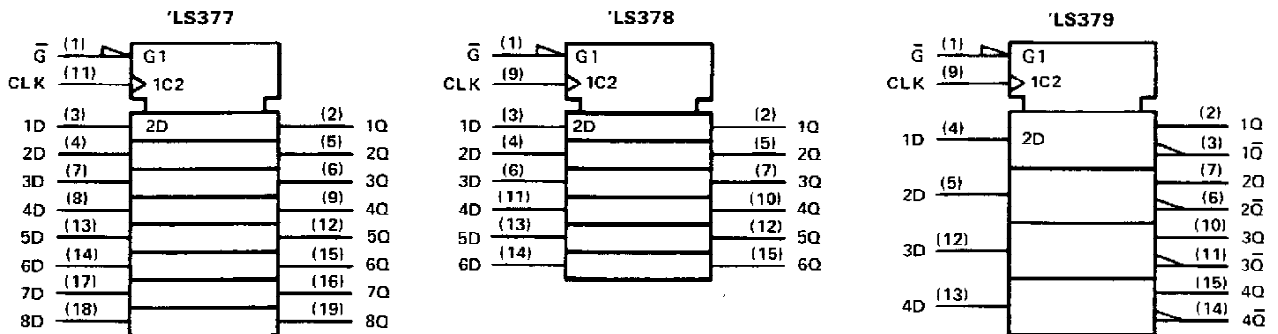


NC - No internal connection

logic diagram (positive logic)



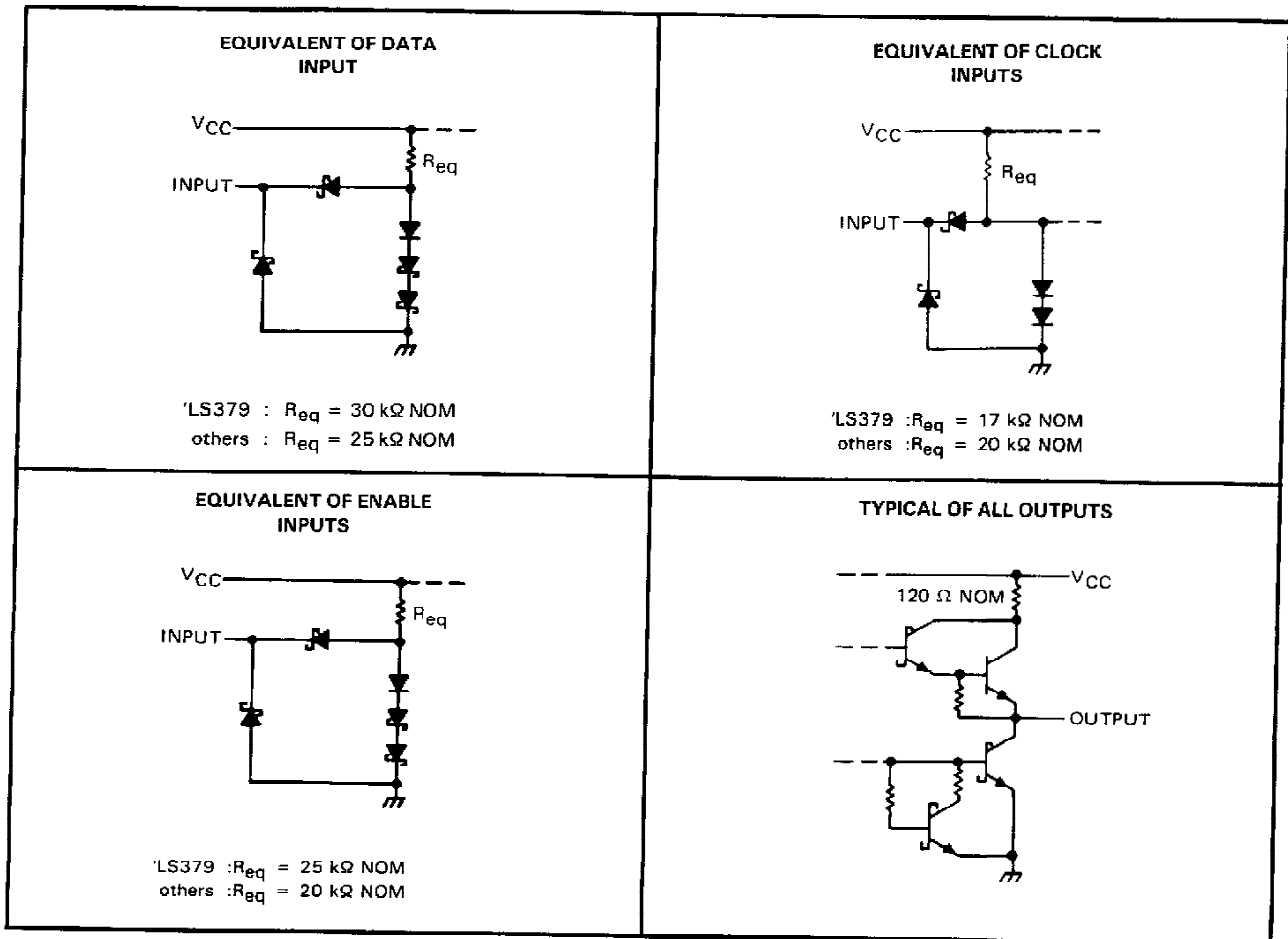
logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

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schematics of inputs and outputs



absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS*	-55°C to 125°C
SN74LS*	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**SN54LS377, SN54LS378, SN54LS379,
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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	20			20			ns
Setup time, t_{SU}	Data input	20†		20†			ns
	Enable active-state	25†		25†			
	Enable inactive-state	10†		10†			
Hold time, t_H		5†			5†		ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT
		MIN	TYP‡	MAX	MIN	
V_{IH} High-level input voltage		2		2		V
V_{IL} Low-level input voltage						0.8
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5		-1.5
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5			2.7 3.5
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}$			0.25	0.4	0.25 0.4
						0.35 0.5
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1		0.1
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		20
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4		-0.4
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100		-20 -100
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS377	17	28		17 28
		'LS378	13	22		13 22
		'LS379	9	15		9 15

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and ground applied to all data and enable inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$	30	40		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clock	$R_L = 2 \text{ k}\Omega$		17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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