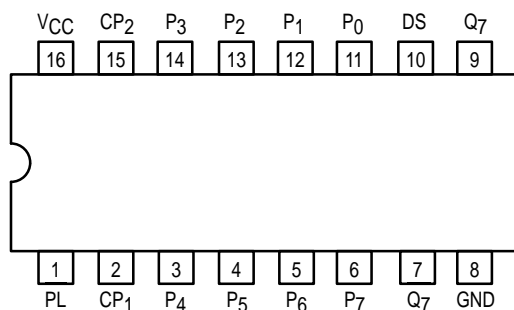




# 8-BIT PARALLEL-TO-SERIAL SHIFT REGISTER

The SN54/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load (PL) input is LOW. With PL HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

### CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

CP <sub>1</sub> , CP <sub>2</sub>	Clock (LOW-to-HIGH Going Edge) Inputs
DS	Serial Data Input
PL	Asynchronous Parallel Load (Active LOW) Input
P <sub>0</sub> -P <sub>7</sub>	Parallel Data Inputs
Q <sub>7</sub>	Serial Output from Last State (Note b)
Q <sub>7</sub>	Complementary Output (Note b)

### LOADING (Note a)

	HIGH	LOW
CP <sub>1</sub> , CP <sub>2</sub>	0.5 U.L.	0.25 U.L.
DS	0.5 U.L.	0.25 U.L.
PL	1.5 U.L.	0.75 U.L.
P <sub>0</sub> -P <sub>7</sub>	0.5 U.L.	0.25 U.L.
Q <sub>7</sub>	10 U.L.	5 (2.5) U.L.
Q <sub>7</sub>	10 U.L.	5 (2.5) U.L.

### NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

### TRUTH TABLE

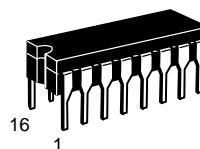
PL	CP		CONTENTS								RESPONSE
	1	2	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	
L	X	X	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>	Parallel Entry
H	L	↗	DS	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Right Shift
H	H	↗	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	No Change
H	↗	L	DS	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Right Shift
H	↗	H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	No Change

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

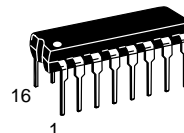
## SN54/74LS165

### 8-BIT PARALLEL-TO-SERIAL SHIFT REGISTER

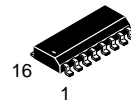
#### LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

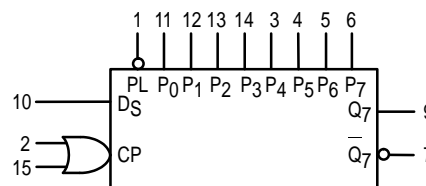


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic  
SN74LSXXXD SOIC

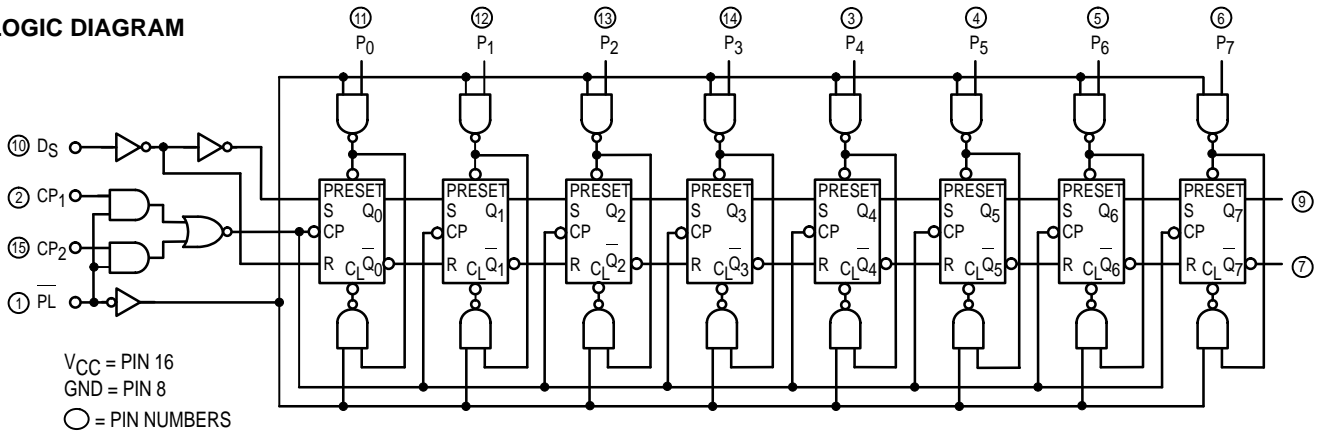
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN54/74LS165

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The SN54/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the PL signal is LOW. The parallel data can change while PL is LOW, provided that the recommended setup and hold times are observed.

For clock operation, PL must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by

applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
$T_A$	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
$I_{OH}$	Output Current — High	54, 74			-0.4	mA
$I_{OL}$	Output Current — Low	54			4.0	mA
		74			8.0	

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage			-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5		V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V		
I <sub>IH</sub>	Input HIGH Current Other Inputs PL Input				20 60	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
	Other Inputs PL Input				0.1 0.3	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current Other Inputs PL Input				-0.4 -1.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)		-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current				36	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
f <sub>MAX</sub>	Maximum Input Clock Frequency		25	35		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay PL to Output			22 22	35 35	ns		
	Propagation Delay Clock to Output			27 28	40 40	ns		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>7</sub> to Q <sub>7</sub>			14 21	25 30	ns		
	Propagation Delay P <sub>7</sub> to Q <sub>7</sub>			21 16	30 25	ns		

# SN54/74LS165

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	CP Clock Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
$t_W$	PL Pulse Width	15			ns	
$t_S$	Parallel Data Setup Time	10			ns	
$t_S$	Serial Data Setup Time	20			ns	
$t_S$	CP <sub>1</sub> to CP <sub>2</sub> Setup Time <sup>1</sup>	30			ns	
$t_H$	Hold Time	0			ns	
$t_{rec}$	Recovery Time, PL to CP	45			ns	

<sup>1</sup> The role of CP<sub>1</sub> and CP<sub>2</sub> in an application may be interchanged.

### DEFINITION OF TERMS:

**SETUP TIME ( $t_S$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_H$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the PL pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

### AC WAVEFORMS

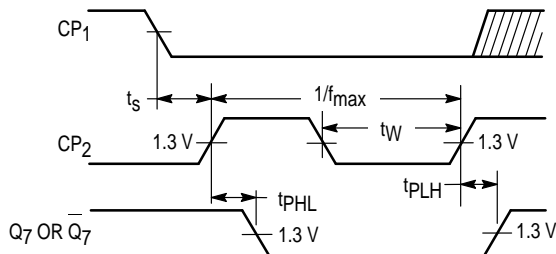


Figure 1

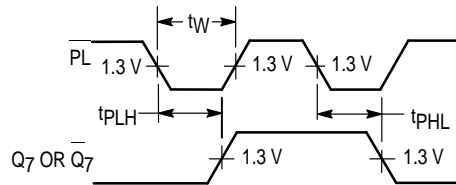


Figure 2

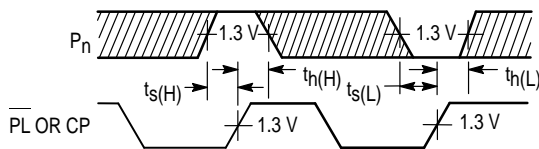


Figure 3

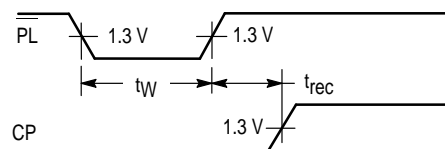


Figure 4