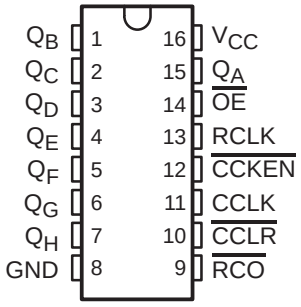
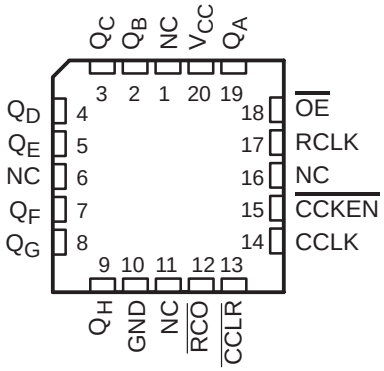
- **8-Bit Counter With Register**
- **High-Current 3-State Parallel Register Outputs Can Drive up to 15 LSTTL Loads**
- **Counter Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D, DW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC590A . . . J OR W PACKAGE
SN74HC590A . . . D, DW, OR N PACKAGE
(TOP VIEW)



SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

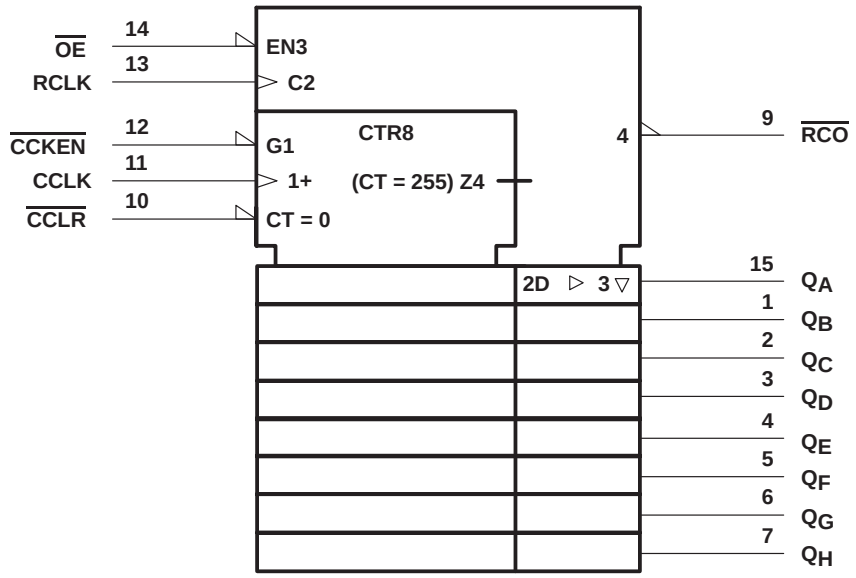
The ’HC590A contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear ($\overline{\text{CCLR}}$) and count-enable ($\overline{\text{CCKEN}}$) inputs. A ripple-carry output ($\overline{\text{RCO}}$) is provided for cascading. Expansion is easily accomplished for two stages by connecting $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{\text{RCO}}$ of each stage to the counter clock (CCLK) input of the following stage.

Both CCLK and the register clock (RCLK) input are positive-edge triggered. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The SN54HC590A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC590A is characterized for operation from –40°C to 85°C.

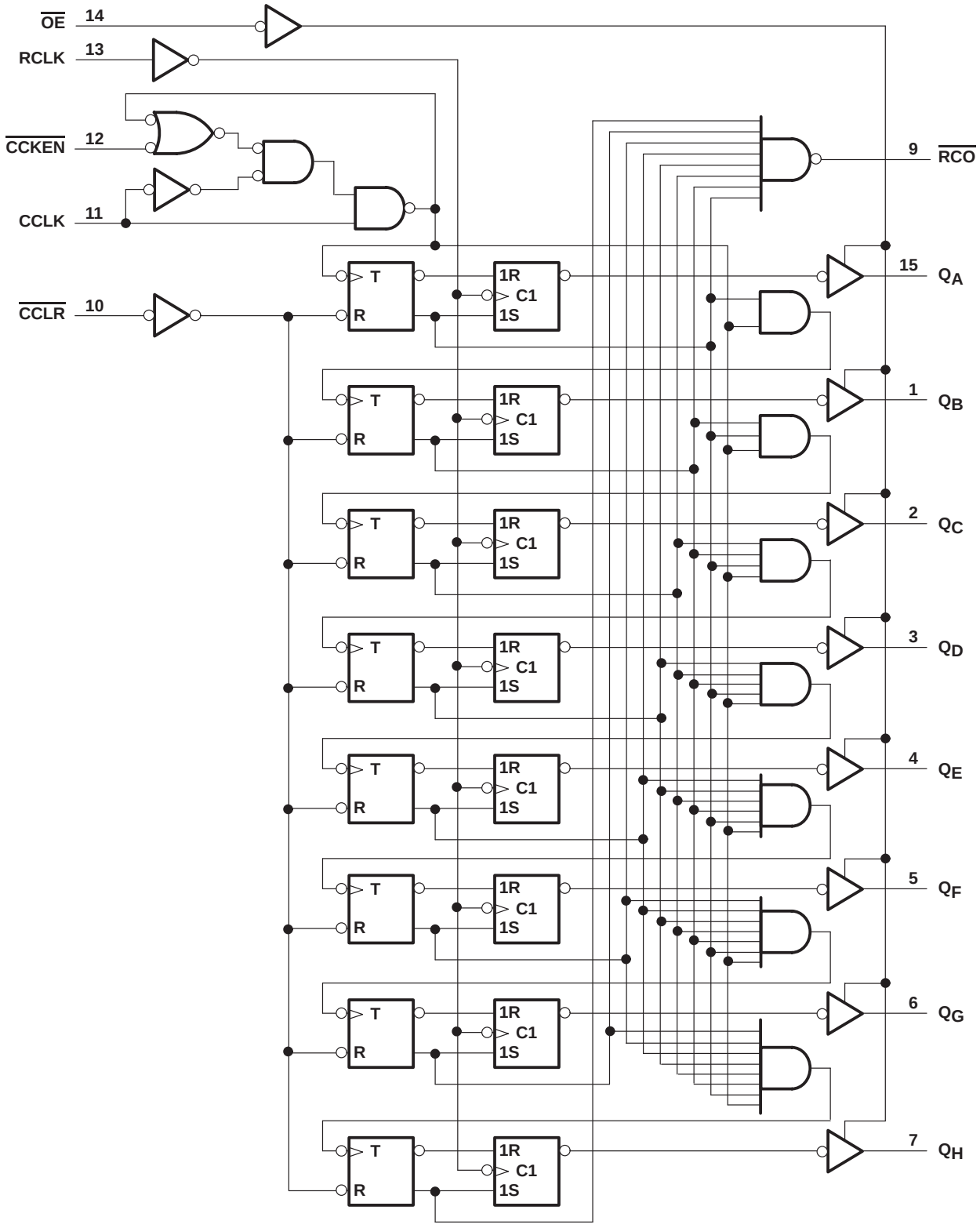
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
DW package . . . . . 105°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC590A			SN74HC590A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$\overline{RCO}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		Q_A–Q_H, I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
		$\overline{RCO}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
		Q_A–Q_H, I_{OH} = –7.8 mA		5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$\overline{RCO}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
		$\overline{RCO}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V			±0.01		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC590A		SN74HC590A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4	0	2.5	0	3.2	MHz
			4.5 V	0	20	0	13		16	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	CCLK or RCLK high or low	2 V	125		200		155		ns
			4.5 V	25		38		31		
			6 V	21		32		26		
		$\overline{CCLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCLK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		$\overline{CCLR}$ high (inactive) before CCLK↑	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
		CCLK↑ before RCLK↑†	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time	$\overline{CCKEN}$ low after CCLK↑	2 V	50		75		60		ns
			4.5 V	10		15		12		
			6 V	9		13		11		

† This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			2 V	4	8		2.5		MHz
			4.5 V	20	35		13		
			6 V	24	40		16		
t_{pd}	CCLK↑	$\overline{RCO}$	2 V		80	150		225	ns
			4.5 V		20	31		45	
			6 V		15	26		38	
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$	2 V		70	130		195	ns
			4.5 V		18	28		39	
			6 V		14	23		33	
t_{pd}	RCLK↑	Q	2 V		70	140		210	ns
			4.5 V		18	31		42	
			6 V		14	25		36	
t_{en}	$\overline{OE}$↓	Q	2 V		80	125		185	ns
			4.5 V		20	30		37	
			6 V		15	28		31	
t_{dis}	$\overline{OE}$↑	Q	2 V		80	125		185	ns
			4.5 V		20	30		37	
			6 V		15	28		31	
t_t*		$\overline{RCO}$	2 V		38	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	
		Q	2 V		38	60		90	
			4.5 V		8	12		18	
			6 V		6	10		15	

* This parameter is not production tested for the SN54HC590A.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			2 V	4	8		3.2		MHz
			4.5 V	20	35		16		
			6 V	24	40		19		
t_{pd}	CCLK↑	$\overline{RCO}$	2 V		80	150		190	ns
			4.5 V		20	30		38	
			6 V		15	26		33	
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$	2 V		70	130		165	ns
			4.5 V		18	26		33	
			6 V		14	22		28	
t_{pd}	RCLK↑	Q	2 V		70	140		175	ns
			4.5 V		18	28		35	
			6 V		14	24		30	
t_{en}	$\overline{OE}$↓	Q	2 V		80	125		155	ns
			4.5 V		20	25		31	
			6 V		15	21		26	
t_{dis}	$\overline{OE}$↑	Q	2 V		80	125		155	ns
			4.5 V		20	25		31	
			6 V		15	21		26	
t_t		$\overline{RCO}$	2 V		38	75		95	ns
			4.5 V		8	15		19	
			6 V		6	13		16	
		Q	2 V		38	60		75	
			4.5 V		8	12		15	
			6 V		6	10		13	

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A				UNIT
				T_A = 25°C			MIN	MAX
				MIN	TYP	MAX		
t_{pd}	RCLK↑	Q	2 V		100	300		447	ns
			4.5 V		24	60		90	
			6 V		20	51		77	
t_{en}	$\overline{OE}$	Q	2 V		90	200		300	ns
			4.5 V		23	40		60	
			6 V		19	34		51	
t_t*		Q	2 V		45	210		315	ns
			4.5 V		17	42		63	
			6 V		13	36		53	

* This parameter is not production tested for the SN54HC590A.

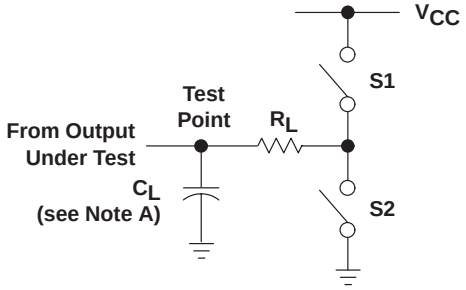
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A				UNIT
				T_A = 25°C			MIN	MAX
				MIN	TYP	MAX		
t_{pd}	RCLK↑	Q	2 V		100	300		380	ns
			4.5 V		24	60		76	
			6 V		20	51		65	
t_{en}	$\overline{OE}$	Q	2 V		90	200		250	ns
			4.5 V		23	40		50	
			6 V		19	34		43	
t_t		Q	2 V		45	210		265	ns
			4.5 V		17	42		53	
			6 V		13	36		45	

operating characteristics, T_A = 25°C

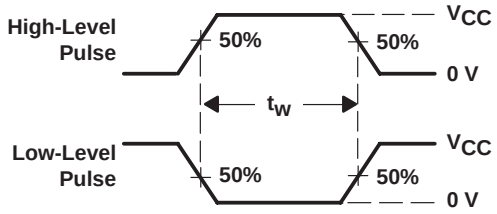
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	250	pF

PARAMETER MEASUREMENT INFORMATION

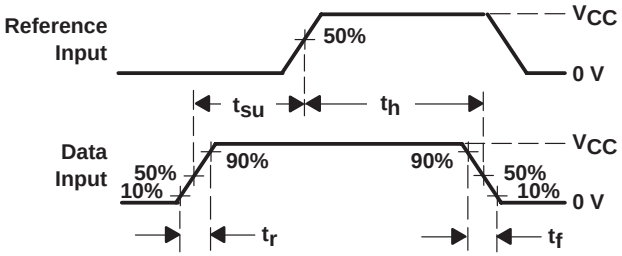


LOAD CIRCUIT

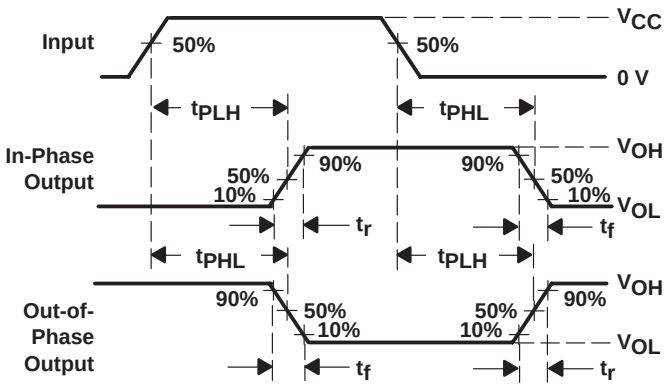
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



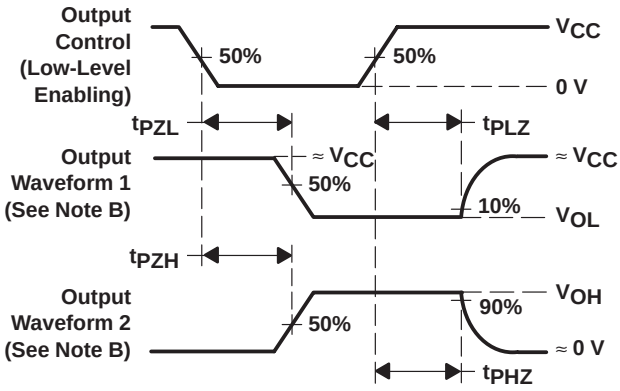
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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