

High Speed CMOS Logic 14-Stage Binary Counter with Oscillator

Features

- Onboard Oscillator
- Common Reset
- Negative Edge Clocking
- Typical $f_{MAX} = 50\text{MHz}$ at $V_{CC} = 5\text{V}$, $C_L = 15\text{pF}$, $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{V}$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8\text{V}$ (Max), $V_{IH} = 2\text{V}$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu\text{A}$ at V_{OL} , V_{OH}

Description

The 'HC4060 and 'HCT4060 each consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which

resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕI (and ϕO). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse-line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section the HCT4060 input pulse switch points are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.

Ordering Information

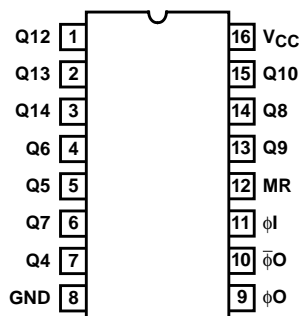
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4060F3A	-55 to 125	16 Ld CERDIP
CD74HC4060E	-55 to 125	16 Ld PDIP
CD74HC4060M	-55 to 125	16 Ld SOIC
CD54HCT4060F3A	-55 to 125	16 Ld CERDIP
CD74HCT4060E	-55 to 125	16 Ld PDIP
CD74HCT4060M	-55 to 125	16 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinout

CD54HC4060, CD54HCT4060
(CERDIP)
CD74HC4060, CD74HCT4060
(PDIP, SOIC)
TOP VIEW



Functional Diagram

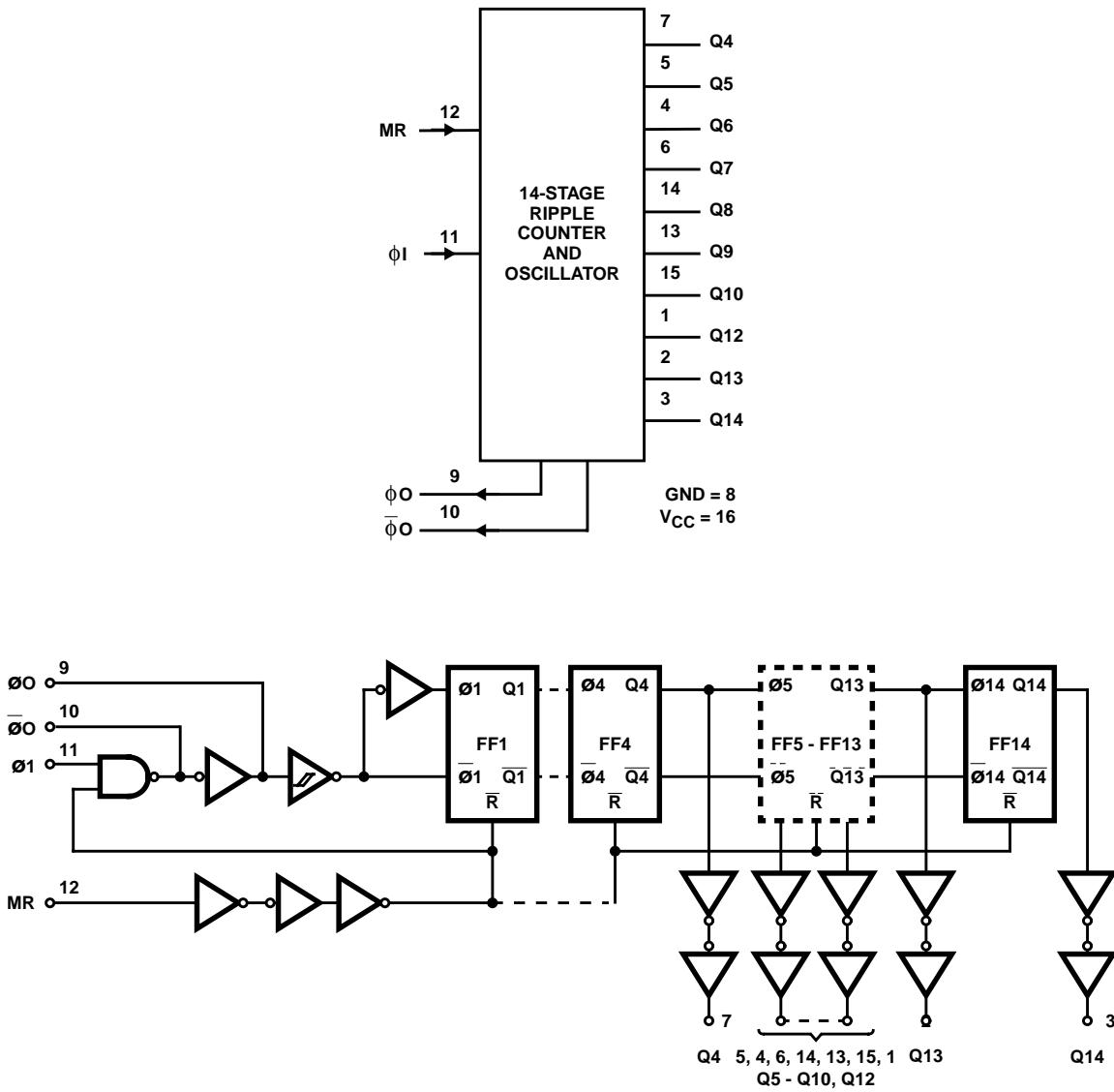


FIGURE 1. LOGIC BLOCK DIAGRAM

TRUTH TABLE

ϕ_1	MR	OUTPUT STATE
\uparrow	L	No Change
\downarrow	L	Advance to Next State
X	H	All Outputs are Low

CD54/74HC4060, CD54/74HCT4060

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	160
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T_A	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage Q Outputs CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage Q Outputs TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage Q Outputs CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage Q Outputs TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage ϕO Output (Pin 10) CMOS Loads	V_{OH}	V_{CC} or GND	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V

CD54/74HC4060, CD54/74HCT4060

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) TTL Loads Note 6	V _{OH}	V _{CC} or GND	-2.6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-3.3	6	5.48	-	-	5.34	-	5.2	-	V
Low-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) CMOS Loads	V _{OL}	V _{CC} or GND	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) TTL Loads	V _{OL}	V _{CC} or GND	2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
			3.3	6	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage ϕ O Output (Pin 9) TTL Loads	V _{OH}	V _{IL} or V _{IH}	-3.2	4.5	3.98	-	-	3.84	-	3.7	-	V
			-4.2	6	5.48	-	-	5.34	-	5.2	-	V
Low-Level Output Voltage ϕ O Output (Pin 9) TTL Loads	V _{OL}	V _{IL} or V _{IH}	-2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
			-3.3	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage Q Outputs CMOS Loads	V _{OH}	V _{IH} or V _{IL} Note 5	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage Q Outputs TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage Q Outputs CMOS Loads	V _{OL}	V _{IH} or V _{IL} Note 5	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage Q Outputs TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) CMOS Loads	V _{OH}	V _{CC} or GND	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) TTL Loads Note 6	V _{OH}	V _{CC} or GND	-2.6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) CMOS Loads	V _{OL}	V _{CC} or GND	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V

CD54/74HC4060, CD54/74HCT4060

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Low-Level Output Voltage $\bar{\phi}$ O Output (Pin 10) TTL Loads	V _{OL}	V _{CC} or GND	2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage ϕ O Output (Pin 9) TTL Loads	V _{OH}	V _{IL} or V _{IH}	-3.2	4.5	3.98	-	-	3.84	-	3.7	-	V
Low-Level Output Voltage ϕ O Output (Pin 9) TTL Loads	V _{OL}	V _{IH} or V _{IL} Note 5	3.2	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	Any Voltage Between V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 4)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTES:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.
5. For pin 11 V_{IH} = 3.15V, V_{IL} = 0.9V.
6. Limits not valid when pin 12 (instead of pin 11) is used as control input.

HCT Input Loading Table

INPUT	UNIT LOADS
MR	0.35

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g. 360μA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Maximum Input Pulse Frequency	t _{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Input Pulse Width	t _W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Removal Time	t _{REM}	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns

CD54/74HC4060, CD54/74HCT4060

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Reset Pulse Width	t _W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
HCT TYPES												
Maximum Input, Pulse Frequency	t _{MAX}	4.5	30	-	-	25	-	-	20	-	-	MHz
Input Pulse Width	t _W	4.5	16	-	-	20	-	-	24	-	-	ns
Reset Removal Time	t _{REM}	4.5	26	-	-	33	-	-	39	-	-	ns
Reset Pulse Width	t _W	4.5	25	-	-	31	-	-	38	-	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay φI to Q4	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	51	-	64	-	78	ns
Q _n to Q _{n+1}	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	80	-	100	-	120	ns
			4.5	-	-	16	-	20	-	24	ns
		C _L = 15pF	5	-	6	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	14	-	17	-	20	ns
MR to Q _n	t _{PHL}	C _L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	45	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _I (TBD)										
Propagation Dissipation Capacitance	C _{PD}	-	-	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay φI to Q4	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	-	-	-	-	-	-ns
			4.5	-	-	66	-	83	-	100	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	-ns
		C _L = 50pF	6	-	-	-	-	-	-	-	-ns

CD54/74HC4060, CD54/74HCT4060

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Q_n to Q_{n+1}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	-	-	-	-	-	ns
			4.5	-	-	16	-	20	-	24	ns
		$C_L = 15\text{pF}$	5	-	6	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	-	-	-	-	-	ns
MR to Q_n	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	-	-	-	-	-	ns
			4.5	-	-	44	-	55	-	66	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	-	-	-	-	-	ns
Output Transition Time	t_{THL}, t_{TLH}	$C_L = 50\text{pF}$	2	-	-	-	-	-	-	-	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	-	-	-	-	-	ns
Input Capacitance	C_I (TBD)										
Propagation Dissipation Capacitance	C_{PD}	-	-	-	40	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i \sum (C_L V_{CC}^2 f_i / M)$ where $M = 2^1, 2^2, 2^3, \dots, 2^{14}$, f_i = input frequency, C_L = output load capacitance.

TYPICAL LIMIT VALUES FOR R_X AND C_X

PARAMETER	TEST CONDITIONS	VOLTAGE	TYPICAL MAXIMUM LIMITS
R_X Minimum	$C_X > 1000\text{pF}$	2	1K Ω
	$C_X > 10\text{pF}$	4.5	
	$C_X > 10\text{pF}$	6	
R_X Maximum	$C_X > 10\text{pF}$	2	20M Ω
	$C_X > 10\text{pF}$	4.5	
	$C_X > 10\text{pF}$	6	
C_X Minimum	$R_X > 10\text{K}\Omega$	2	10pF
	$R_X > 10\text{K}\Omega$	4.5	
	$R_X > 10\text{K}\Omega$	6	
	$R_X = 1\text{K}\Omega$	2	1000pF
	$R_X = 1\text{K}\Omega$	4.5	10pF
	$R_X = 1\text{K}\Omega$	6	10pF
Maximum Astable Oscillator Frequency	$C_X = 1000\text{pF}$, $R_X = 1\text{K}\Omega$	2	0.5MHz (Note 9)
	$C_X = 100\text{pF}$, $R_X = 1\text{K}\Omega$	4.5	3MHz (Note 9)
	$C_X = 100\text{pF}$, $R_X = 1\text{K}\Omega$	6	3MHz (Note 9)

NOTE:

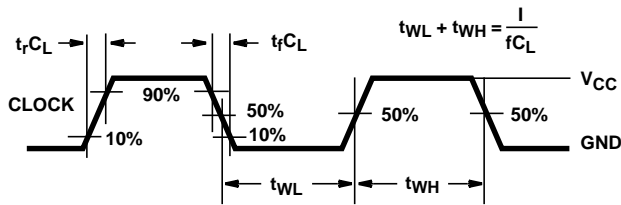
- At very high frequencies $f = 1/2.2 R_X C_X$ no longer gives an accurate approximation.



NOTE: OSC Frequency $\approx 1/2.2 R_X C_X$
For $1\text{M}\Omega > R_X > 1\text{K}\Omega$, $C_X > 10\text{pF}$, $f < 1\text{MHz}$

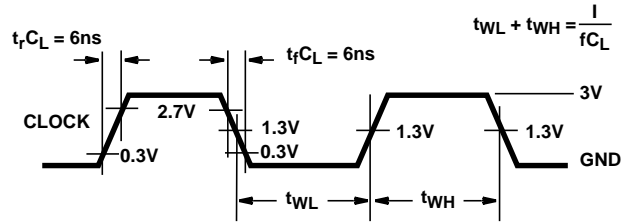
FIGURE 2. FREQUENCY OF ON-BOARD OSCILLATOR AS A FUNCTION OF C_X AND R_X

Typical Performance Curves



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



FIGURE 5. HC AND HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.