EPSON

SED1520 Series

Dot Matrix LCD Controller Driver

- Ultra Low Power Consumption
- Built-in Video RAM

■ DESCRIPTION

The SED1520 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations
The SED1520 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The SED1520 which is able to drive two lines of twelve characters each.
- The SED1521 which is able to drive 80 segments for extention.
- The SED1522 which is able to drive one line of thirteen characters each.

■ FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  $V_{DD} – V_{SS}$: –2.4 to –7.0 V
  $V_{DD} – V_5$: –3.5 to –13.0 V
- Low-power CMOS

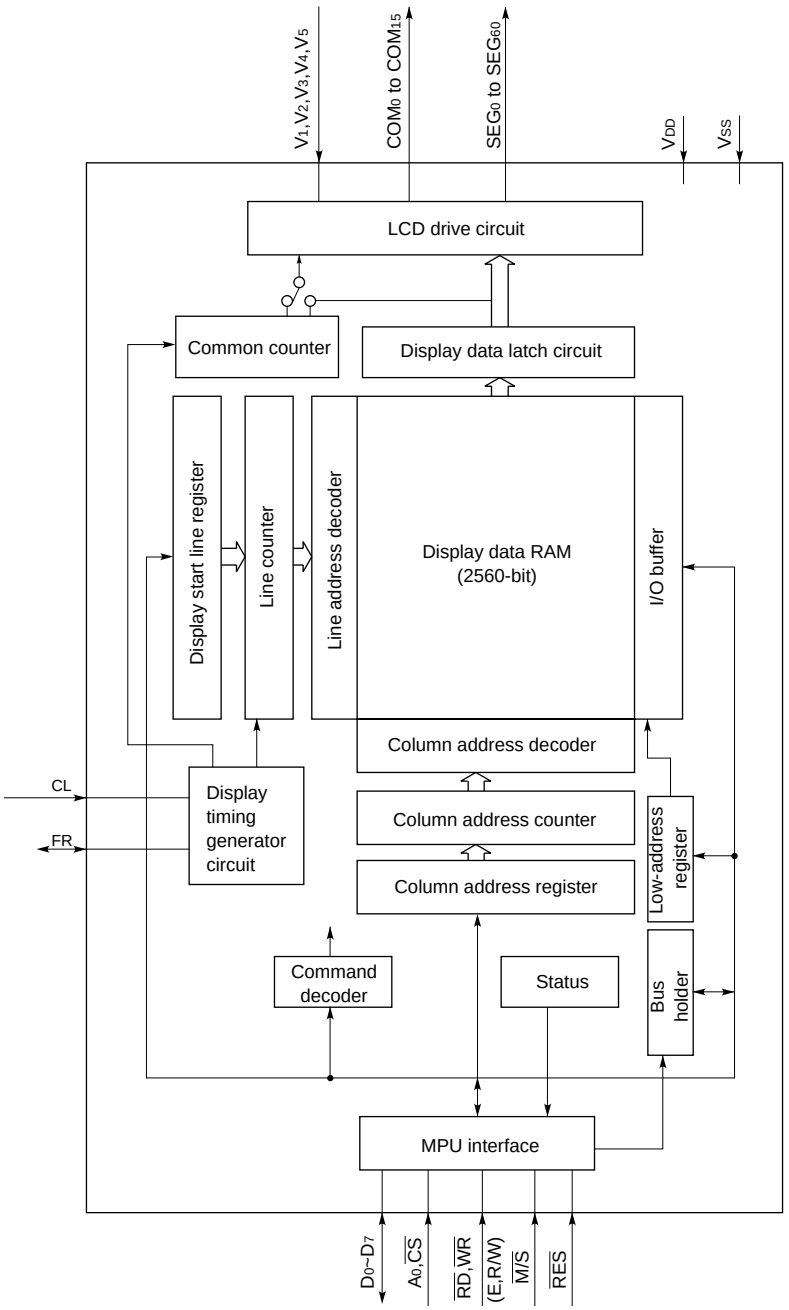
■ LINE-UP

Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers	Duty
	On-Chip	External				
SED1520*0*	18 kHz	18 kHz	SED1520*0*, SED1521*0*	61	16	1/16, 1/32
SED1521*0*	—	18 kHz	SED1520*0*, SED1522*0*	80	0	1/8 to 1/32
SED1522*0*	18 kHz	18 kHz	SED1522*0*, SED1521*0*	69	8	1/8, 1/16
SED1520*A*	—	2 kHz	SED1520*A*, SED1521*A*	61	16	1/16, 1/32
SED1521*A*	—	2 kHz	SED1520*A*, SED1522*A*	80	0	1/8 to 1/32
SED1522*A*	—	2 kHz	SED1522*A*, SED1521*A*	69	8	1/8, 1/16

- Package code (For example SED1520)
  SED1520T
  SED1520F**: PKG ┬ QFP5-100pin (plastic): SED1520F*A
  └ QFP15-100pin (plastic): SED1520F*C
  SED1520D**: Die form ┬ Al pad: SED1520D*A
  └ Au bump: SED1520D*B

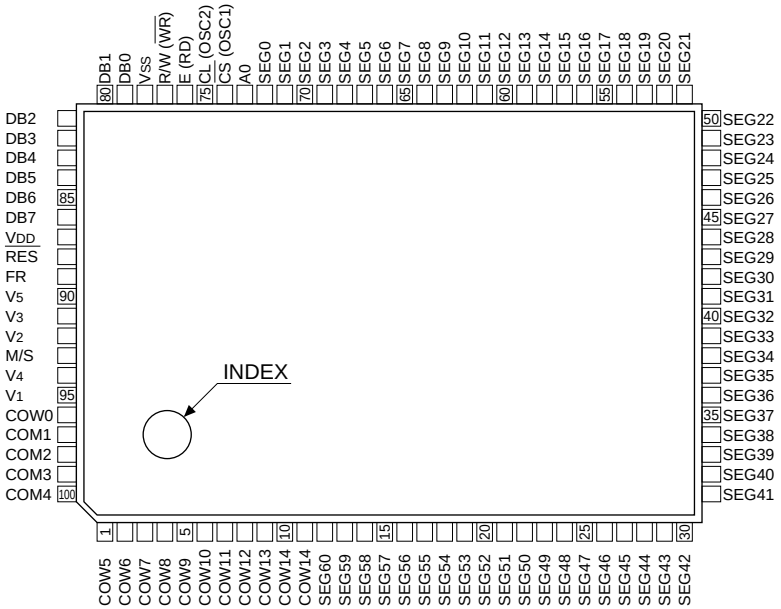
■ BLOCK DIAGRAM

An example of SED1520*AA:

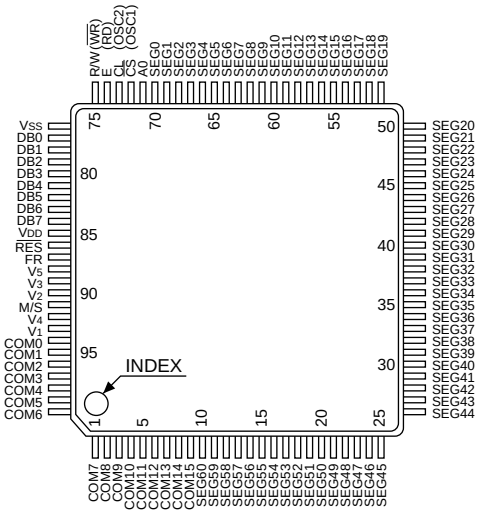


■ PACKAGE CONFIGURATION

QFP5-100pin



QFP15-100pin



Note: This is an example of SED1520F pin assignment. The modified pin names are given below.

Product Name	Pin/Pad Number					
	74	75	96 to 100, 1 to 11	93	94	95
SED1520F0A	OSC1	OSC2	COM0 to COM15*	M/S	V_4	V_1
SED1521F0A	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1522F0A	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
SED1520FAA	CS	CL	COM0 to COM15*	M/S	V_4	V_1
SED1521FAA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1522FAA	CS	CL	COM0 to 7, SEG68 to 61	M/S	V_4	V_1

SED1520: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.
SED1522: Common outputs COM0 to COM15 of the master LSI correspond to COM15 to COM8 of the slave LSI.

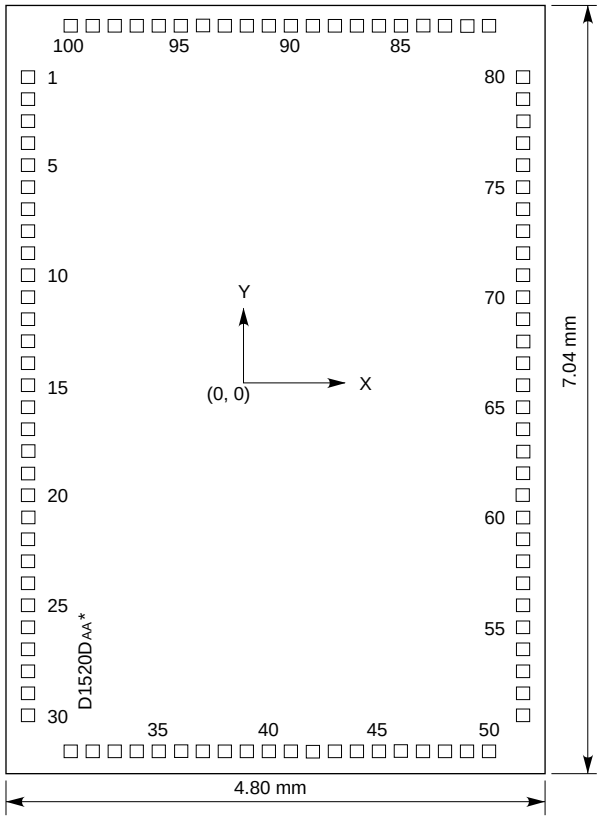
■ PAD LAYOUT

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 μm

Chip specifications of gold bump package

Chip size: 4.80×7.04×0.525 mm
Bump pitch: 199 μm (Min.)
Bump height: 22.5 μm (Typ.)
Bump size: 132×111 μm (±20 μm) for mushroom model
116×92 μm (±4 μm) for vertical model



Note: An example of SED1520DAA die numbers is given. These numbers are the same as the bump package.

■ PAD ARRANGEMENT

An example of SED1520DA* pin names is given. The asterisk (*) can be A for AL pad package or B for gold bump package.

SED1520DAB Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	COM8	159	5909
5	COM9	159	5709
6	COM10	159	5510
7	COM11	159	5310
8	COM12	159	5111
9	COM13	159	4911
10	COM14	159	4712
11	COM15	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	CS	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V_5	2499	6884
91	V_3	2300	6884
92	V_2	2100	6884
93	M/S	1901	6884
94	V_4	1701	6884
95	V_1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

The other SED1520 series packages have the different pin names as shown.

Package/Pad No.	74	75	96 to 100, 1 to 11	93	94	95
SED1520D0*	OSC1	OSC2	COM0 to COM15 *	M/S	V_4	V_1
SED1522D0*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
SED1522DA*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
SED1521D0*	$\overline{CS}$	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1521DA*	$\overline{CS}$	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{SS}	–8.0 to +0.3	V
Supply voltage (2)	V_5	–16.5 to +0.3	V
Supply voltage (3)	V_1, V_4, V_2, V_3	V5 to +0.3	V
Input voltage	V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature time at lead	T_{sol}	260, 10	°C, sec

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must be always hold
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

● DC Characteristics

(Ta = –20 to 75 °C, V_{DD} = 0 V unless stated otherwise)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Operating voltage (1) *1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_5			–13.0	—	–3.5	V	V_5 *10.
	Allowable				–13.0	—	—		
	Allowable	V_1, V_2			0.6×V_5	—	V_{DD}	V	V_1, V_2
	Allowable	V_3, V_4			V5	—	0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	*2, *3
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		
		V_{IHT}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		*2, *3
		V_{IHC}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		
Low-level input voltage		V_{ILT}			V_{SS}		V_{SS}+0.8		*2, *3
		V_{ILC}			V_{SS}		0.8×V_{SS}		
		V_{ILT}	V_{SS} = –3 V		V_{SS}		0.85×V_{SS}		*2, *3
		V_{ILC}	V_{SS} = –3 V		V_{SS}		0.8×V_{SS}		
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	OSC2 *4, *5
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		
		V_{OHT}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}			V	*4, *5 OSC2
		V_{OHC1}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}				
		V_{OHC2}	V_{SS} = –3 V	I_{OH} = –50 µA	0.2×V_{SS}				

(continued)

● **DC Characteristics (Cont'd)**

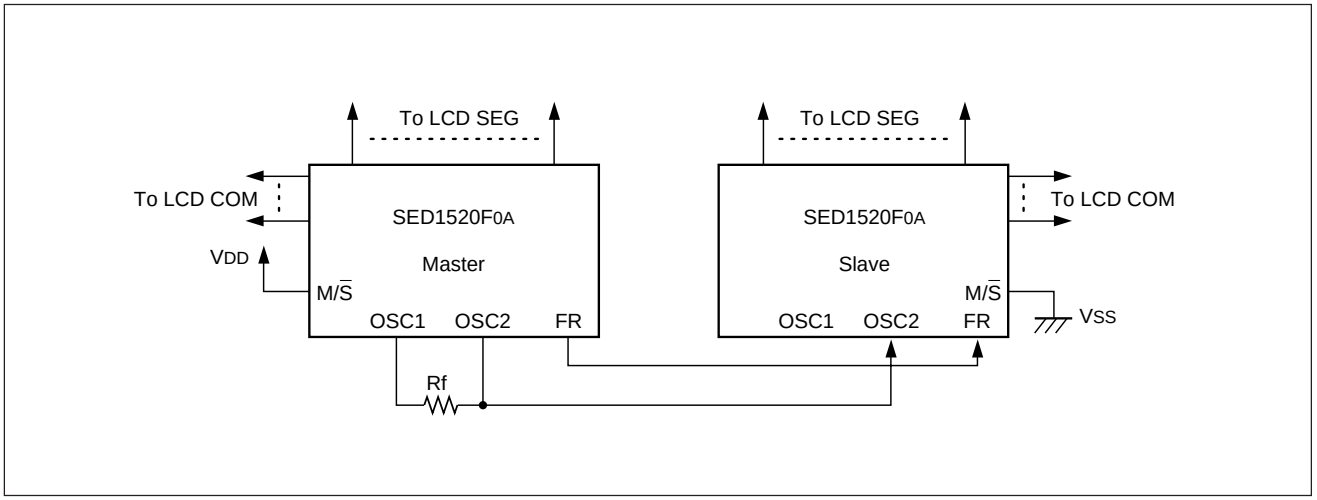
(Ta = –20 to 75 °C, V_{DD} = 0 V unless stated otherwise)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Low-level output voltage	V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS}+0.4	V	OSC2 *4, *5
	V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS}+0.4		
	V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×V_{SS}		
	V_{OLT}	V_{SS} = –3 V	I_{OL} = 2 mA			0.8×V_{SS}	V	*4, *5 OSC2
	V_{OLC1}	V_{SS} = –3 V	I_{OL} = 2 mA			0.8×V_{SS}		
	V_{OLC2}	V_{SS} = –3 V	I_{OL} = 50 µA			0.8×V_{SS}		
Input leakage current	I_{LI}			–1.0	—	1.0	µA	*6
Output leakage current	I_{LO}			–3.0	—	3.0	µA	*7
LCD driver ON resistance	R_{ON}	Ta = 25 °C	V_5 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, *11
			V_5 = –3.5 V	—	10.0	50.0		
Static current dissipation	I_{DDQ}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	I_{DD} (1)	During display V_5 = –5.0 V	f_{CL} = 2 kHz	—	2.0	5.0	µA	V_{DD} *12, *13, *14
			R_f = 1 MΩ	—	9.5	15.0		
			f_{CL} = 18 kHz	—	5.0	10.0		
		During display V_5 = –5 V V_{SS} = –3 V	f_{CL} = 2 kHz		1.5	4.5	µA	V_{DD} *12, *13
			Rf = 1 MΩ		6.0	12.0		
	I_{DD} (2)	During access t_{cyc} = 200 kHz		—	300	500	µA	*8
		V_{SS} = –3V, During access t_{cyc} = 200 kHz			150	300		
Input pin capacitance	C_{IN}	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	R_f = 1.0 MΩ ±2%, V_{SS} = –5.0 V		15	18	21	kHz	*9
		R_f = 1.0 MΩ ±2%, V_{SS} = –3.0 V		11	16	21		
Reset time	t_R			1.0	—		µS	$\overline{RES}$ *15

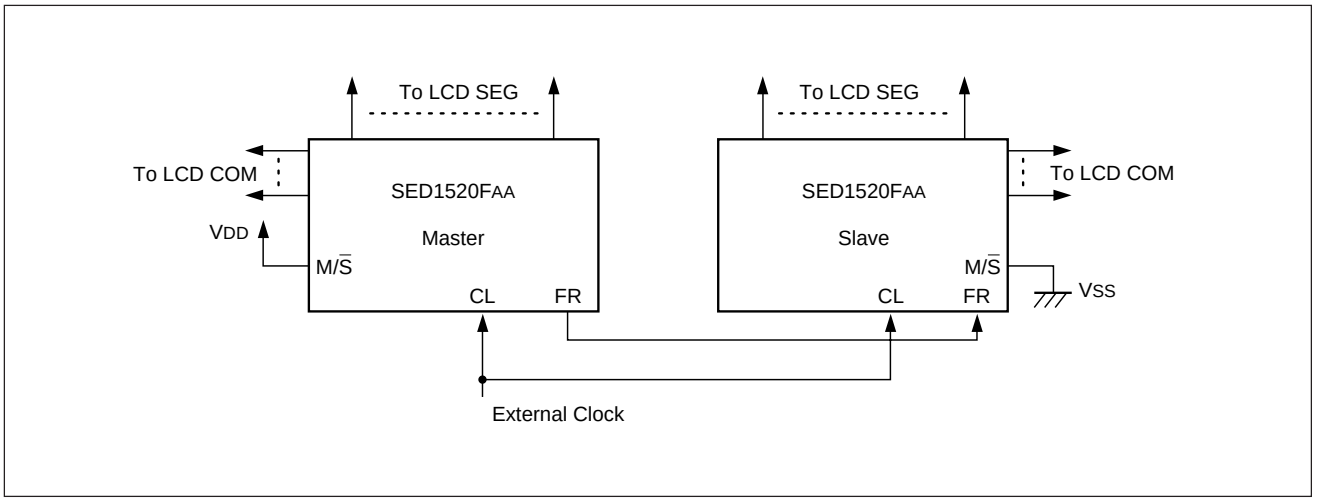
Notes: *1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
*2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
*3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
*4. D0 to D7
*5. FR
*6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/$\overline{S}$ and $\overline{RES}$
*7. When D0 to D7 and FR are high impedance.
*8. During continual write acess at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
*9. See figure below for details
*10. See figure below for details
*11. For a voltage differential of 0.1 V between input (V_1, …, V_4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
*12. SED1520$_{*A*}$ and SED1521$_{*A*}$ and SED1522$_{*A*}$ only. Does not include transient currents due to stray and panel capacitances.
*13. SED1520$_{*0*}$ and SED1522$_{*0*}$ only. Does not include transient currents due to stray and panel capacitances.
*14. SED1521$_{*0*}$ only. Does not include transient currents due to stray and panel capacitances.
*15. t_R (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the SED1520 series enters the normal operation status after this t_R.

■ LCD PANEL CONNECTION EXAMPLE

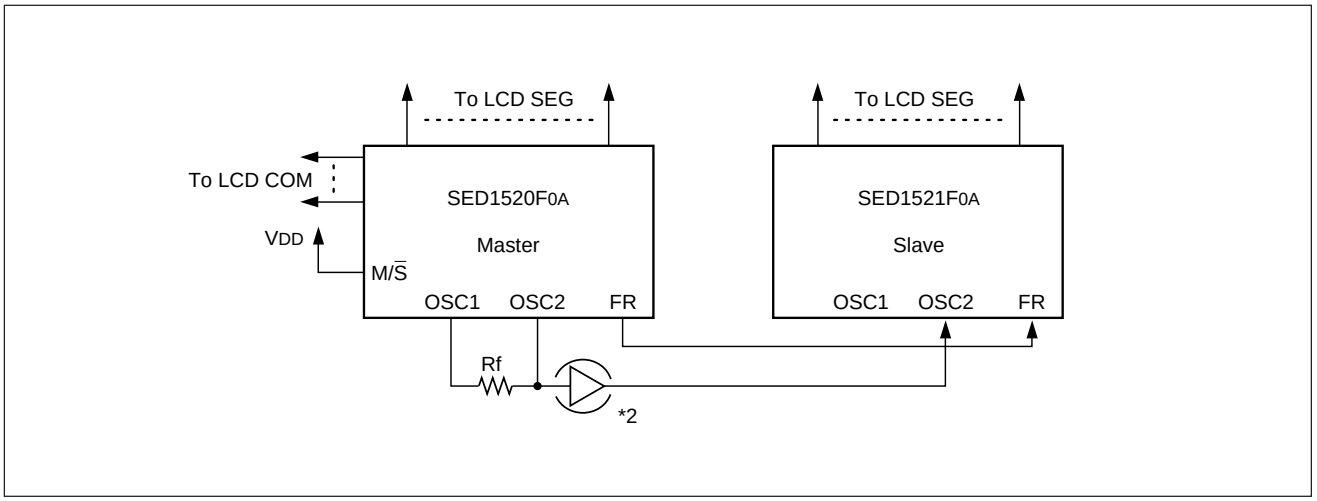
● SED1520F0A–SED1520F0A/SED1522F0A–SED1522F0A



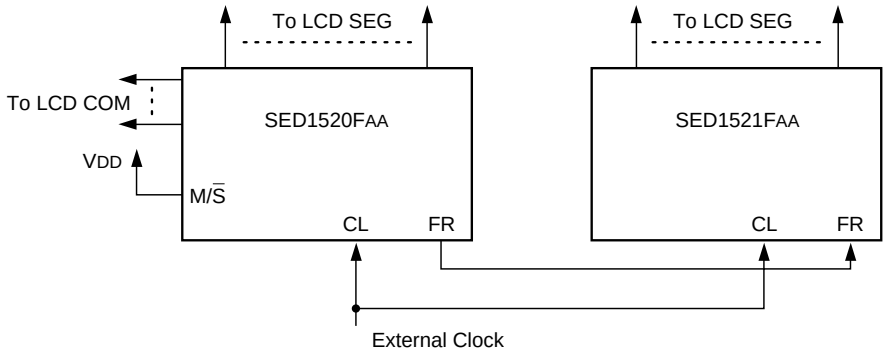
● SED1520FAA–SED1520FAA/SED1522FAA–SED1522FAA



● SED1520F0A/SED1522F0A–SED1521F0A (See note 1)



● **SED1520FAA–SED1521FAA**

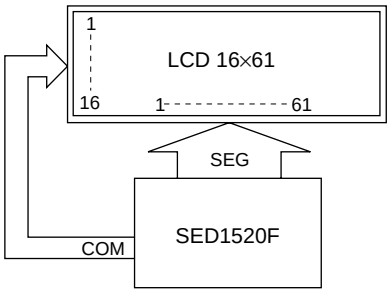


Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

■ LCD PANEL CONNECTION EXAMPLE
(The full-dot LCD panel displays a character in 6×8 dots.)

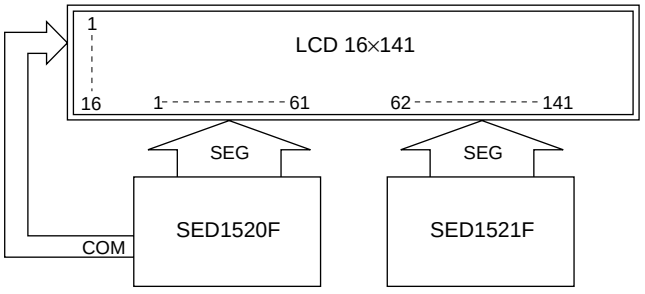
● **1/16 duty:**

• 10 characters × 2 lines



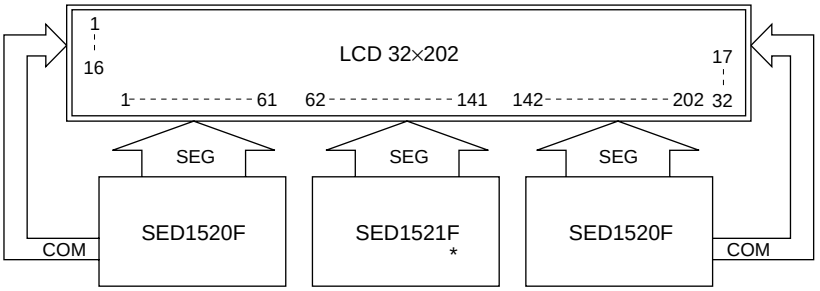
● **1/16 duty:**

• 23 characters × 2 lines



● **1/32 duty:**

• 33 characters × 4 lines



* The SED1521F can be omitted (the 32×122-dot display mode is selected).

Note: A combination of AB or AA type chip (that uses internal clocks) and 0B or 0A type chip (that uses external clocks) is NOT allowed.

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First issue December, 1994 Ⓢ
Printed in Japan