Master's Thesis

Vertical Heterostructure III-V Nanowire MOSFETs

Adam Jönsson

Department of Electrical and Information Technology,
Faculty of Engineering, LTH, Lund University, 2016.

Vertical Heterostructure III-V Nanowire MOSFETs

Adam Jönsson
adamkaffi@gmail.com

Department of Electrical and Information Technology
Lund University

Supervisors: Lars-Erik Wernersson & Olli-Pekka Kilpi

August 31, 2016

Printed in Sweden
E-huset, Lund, 2016

Abstract

"If cars had developed as fast as processors they would go at 470,000 mph, get 100,000 miles to the gallon, and cost 3 cents" claims Paul Ottelini, Intel CEO 2005-2013. This serves as a reminder of how fast the field of nanoelectronics is developing due to constant demand for faster and more energy efficient integrated circuits. The still ongoing electronics revolution was accelerated by the innovation of one simple and elegant device, namely the Si-based metal-oxide-semiconductor-field-effect-transisor MOSFET in 1959. The pillar of economic growth has since been based on downscaling the MOSFET and increasing the density of transistor per chip area. Downscaling of the transistor has favourably led to more efficient and faster devices. MOSFETs today are approaching sizes which only include few monolayers of atoms, basically dimensions of a few nanometer. Conventional electronics has thus been pushed into the quantum realm forcing future improvements to be based on innovation rather than simply downscaling. To win the battle against Heisenberg's uncertainty leading to leakage currents and various other effect due to reduced size, new 3d geometries has been introduced. Amongst these new geometries is the bottom up approach utilizing vertical nanowires. The vertical geometry also enables easier integration of alternative high mobility semiconductor materials on a Si substrate. A potential canditate for integration on Si is the III-V compound semiconductors due improvements in charge carrier transport capabilities.

To further motivate a switch in transistor geometry the full infrastructure of devices need to be present, not only satisfying the logical domain. Therefore, in parallel to the digital branch, a wish for developing better analog RF-transistors is present. The requirements for an RF-transistor are quite different where stability and high frequency signal gain is of importance. In an RF circuit power dissipation can be sacrificed for increased performance, lending more room for new innovations.

In this thesis the use of the vertical nanowire geometry for MOSFET is further investigated by implementing a III-V, InAs/InGaAs, graded heterostructure, inside the channel, optimized for increased stability and low resistance ohmic-contacts. A Si-substrate with grown III-V nanowires, on top of a InAs buffer layer, is provided and afterwards processed into a complete set of devices. The orientation of the grading is chosen with an abrupt junction from the InAs buffer layer to InGaAs slowly graded back to InAs at the top, by implementing 550

nm long nanowires. The measured DC-characteristics indicates a presence of the heterostructure due to good saturation, low output conductance $g_d \approx 2$ μS/μm at $V_{ds} = 0.5V$ and $V_{gs} = 0.5V$. Amplification and current does not reach intended values because of large access resistance, $R_c \approx 1500\ \Omega\mu m$, with transconductance $g_{m,max} = 280$ μS/μm. Good gate control is indicated with devices showcasing low sub-threshold swing SS down to 80 mV/dec.

Motivation of introducing a heterostructure is clear due to higher breakdown and increased linearity but the choice of the grading orientation is not. Contact resistance is mostly originating from the source side, which means that there is large room for improvement by tweaking the process. The nanowires also had a tendency to collapse which decreased the performance. In other words the theory of implementing a heterostructure with abrupt junction for larger breakdown voltage and increased linearity is promising and cannot yet be disregarded.

Populärvetenskaplig Sammanfattning

"Om bilar hade utvecklats så snabbt som processorer skulle de färdas i en hastighet på 760,000 km/h, gå 42 000 km per liter och kosta 25 öre" hävdar Paul Ottelini, Intel VD mellan 2005-2013. Detta påminner oss om vilken rasande fart utvecklingen har inom nanoelektronik branschen där elektroniska kretsar ständigt blivit billigare samt mindre under det senaste halvseklet. Miniatyriseringen har fördelaktigt gått hand i hand med ökad prestanda. Den huvudsakliga beståndsdelen som används i dessa kretsar, som exempelvis en processor, är en transistor. Uppgiften för en transistor är att styra strömmar på så sätt att de kan stängas av eller på.

Transistorn består av tre huvudsakliga elektroder, där elektrisk spänning kan appliceras. Mellan två av elektroderna kan en ström färdas såsom igenom ett vanligt motstånd. Med den tredje, som brukar kallas gate, kan resistansen manipuleras vilket ändrar strömmen som färdas mellan de två övriga elektroderna. I en dator krävs det att transistorn ska fungera som ett relä, helt enkelt en effektiv av/på knapp. Här är prestandan väldigt beroende av hur många transistorer, logiska kretsar, som får plats på ett chip för att i slutändan kunna utföra många beräkningar samtidigt.

För analoga applikationer däremot, i till exempel radiosändare och mottagare, ställs andra krav. Här kan det räcka med endast ett fåtal transistorer som effektivt kan tolka och förstärka en signal som varierar över tiden. När frekvensen på signalen som ska sändas, eller mottagas, ökar kan även mer information transporteras. I framtiden krävs därmed pålitliga transistorer som hinner tolka snabba strömändringar på grund av signal-frekvenser på flera 100 GHz.

I den digitala världen har den pågående miniatyriseringen av de logiska kretsarna lett till att många dimensioner endast är tiotals atomer. Därmed uppkommer flera utmaningar vid vidare miniatyrisering av kretsarna som leder till att man fullkomligt förlorar kontrollen över gaten. För fortsatt utveckling tittar man då på alternativa material samt andra utformningar av transistorerna. Det tål att nämnas att det som sker i den digitala världen självklart påverkar den analoga sfären.

I detta arbete har möjligheten att skapa transistorer av stående cylindriska pelare, även kallade nanotrådar, undersökts. På dessa nanotrådar kan gaten lin-

das runt själva tråden för att få bästa möjliga kontroll av strömmen. Dessutom är olika material blandade inuti tråden för att uppnå gynnsamma villkor. Dessa villkor är att elektroner enkelt ska kunna färdas genom materialet samtidigt som transistorn ska vara pålitlig vid ett stort omfång av applicerad spänning på elektroderna. Därför har en blandning av indiumarsenid, som bidrar med hög rörlighet för elektroner, och indiumgalliumarsenid använts. Det sistnämnda materialet bidrar med extra pålitlighet. Den färdiga transistorn uppvisade god kontroll av strömmen med aningen begränsad prestanda. Notera att dessa transistorer är, i grund och botten, skapade ovanpå ett kiselprov, vilket gör denna teknologi överförbar till industriell skala.

Acknowledgements

"Now this is not the end. It is not even the beginning.
But it is perhaps the end of the beginning."
Sir Winston Leonard Spencer-Churchill

My time as a student at Lunds University is coming to an end, or perhaps, a new beginning. When my interests of continuing on the academic path where flailing, a few people made me realise my potential. Among these people there are a two professors in particular, namely Dan Hessman and Lars-Erik Wernersson. The pursuit itself is priceless and the end result is necessarily not the most important. This is the way of the researcher. So from the bottom of my heart I would like to thank you for all your support.

I would also like to extend my gratitude to my practical coach Olli-Pekka, who tirelessly taught me a very long and complicated process, and Johannes Svensson, who had to developed an all new nanowire growth recipe. I am greatly humbled by the skill level possessed by these individuals.

My family has always been a source for inspiration and pushing me to pursue my dreams, therefore I thank Lars, Charita and Max.

Abbreviations & symbols

Abbreviations

ADC	analogue-to-digital converter
ALD	atomic layer deposition
Al_2O_3	aluminium oxide
Ar	argon
As	arsenic
AsH_3	arsine
Au	gold
BOE	buffered oxide etch
BTBT	band-to-band tunneling
C	carbon
DR	double row array
EBL	electron beam litography
GAA	gate all-around
GaAs	gallium arsenide
GaN	gallium nitride
GaSb	gallium antimonide
Ge	germanium
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
HF	hydro fluoride
HfO_2	hafnium dioxide
HSQ	hydrogen silsesquioxane

ICP-RIE	inductively coupled plasma reactive-ion etching
In	indium
InAs	indium arsenide
InGaAs	indium gallium arsenide
InP	indium phosphide
InSb	indium antimonide
IPA	2-propanol
MESFET	metal-semiconductor field effect transistor
MOSFET	mteal-oxide-semiconductor field effect transistor
MOVPE	metalorganic vapour phase epitaxy
N_2	nitrogen
Ni	nickel
NW	nanowire
NWFET	nanowire field effect transistor
O	oxygen
PMMA	poly(methyl methacrylate)
RF	Radio frequency
RIE	reactive-ion etcher
SEM	scanning electron microscopy
Si	silicon
SiO_2	silicon dioxide
SiO	silicon monoxide
Sn	tin
TESn	tetraethyltin
TFET	tunnel field effect transistor
TiN	titanium nitride
TMAH	tetramethylammonium hydroxide
TMGa	tetramethylgallium
TMIn	tetramethylindium
UV	ultraviolet
UVL	ultraviolet litography
VLS	vapor-liquid-solid
W	tungsten

Physical constants

ε_0	vacuum permittivity	$8.854 * 10^{-12}$ F/m
k_B	boltzmanns constant	$8.617 * 10^{-5}$ eV/K
e	eulers number	2.718
q	elementary charge	$1.602 * 10^{-}19$ C

Symbols

a	lattice constant	m
A	area	m^2
A_v	open circuit amplification	-
C_{ox}	intrinsic oxide capacitance	F/m^2
C_{gd}	gate-drain capacitance	F/m^2
C_{gs}	gate-source capacitance	F/m^2
d	distance	m
D_{it}	density of interface traps	m^{-3}
E_C	conduction band energy	eV
E_F	fermi-level	eV
E_g	band gap	eV
E_V	valence band energy	eV
f_t	cut-off frequency	Hz
g_d	output conductance	S
g_m	transconductance	S
I_{ds}	drain-source current	A
I_{on}	on-state current	A
I_{on}	off-state current	A
N_d	donors	m^{-3}
N_a	acceptors	m^{-3}
V_{ds}	drain-source voltage	V
V_{gs}	gate-source voltage	V
V_t	threshold voltage	V
R_{ch}	channel resistance	Ωm
R_d	drain resistance	Ωm
R_c	access resistance	Ωm
R_{on}	on-resistance	Ωm
R_s	source resistance	Ωm
SS	sub-threshold slope	mV/dec

ε_r	relative permittivity	-
κ	dielectric constant	F/m
μ_e	electron mobility	$cm^2V^{-1}s^{-1}$
μ_p	hole mobility	$cm^2V^{-1}s^{-1}$
ϕ_B	Schottky barrier potential	V
ϕ_M	metal work function	V
ϕ_s	semiconductor work function	V
χ_s	semiconductor electron affinity	V

Table of Contents

1 Introduction **1**
- 1.1 Semiconductor Physics . . . 2
- 1.2 Background & Future of MOSFET . . . 5

2 MOSFET Performance Metrics **13**
- 2.1 On-resistance . . . 14
- 2.2 Output Conductance . . . 14
- 2.3 Transconductance . . . 15
- 2.4 Threshold Voltage . . . 15
- 2.5 Voltage Gain . . . 16
- 2.6 Subthreshold Swing . . . 16
- 2.7 Cut-off Frequency . . . 16

3 MOSFET Evolution **17**

4 MOSFET Fabrication **21**
- 4.1 Nanowire Growth . . . 22
- 4.2 Top Metal Deposition . . . 23
- 4.3 Drain Pad and Bottom Spacer . . . 24
- 4.4 Gate Deposition . . . 25
- 4.5 Via Holes and Top Contact . . . 27

5 Result & Analysis **29**
- 5.1 Processing . . . 29
- 5.2 Measurements . . . 32
- 5.3 Benchmarking . . . 37
- 5.4 Breakdown . . . 38

6 Conclusion & Outlook **41**

References **43**

A Batch #1 metrics **47**

List of Figures

1.1 A simplified sodium crystal containing only three atoms to model the total potential seen by the charge carriers. The valence electrons in the structure are shared, and can move between atoms. (a) The potential for the free charge carriers can be modelled by a simple square potential where local potential shift originating from the atomic nucleus is neglected. This modelling is sufficient to introduce the concept of effective mass. (b) Another layer is added to the model where a periodic pertubation, depending on lattice constant a, is added. Crucial for the derivation of energy band gap seen by free charge carriers. 3

1.2 A typical shift in fermi-level E_F during different doping. The intrinsic Fermi level $E_{F,i}$ resides in the middle of the band gap meaning that few free carriers are available and the material is highly resistive. The amount of free carriers n or p at room temperature is inversely dependant on the band gap $\frac{1}{E_g}$. When adding donors N_d to the semiconductor the fermi level is shifted upwards to $E_{F,n}$ and in this case reaches above degenerate limit meaning that chemical potential is inside the conduction band. The same shift occurs downwards in energy when adding acceptors N_a and the potential ends up at $E_{F,p}$. 3

1.3 Dense version of the periodic table with atoms involved in high speed electronic devices. III-V compounds with typical dopants Sn or Si can give both p and n-doping. *Source: Wikimedia Commons* 4

1.4 The formed Schottky barrier, according to Schottky-Mott rule, in a metal-semiconductor junction. The height of the barrier is determined by the difference between metal work function ϕ_M and electron affinity of the semiconductor χ_s, see equation 1.1. Work function of the semiconductor ϕ_s is also given. Notice that W depicts the width of the depletion region in the semiconductor in which the band bending takes place. 5

1.5 Overview of how a MOSFET typically works. Depicting a planar n-transistor with no gate overlap (a) with the symbol describing a MOS transistor (b) in a circuit schematic. The schematic is used here to highlight relative position of terminals gate, drain and source in the band diagrams. The band simulations shows both off- (c) and on-state (d). Below threshold voltage $V_{gs} < V_t$ the biasing is insufficient for creating an n-channel and the potential barrier quenches the thermionic emission of electrons. Above threshold $V_{gs} > V_t$ the charge carriers can move past the potential barrier. 6

1.6 Innovation flow in commercial logic transistors presented by *Intel* [18]. Change in high κ was implemented in order to increase gate-thickness supressing leakage currents. 3d structures (lateral nanowires) for increased electrostatics has also already been introduced. 7

1.7 Cross-sectional illustration of different gate geometries including planar, tri-gate and gate-all-around (GAA). (a) Side view of the conventional planar layout creating a sandwich of layers. (b) 3d implementation of lateral nanowires by tri-gate leading to better gate coverage, thus increased electrostatics compared to planar. (c) Complete overview of a GAA geometry, created with vertical nanowires, where ratio between gate width and cross-sectional channel area is maximized optimizing electrostatic control. 9

1.8 Effects during high bias conditions. In impact ionization electrons in the conduction band gain enough energy, due to an external electric field, to create extra electron-hole pairs during a scattering event. With BTBT (band-to-band-tunneling) the potential barrier is sufficiently thin to allow quantum tunneling, also generating extra electron hole-pairs. 11

2.1 A schematic of a MOSFET indicating the biasing points for an intrinsic device with added series resistance. Source is normally connected to ground as a reference which means that biasing is controlled through the gate V_{gs} and drain V_{ds} electrodes. Biasing results in pulling a current from drain to source I_{ds}. 13

2.2 Output conductance of an actual MOSFET, illustrating extraction of g_d and R_{on}. Notice that on-resistance R_{on} is extracted below the saturation region and given as the inverse of the derivative. 14

2.3 A typical example of transfer characteristics for an enhancement mode MOSFET, in linear (a) and logarithmic scale (b). Example extracted from an actual measured transistor. g_m represents the derivative of the I_d-V_{ds} characteristics. V_t extrapolation carried out with the tangent of the voltage that yields maximum g_m. SS is given by the slope of the exponentially increasing sub-threshold, $V_{gs} < V_t$, segment. I_{on} is defined as one drive voltage $V_{dd} = 0.5V$ above a fixed I_{off} current of 100 nA/μm 15

3.1 a) The conventional "drain last" process developed by Sofia Johansson. b) Comparison done with self aligned gate process, "drain first", outlined by Martin Berg [46, 47]. *Schematic used, with permission, from doctoral thesis by Martin Berg.* 17

3.2 Showing the benefits, by band-structure simulation, of incorporating InGaAs [50]. *Schematic used, with permission, from doctoral thesis by Jun Wu.* 18

3.3 A sketch for the nanowire MOSFET optimized for high breakdown, processed in this thesis. Bottom contact consists of the substrate (a) and top contact will cover the (d) segment. 19

3.4 A sketch for composition of the nanowires processed in this thesis. Due to limitations and variations during growth there is a difference between the target composition and final batch. 20

4.1 An overview of the finished transistor in top ground configuration. The structure can also be bottom grounded meaning that the source and drain contacts, in this case, are switched. The choice of the optimal configuration, top ground, is motivated by band-simulations, see Fig 3.3. 21

4.2 High resolution SEM images of the grown nanowires. Gold particle diameter defined by EBL is 28 nm. (a) A full set of double row arrays with internal spacing of 200 nm. (b) Zoom in of a few nanowires in the array to highlight the smooth surface which indicates good crystal quality. 22

4.3 A schematic image depicting the top contact deposited by sputtering and ALD. 23

4.4 The finished top metal deposition, see schematic in Fig 4.3. Notice the unwanted residues left on the surface. Showing double row array (a) and single (b) nanowire structure. 24

4.5 The creation of the first spacer. 1 A SiO_2 spacer is first applied via ALD. Organic resist is later spun onto the sample and thinned down via O_2 dry etching. 2 The SiO_2 spacer is etched via HF (1:100 H_2O) wet etch with the organic spacer acting as a etch mask. 3 The resist spacer is removed with acetone leaving only the finished first spacer. 25

4.6 Deposition of the gate contact. 1 Etching is performed targeting the exposed semiconductor effectively thinning it below 30 nm of diameter. 2 60 nm of tungsten is sputtered onto the sample. A organic spacer is created via spun on resist and dry etching. 3 The exposed tungsten is removed via SF_6 dry etch. The organic spacer is afterwards removed via aceton. 26

4.7 The result of the gate length definition. Showing a double row array (a) after high-κ deposition and (b) post gate etch. 27

4.8 Deposition of the second spacer and top contact. 1 An organic spacer is spun onto the sample, permanently baked and thinned down via O_2 dry etching. 2 Via holes are etched with sacrificial resist layer acting as etch mask where via holes are exposed, one at a time, via UV litography. 3 Top contact is sputtered consisting of Ni, W and Au. 28
4.9 Showing the finished top metal layout in top grounded configuration. 28

5.1 Two single nanowire structures after removal of the temporary HSQ spacer. Highlighting the metal surface roughness for comparison, ... 31
5.2 The damage after fabricating the top metal in batch #1. Hollow top metals are visible and the metal surface roughness is clearly shown. 31
5.3 Nanowires after digital etch and high-κ deposition for both samples in batch #2. High-κ thickness is 4.5 nm according to SEM inspections, thus the mean diameter of the specific array in *Sample A* is 29 nm and 35 mn in *Sample B*. 31
5.4 Overview of all arrays in batch 2. No sidewall etch was performed on *sample B*, meaning that the effective diameter of the nanowires are smaller in *sample A*, see Table 5.1. (a)-(b) shows the correlation between extracted values R_{on} and $g_{m,max}$, clearly showing the expected exponential trend when decreasing the total resistance. (c)-(d) Outlines SS dependence of $g_{m,max}$, showing no clear trend. 33
5.5 Exhibiting the SS-V_t and R_{on}-L_g dependence. Attempts for extrapolating the access resistance, $R_c = R_s + R_d$, are performed with taking all values into account (#1) and a selected few (#2) that are highlighted. A smaller ratio of collapsed nanowires seem to be present in the highlighted devices. Note that the L_g values are based on estimates from SEM pictures that, in this case, might be insufficient due to large thickness variation of the bottom spacer. . 34
5.6 Transfer characteristics, plotted in logarithmic scale, for the hero device found batch #2. Metrics compiled in Fig 5.2.1. 35
5.7 Output characteristics for the hero device found batch #2. Metrics compiled in Fig 5.2.1. 36
5.8 Output characteristics for a representative, double row, device at bias conditions close to its breakdown at 4 V. The device is found batch #2-*sample A*. The transistor can operate up to 3.5 V, but showcases bad saturation with high g_d. Different segments can be identified with (a) being well saturated and (b) showing impact ionization that accelerates further in (c). 38
5.9 Comparing output characteristics for top and bottom ground configuration in a representative, double row, device. The device is found batch #2-*sample A*. The transistor breaks at 2.2 V in bottom ground. Different segments can be identified with (a) being well saturated and (b) showing impact ionization that accelerates further in (c). 39

List of Tables

1.1 Comparing dielectrics materials that are generally used for MOSFET. Both large offset $\Delta E_{c,InAs}$ and bandgap is crucial for reduction of leakage. [24] 8

1.2 Outlining important material parameters for selected IV and III-V semiconductors. Superior transport μ_n is shown for the III-V compounds compared to silicon. Parameters taken from [37]. Notice that the injection velocity for electrons $v_{inj,e}$ is extracted from virtual source modelling with $L_g = 30$nm [34]. 10

5.1 A quick comparison between processed samples. [1]Top contact quality and gate alignment greatly improved between batches, with the first batch having $\sim$ 20 nm of ungated channel area. [2]All processing was optimized for the double row (DR) arrays in the second batch. The gate length is varying between devices due to both the bottom spacer and position of the top contact. 30

5.2 A measurement overview showing the best devices from each processed batches. L_g and diameter is inspected via SEM. $g_{m,max}$ and SS_{min} are extracted from measurements. Notice that $g_{m,max}$ is normalized via inspections which is a quite crude method. 32

5.3 Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. [1]Bias conditions are chosen in active region of the transistor at $V_g = 0.5$ and $V_{ds} = 0.5V$. 36

5.4 A comparison with mainly other work from the research group (Nanoelectronics Group), created in the same lab using mostly the same equipment. V highlight the vertical orientation of the device, other devices utilize a lateral geometry. Notice that all V-NW devices are integrated on silicon while the both the HEMT and record device are based on an InP(III-V) substrate. 37

A.1 Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. [1]*A mean value has been extracted from SEM inspections of other pads* [2]*Bias conditions are chosen in active region of the transistor at* $V_g = 0.5$ *and* $V_{ds} = 0.6V$. 47

Chapter 1
Introduction

In the year 1925 Julius Edgar Lilienfeld filed a patent for the field effect transistor FET, describing the basics of what later would be known as the metal-oxide-semiconductor field effect transistor MOSFET [1]. Due to high purity semiconductors not being available the concept was experimentally confirmed decades later by Bell Labs in 1948. Further development was, at the time, not pursued due to problems connected to the surface of the semiconductor. Instead the germanium based point-contact transistor, invented in 1947, stole the show and became commercially available for use in the early pocket radios, replacing the bulky vacuum tubes [2]. Connected to improvement in semiconductor quality and advent of integrated circuits (ICs) based on silicon in the 1960s the dreams of the MOSFET once again resurfaced. At this point the interface problems had been resolved by means of taming the strong native oxide found in silicon. The emergence of the computer industry further pushed the revolution with constant demands for faster and more energy efficient circuits.

Gordon E. Moore released his predictions (Moore's law) in 1965 stating that the number of transistors per chip area will roughly double every 24 months via geometrical downscaling [3]. The predictions was based on the fact that increased packing density leads to exponential increase in performance as well as lower power dissipation of the circuits. Moore's law was followed strictly up until 2002 when the downscaling became constricted by power dissipation of 100 W/cm^2 [4]. To avoid overheating increase of performance was now pursued with multi-core systems and parallelization of computer tasks rather than speed.

Today the industry is in a place where things are shaken up with uncertainty. Improvements in transistor technology is now heavily dependent on innovations rather than downscaling. The technology demands has also changed with the upcoming era of IoT (Internet of things) setting up new standards for RF-transistors used in wireless communications [5]. A potential candidate for meeting the demands is to integrate III-V high speed material, on silicon substrates, utilizing a nanowire geometry with gate all-around (GAA) configuration. This alternative is further examined in this thesis. The needed background for absorbing and understanding the benefits of the work in this thesis is given in this chapter.

1.1 Semiconductor Physics

To grasp the concept of transistor technology it is important to have a fundamental understanding of its building blocks, namely the semiconductor. Normally a semiconductor consists of a solid chemical element or compound, for example III-V semiconductors, and is used for integrated circuits due to its ability to conduct electricity during some circumstances but not others. To explain this behaviour concepts of chemical potential and band gap are introduced. An intrinsic semiconductor has its chemical potential, described by Fermi-Dirac statistics, placed inside the band gap typically ranging from 0.5 up to 8 eV. Few charge carriers are typically available in a semiconductor leading to poor conductance. To circumvent this issue doping is introduced increasing the amount of charge carriers inside the conduction band. The concepts are further explained in this chapter.

1.1.1 The Origin of Band Structure

In a single atom the energy levels for orbiting electrons (fermions) are quantized maintaining a unique quantum number, described by the Pauli Principe [6]. Charge of the nucleus determines the amount of orbiting electrons, and size of the electron cloud, which controls the properties of the atom. In case of a semiconductors the atoms align in form of a crystal. When the atoms become tightly packed (lattice constant order of magnitude $a \sim$ Å) hybridization occurs, wave functions overlap and mutual orbits for electrons are created. Pauli principle still applies, therefore the orbits spread in energy, see Fig 1.1. Two electrons can still have the same relative energy but will not share the same spin. The size of the bands depend on the energy of the bound states where the electrons originated from. To decide if a solid is in fact a semiconductor, metal or even an insulator the concept of a chemical potential, Fermi-level E_F, is introduced showing the statistical energy of the free charge carriers inside the crystal. Definitions of conduction and valence band are also introduced, with the valence band being the last filled energy band and conduction band being the next band with higher energy. Thus a metal has a Fermi level placed inside the conduction band and a semi-conductor has its potential placed inside a band gap, meaning that there are no free carriers inside the conduction band at absolute zero temperature 0 K. In reality there is always carriers inside the conduction band due to thermal excitation.

A general concept is that the crystal structure shares electrons that can move "freely" inside the crystal lattice [7]. But since the electrons are moving inside a cluster of charge this is modelled by introducing a different effective mass m^* for the charge carriers, see Fig 1.1 (*free electron model*). The potential of each atomic nucleus can be seen as a periodic perturbation in the free electron model, thus at certain wave vectors $\vec{k} = n\pi/a$ ($n \epsilon \mathbb{Z}$) the periodicity of the carriers will resonate with the perturbation effectively shifting the kinetic energy of the carriers creating a band gap (*nearly free electron model*).

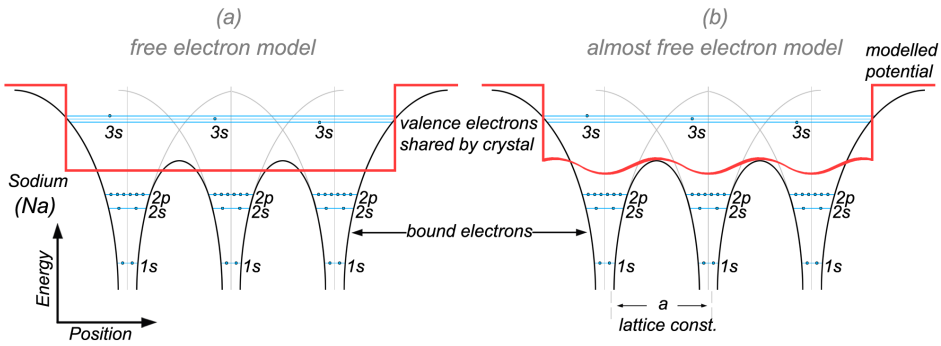

Fig 1.1: A simplified sodium crystal containing only three atoms to model the total potential seen by the charge carriers. The valence electrons in the structure are shared, and can move between atoms. (a) The potential for the free charge carriers can be modelled by a simple square potential where local potential shift originating from the atomic nucleus is neglected. This modelling is sufficient to introduce the concept of effective mass. (b) Another layer is added to the model where a periodic pertubation, depending on lattice constant a, is added. Crucial for the derivation of energy band gap seen by free charge carriers.

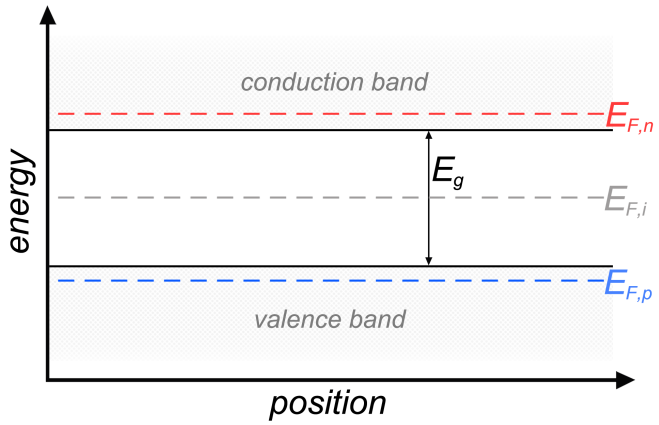

Fig 1.2: A typical shift in fermi-level E_F during different doping. The intrinsic Fermi level $E_{F,i}$ resides in the middle of the band gap meaning that few free carriers are available and the material is highly resistive. The amount of free carriers n or p at room temperature is inversely dependant on the band gap $\frac{1}{E_g}$. When adding donors N_d to the semiconductor the fermi level is shifted upwards to $E_{F,n}$ and in this case reaches above degenerate limit meaning that chemical potential is inside the conduction band. The same shift occurs downwards in energy when adding acceptors N_a and the potential ends up at $E_{F,p}$.

1.1.2 Doping

To manipulate the placement of the chemical potential, thus changing the electrical properties of the semiconductor, impurities are introduced effectively doping the crystal, see Fig 1.2 [8]. Doping means that few atoms inside the crystal lattice of a semiconductor is substituted with compatible atoms from another material to create an abundance (n-type) or absence (p-type) of electrons. Absence of electrons can be modelled as quasi-particles called holes, normally with higher effective mass m^* compared to electrons. Substituted atoms lending extra electrons are called donor states N_a and respectively when removing electrons they are called acceptor states N_d.

In this work a n-doping is used in the order of $N_d \approx 10^{18}$ cm^{-3}, for comparison the concentration of atoms in a crystal is approximately $1/a^3 \approx 10^{21}$ cm^{-3}. III-V compounds, in many cases, have quite large lattice constant, small atom density, compared to Si which means that relatively small doping leads to degenerate Fermi-level [9]. A semiconductor overview and comparison is given in Table 1.2.

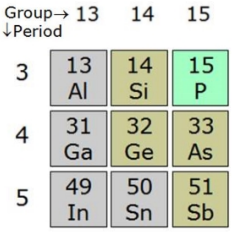

Fig 1.3: Dense version of the periodic table with atoms involved in high speed electronic devices. III-V compounds with typical dopants Sn or Si can give both p and n-doping. *Source: Wikimedia Commons*

In this thesis III-V compound InGaAs are doped during epitaxial growth, called in-situ doping, with Sn to add donors N_d. Seen from Fig 1.3 the gallium(Ga) or indium(In) atoms in InGaAs compound need to be substituted with impurities in order to achieve n-doping.

1.1.3 Schottky Barrier

Necessary for further understanding of transistor device physics is the formation of Schottky barriers in metal-semiconductor junctions, see Fig 1.4. In early studies it was believed that the height ϕ_B of the formed potential barrier was only dependent on the difference between metal work function ϕ_M and electron affinity χ_s of the semiconductor, described by the Schottky-Mott rule [10]

$$q\phi_B \approx q(\phi_M - \chi_s) \tag{1.1}$$

where q is the elementary charge. The length of the depletion region W, inside the semiconductor, can be reduced with higher doping according to

$$W \sim \frac{1}{\sqrt{N_d}}. \tag{1.2}$$

A thinner barrier allows higher chance of tunneling events which translates to less resistance in the junction [36].

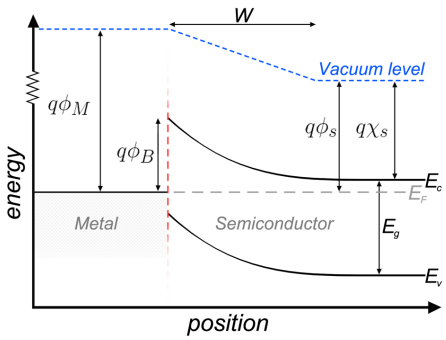

Fig 1.4: The formed Schottky barrier, according to Schottky-Mott rule, in a metal-semiconductor junction. The height of the barrier is determined by the difference between metal work function ϕ_M and electron affinity of the semiconductor χ_s, see equation 1.1. Work function of the semiconductor ϕ_s is also given. Notice that W depicts the width of the depletion region in the semiconductor in which the band bending takes place.

In practice the characterisation of the junction is much more complex because the height of the Schottky barrier is heavily dependent on surface states, known as metal induced gap states (MIGS), formed at the surface in between materials [11]. Therefore certain semiconductors exhibit different degrees of Fermi level pinning, meaning that the Fermi level of the semiconductor pins to certain positions relative to the chemical potential of the metal. Basically the gap states gets charged and drive the band lineup to a new equilibrium state. The Fermi level pinning needs to be taken into account when choosing transistor material.

1.2 Background & Future of MOSFET

MOSFET uses manipulation of energy-barriers to either quench or conduct a current, toggling between on- and off-state [13]. The transistor is comprised of normally four different terminals; gate(G), drain(D), source(S) and body(B). The body terminal consists of the substrate itself in planar cases but when utilising the geometry of a NWFET the substrate is not a part of the active region effectively making it into a three terminal device. Active region of the MOSFET is called channel which is controlled via the gate terminal through a metal-oxide-semiconductor MOS interface, using an oxide as insulator. The MOS structure gives rise to a capacitance that makes it possible to control the potential of the free charge carriers inside the semiconductor channel. Different regimes are therefore defined to further describe the state of the charge carriers in the channel under different bias conditions applied to the gate electrode V_{gs}, namely accumulation, depletion and inversion. During accumulation the charge carriers, that constitutes the majority, are attracted to the semiconductor surface, along the oxide interface,

and in depletion these carriers are instead greatly reduced. When increasing the degree of depletion, by modulating the gate bias above a certain threshold voltage $V_{gs} > V_t$, new minority charge carriers are being generated effectively inverting the channel, thus inversion is achieved.

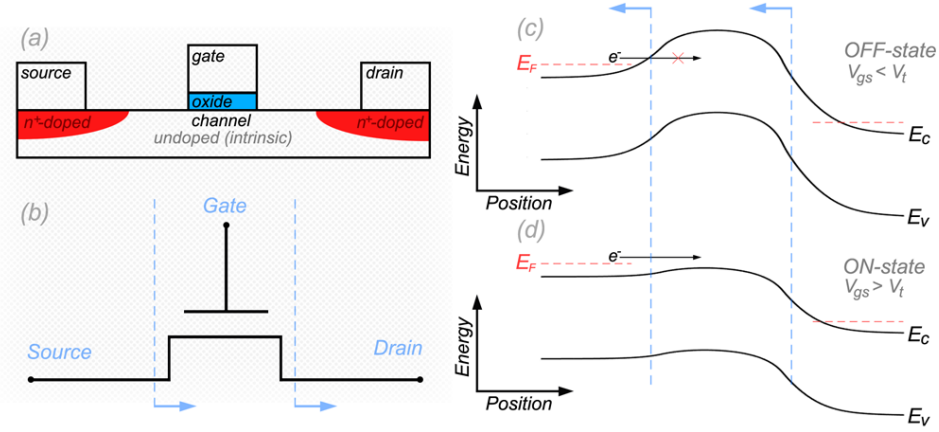

Fig 1.5: Overview of how a MOSFET typically works. Depicting a planar n-transistor with no gate overlap (a) with the symbol describing a MOS transistor (b) in a circuit schematic. The schematic is used here to highlight relative position of terminals gate, drain and source in the band diagrams. The band simulations shows both off- (c) and on-state (d). Below threshold voltage $V_{gs} < V_t$ the biasing is insufficient for creating an n-channel and the potential barrier quenches the thermionic emission of electrons. Above threshold $V_{gs} > V_t$ the charge carriers can move past the potential barrier.

At the two ends of the channel the source and drain terminals are situated and used to control the electric field, by V_{ds}, in the direction of the channel, hence controlling the passing current I_{ds}. If there is an energy barrier present inside the channel, due to difference in doping levels between channel and source/drain terminals, the current will not be able to flow from D- to S-terminal without external bias, called an enhancement mode device [14]. An example of a n-type enhancement mode device is depicted in Fig 1.5, where accumulation of electrons inside the channel turns the device on [15].

Compared to other transistors the MOSFET offers low leakage current from the gate electrode due to the insulating oxide in the MOS interface [16]. Maintaining a low off-state leakage is key for reaching higher energy-efficiency in logical circuits where the amount of transistors is correlated to increased processing power. Available field effect transistor without the metal-oxide-semiconductor interface is for example high-electron-mobility-transistor HEMT or metal-semiconductor-field-effect-transistor MESFET. A HEMT uses a wide bandgap material, as substitute for a dielectric, between metal and channel which leads to good quality semiconductor interfaces sacrificing energy-efficiency for improved carrier transport properties [17]. These characteristics are beneficial for transistors used in RF

applications.

1.2.1 Importance of High-κ Oxides

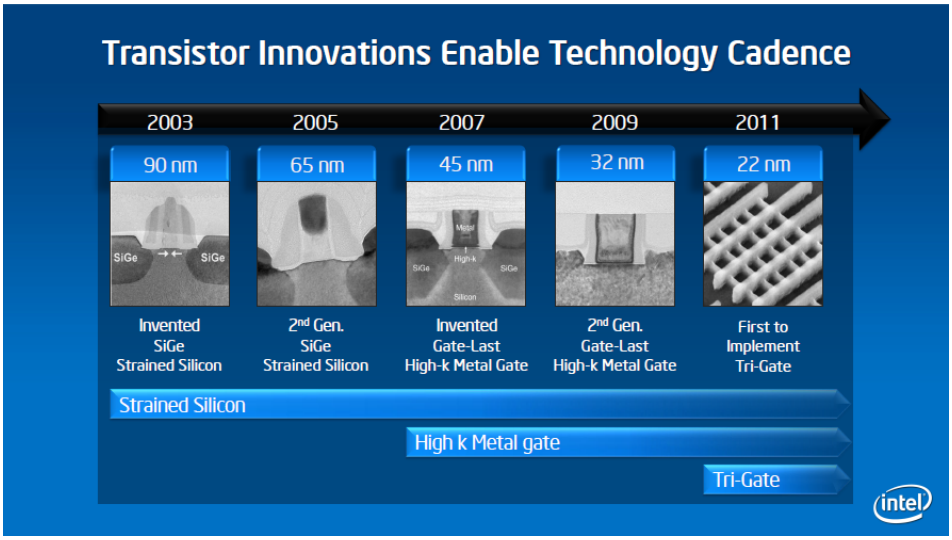

Fig 1.6: Innovation flow in commercial logic transistors presented by *Intel* [18]. Change in high κ was implemented in order to increase gate-thickness supressing leakage currents. 3d structures (lateral nanowires) for increased electrostatics has also already been introduced.

The on-going down scaling outlined by Moore's Law has started to reach a certain limit where several quantum effects cannot be disregarded [12]. Amongst these effects are quantum tunneling, through the gate, which means that the oxide insulator inside the MOS structure is so thin that the wave-function of the charge carriers start to reach beyond the oxide, leading to an unwanted gate-leakage current [36]. In industry today silicon (Si) is widely used due to its availability, but also its native oxide SiO_2. Due to silicon having a strong native oxide (SiO_2), the interface created between the materials has low density of interface traps D_{it} [19]. SiO_2 also acts as a good insulator with sufficiently high permittivity $\varepsilon_r\varepsilon_0 \equiv \kappa$.

A simple expression for the oxide capacitance C_{ox} [F/m^2] is given as

$$C_{ox} = \frac{\varepsilon_r\varepsilon_0}{d} \equiv \frac{\kappa}{t_{ox}}$$

with t_{ox} as the thickness of the dielectric. According to this simple formula tunneling effects, gate leakage, can be circumvented by keeping a thick oxide (~ nm) and change to another dielectric material with higher κ to preserve electrostatics, see Table 1.1. A typical oxide with high κ-value is HfO_2 and is presently used by Intel instead of SiO_2 see Fig 1.6 [22]. When introducing new oxide materials, issues regarding interface traps D_{it} are more prominent due to dangling bonds and point defects [23]. In this work III-V semiconductors are utilized which lacks

good native oxides. Implementing a high-κ oxide on III-Vs can hence lead to insufficient electrostatic control [20]. To minimize interface states, bi-layers can be utilized with for example Al_2O_3 as a buffer layer between semiconductor and HfO_2. Another source of D_{it} is doping of the semiconductor, where in-situ doping can degrade the crystal quality and therefore also the high-κ interface [21].

Table 1.1: Comparing dielectrics materials that are generally used for MOSFET. Both large offset $\Delta E_{c,InAs}$ and bandgap is crucial for reduction of leakage. [24]

Dielectric		κ/ε_0	Bandgap [eV]	$\Delta E_{c,InAs}$ [eV]
Silicon dioxide	SiO_2	3.9	9	4.1
Silicon Nitride	Si_3N_4	7	5.3	2.7
Hafnium dioxide	HfO_2	25	5.8	2.5
Aluminium oxide	Al_2O_3	9	8.8	3.6
Zirconium oxide	ZrO_2	25	5.8	-

1.2.2 Benefits of NWFET and III-Vs

Due to the nature of the vertical nanowire geometry, strain between different crystal planes (lattice mismatch) can more easily be relaxed [26]. This creates vast opportunities of mixing different materials in so called heterojunctions to improve transistor performance. III-V nanowires can thus be integrated on top of a Si-substrate creating a more industry compatible and sustainable process [28]. Predictions have already been made stating that III-V compounds will be integrated on Si in commercial CMOS to benefit from the good transport properties, see Table 1.2, in order to improve energy efficiency and speed. The vertical geometry leads to increased packing density with the footprint area decoupled from the gate length L_g with corresponding metal contacts [27]. III-V wafers are small, brittle and expensive compared to Si-wafers, III-V materials are also less abundant in the earths crust making it crucial to still use Si-wafers [25].

Main benefit of changing to a more complex 3D structure is to improve electrostatic control with wrap-around gate configurations such as tri-gate (Fig 1.6) and gate-all around (GAA). This means that ratio between cross-sectional area of the channel and gate width is large, compared to its planar counterpart, maximizing gate control, see Fig 1.7. Continued downscaling of MOSFET devices has increased packing density and reduced drive voltage, in other words overall improvement of performance and cost per device. However, in the last decade, shrinking dimensions has also lead to undesirable short channel effects (SCE) such as drain induced barrier lowering DIBL and increased subthreshold swing SS, especially at $L_g \leq 30$ nm [29]. Switching from Si to III-V semiconductors will mean that drive voltage can be lowered without further downscaling of the gate length L_g, due to superior mobility [30]. With better transport properties, the mean free path for charge carriers is increased which can potentially make the device oper-

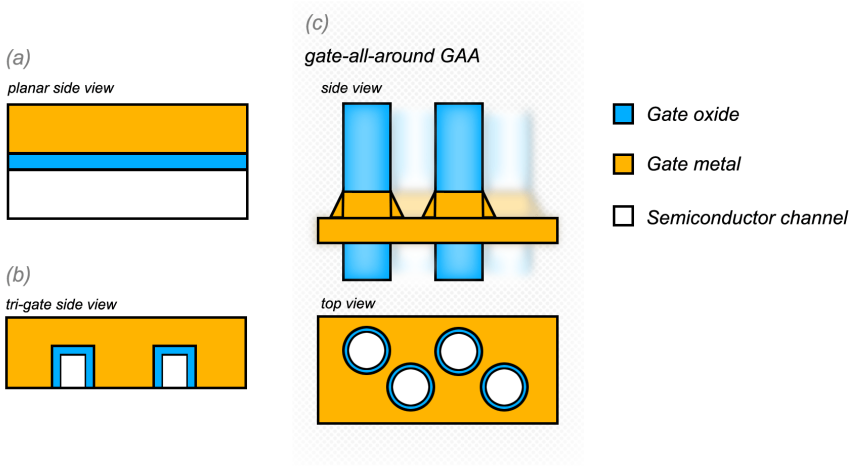

Fig 1.7: Cross-sectional illustration of different gate geometries including planar, tri-gate and gate-all-around (GAA). (a) Side view of the conventional planar layout creating a sandwich of layers. (b) 3d implementation of lateral nanowires by tri-gate leading to better gate coverage, thus increased electrostatics compared to planar. (c) Complete overview of a GAA geometry, created with vertical nanowires, where ratio between gate width and cross-sectional channel area is maximized optimizing electrostatic control.

ate in the ballistic regime, with no scattering events occuring inside the channel. Intel has already improved transport properties ($\sim$ 70%) by implementation of strained silicon as channel material, see Fig 1.6 [31].

Table 1.2 shows material parameters for selected semiconductors. III-V compounds has in several cases better mobility μ_n compared to silicon (Si), but this is not the case for hole mobility μ_p. Having overall good performance for both holes and electrons is necessary for CMOS implementation in logic circuits. In this work however the processed MOSFET devices will be optimised for high frequency RF application, meaning that electron mobility (n-doping) is of importance. Observe that there is a fundamental correlation between lattice constant a_0 and bandgap E_g as $a_0 \sim 1/E_g$. Implementing materials with a small bandgap might seem beneficial due to high mobility, but will lead to sensitivity such as thermal instability and low breakdown voltage. Notice that Si suffers from indirect bandgap which degrades the effective mass. Therefore III-V materials has been the first choice for optoelectronic devices, such as light-emitting-diode LED [32]. The currents are necessarily not higher in a MOSFET utilizing a high mobility III-V compound due to larger crystal lattice constant a_0, which translates to reduced density of states. The main benefit is that the ballistic regime, with no scattering inside the channel, can be reached at larger gate lengths ($L_g \leq 30$ nm) due to longer mean free path. The performance of a ballistic transistor is dependent on the injection velocity v_{inj} of the charge carriers, which scales inversely with effective mass $v_{inj} \sim 1/m^*$ [33].

Table 1.2: Outlining important material parameters for selected IV and III-V semiconductors. Superior transport μ_n is shown for the III-V compounds compared to silicon. Parameters taken from [37]. Notice that the injection velocity for electrons $v_{inj,e}$ is extracted from virtual source modelling with L_g = 30nm [34].

Semi -conductor	μ_n [cm^2/Vs]	μ_p [cm^2/Vs]	E_g [eV]	a_0 [Å]	m^*/m_e	$v_{inj,e}$ [cm/s]
Si	1400	450	1.12	5.43	0.36	$1.2{\cdot}10^7$
Ge	3900	1900	0.66	5.66	0.22	
GaAs	8500	400	1.42	5.65	0.063	
InAs	40000	500	0.354	6.06	0.023	$3.7{\cdot}10^7$
$In_{0.53}Ga_{0.47}As$	12000	300	0.74	5.87	0.041	$2.8{\cdot}10^7$
InSb	77000	850	0.17	6.48	0.014	
GaSb	3000	1000	0.73	6.10	0.041	

1.2.3 Design of RF Transistors

Radio frequency (RF) transistors are designed to handle high frequencies, well above 100 GHz, and still maintain both current and power gain. Emphasis is also put on the transistors ability to showcase high breakdown and stable saturation of the output conductance g_d. Further discussion of important metrics for high frequency performance are given in Chapter 2. Breakdown is the ability of the device to handle large currents during significant voltage bias ($V_{ds} \geq 4$ V) and is quantified by the destructive breakdown voltage V_B at which the device physically breaks.

Effects leading to poor saturation and low V_B, when disregarding short channel effects (SCE), are impact ionization and band-to-band tunneling (BTBT), see Fig 1.8. Both effects are inversely dependent on the band gap, $\sim 1/E_g$, of the active material that constitutes the MOSFET channel area [39, 42]. Impact ionization occurs when the kinetic energy of the charge carriers surpass the energy needed for excitation of extra electrons over the band gap. Thus when energy is lost via scattering events the probability of creating new electron-hole pairs is high [40]. This leads to a chain of events where the amount of free charge carriers are greatly accelerated. In a MOSFET impact ionization effects will lead to a sudden increase of the output current that can damage and ultimately lead to destructive breakdown of the device. The band-to-band tunneling effect, on the other hand, is dependent on the distortion of the potential seen by the charge carriers. When the potential barrier shrinks, under certain bias conditions, quantum tunneling is enabled through the band gap itself and new electron-hole-pairs can be generated [36]. These different effects likely occur if the provided energy, by a certain voltage drop V_{bias}, is significantly larger than the band gap, $qV_{bias} >> E_g$ with q as the elementary charge, inside a segment of the channel material.

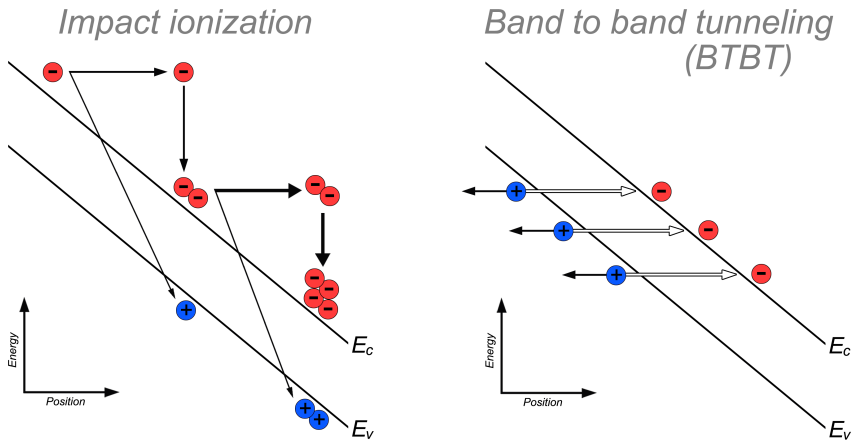

Fig 1.8: Effects during high bias conditions. In impact ionization electrons in the conduction band gain enough energy, due to an external electric field, to create extra electron-hole pairs during a scattering event. With BTBT (band-to-band-tunneling) the potential barrier is sufficiently thin to allow quantum tunneling, also generating extra electron hole-pairs.

Larger band gap leads to degraded carrier mobility, see Table 1.2. Notice that the amount of free charge carriers, density of states, is greatly sacrificed when aiming for higher mobility. Therefore when designing the channel there will be a trade off between speed and reliability of the transistor. Smart use of heterostructures can be employed to combine benefits of different semiconductors, ranging from large band gap or good transport to low D_{it}. Benefits when mixing materials has already been demonstrated in modern HBT (heterojunction bipolar transistor) for increasing the performance at high frequencies [35]. Wide band gap materials such as GaN, with E_g = 3.4 eV and μ_n = 440 cm^2/Vs, has attracted increased attention due to its relatively high mobility for future integration in high power amplifiers [41].

Chapter 2

MOSFET Performance Metrics

When benchmarking a functioning MOSFET device certain standardized metrics has been established. In this chapter the definitions for quantifying the performance of the transistors are outlined. Extracting these metrics is crucial for making accurate models which leads to greater understanding of the device and its use in circuit integration. Parasitic elements, unwanted resistance and capacitance, in a MOSFET can greatly limit the performance and can also be extracted by device modelling. Definitions covered are mainly DC metrics acquired with an input signal constant over time.

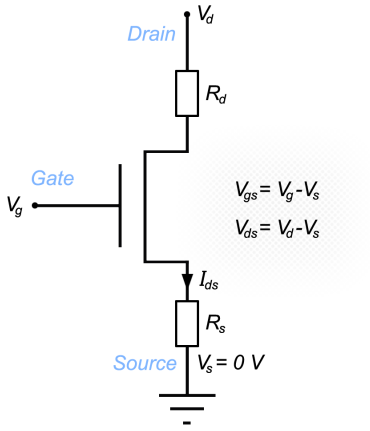

Fig 2.1: A schematic of a MOSFET indicating the biasing points for an intrinsic device with added series resistance. Source is normally connected to ground as a reference which means that biasing is controlled through the gate V_{gs} and drain V_{ds} electrodes. Biasing results in pulling a current from drain to source I_{ds}.

When measuring on a transistor all the metrics are extracted by sweeping either the gate voltage V_{gs}, at constant V_{ds}, or the drain voltage V_{ds}, at constant V_{gs}, and studying the change in the drain-current I_{ds}, see Fig 2.1. A transistor for radio frequency (RF) applications needs to have a certain bias in order to be in its active mode (saturation). The input signal will then be applied and modelled as

a small signal shift of the voltage. To evaluate the small signal response different parameters describing the shapes of the DC curves are defined.

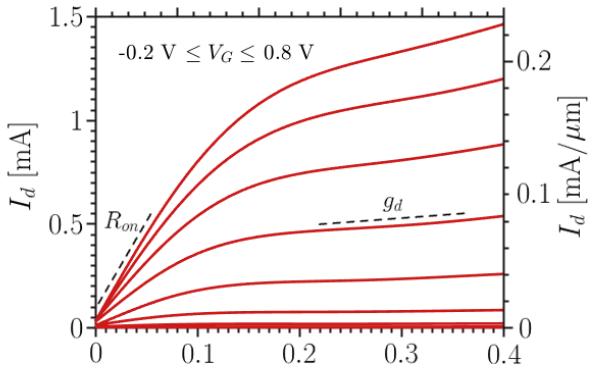

Fig 2.2: Output conductance of an actual MOSFET, illustrating extraction of g_d and R_{on}. Notice that on-resistance R_{on} is extracted below the saturation region and given as the inverse of the derivative.

2.1 On-resistance

Regarding output characteristics shown in Fig 2.2. Inside the linear, non-saturated, region of the characteristics the on resistance R_{on} can be extracted as the inverse of the slope $\frac{\partial I_{ds}}{\partial V_{ds}}$ when $V_{ds} \to 0$ V. The on resistance is comprised of mainly three different sources of resistance originating from source R_s, drain R_d and the channel R_{ch}, see Fig 2.1. The source and drain resistance can be greatly reduced by making good contacts and decreasing series resistance of the MOSFET.

$$R_{on} = R_s + R_d + R_{ch} \tag{2.1}$$

The resistance originating from both source and drain, $R_s + R_d$, is referred to as access resistance R_c.

2.2 Output Conductance

Compared to transconductance, output conductance g_d is instead the response of the drain current when changing source drain biasing V_{ds}. The definition is therefore defined as partial derivative of drain current with respect to source-drain voltage

$$g_d \equiv \frac{\partial I_d}{\partial V_{ds}}. \tag{2.2}$$

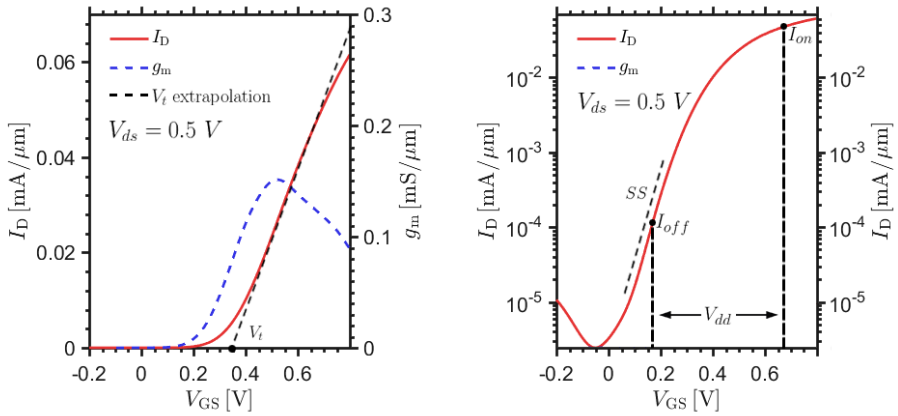

Fig 2.3: A typical example of transfer characteristics for an enhancement mode MOSFET, in linear (a) and logarithmic scale (b). Example extracted from an actual measured transistor. g_m represents the derivative of the I_d-V_{ds} characteristics. V_t extrapolation carried out with the tangent of the voltage that yields maximum g_m. SS is given by the slope of the exponentially increasing sub-threshold, $V_{gs} < V_t$, segment. I_{on} is defined as one drive voltage $V_{dd} = 0.5V$ above a fixed I_{off} current of 100 nA/μm

An ideal MOSFET has zero g_d in saturation, meaning that channel length modulation has no effect on the resistance of the active area.

2.3 Transconductance

A transistor metric important for transistor in RF application is transconductance g_m, defined as the partial derivative of the drain current with respect to gate voltage

$$g_m \equiv \frac{\partial I_d}{\partial V_{gs}}. \tag{2.3}$$

When applying a small signal input at the gate electrode the given response at the drain current is quantified by this metric.

2.4 Threshold Voltage

At a certain threshold voltage V_t the transistor switches from ON to OFF-state, see Fig 1.5. Typically defined as the gate voltage needed to initiate inversion of the channel. To register the threshold voltage via the I_{ds}-V_{gs} curve the tangent from the V_{gs} point, corresponding to the peak value of transconductance $g_{m,max}$, is extrapolated down to zero drain current, see Fig 2.3. The threshold voltage is in reality not well defined which makes extraction of this metric quite arbitrary.

2.5 Voltage Gain

With transconductance g_m and output conductance g_d given the small signal voltage gain of the transistor, in CS configuration, can be derived from

$$A_v = \frac{\partial V_{ds}}{\partial V_{gs}} = \frac{g_m}{g_d}. \tag{2.4}$$

Notice that the given voltage gain A_v is for a transistor in open circuit configuration.

2.6 Subthreshold Swing

Thermionic emission will always be limited by the amount of available free carriers above a certain potential barrier. When heat is applied to a system the carriers are redistributed according to Fermi-distribution. At high enough temperature, such as room temperature ($\sim$ 300 K), the distribution can be referred to as a Fermi-tail (similar to Boltzmann distribution) that is decaying exponentially when moving to higher energies compared to the conduction band, see Fig 1.2. The theoretical limit is hence naturally dependent on the distribution described by the Fermi-function and referred to as subthreshold slope

$$SS = -\frac{1}{log_{10}(e)}\frac{k_B T}{q}. \tag{2.5}$$

q represents the elementary charge, k_B boltzmanns constant and e Euler's number. SS is identified from the transfer characteristics, in logarithmic scale, as the linear increase in the sub-threshold region, see Fig 2.3.

For logic circuits SS is an essential parameter since a logic device is systematically switched between ON and OFF-state. In other words SS describes how well a MOSFET works as a relay switch.

2.7 Cut-off Frequency

The only AC-metric covered in this chapter, quantifying at what frequency f_t of the input signal, applied to the gate, the MOSFET showcases gain. Mentioned to underline the importance of g_m and is described as

$$f_t \approx \frac{g_{m,i}}{2\pi(C_{gd} + C_{gs})} \tag{2.6}$$

with intrinsic transconductance $g_{m,i}$. Notice that extrinsic capacitances are approximated as the dominant source of parasitics and also access resistance, R_s & R_d, are disregarded. In other words the f_t scales linearly with g_m.

Chapter 3
MOSFET Evolution

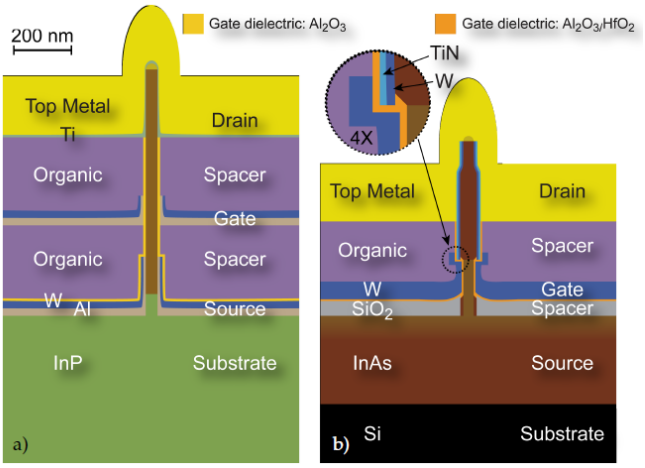

Fig 3.1: a) The conventional "drain last" process developed by Sofia Johansson. b) Comparison done with self aligned gate process, "drain first", outlined by Martin Berg [46, 47]. *Schematic used, with permission, from doctoral thesis by Martin Berg.*

The process used for manufacturing vertical nanowire MOSFET in this thesis was developed by Martin Berg and Karl-Magnus Persson [47]. Vertical processing require high precision tools optimized for an all new direction, namely normal to the substrate. Since lateral processing is utilized in industry and refined for more than half a century switching to vertical is challenging [43]. This type of processing is still in its cradle and is facing some of the challenges that was eventually resolved for the planar architecture. However vertical processing is fundamentally different from lateral due to the device being built from bottom to the top in a "bottom-up" fashion. In the bottom-up approach a system is pieced together to add up to a bigger and more complex system.

Previous processes optimized for RF-performance has included sub-sequentially adding all the pieces from bottom to the top. Starting with a wafer containing nanowires a first spacer is deposited followed by a gate and afterwards the second

spacer is added followed by the top contact. This method of conventionally depositing the top contact last was spearheaded by Sofia Johansson who developed vertical transistor that showcased gain at high frequency input, f_t = 140 GHz, see Figure 3.1 [44]. In this thesis however the process starts with deposition of the top contact which enables a self-aligned gate process and also lends more margins in the high precision alignment steps.

A self-aligned process is crucial for increased performance due to complete gate coverage of the channel which enables lower series resistance. With larger currents, high amplification g_m is possible which is fundamental for high RF-performance. The downside of tighter dimensions is larger parasitic which puts more emphasis on low-κ integration, possibly with the use of air spacers.

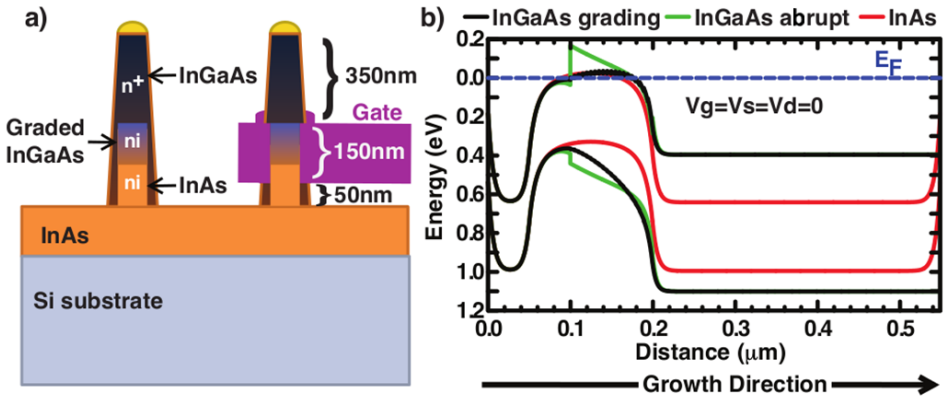

Fig 3.2: Showing the benefits, by band-structure simulation, of incorporating InGaAs [50]. *Schematic used, with permission, from doctoral thesis by Jun Wu.*

The first generation of the gate last process consisted of pure InAs nanowires to accommodate both the digital and RF domain, see Fig 3.1. Growth techniques where adapted to decrease the resistance of the wire including a highly doped InAs overgrowth creating a shell for good ohmic contact. In later steps the shell could be selectively etched revealing the intrinsic or lowly doped gate area for high-κ and metal deposition. The first generation transistors showcased instability, with high output conductance g_d and low breakdown, due to the narrow bandgap of InAs.

In the second generation of NWFET these issues where addressed by incorporating a heterostructure featuring InAs and InGaAs, see Figure 3.2. Where the composition of the nanowire is gradually changed from InAs to InGaAs when moving from bottom to the top [49]. The overgrown shell, in this case, consisted of highly doped InGaAs. The result of this update in the NWFET remains unpublished.

Parallel to the second generation of devices a test is carried out, in this thesis, where the heterostructure is inverted, see Fig 3.3. Instead of gradually grading from InAs to InGaAs, the InGaAs is abruptly incorporated in the bottom

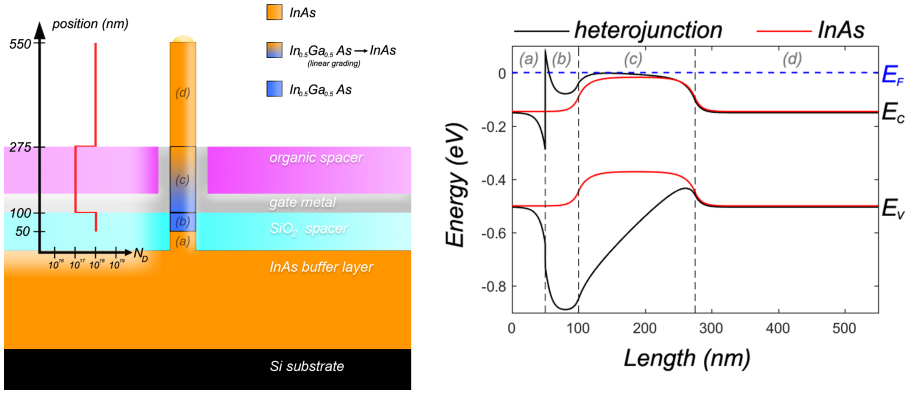

Fig 3.3: A sketch for the nanowire MOSFET optimized for high breakdown, processed in this thesis. Bottom contact consists of the substrate (a) and top contact will cover the (d) segment.

and graded back to InAs at the top. An abrupt junction creates an unwanted hetero-barrier, but the concept has possibilities of showcasing greater breakdown performance with the help of decoupling the ohmic contact performance from the Ga concentration, since InAs has better fermi-level pinning [45]. Low resistance in all ungated areas is crucial for high performance, thus the top and bottom segments are highly doped with $N_d \geq 10^{18}$ cm^{-3} to reduce contact resistance R_c. A degenerate semiconductor at the bottom can compensate for the presence of a Schottky barrier. The placement of the gate is designed to cover the graded segment to benefit from the larger bandgap of $In_{0.5}Ga_{0.5}As$ ($E_g \approx 0.75eV$). This configuration is optimized for the top segment acting as ground and the InAs buffer layer as drain. Notice that the final composition of the nanowire changed compared to the target sketch due to limitations during growth, see Fig 3.4

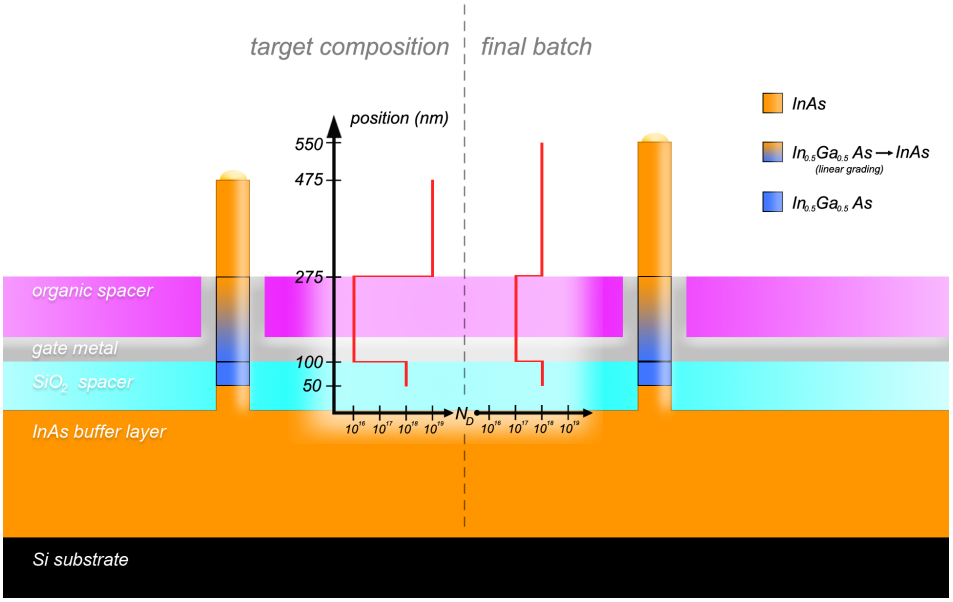

Fig 3.4: A sketch for composition of the nanowires processed in this thesis. Due to limitations and variations during growth there is a difference between the target composition and final batch.

Chapter 4

MOSFET Fabrication

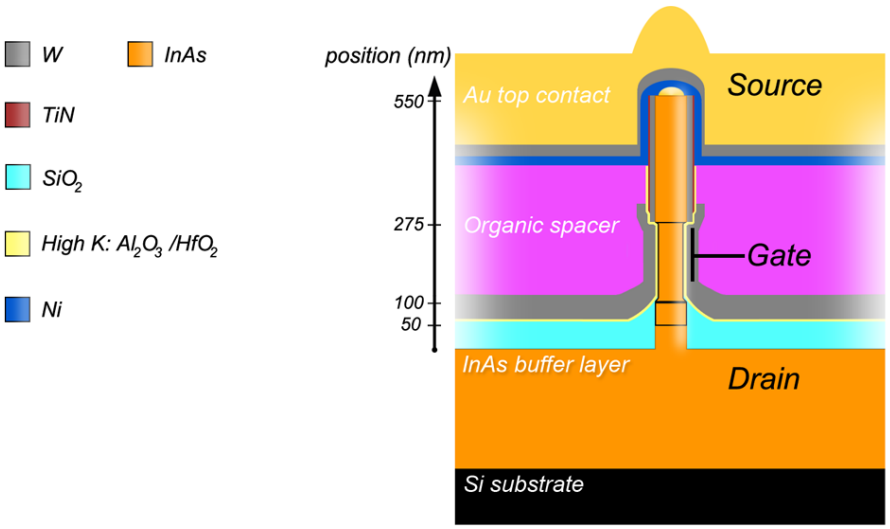

Fig 4.1: An overview of the finished transistor in top ground configuration. The structure can also be bottom grounded meaning that the source and drain contacts, in this case, are switched. The choice of the optimal configuration, top ground, is motivated by band-simulations, see Fig 3.3.

The fabrication of the vertical MOSFET is a complex and involves many steps in order to deposit the top metal first for creating sufficient gate-overlap and, in the end, realize the final structure, see Fig 4.1. All the steps are thoroughly covered, in this chapter, combined with theory needed for greater understanding of process sensitivity.

4.1 Nanowire Growth

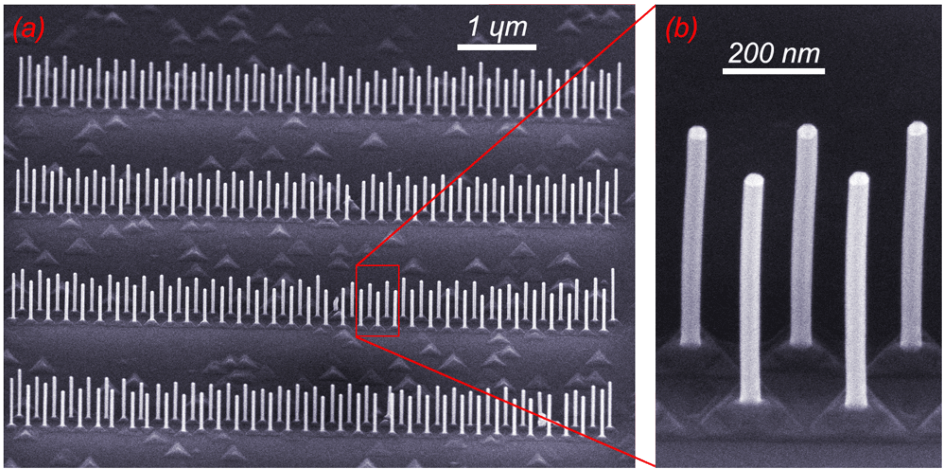

Fig 4.2: High resolution SEM images of the grown nanowires. Gold particle diameter defined by EBL is 28 nm. (a) A full set of double row arrays with internal spacing of 200 nm. (b) Zoom in of a few nanowires in the array to highlight the smooth surface which indicates good crystal quality.

The device performance will always be limited by the quality of the nanowires making up the final transistor. The growth of the nanowires was therefore outsourced to an experienced researcher, namely Dr. Johannes Svensson at EIT department, Lund University. Therefore the growth process is described mostly qualitatively.

To alleviate lattice stress and enable growth of good quality III-V nanowires, on top of a silicon substrate, a 260 nm thick InAs layer is grown by metal organic vapor phase epitaxy MOVPE. In this epitaxy technique the sample is placed inside a chamber and flooded with precursor gases (TMIn, AsH_3), at elevated temperature, which reacts on top of the substrate surface to form the final crystalline InAs buffer layer. The silicon substrate, now covered with InAs, is later patterned with gold dots by an EBL defined lift off process using a PMMA film. The gold dots will act as catalysts in the vapor-liquid-solid (VLS) process. In this mechanism, the catalyst dots create liquid alloy droplets at high temperature (420^o C-470^o C) by adsorbing the vapors inside the MOVPE chamber [51]. Thus local supersaturation of the alloy occurs, which means that the concentration of components exceed its equilibrium. The system then strives to lower its energy which in turn enables 1D growth that continues as long as precursor gases are supplied, creating nanowires. By controlling the supply of precursor gases (TMIn, AsH_3, TMGa), during the process, InGaAs composition of the nanowire can be controlled along the growth direction [49].

Different patterns are defined by the EBL process including double row arrays, pads and single nanowire structures. The growth is thus optimized for the most

reoccuring structure, namely the zigzag double row array, see Fig 4.2.

Doping of the wires are carried out in-situ, meaning that they are doped in conjunction with deposition [52]. The dopants are added by another precursor gas, namely TESn, which adds n-doping by substitution with Sn atoms. The precision of the in-situ doping is limited by diffusion mechanisms leading to dopant atoms relocating and spreading at elevated temperatures to reduce induced strain. These effects amounted to a slightly different outcome in doping concentration and length in the final batch compared to target composition, see Fig 3.4.

4.2 Top Metal Deposition

The top contact is deposited by sputtering of 20 nm tungsten (W) and ALD of 3 nm of titanium-nitride (TiN) by utilizing a sacrificial spacer, see Fig 4.3. Sputtering amounts to good step coverage with thickness of approximately 1/3 on the sidewalls compared to the planar surface. This ratio will vary depending on nanowire spacing due to shadowing effects. The ALD process, on the other hand, leads to complete uniform step coverage independent of spacing, therefore the thin TiN film will serve as extra protection for the inner metal shell, on the nanowire sidewalls, in later etching steps. The metal film on the planar surface is specifically targeted with anisotropic dry etching in an ICP-RIE using SF_6 and CF_4F_8 gas supported by argon ions (Ar^+). The etch time (85 s) is calibrated to completely remove metal on the planar surface and reveal the gold particles situated on the tip of the wires. The final result is given with SEM in Fig 4.4.

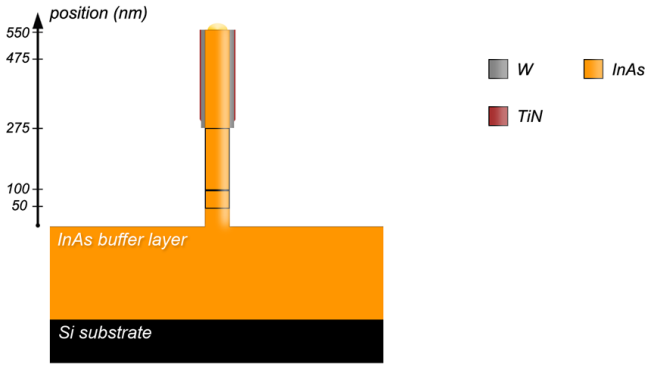

Fig 4.3: A schematic image depicting the top contact deposited by sputtering and ALD.

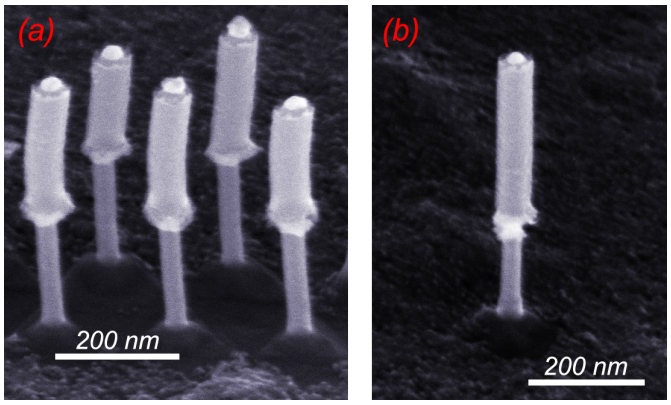

Fig 4.4: The finished top metal deposition, see schematic in Fig 4.3. Notice the unwanted residues left on the surface. Showing double row array (a) and single (b) nanowire structure.

4.3 Drain Pad and Bottom Spacer

The 260 nm InAs buffer layer covering the silicon substrate is highly doped ($N_D = 5 \cdot 10^{19}$ cm^{-3}) and is therefore highly conductive. To further isolate the different devices, present on a single sample, from each other, a mesa etch has to be carried out. The etch removes the excess of the InAs layer which is crucial for good RF-performance by minimizing overlapping parasitic capacitance. The material left on the surface creates a pad that acts as the bottom contact and constitutes the drain. The pad is defined via optical lithography utilizing, spun on and baked, S1813 photoresist at 4000 rpm, resulting in a thickness of 1300 nm. The pattern is defined via a mask aligner (soft UV) later developed with MF 319 containing highly diluted TMAH 2.2 % [55]. Unwanted resist residues are thoroughly removed via an oxygen plasma. The resist acts as an etch mask when using InAs wet etch consisting of H_3PO_4:H_2O_2:H_2O(1:1:25) and can afterwards easily be removed with an acetone and IPA rinse.

To fabricate the bottom spacer a 50 nm thick SiO_2 layer is deposited via ALD and etched with the help of a resist mask using a "etch-back" process, see Fig 4.5. In this method the resist (S1813) is deposited on top of the SiO_2 layer, by spinning and baking, and thinned by RIE with oxygen plasma until the top of the nanowires are visible. Desired resist thickness is around 200 nm ensuring step coverage of the mesa etch. Diluted HF (1:100) is used for controllable wet etch to remove the SiO_2 from the nanowire sidewalls until only the desired spacer is left. The resist mask is then completely removed via acetone and IPA rinse.

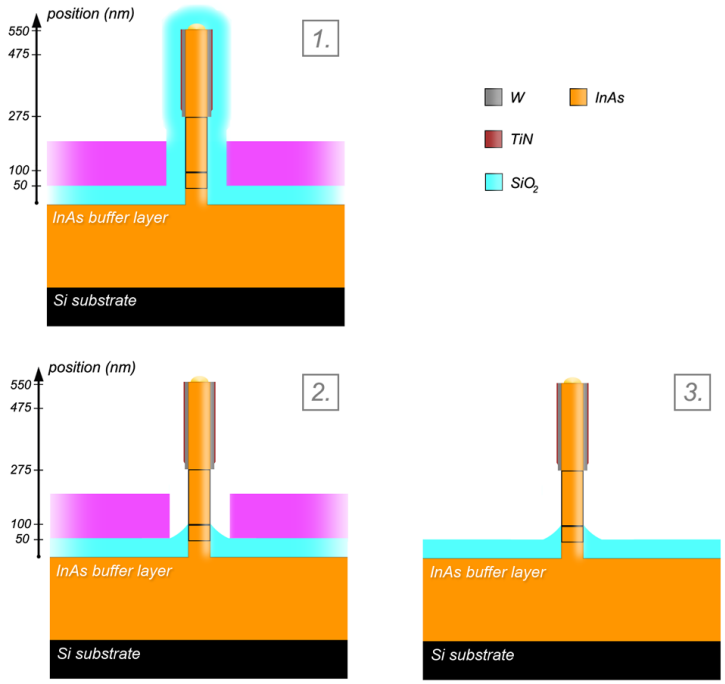

Fig 4.5: The creation of the first spacer. 1 A SiO_2 spacer is first applied via ALD. Organic resist is later spun onto the sample and thinned down via O_2 dry etching. 2 The SiO_2 spacer is etched via HF (1:100 H_2O) wet etch with the organic spacer acting as a etch mask. 3 The resist spacer is removed with acetone leaving only the finished first spacer.

4.4 Gate Deposition

Schematic illustrations for the gate deposition process is given in Fig 4.6. To increase electrostatic control, of the channel, sidewall etching is performed targeting the exposed part of the nanowire, later acting as the gate area. A long nanowire will be subject to more capillary force during H_2O or IPA rinsing steps, specifically during drying [56]. Based on previous calibrations the etching is used to reach a diameter slightly above 25 nm with a nanowires around 550 nm long.

After sufficient reduction of the gate diameter the high-k dielectric can be deposited via ALD, see Fig 4.7. Chosen dielectric consist of a bilayer with hafnia HfO_2 and sapphire Al_2O_3. Sapphire is known to create a good interface and is therefore used as a thin 1 nm buffer layer while the 4 nm HfO_2 layer, with higher κ-value, contributes to greater electrostatics. The deposition is in the end carried out with 10 cycles of Al_2O_3 and 40 cycles of HfO_2 leading to an approximate high-κ thickness of approximately 45 Å.

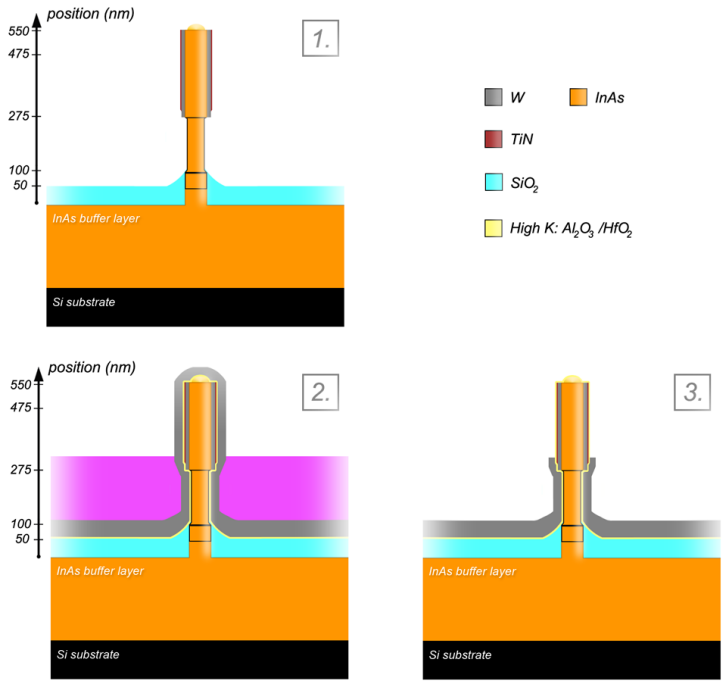

Fig 4.6: Deposition of the gate contact. 1 Etching is performed targeting the exposed semiconductor effectively thinning it below 30 nm of diameter. 2 60 nm of tungsten is sputtered onto the sample. A organic spacer is created via spun on resist and dry etching. 3 The exposed tungsten is removed via SF_6 dry etch. The organic spacer is afterwards removed via aceton.

60 nm gate metal, of tungsten (W), is applied via sputtering, completely covering the nanowires as well as the planar surface. A resist (S1813) is spun on, baked and thinned down with oxygen plasma in a RIE until desired gate-length is reached. High precision is needed for sufficient overlap as well as leaving margins for the second organic spacer. Minimizing the overlap is further important to reduce parasitic capacitance, but its presence is necessary to ensure good DC-performance. Exposed tungsten can be removed via dry etching utilizing SF_6 gas in a RIE process, see Fig 4.7(b). The S1813 is removed, with a usual acetone and IPA rinse, in order to spin on a new resist for use in UV-litography to define the gate pad. After the pattern is exposed in a mask aligner (soft UV) and removed via MF319 the excess tungsten is removed with dry etching (SF_6).

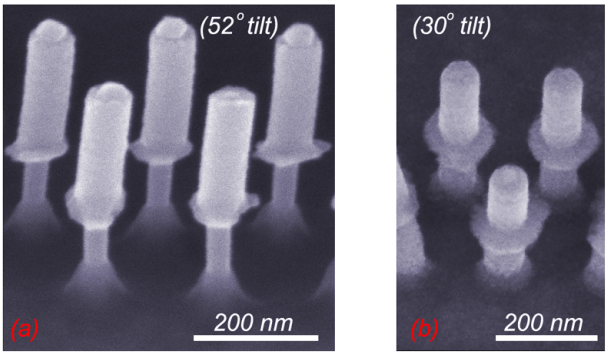

Fig 4.7: The result of the gate length definition. Showing a double row array (a) after high-κ deposition and (b) post gate etch.

4.5 Via Holes and Top Contact

A second organic spacer is fabricated with spun on S1813, now permanently baked and thinned down until 50-100 nm of the top metal is visible, see Fig 4.8. To enable metal-to-metal connection of the top contact the high-κ is removed with a BOE (HF) wet etch. All terminals must further be available for connection via the top metal, thus via holes for both the gate and drain has to be etched. A resist etch mask (S1813) is spun on and baked, and via holes are exposed, one at a time, with mask alignment (soft UV) and development. The gate via is completely cleaned out with oxygen plasma, locally removing the organic spacer, in a RIE. The drain via is also cleaned out with a oxygen plasma followed by a BOE etch for high-κ and bottom spacer removal. Sputtering is used to deposit the top contact consisting of 15 nm nickel (Ni), 30 nm tungsten (W) and 200 nm gold (Au). With the tungsten acting as a diffusion barrier and Ni for creating a good metal-to-metal interface.

The top metal layout, shown in Fig 4.9, is designed to isolate the gate, source and drain terminals from each other and is defined with a UV patterned resist (S1813) mask followed by three individual etch steps. The gold is wet etched using potassium-iodine (KI), the tungsten via SF_6 dry etching and Ni with H2O:H2SO4:HNO3:CH3COOH (10:5:5:2) wet etching.

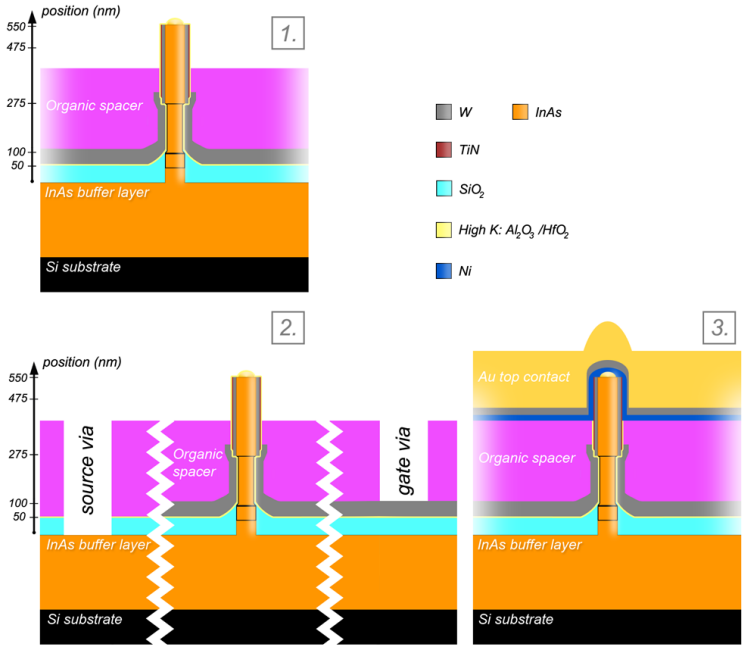

Fig 4.8: Deposition of the second spacer and top contact. 1 An organic spacer is spun onto the sample, permanently baked and thinned down via O_2 dry etching. 2 Via holes are etched with sacrificial resist layer acting as etch mask where via holes are exposed, one at a time, via UV litography. 3 Top contact is sputtered consisting of Ni, W and Au.

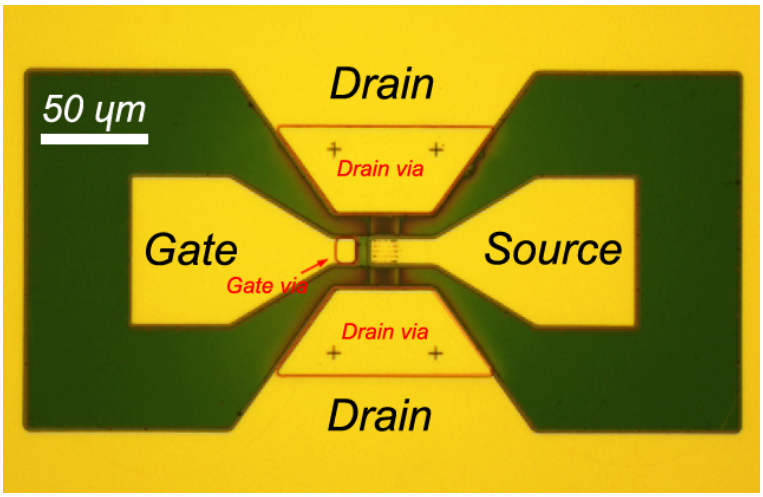

Fig 4.9: Showing the finished top metal layout in top grounded configuration.

Chapter 5
Result & Analysis

Two batches were finalized during this diploma work, with each batch containing two full-scale samples. The first processed batch only resulted in one device with transistor DC-characteristics and the second one showcased promising results with a high yield of approximately 20, of 110 in total, working transistors on each sample. Techniques for RF-optimization were not employed, such as minimizing overlap capacitance with finger contacts, thus only DC-characteristics were measured. To further reach sufficient results with high RF-performance, the g_m is crucial and scales linearly with cut off frequency f_t (equation 2.6), but also high breakdown ($V_{ds} \geq 4$ V) is essential as proof-of-concept. The measurements of the devices were carried out in a probe station.

5.1 Processing

This section serves to highlight differences between the processed samples and also discuss challenges during certain processing steps. Many of the used machines such as the ICP-RIE and RIE are not dedicated for a certain set of materials. Thus the chambers are constantly contaminated with many different substances during their life cycles. For this process it has meant that the etch rates were constantly varying which required extra caution and frequent SEM inspections. Bear in mind that many machines are not optimized for vertical processing making it even more tedious when high precision alignment is required.

Chamber conditions and bad calibration of the anisotropic dry etching steps led to the first batch showcasing extra roughness of the fabricated top contact. In many instances the gold particle was completely etched away including the semiconductor material underneath leaving a hollow top metal contact, see Fig 5.1(a). The majority of devices where therefore completely destroyed during the many processing steps ahead. Fig 5.2 shows the severity of damage to one of the few surviving double row arrays.

During the second batch the ICP-RIE was correctly calibrated but the chamber was not sufficiently cleaned. A residual film was therefore left on the surface after anisotropic etching and removal of the HSQ spacer, see Fig 5.1(b). The origin and composition of the film could not be confirmed due to the lack of proper tools for analysis. *Sample B*, in the second batch, was heavily damaged by the

residual film and therefore extra wet etching steps where tested for removing the film. The sample was, after top metal fabrication, put in extended BOE(HF) etch followed by hydrogen passivation in H_2SO_4, both steps had limited effect and mostly etched the exposed nanowire sidewalls. *Sample A* was also covered by the residual film but to less extent so no extra etching steps were performed. Notice that many nanowire arrays, especially in *Sample B*, were completely collapsed after the top contact fabrication. Most likely due to residues ripping away from the planar surface during the HSQ removal. In contrast to the first batch the quality of the top contact was greatly improved for batch #2. A fair comparison between the top contacts of single nanowire structures are performed in Fig 5.1.

Extra caution for further collapse had to be taken during the targeted sidewall etching. Therefore etching was only performed on *Sample A* and not on *Sample B*. Therefore the diameter was significantly smaller on *Sample A* potentially leading to better electrostatic control of the gate. The difference is given in Fig 5.3 showing nanowire arrays, with the same relative position, on each sample. Table 5.1 states the important differences between the processed batches later necessary for understanding of measurement data.

Table 5.1: A quick comparison between processed samples. [1]Top contact quality and gate alignment greatly improved between batches, with the first batch having ~ 20 nm of ungated channel area. [2]All processing was optimized for the double row (DR) arrays in the second batch. The gate length is varying between devices due to both the bottom spacer and position of the top contact.

	type	**state**	**remarks**	**Fig.**
Batch #1	top contact quality	visibly bad		5.1(a)
	bottom spacer	50-100 nm	pads & singles	
	gate coverage	insufficient[1]	DR arrays	
Batch #2	top contact quality	OK[1]		5.1(b)
Sample A	bottom spacer	50-200 nm	DR arrays[2]	
	sidewall etch	~ 3 nm etch	isotropically	
	diameter	31-37 nm		
	gate coverage	complete[1]		4.7(b)
	gate length L_g	60-180 nm	DR arrays[2]	5.3
Batch #2	top contact quality	OK[1]		5.1
Sample B	bottom spacer	50-180 nm	DR arrays[2]	
	sidewall etch	none		
	diameter	29-33 nm		
	gate coverage	complete[1]		4.7(b)
	gate length L_g	80-180 nm	DR arrays[2]	5.3

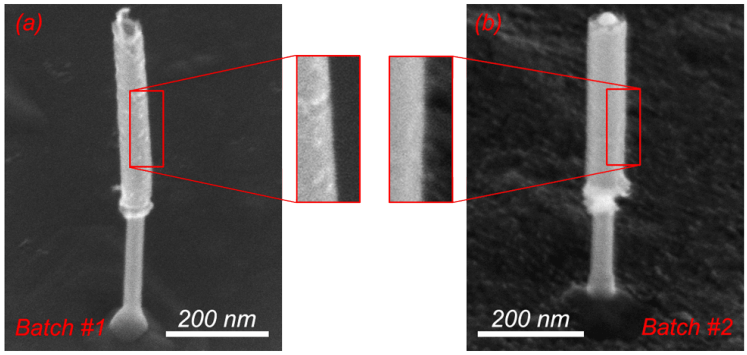

Fig 5.1: Two single nanowire structures after removal of the temporary HSQ spacer. Highlighting the metal surface roughness for comparison,

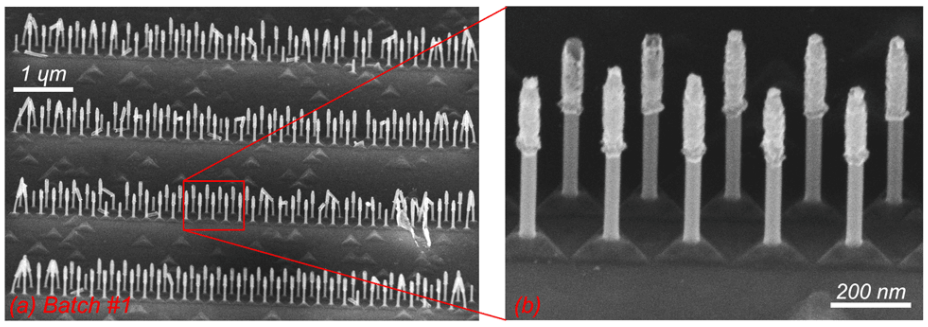

Fig 5.2: The damage after fabricating the top metal in batch #1. Hollow top metals are visible and the metal surface roughness is clearly shown.

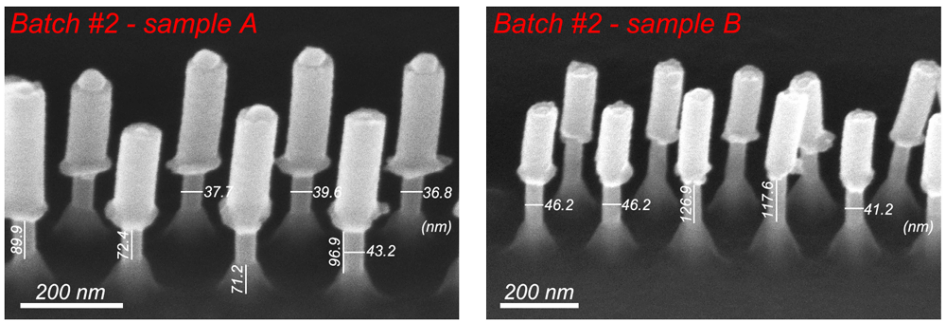

Fig 5.3: Nanowires after digital etch and high-κ deposition for both samples in batch #2. High-κ thickness is 4.5 nm according to SEM inspections, thus the mean diameter of the specific array in *Sample A* is 29 nm and 35 mn in *Sample B*.

5.2 Measurements

Approximately 100 devices where measured in this project with ~1% boasting good DC performance. A small summary of the best devices are given in Table 5.2. Batch #1 is included to highlight the importance of tweaking the process. The sample subject to digital etch (Table 5.1) shows overall improved g_m as well as lower *SS* which is expected due to increased electrostatic control. Notice that the overall g_m performance is low for all devices, see Table 5.4 for benchmarking, which indicates high resistance in the system.

Most devices, containing DR arrays, were subject to high rate of collapsed nanowires. The collapse can introduce inhomogeneous strain and degrade the crystal quality, which might lead to higher resistance and low g_m. No detailed study has been performed regarding degradation of the currents in collapsed nanowire structures, which means the influence is not taken into consideration when normalizing the currents.

Table 5.2: A measurement overview showing the best devices from each processed batches. L_g and diameter is inspected via SEM. $g_{m,max}$ and SS_{min} are extracted from measurements. Notice that $g_{m,max}$ is normalized via inspections which is a quite crude method.

	type	L_g	Diam.	$g_{m,max}$ (tg/bg)	SS_{min} (tg/bg)
	nm	nm	mS/μm	mV/dec	
batch #1	pad	220	31	0.010/0.002	92/103
batch #2	DR	80	30	0.28/0.24	80/130
sample A	DR	120	29	0.24/0.21	71/122
	DR	60	27	0.22/0.20	96/123
	DR	120	29	0.19/0.15	152/135
batch #2	pad	200	31	0.18/0.30	99/104
sample B	single	220	38	0.13/0.17	182/114
	DR	140	35	0.08/0.13	98/110
	DR	140	35	0.07/0.12	110/106

Table 5.2 contains a complete overview of important metrics necessary for later benchmarking. Notice that the thick bottom spacer in the second batch leaves large ungated segments of the channel in the DR arrays. When a heterostructure is present (Fig. 3.3) the gate placement is important and will yield different results. For minimizing the resistance originating from the heterobarrier and large bandgap at the bottom contact, top ground (tg) configuration should be beneficial compared to bottom ground (bg). This holds true for *sample A* where both $g_{m,max}$ and *SS* is higher for tg. *Sample B*, that inherits the record $g_{m,max}$ only for bg, indicates that the improved performance in tg, for *sample A*, could be due to extra resistance originating from the ungated segment. Leaving an

ungated segment adds series resistance which lowers the effective voltage drop over the channel. However the g_m of the record device is still too low for RF implementation, where the goal is at least $g_{m,max} \geq 1$ mS/μm. The measurements in general narrows the main source of resistance down to the insufficient quality of the fabricated top contact for all processed samples. The deposition method and choice of tungsten (W) for the top contact can therefor be questioned.

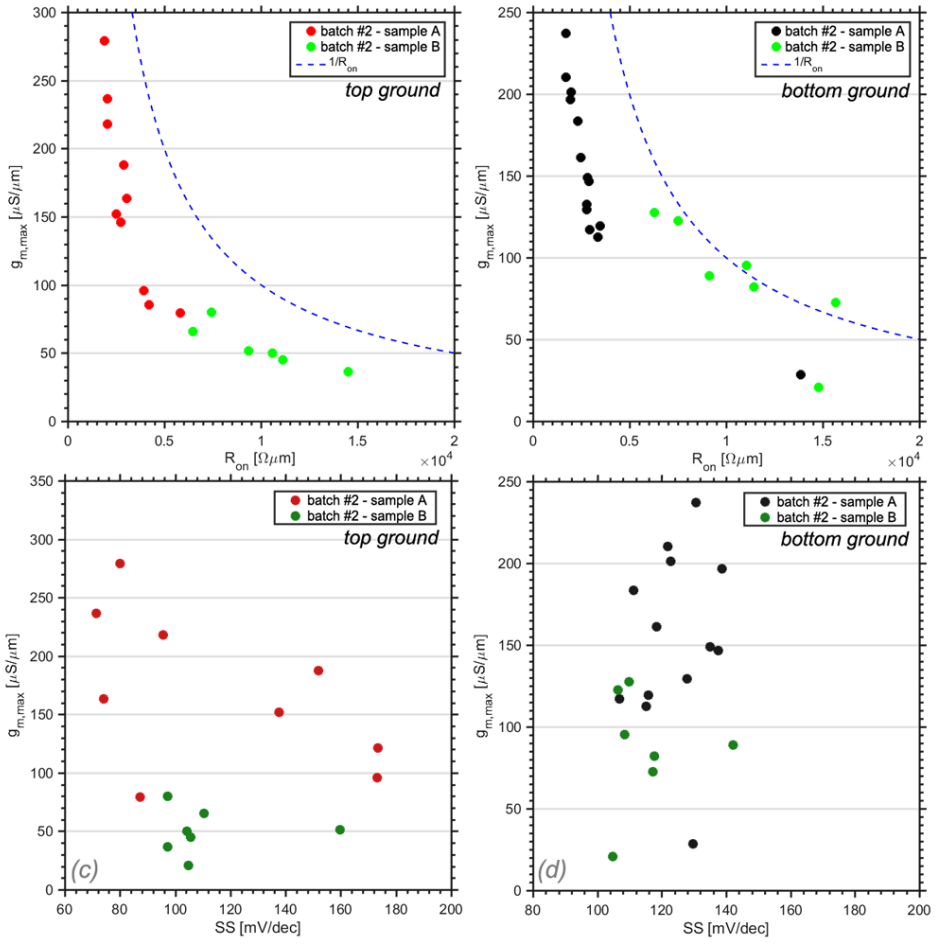

Fig 5.4: Overview of all arrays in batch 2. No sidewall etch was performed on *sample B*, meaning that the effective diameter of the nanowires are smaller in *sample A*, see Table 5.1. (a)-(b) shows the correlation between extracted values R_{on} and $g_{m,max}$, clearly showing the expected exponential trend when decreasing the total resistance. (c)-(d) Outlines *SS* dependence of $g_{m,max}$, showing no clear trend.

The importance of lowering the resistance of the system, quantified by R_{on}, is visually presented in Fig. 5.4 where measured g_m is proven to be inversely proportional to R_{on}. *Sample B* has in general a boost in performance when switching from tg to bg configuration. The opposite is true for *sample A* where the highest g_m devices are shifted downwards, but the trend is not consistent for all devices. An increase in gate control, quantified by SS, can be observed for *sample A* and for tg in general. Increased gate control overall is not consistent with a boost in g_m.

The SS dependence on V_t is further explored in Fig 5.5 and the access resistance $R_c = R_s + R_d$ is extracted. Turning a device on at a faster rate could lower the threshold voltage, but no clear correlation can be seen. This is likely due to other effects being more prominent such as voltage division over the contacts. Therefore the access resistance is examined for the best sample and estimated to 1500 $\Omega\mu$m. Due to collapsed structures leading to increased resistance all devices with $R_{on} > 2800$ $\Omega\mu$m are discarded for a fair extrapolation. Notice that the extrapolated values are used as a rough estimate of the present access resistance. The slope of the extrapolation indicates that the resistance inside the channel is also large with a 1:1 ratio at $L_g = 180$ nm which is likely a combination of of potential barriers together with the higher bandgap of InGaAs. Compared to previous InAs devices fabricated with the same process the resistance was estimated to a lower value of $R_c = 750$ $\Omega\mu$m [48]. These devices, on the other hand, had a highly doped overgrown InAs shell which likely decreased the resistance originating from the Schottky contacts. The short gate-length is a result of both long top metal but also a large bottom spacer, $\approx$ 120 nm. This does not seem to influence on the contact resistance greatly, in tg, due to the clear reduction of R_{on} for the short L_g devices.

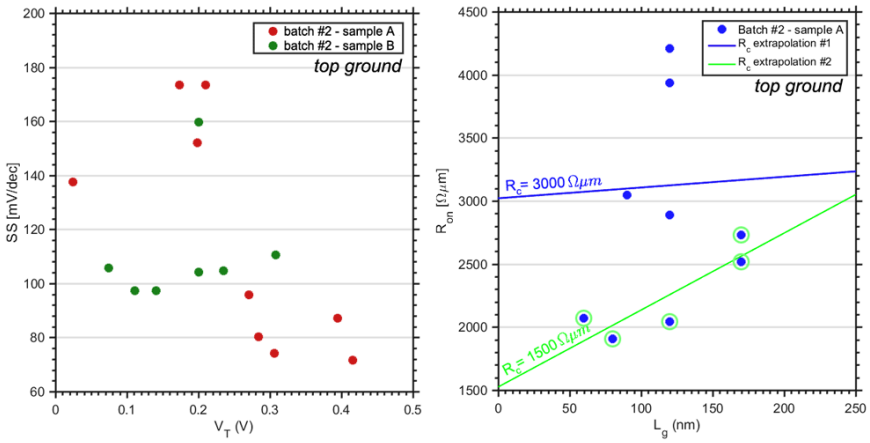

Fig 5.5: Exhibiting the SS-V_t and R_{on}-L_g dependence. Attempts for extrapolating the access resistance, $R_c = R_s + R_d$, are performed with taking all values into account (#1) and a selected few (#2) that are highlighted. A smaller ratio of collapsed nanowires seem to be present in the highlighted devices. Note that the L_g values are based on estimates from SEM pictures that, in this case, might be insufficient due to large thickness variation of the bottom spacer.

5.2.1 Device Characteristics

One device with good characteristics have been hand picked to delve into all performance metrics. Many devices showed improved current levels in bottom ground configuration which is contrary to the band gap simulations, see Table 5.2. The greatest transistors broke the trend with slightly improved currents in top ground indicating that the R_s, originating from the top contact, for these devices were likely low. DC characteristics for the best, and most representative, device is seen in Fig 5.6 & 5.7 and metrics are compiled in Table 5.2.1.

The device shows promising off-state performance with low SS, of 80 mV/dec, being close to constant from $V_{gs} = -0.16$ V to $V_{gs} = 0.2$ V. The maximum g_m hits the mark of 280 μS/μm, in top ground, and slightly lowered to 250 μS/μm when switching configuration. The off-state current is improved many orders of magnitude with tg. A promising metric is the low g_d (at V_{ds}, $V_{gs} = 0.5$ V) which is 2 μS/μm. It is expected to get better saturation, low and consistent g_d, when the potential drop occur over the high band gap segments. This should be reflected in tg, which is not the case. This raises questions about the InAs present in the bottom, or gate-misalignment of the nanowire, see Fig 4.1. Overall the R_{on} metric is large (1700 $\Omega\mu$m) and has to be reduced with better contacts in order to reach competitive values, see Table 5.4. The goal was to keep the channel intrinsic to ensure good crystal quality, but in reality the segment is unintentionally doped which can reduce the crystal quality, see Fig 3.4. Therefore the channel itself is also providing large resistance to the system.

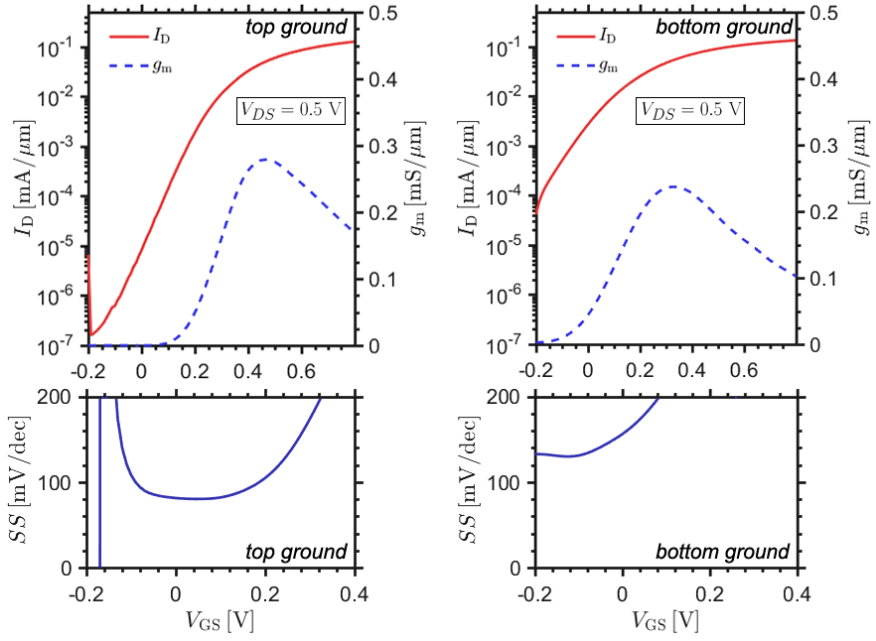

Fig 5.6: Transfer characteristics, plotted in logarithmic scale, for the hero device found batch #2. Metrics compiled in Fig 5.2.1.

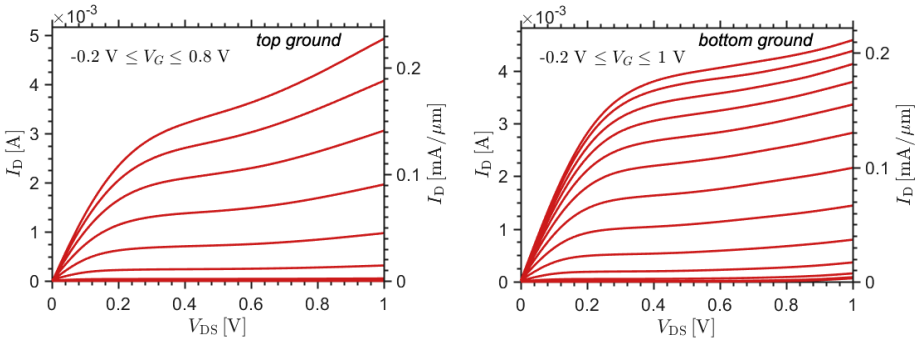

Fig 5.7: Output characteristics for the hero device found batch #2. Metrics compiled in Fig 5.2.1.

Table 5.3: Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. [1]Bias conditions are chosen in active region of the transistor at $V_g = 0.5$ and $V_{ds} = 0.5V$.

Batch #2	Metric	Value	Unit	*remarks*
	geometry	double row	-	
	# of nanowires	300	-	
	diameter	30	nm	
	high κ: Al_2O_3/HfO_2	10/40	cycles	
	high κ thickness	4.5	nm	
	gate length L_g	80	nm	
	gate leakage I_g	~ 1	pA	
bottom ground	$g_{m,max}$	250	μS/μm	
	SS	130	mV/dec	
	g_d	2	μS/μm	
	Q	1.9	kS·dec/Vm	
	$A_{v,oc}$	25	125	*bias* [1]
	R_{on}	1700	Ω · μm	*bias* [1]
	I_{on}	54	μA/μm	*bias* [1]
	V_t	0.1	V	
top ground	$g_{m,max}$	280	μS/μm	
	SS	80	mV/dec	
	g_d	2	μS/μm	*bias* [1]
	Q	3.5	kS·dec/Vm	
	$A_{v,oc}$	140	-	*bias* [1]
	R_{on}	1900	Ω · μm	*bias* [1]
	I_{on}	84	μA/μm	*bias* [1]
	V_t	0.28	V	

5.3 Benchmarking

To understand the possibilities and motivate key choices in processing it is crucial to do benchmarking, see Table 5.4. The general, and expected, trend is improved g_m with decreased dimensions, specifically L_g. The off-state performance is also sacrificed to reach high g_m with SS-values well above 60 mV/dec (theoretical limit) for the record devices. The first batch had catastrophic transconductance $g_{m,max}$ with only a single device with sufficient gate-control, SS = 103 mV/dec. In the second batch the current levels and g_m were drastically improved but still low in comparison similar vertical devices. Previous generation utilized an overgrown highly doped InAs shell, covering the nanowires, which will improve the contact (Schottky) between semiconductor and metal [59]. This overgrowth is not present on the nanowires used in this thesis. To improve interface the semiconductor-metal interface alternative metals can be used such as nickel (Ni). The Ni metal has a tendency to react and form an alloy between the metal and semiconductor decreasing the resistance and transfer length [60].

Table 5.4: A comparison with mainly other work from the research group (Nanoelectronics Group), created in the same lab using mostly the same equipment. V highlight the vertical orientation of the device, other devices utilize a lateral geometry. Notice that all V-NW devices are integrated on silicon while the both the HEMT and record device are based on an InP(III-V) substrate.

Technology	Channel	$g_{m,max}$ mS/μm	SS_{min} mV/dec	L_g nm	reference
V-NW MOSFET	InGaAs/InAs	0.28	80	110	batch #2
V-NW MOSFET	InGaAs/InAs	0.01	103	220	batch #1
V-NW MOSFET	InAs	1.02	124	130	[47]
V-NW MOSFET	InAs	0.73	420	150	[44]
NW MOSFET	InGaAs	3.30	118	60	[57]
HEMT	InGaAs	2.5	115	40	[58]

5.4 Breakdown

A few devices, from batch #2, was chosen for testing the limit for destructive breakdown V_B and is reported to occur slightly below $V_{ds} = 4V$ in the standard top ground configuration, see Fig 5.8. Different devices could be continually pushed to high bias conditions, with $V_{ds} \leq 3.5V$, and show repetition of largely the same output characteristics with no major sign of damage. Notice that the currents are still relatively low and the effective voltage over the gate is also reduced due to large contact resistance. Impact ionization can be spotted starting from 0.6 V and accelerating after 2.2 V. The impact ionization might not be the only effect leading to increased currents, also tunneling can be present, see Fig 1.8.

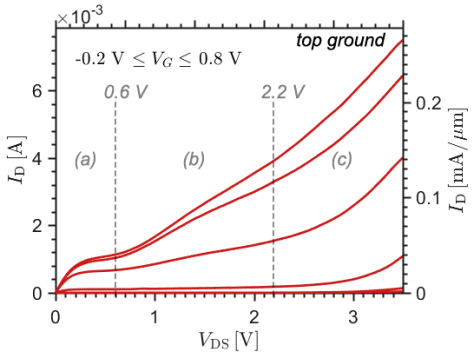

Fig 5.8: Output characteristics for a representative, double row, device at bias conditions close to its breakdown at 4 V. The device is found batch #2-*sample A*. The transistor can operate up to 3.5 V, but showcases bad saturation with high g_d. Different segments can be identified with (a) being well saturated and (b) showing impact ionization that accelerates further in (c).

In top ground the voltage drop will occur in a high bandgap region unlike bottom ground where only InAs is present, see Fig 3.3. To study if this is actually translated to the processed devices, the destructive breakdown for both configurations is given in Fig 5.9. The theory can be clearly confirmed with the device breaking at 2.2 V in bg compared to 4 V when switching configuration. Surprisingly the trends of the curves are completely different with tg indicating some form of extra potential barriers suppressing the current which might be linked to the heterobarrier present in the nanowire structure.

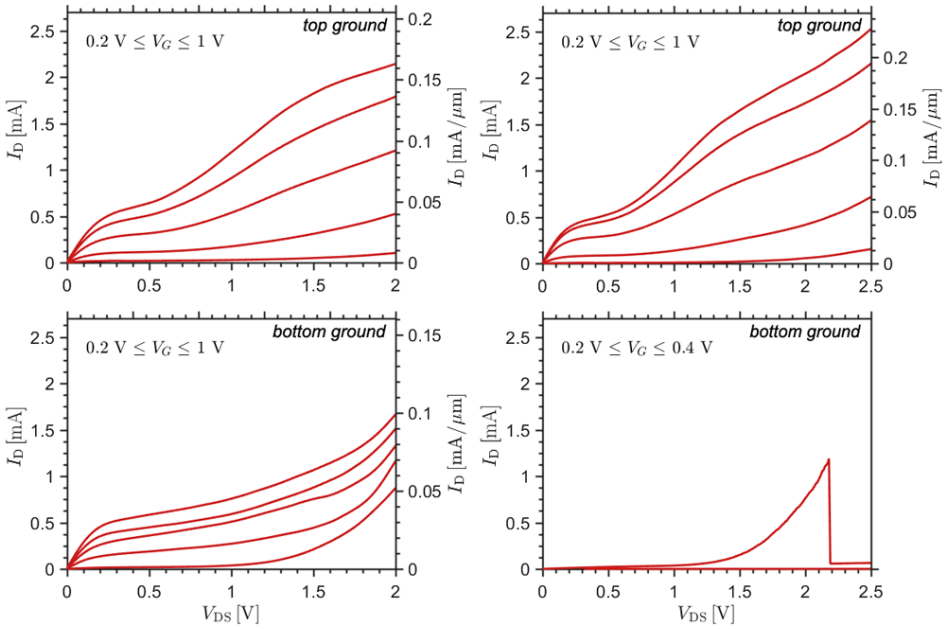

Fig 5.9: Comparing output characteristics for top and bottom ground configuration in a representative, double row, device. The device is found batch #2-*sample A*. The transistor breaks at 2.2 V in bottom ground. Different segments can be identified with (a) being well saturated and (b) showing impact ionization that accelerates further in (c).

Chapter 6

Conclusion & Outlook

The benefits of introducing an InGaAs/InAs heterostructure as channel material has proven necessary for improved stability of the transistors, with good saturation of g_d. In the end mixing of III-V materials is a great advantage and possibility when utilizing the bottom up approach with epitaxial growth of nanowires. Therefore this study has served to gain evidence of the quality and control of growth techniques. Initially the control of doping was questioned, if the in-situ doping would provide enough precision for doping of the short bottom segment present at the drain side while keeping the channel close to intrinsic (unintentionally doped). The typical characteristics of a junctionless transistor is bad modulation of current and a depletion type transistor (on-state by default). The processed transistors exhibit none of these behaviours with $V_t > 0$ V and $SS < 90$ mV/dec.

Quality of the bi-layer high-κ is also surprisingly good (low SS and gate leakage) and is likely connected to the state of the ALD chamber. Nonetheless it proves the presence of a good nanowire surface for the high-κ interface and motivates further implementation of the bi-layer.

The created transistors are also commercially viable due to the III-V integration on top of silicon. The geometry itself has conceptually many benefits with its GAA configuration and decoupling of footprint area with the actual length of the device.

The DC characteristics are insufficient for further investigation of RF capabilities due to the high resistance of the structure $R_c \approx 1500\Omega\mu$m and collapse of nanowires. Both of these problems can be addressed in the near future by utilizing shorter nanowires ($\sim$ 300 nm), introducing annealing, better control of the ICP-RIE process and possibly using a highly doped overgrowth. The latter steps are necessary for improvement of the metal-semiconductor junction, notice that a change in top metal all together is also possible.

The orientation of the heterostructure lends itself to top grounded configuration with the drain pad situated at the bottom. Which might prove useful due to heat developing in the substrate rather than top contact. After creating matching networks and other necessary circuity, in addition to the devices, heat development in the substrate is convenient for efficient cooling.

References

[1] R. G. Arns, "The other transistor: Early history of the metal-oxide semiconductor field-effect transistor," *Engineering Science and Education Journal*, vol. 7, issue 5, pp. 233–240 (1998)

[2] A. G. Levine, "John Bardeen, William Shockley, Walter Brattain; Invention of the transistor - Bell laboratories," *APS physics* (2010)

[3] G. E Moore, "Cramming more components onto integrated curcuits," *Electronics* vol. 38, no. 8, pp. 114-117 (1965)

[4] D. J. Frank, "Power constrained CMOS scaling," *IBM Journal of Research and Development* vol. 46, issue 2.3, pp. 235-244 (2010)

[5] F. Mattern & C. Floerkemeier, "From the internet of computers to the internet of things," *Active Data Management on Event-Based Systems and More* vol. 6462, pp. 242-259 (2010)

[6] A. Wacker, "Notes for solid state theory," *Matematisk Fysik, Lund University*, chapter 1, pp. 1–14 (2014)

[7] G. Grossman, "Fasta tillståndets fysik," *Lund University*, chapter 5, pp. 113–143 (2014)

[8] C. R. Nave "The doping of semicondictors," *Hyperphysics* (2005)
`http://hyperphysics.phy-astr.gsu.edu/hbase/solids/dope.html`

[9] NPTEL "Fundamental concepts of semiconductors," *IIT DELHI* (2013)
`http://nptel.ac.in/courses/115102025/8`(2016-08-15)

[10] W. Mönch, "Role of Virtual Gap States and Defects in Metal-Semiconductor Contacts," *Universität Duisburg*, vol. 4, pp 224-227, (1990)

[11] R. Islam et al., "Schottky barrier height reduction for holes by Fermi level depinning using metal/nickeloxide/silicon contacts," *App. Phys. Let.*, No. 105, 182103 (2014)

[12] S. E. Thompson et al., "Moore's law: the future of Si microelectronics," *Elsevier ltd.* vol. 9 (2006)

[13] Electronics Tutorial, "The MOSFET" (2014)
http://www.electronics-tutorials.ws/transistor/tran_6.html/(2016-05-22)

[14] W. J. Dally & J. W. Poulton, "Digital System Engineering," *Cambridge University press* p. 158 (1998)

[15] B. J. Zeghbroeck, "The energy band diagram of the Metal-Oxide-Silicon (MOS) Capacitor," chapter 6.2 (1996)
http://ecee.colorado.edu/~bart/book/moseb.htm/

[16] W. Liu, "Fundamentals of III-V devices: HBTs, MESFETs, and HFETs/HEMTs," *Wiley-Interscience publication* (1999)

[17] H. Brech, "Optimization of GaAs based High Electron Mobility Transistors by Numerical Simulations: The Principles of a HEMT," dissertation, chapter 2 (1998)

[18] P. Abrahams et al., "Intel 22 nm 3-D tri-gate transistor technology," *Intel* (2011)
newsroom.intel.com/press-kits/
intel-22nm-3-d-tri-gate-transistor-technology/ (2016-07-15)

[19] L. M. Terman. "Solid State electronics: An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Elsevier ltd.*, vol. 5, issue 5, pp. 285–299 (1962)

[20] J. Robertson et al. "Defect State Passivation at III-V – oxide Interfaces for CMOS devices ," *J. Appl. Phys.* no. 117, 112806 (2015)

[21] J. Wu et al., "Low Trap Density in InAs/High-k Nanowire Gate Stacks with Optimized Growth and Doping Conditions," *Nanoletters* (2016)

[22] R. S. Chau et al., "Intel's Breakthrough in High-K Gate Dielectric Drives Moore's Law Well into the Future," *Technology@Intel Magazine January* (2004)

[23] G. Ribes et al., "Review on High-k Dielectrics Reliability Issues," *IEEE* vol. 5, No. 1 (2005)

[24] J. Robertson et al., "High dielectric constant oxides," *Eur. Phys. J. Appl. Phys* vol. 28, pp. 365–291 (2004)

[25] D. Liang & J.E. Bowers, "Photonic integration: Si or InP substrates?" *Electronics Letter* vol. 45, no. 12 (2009)

[26] L. C. Chuang et al., "Critical diameter for III-V nanowires grown on lattice-mismatched substrates," *Appl. Phys. Lett.* No. 90, 043115 (2007)

[27] D. Yakimets et al., "Vertical GAAFETs for the Ultimate CMOS scaling," *IEEE* pp. 1433-149, 15072197 (2015)

[28] J. A. del Alamo et al., "Nanometre-scale electronics with III–V compound semiconductors," *Nature* vol. 479, pp. 317–323 (2011)

[29] F. D'Agostino & D. Quercia, "Short channel effects in MOSFETs," *VLSI report* (2000)
http://www0.cs.ucl.ac.uk/staff/ucacdxq/projects/vlsi/report.pdf/ (2016-07-20)

[30] A Lubow et al., "Comparison of drive currents in metal-oxide-semiconductor field-effect transistors made of Si, Ge, GaAs, InGaAs, and InAs channels," *App. Phys. Letter* No 96 (2010)

[31] T. Pesic-Berdanin et al., "Strained Silicon Layer in CMOS Technology," *Electronics* vol. 18, no. 2 (2014)

[32] J. Y. Tsao, "The world of compound semiconductors: A guidebook to the core science and tehcnology," *Sandia National Laboratories* pp. 1-7 (2004)

[33] R. Kim et al., "Comprehensive performance benchmarking of III-V and Si nmosfets (gate length=13 nm) considering supply voltage and off-current," *Electron Devices, IEEE transactions on,* vol. 62, no. 3, pp. 713-721 (2015)

[34] D. Kim et al., "Extraction of virtualsource injection velocity in sub-100 nm III-V hfets," *Electron Devices Meeting (IEDM), 2009 IEEE International,* pp. 1-4 (2009)

[35] R. Flückiger et al., "Type II InP/GaAsSb double-heterojunction bipolar transistor with $f_{MAX} > 700$ GHz," *Applied Physics Exress* vol. 7 (2004)

[36] E. O. Kane et al., "Theory of tunneling," *Journal of applied physics* (1961)

[37] J. H. Davies et al., "The physics of low-dimensional semiconductors," *Cambridge University Press,* Appendix 2, pp. 410-411 (2009)

[38] X. Mei et al., "First demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor," *IEEE Electronic Device Letters* vol. 36 (2015)

[39] W. Maes et al., "IMPACT IONIZATION IN SILICON: A REVIEW AND UPDATE ," *Solid-State electronics,* vol. 33, No. 6, pp 705-718 (1990)

[40] O. Triebl et al., "Reliability issues in High Voltage Semiconductors," *Vienna University* chapter 5.1, (2013)

[41] W. Jo et al., "First Demonstration of GaN based Vertical Wanowire FET with Top-Down approach," *IEEE* (2015)

[42] T. Krishnamohan et al., "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and <60mV/dec Subthreshold Slope," *IEEE*, Stanford University, CA (2008)

[43] G. Constable et al., "A century of innovation: Twenty engineering achievements that transformed our lives," *Joseph Henry Press* (2003) `http://www.greatachievements.org/?id=3956`(2016-07-16)

[44] S. Johansson et al., "RF Characterization of Vertical InAs Nanowire MOSFETs with ft and fmax above 140 GHz," *IEEE*, Lund University (2010)

[45] B. Feng et al., "Schottky barrier heights at the interfaces between pure-phase InAs nanowires and metal contacts," *J. Appl. Phys. 119,* 054304 (2016)

[46] Sofia. Johansson, "Vertical Nanowire High-Frequency transistors," *EIT, Lund University* Doctoral dissertation (2014)

[47] M. Berg, "Vertical InAs Nanowire Devices and RF circuits," *EIT, Lund University* Doctoral thesis (2015)

[48] M. Berg et al., "Self-Aligned, Gate-Last Process for Vertical InAs Nanowire MOSFETs on Si," *IEDM15-805, Lund University* (2015)

[49] J. Wu et al. "Control of composition and morphology in InGaAs nanowires grown by metalorganic vapor phase epitaxy," *Journal of crystal growth* vol. 383, pp 158-165 (2016)

[50] J. Wu, "Vertical III-V/High-k Nanowire MOS Capacitors and Transistors," *EIT, Lund University*, doctoral thesis (2016)

[51] H. J. Choi et al., "Semiconductor Nanostructures for optoelectronic devices," *Springer-Verlag* chapter 1, pp. 3-10 (2012)

[52] W. Ahmed et al., "Ion implantation and in-situ doping of silicon," *Materials, Chemistry & Physics*, 37, pp. 289-294 (1994)

[53] Dow Corning corporation., "Information about FOx-1x and FOx-2x flowable oxides," *Product Information*, No. 10-713A-01 (2005)

[54] E. Memisevic et al., "The electron beam defined hydrogen sisesquioxane spacers for vertical nanowire transistors," *JVSTB*, 32, 051211 (2005)

[55] ROHMHAAS Electronic Materials., "Material Safety Data Sheet; MF319" (2004)

[56] J. J. Hill et al., "Eliminating Capillary Coalescence of Nanowire Arrays with Applied Electric Fields", *ACS Appl. Mater. Interfaces*, 2 (7), pp 1992–1998 (2010)

[57] C. B. Zota et al., "Single suspended InGaAs nanowire MOSFETs", *IEDM15-811*, (2015)

[58] X. Zhao et al., "Vertical nanowire ingaas mosfets fabricated by a top-down approach," *IEDM*, (2013)

[59] J. M. Shannon et al. "Control of Schottky barrier height using highly doped surface layers," *Elsevier ltd.*, vol. 19, issue 6, pp 537-543 (1976)

[60] S. H. Kim et al. "Self-Aligned Metal Source/Drain InxGa1-xAs n-Metal–Oxide–Semiconductor Field-Effect Transistors Using Ni–InGaAs Alloy," *Applied Physics Express*, vol. 4, no. 2 (2011)

Appendix A

Batch #1 metrics

The metrics for the first batch containing only one working transistor is included in this appendix.

Table A.1: Outlining all metrics for the best device in batch #1. Values are extracted from SEM inspections. All data is normalized to the total circumference of the nanowires. [1]*A mean value has been extracted from SEM inspections of other pads* [2]*Bias conditions are chosen in active region of the transistor at* $V_g = 0.5$ *and* $V_{ds} = 0.6V$.

Batch #1	Metric	Value	Unit	*remarks*
	geometry	pad	-	
	# of nanowires	107	-	
	diameter	31	nm	*mean* [1]
	high κ: Al_2O_3/HfO_2	10/40	cycles	
	high κ thickness	4.5	nm	*mean* [1]
	gate length L_g	220	nm	
bottom ground	$g_{m,peak}$	10	mS/mm	
	SS	103	mV/dec	
	g_d	-	mS/mm	*no sat.*
	Q	0.097	kS·dec/Vm	
top ground	$g_{m,peak}$	2.5	mS/mm	
	SS	92	mV/dec	
	g_d	0.10	mS/mm	*bias* [2]
	Q	0.027	kS·dec/Vm	
	$A_{V,OC}$	25	-	*bias* [2]
	R_{ON}	$940 * 10^3$	$\Omega \cdot \mu$m	*bias* [2]

LUND
UNIVERSITY

Series of Master's theses
Department of Electrical and Information Technology
LU/LTH-EIT 2016-537
http://www.eit.lth.se