Master's Thesis

Design and Test of an L-Band (GNSS) Low Noise Amplifier and Limiter

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Together ahead. RUAG

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MASTER THESIS

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Abstract

This thesis work was performed at RUAG Space AB, Göteborg, Sweden. The aim of this thesis is to test the performance boundaries of SiGe based heterojunction bipolar transistor in designing a low noise amplifier meant for GNSS applications.

After careful consideration of different alternatives for active components in SiGe HBT process, BFY640-04 from Infineon [1] was selected as the active component for the design. Later, different topologies have been evaluated in Advanced Design System (ADS) software and finally a common emitter topology is selected considering cost-effectiveness, performance and simplicity. Apart from this, the functionality of a limiter component namely, GG-77015-01 from Microsemi [2] has been tested by placing it in front of the LNA. The purpose of this is to know if it can prevent the LNA from high power levels and to study its overall effect on noise figure, gain and linearity. The prototypes were fabricated on a hardback PCB consisting of Roger Duroid 6002 substrate [3].

The designed LNA has less than 1 dB (excluding limiter) noise figure, gain of 17-13 dB and input return loss of 6 dB. It is powered by a single positive supply of +5 V and has very low DC power consumption of 15 mW. Also, the noise figure is fairly low in the entire L-band apart from current GNSS bands, which provides possibility of this design to be useful in future GNSS applications too.

Acknowledgement

First of all, I would like to express my heartfelt thanks to Robert Petersson for providing me this opportunity to perform my thesis work on such an interesting topic at RUAG Space AB. His wide experience, understanding and friendly behaviour has served as a source of inspiration.

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1. INTRODUCTION

1.1 Overview

As defined by IEEE [4], L band is 1 to 2 GHz range of radio spectrum. This frequency band is widely used for Global Navigation Satellite System (GNSS) applications. GNSS is worldwide set of satellite navigation constellations, civil aviation augmentations, and user equipment. It constitutes mainly of the following navigation systems: the U.S. Global Positioning System (GPS), Russian GLONASS, European Galileo, Chinese Compass, Japanese Quasi Zenith Satellite System, and Indian Regional Navigation Satellite System (IRNSS). Out of these, current international GNSS standards for civil aviation- ICAO's Standards and Recommended Practices (SARPs) [5] address only two core constellations: the U.S. Global Positioning System (GPS) and the Russian Federation's GLONASS. The frequency allocation for each of these systems is shown in figure 1.

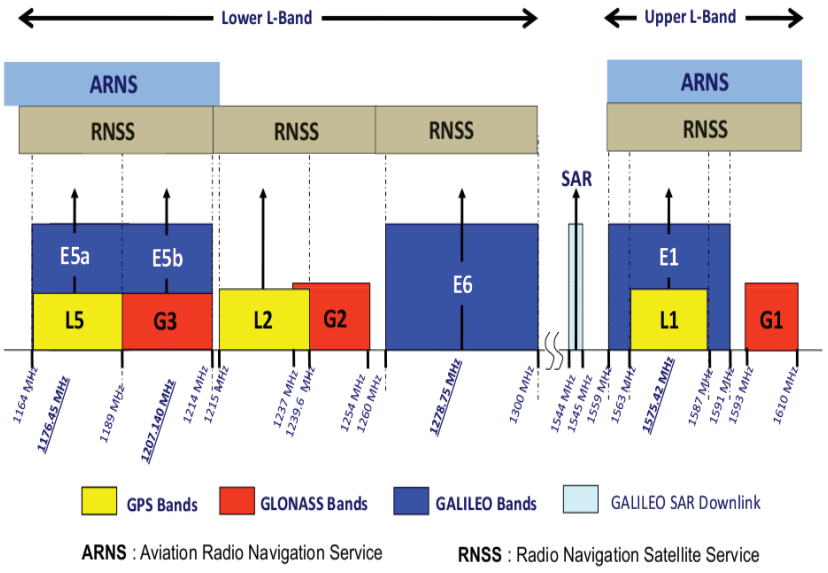


Figure 1 GNSS Frequency band allocation

GPS presently provides two services: one for civilian users referred to as the Standard Positioning Service (SPS) and one available only to authorized users (primarily the U.S. military, and the militaries of U.S. allies) referred to as the Precise Positioning Service (PPS).Glonass is newer and is used for similar applications. The only difference is that it has more satellites per orbital plane

and the code for all satellites in each frequency band is same unlike in GPS system.

1.2 Motivation

HEMT based low noise amplifier design for GNSS applications are already available at RUAG. One drawback, amongst others with those designs is that it uses two supply voltages. The aim of this thesis is to test the performance of a SiGe based heterojunction bipolar transistor (HBT) which uses only single supply and can push the performance limits of the current HEMT designs. Furthermore, a limiter component is placed and tested in front of the designed LNA with the aim that it shall help improve the overdrive capability of the LNA and hence protect the LNA against destruction.

1.3 Thesis contribution and outline

The thesis presents a design of a SiGe based low noise amplifier and PIN diode type limiter covering the entire L-Band. Hence, it's not only useful for currently allocated frequencies but for new GNSS signals as well. Emphasis was made on the most promising design and after optimization and layout work, a prototype was fabricated. Finally, RF performance of the complete circuit was measured and analyzed.

Chapter 2 covers theory regarding design of LNAs. Chapter 3 points out the design specifications. Chapter 4 describes choice of building practice, substrate, transistor and limiter to be used. Chapter 5 discusses the simulation tool used in the design. Chapter 6 discusses the transistor model and investigates various topologies. Chapter 7 presents detailed LNA design methodology and layout. Chapter 8 describes RF measurements and performance of the designed LNA. Finally, conclusion and future work are outlined in Chapter 9.

2. THEORY

Low noise amplifiers (LNAs) play a key role in radio receiver performance. As the received signal might be very weak, an LNA is used to amplify the signal with adding minimum noise to the signal. It tends to dominate the noise figure and sensitivity of the complete receiver. Figure 2 [6] shows the set of variables that affect LNA performance at the device and board design levels. The designer needs to find out most appropriate trade-offs between competing characteristics to optimize the receiver sensitivity and selectivity.

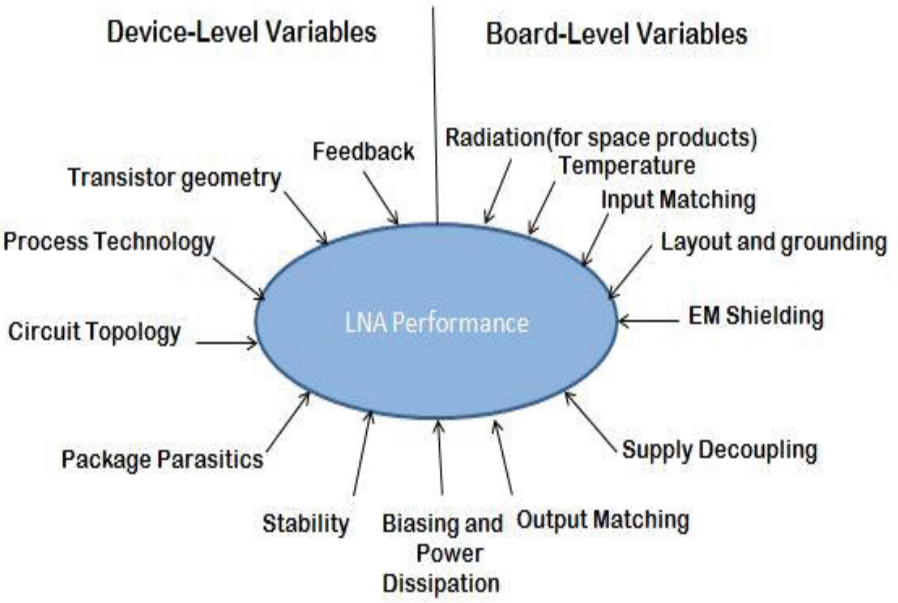


Figure 2 LNA Performance Variables

The various parameters that influence the design of LNA are discussed in detail below:

2.1 Noise figure

It is defined as ratio of available signal-to-noise ratio at the input to the available signal-to-noise ratio at the output [7], according to equation 1.

$$\mathrm{NF} = \frac{\mathrm{SNRin}}{\mathrm{SNRout}} \tag{1}$$

For a chain of n-cascaded amplifiers, total noise figure is given by Friis formula as:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_2 - 1}{G_1.G_2} + \frac{NF_3 - 1}{G_1.G_2.G_3} \ldots\ldots \frac{NF_n - 1}{G_1.G_2.G_3 \ldots\ldots G_n} \tag{2}$$

where G is the available power gain. From equation 2, we see that noise contribution from stage 1 is the significant contributor and must be dealt with utmost care for high performance receiver system. In order to achieve as low noise figure as possible, it is desirable to have low noise figure and high gain in the first amplifier stage.

In order to obtain minimum noise figure at the input of first stage of a receiver, matching needs to be performed at the input. This is explained using the following equation [8]:

$$NF = 10 \cdot \log(F_{min} + \frac{R_n}{Re(Y_{source})} \cdot \left|Y_{source} - Y_{opt}\right|^2) \qquad (3)$$

- Y_{opt} is the normalized input admittance at which noise figure is minimum. Complex conjugate of Y_{opt} (S_{opt} in terms of reflection coefficient) must be presented to the LNA input for best possible noise performance,
- F_{min} is minimum achievable noise figure when $Y^*_{source} = Y_{opt}$ (or, $Y^*_{opt} = Y_{source}$),
- R_n is the equivalent noise resistance
- Y_{in} is the normalized input admittance for maximum power transfer
- Y_{source} is the normalized admittance presented to LNA input

2.2 Bias selection

Setting the bias for LNA is the first most critical step in the implementation. In most cases, where the active device to be used is known, we must carefully select the right bias point to find best compromise between gain, noise figure, linearity for any given application.

2.3 Stability

LNA design becomes incomplete without checking its stability. The idea is to make the LNA unconditionally stable.

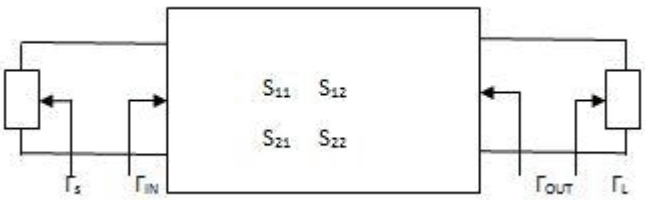


Figure 3 Active two-port network

Figure 3 shows an active two-port network characterized by its scattering matrix, S. Mathematically unconditional two-port stability exists when [9]

$$|\Gamma_S\Gamma_{IN}| < 1 \text{ and } |\Gamma_L\Gamma_{OUT}| < 1 \text{ for all } |\Gamma_S| \leq 1, |\Gamma_L| \leq 1 \qquad (4)$$

This implies:

$$|\Gamma_{IN}| = \left|s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1-s_{22}\Gamma_L}\right| < 1 \text{ and } |\Gamma_{OUT}| = \left|s_{22} + \frac{s_{12}s_{21}\Gamma_L}{1-s_{11}\Gamma_s}\right| < 1 \qquad (5)$$

The above is guaranteed when the stability factor K is greater than unity,

That is, $K = \frac{1-|s_{11}|^2-|s_{22}|^2+|\Delta|^2}{2|s_{12}s_{21}|} > 1$

And, $|\Delta| = |s_{11}s_{22} - s_{12}s_{21}| < 1$

If a two-port network satisfies both the above conditions it is said to be unconditionally stable. Otherwise it is potentially unstable.

In the above definition, two conditions are required to guarantee stability. Also, the magnitude of K doesn't give us much insight as to what to do when the value is less than 1. In another approach only one condition is needed to be fulfilled [10]. It is given as:

$$\mu = \frac{1-|s_{11}|^2}{|s_{11}-\Delta(s_{22}{}^*)|+|s_{12}s_{21}|} > 1 \qquad (6)$$

It gives the distance from center of Smith Chart to the nearest output (load) stability circle or nearest point of instability on input stability circle. Similarly, μ' can also be calculated and it will give the distance from output stability circle. Furthermore, in order to analyze stability such that all loop oscillations are well predicted an S-probe method is used [10]. It can detect special cases of instability involving active terminations and is very useful for multistage active circuits. In this technique, near lossless circuit elements called s-probes are placed at the input and output of active network in the simulation tool. The s-probe circuit extracts the terminating impedances $\mathrm{Z_S}, \mathrm{Z_{IN}}, \mathrm{Z_{OUT}}$ and $\mathrm{Z_L}$. From these impedances reflection coefficients are calculated and checked against oscillations for a two-port network in the simulation tool. Network stability is also assessed by observing if polar plots of frequency versus reflection coefficient products for given source and load terminations encircle the critical point (1,0).

2.4 Input and output matching network

On the input side, impedance matching is needed to minimize reflection and obtain an acceptable noise figure and gain. Obtaining minimum noise figure and maximum gain at the same time is usually difficult. By use of an input match network, we can get optimum reflection coefficient. And then depending on design requirements, we can design to get either optimum gain or noise figure. It mostly requires some compromise. The most important objective is usually to

have a good noise figure. At the same time, good input return loss can be achieved with two parallel stages in 90° hybrid configuration where the reflection is terminated in a load connected to the 90° hybrid. Similarly, on the output side, matching network is implemented to get best compromise between maximum gain, OIP3 and P1dB [6]. In case of a design consisting of several transistor stages, inter stage matching is done at the output of each stage. All these matching circuits can be designed either by using lumped components or distributed elements.

3. DESIGN SPECIFICATIONS

The various specifications for the design of low noise amplifier are listed below:

a) Noise figure: A noise figure less than 1 dB was desired.
b) Stability: As stability issues were generated in a previous work carried out on L-band LNA at RUAG, a highly stable amplifier was very important consideration for the design.
c) Gain: Only a single stage transistor was to be designed. So, a sufficient gain of at least greater than 10 dB was needed.
d) Input return loss: A balanced design [11] consisting of two transistors in a 90° hybrid configuration to give good input return loss was already available at RUAG. Hence, it was just needed to obtain as good as possible noise figure from the designed LNA.
e) Output return loss: As inter-stage matching would be done later when the design is used in multi-stage LNA, there was no requirement on output return loss.
f) Limiter component: In order to make the LNA capable of working under high input power conditions, a limiter component was needed to be designed and tested.

4. CHOICE OF BUILDING PRACTICE, SUBSTRATE, TRANSISTOR AND LIMITER

4.1 Building practice

Various options for building practice are available for designing LNAs. These are discussed as follows:

1. Using discrete packaged components and transmission lines implemented on printed circuit board
2. Using bare-die chip connected by bond wires and transmission lines implemented on printed circuit board
3. Using Monolithic microwave integrated circuit(MMIC)
4. Using hybrid which is a mix of discrete, distributed and bare die chip components

As discrete packaged component was a presumption for this thesis, hence alternative 1 is chosen for the LNA design.

4.2 Substrate

A Roger Duroid 6002 substrate was selected to realize the LNA design. It has low loss and low dielectric constant which offers superior electrical and mechanical properties essential in developing complex microwave structures which are mechanically reliable and electrically stable. It has excellent high frequency performance and has low outgassing making it ideal for space applications.

The substrate parameters definition used in ADS simulation is shown in Table 1.

Table 1 Substrate Parameters

Parameter	**Value**
Dielectric constant, ε_r	2.94
Substrate Thickness, H	15 mil
Dissipation factor, δ	0.0012
Roughness	1.9 µm
Conductor Thickness, Cond	58.5 µm

4.3 Transistor

For the LNA design, a SiGe based HBT transistor was proposed to be used as it essentially eliminate the need of two (positive and negative) supply voltages, instead a single supply voltage can be used, which is easier to be implemented. Two candidates namely BFY640-04 and BFP840FESD from Infineon were suggested. Both these transistors have high gain and low intrinsic noise [1,12]. But, the former is a space qualified transistor so it was decided to proceed with that transistor in further design work.

4.4 Limiter

In order to prevent the low noise amplifier from destruction by high power input signal, a component called limiter is introduced in the design. In its most fundamental form shown in figure 4 [13], it consists of a PIN diode connected with an RF choke inductor. Both of these are connected in shunt with the main signal path.

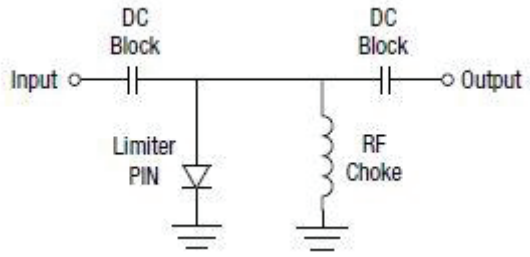


Figure 4 Single Stage limiter circuit

The PIN diode acts as an incident power-controlled, variable resistor. When no large input signal is present, the impedance of the limiter diode is at its maximum resulting in minimum insertion loss. While in case of high power input signal, the impedance of the diode goes to a very low value producing an impedance mismatch. A bias current flow through the PIN diode and the loop is completed via the RF choke. Most of the input signal power gets reflected back towards the source. When large input signal is no longer present, impedance of the diode reverts from the very low value to its maximum value after a brief delay elapses. In another kind of limiter circuit, two rectifying diodes (which could be Schottky or PN junction diodes) are utilized to limit the peak voltage of the positive and negative signal alternations, either referenced to ground or to some arbitrarily selected DC level. But these limiter circuits are typically used for low frequency applications, nominally at VHF and below. In all limiter circuits, DC blocks are used at both ends to prevent DC signals entering into the limiter.

The limiter component used in this design is GG-77015-01 from Microsemi. It has a usable frequency range of 10 MHz to 3 GHz. It provides very low insertion loss up to 0.25 dB for frequencies ≤2 GHz. The transfer curve of the limiter is shown in figure 5.

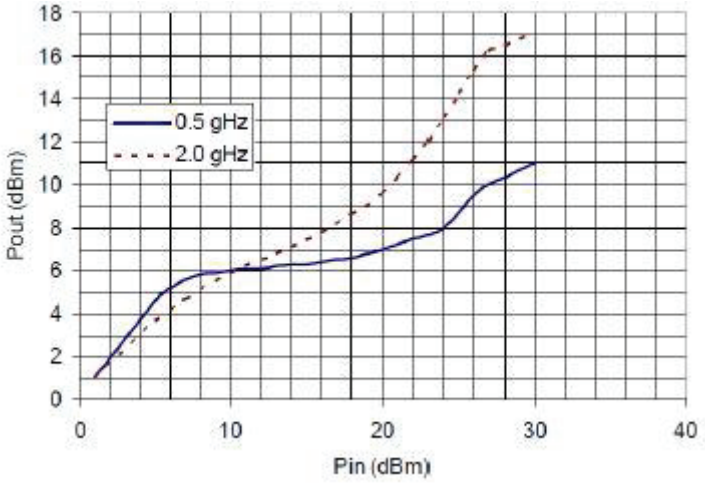


Figure 5 Output Power versus Input Power of GG-77015-01

5. SIMULATION TOOL

The design environment used in this project was Advanced Design System (ADS). It is an electronic design automation software which focuses on RF and microwave design. It supports all steps of the design process –schematic capture, layout, design rule checking, frequency domain and time domain circuit simulation, and electromagnetic field simulation—allowing the engineer to fully characterize and optimize an RF design.

6. TRANSISTOR MODEL AND INVESTIGATION OF TOPOLOGIES

In order to design the LNA with minimum noise, noise data in the band of interest (1160.5 GHz-1585.65 GHz) was required. But, neither any noise data nor large/small signal model of the transistor was available from the manufacturer. So, another SiGe transistor which had similar properties in terms of maximum stable gain and noise figure was chosen as a reference. Its large signal model was modified to obtain similar S-parameters as that of the transistor in use. The main dissimilarity between these two transistors was in their packaging. The reference has TSFP package while BFY640-04 has micro-X package. Hence the package parasitics needed to be modified. The other dissimilarity comes from the difference in reference plane of measurement. For the micro-X package BFY640-04 transistor, the reference plane is as shown in figure 6:

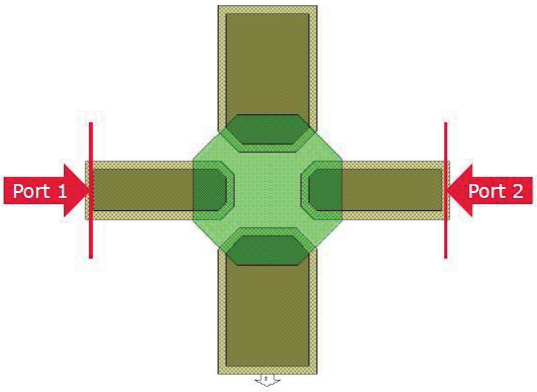


Figure 6 Reference Plane of BFY640-04

The reference plane was shifted by means of de-embedding of the transmission lines from the input and output in the s-parameter file of micro-x packaged BFY640-04 transistor as shown by the setup in figure 7.

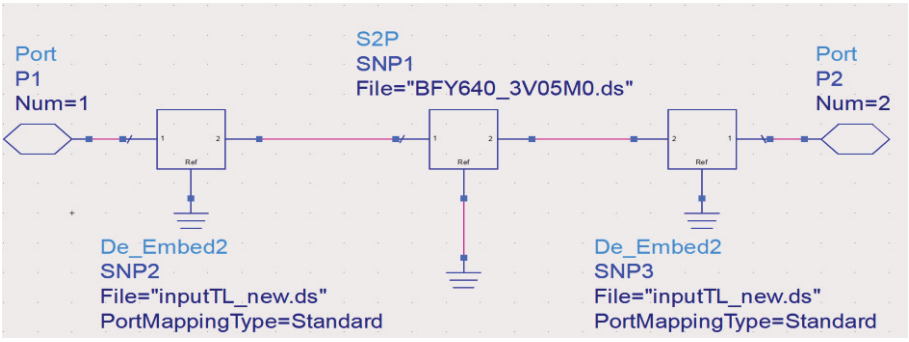


Figure 7 Simulation of De-embedded transistor (BFY640-04)

In order to deal with package parasitics dissimilarities, package parasitics of BFP640F transistor were removed and parasitics corresponding to micro-X package was added instead. The package parasitics of micro-X package was obtained from CFY25 transistor (also micro-X) and added to the large signal model of BFP640F transistor.

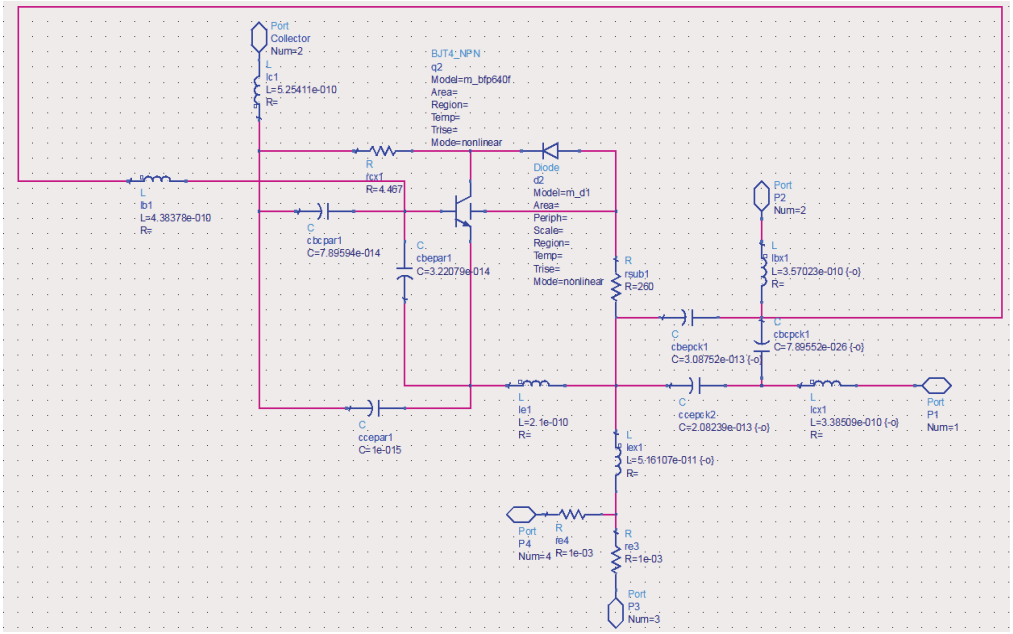
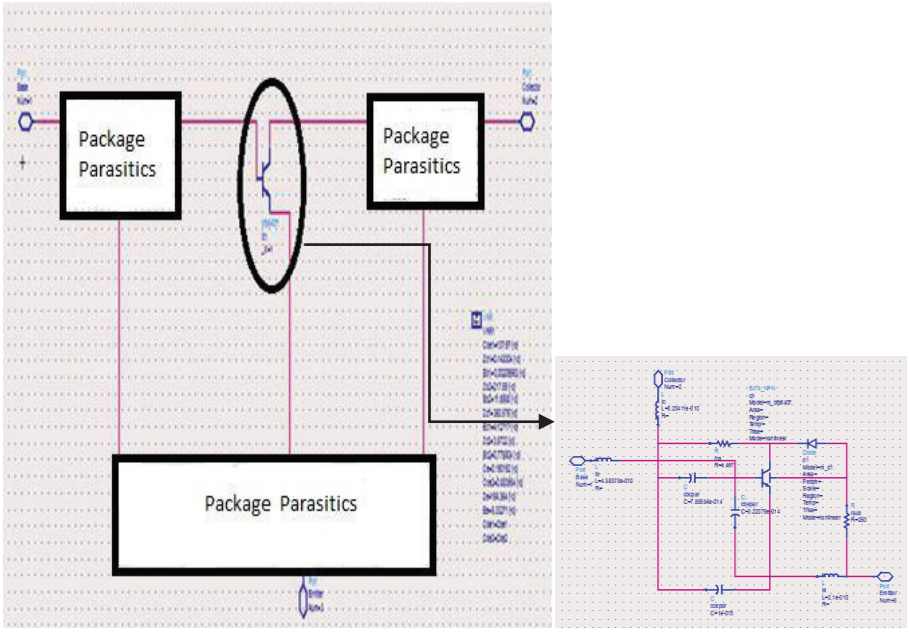


Figure 8 Large signal model of BFP640F transistor (including parasitics of TSFP package)



(a) (b)

Figure 9(a) Complete transistor model (containing micro-x package parasitics), (b) Intrinsic BFP640F transistor

The micro-x package parasitics were optimized until a good match was found with s-parameters of measured data (BFY640-04). Figure 10 shows comparison between measured data of BFY640-04 transistor after de-embedding (shown in blue) and optimized large signal model of BFP640F transistor (shown in red) for a frequency range of 50 MHz to 10 GHz.

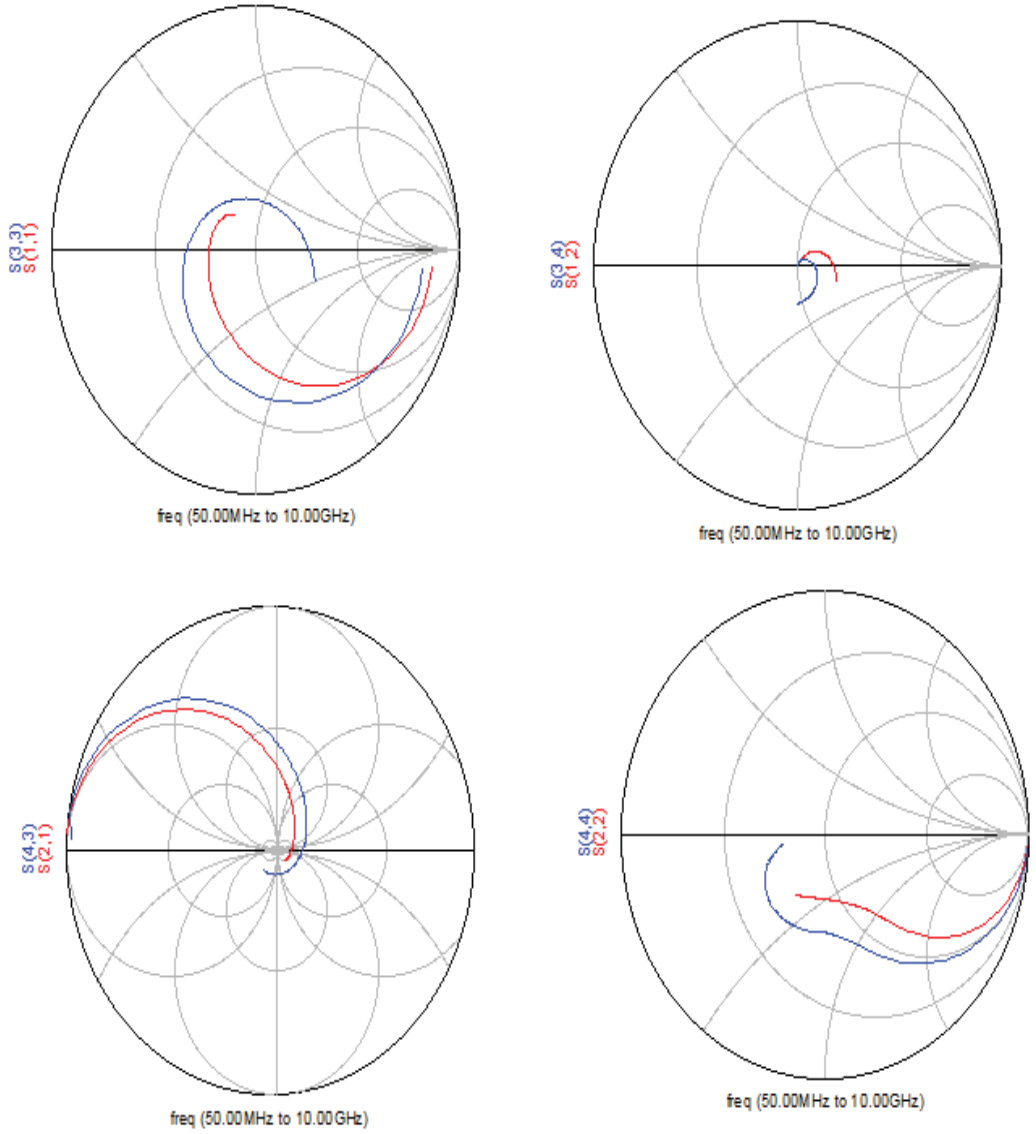


Figure 10 Comparison between measured data and large signal model

From figure 10, we can see that a good match exists between the measured data and large signal model. Now, once the transistor model was ready, it was possible to design an LNA with available noise and S-parameters from the model. Before going further with design it was considered important to analyze various topologies to get minimum noise figure from the intrinsic transistor. Different topologies analyzed at the same bias point(3V, 5 mA) are discussed in detail.

6.1 Common Emitter (Single transistor)

The noise characteristics and S parameters from a single BFY640-04 transistor without any matching network (only 50 Ω terminations) were simulated in ADS for the frequency range 1-2 GHz by selecting Ic= 5mA and Vce=5V as bias point.

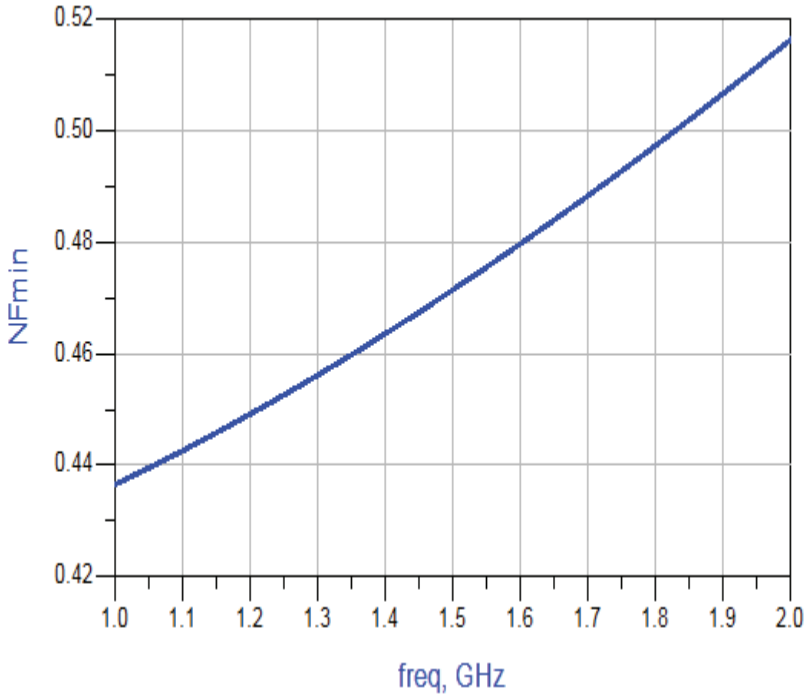


Figure 11 Minimum noise figure for single transistor

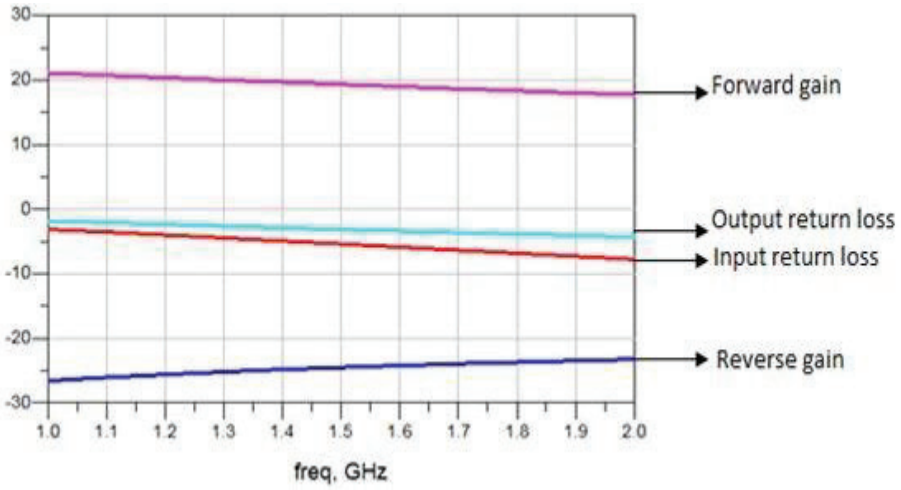


Figure 12 S parameters in Common Emitter topology

6.2 Common Emitter with inductive degeneration

In this configuration, an inductor is connected between emitter and ground. Schematic simulations were performed using ADS. This configuration helped in reducing noise figure but only by small extent. On the other hand, it had lower gain and as it could result in instability as seen in previous work done at RUAG, emitter degeneration wasn't considered beneficial for the design.

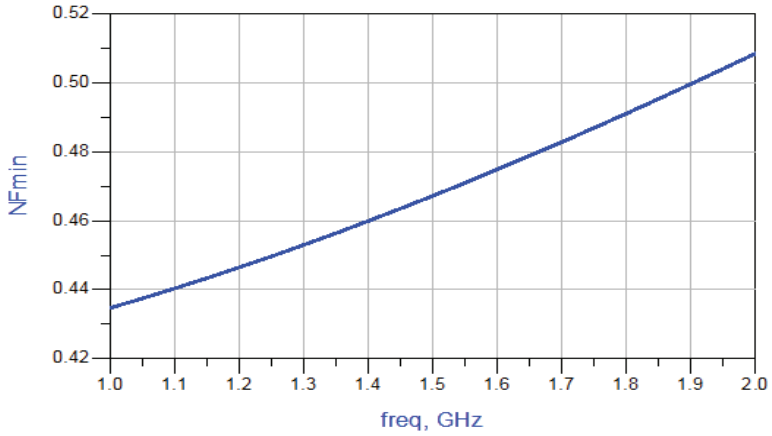


Figure 13 Minimum noise figure of Inductive Emitter Degeneration topology

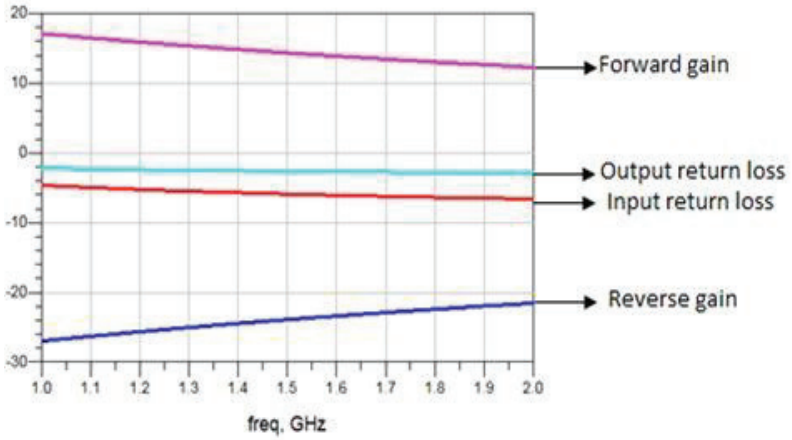


Figure 14 S-parameters of Inductive Emitter Degeneration topology

6.3 Parallel

Two transistors T1 and T2 connected in parallel are shown in figure 15. This topology had better minimum noise figure compared to single transistor topology. In theory, the optimal noise impedance (Z_{min}) for n transistors connected in parallel becomes Z_{min}/n [14]. This reduced input impedance results in reduction in noise figure.

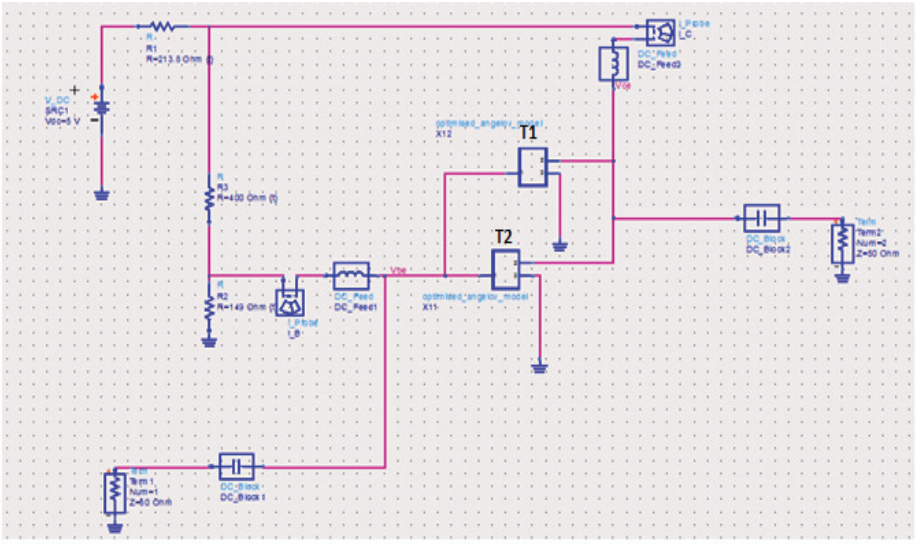


Figure 15 Schematic for Parallel Topology

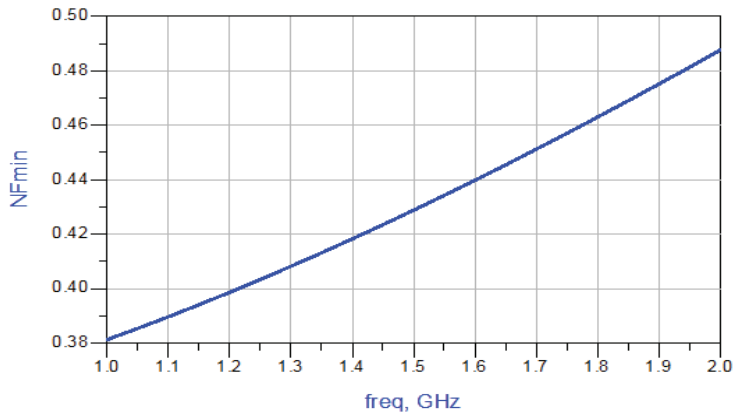


Figure 16 Minimum noise figure in Parallel topology

Although the parallel topology has better noise figure compared to single transistor configuration, it has less gain and worse input return loss in the GNSS band. This is shown in figure 17.

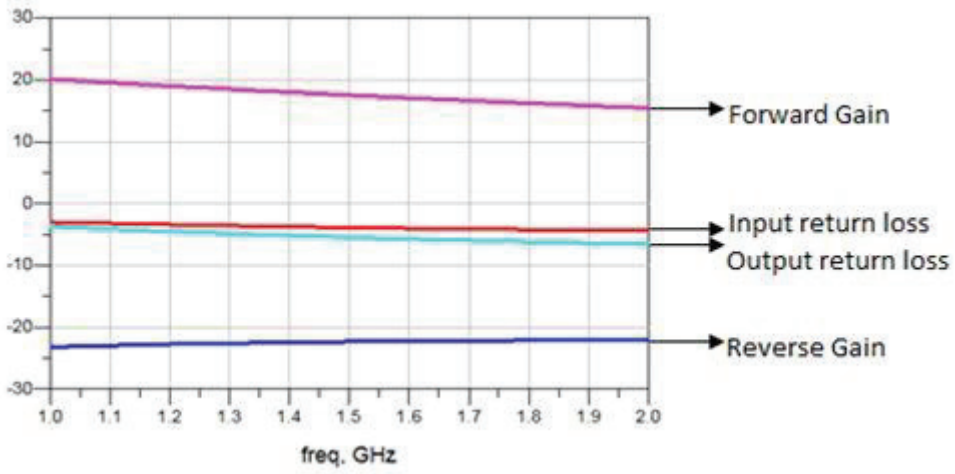


Figure 17 S-parameters in parallel topology

Owing to the advantages of creating wideband LNA [15], cascode topology in which collector of one transistor is connected to emitter of another was also tried. However, it was cumbersome to obtain right bias point for this configuration. So, it was decided not to move further with this configuration.

Hence, amongst all the four alternatives, the topology consisting of a single transistor was considered most promising with respect to achieving minimum noise, highest gain and smallest circuit size as shown in table 2.

Table 2 Comparison of different topologies for LNA design

Topology	Minimum noise figure, dB	Gain, dB	Size
Common Emitter	0.436	21	Smallest
Inductive Emitter degeneration	0.435	17	Small
Parallel	0.38	20	Large
Cascode	-	-	Large

7. DESIGN METHODOLOGY

A step by step logical procedure was followed to design the low noise amplifier, keeping in mind that the most important requirement for the design was to achieve a noise figure less than 1 dB. These are discussed as follows:

7.1 Selection of dc bias point

Biasing the transistor is the process of setting the dc operating voltages and currents to the correct level so that the ac input signal can be amplified correctly by the transistor. The goal was to select an operating point that would give sufficient output power and have very low noise figure in the GNSS band (1160.5 MHz-1585.65 MHz). From the datasheet of the reference transistor BFP640F, it was found that for I_c=5 mA and V_{CE}= 3V with Z_s= 50Ω shown in Figure 18, minimum noise figure could be obtained for the transistor in the frequency band of interest. Hence, it was selected as the bias point.

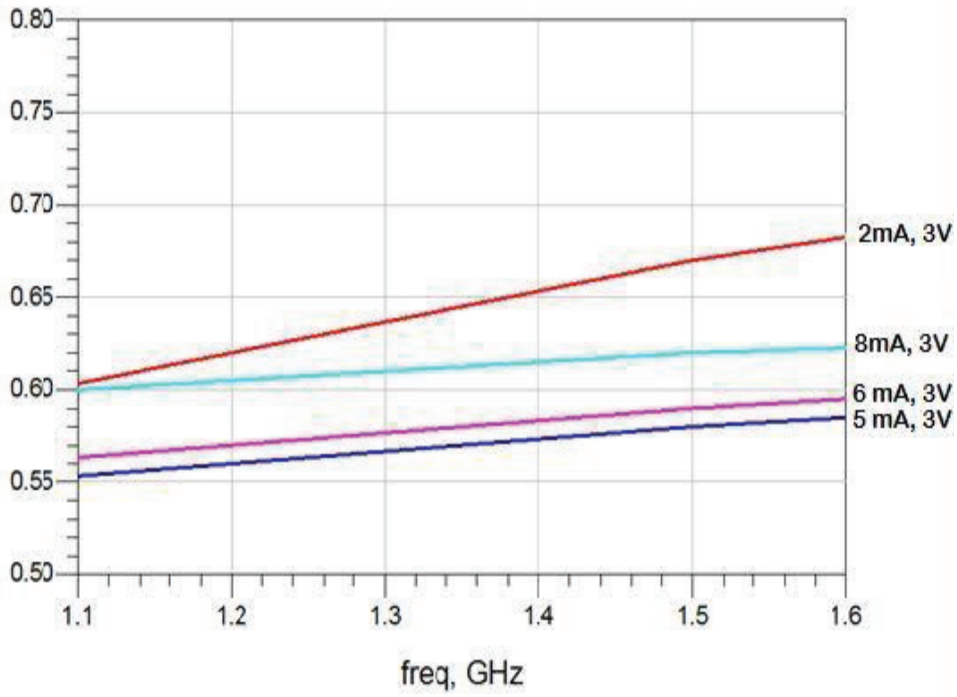


Figure 18 Minimum noise figure at various bias points

7.2 Bias Circuit Design

For the bias circuit, a collector feedback configuration is used as shown in Figure 19. The transistor is always biased in active region regardless of the value of current gain, β. If the collector current increases, collector voltage drops, reducing the base drive and thereby automatically reducing the collector current. It is a simple and low cost biasing scheme for RF and microwave circuits.

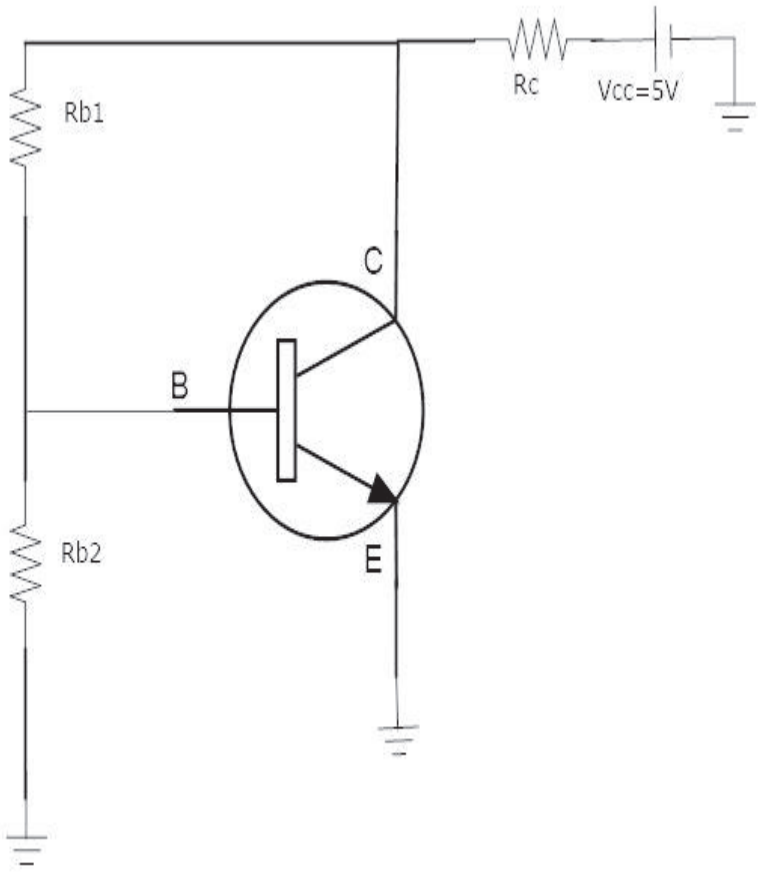


Figure 19 Bias circuit design

7.3 Output network

The complete output network is represented by the block diagram shown in Figure 20. Section 1 is responsible for obtaining unconditional stability in the design while section 2 is responsible for improving output return loss.

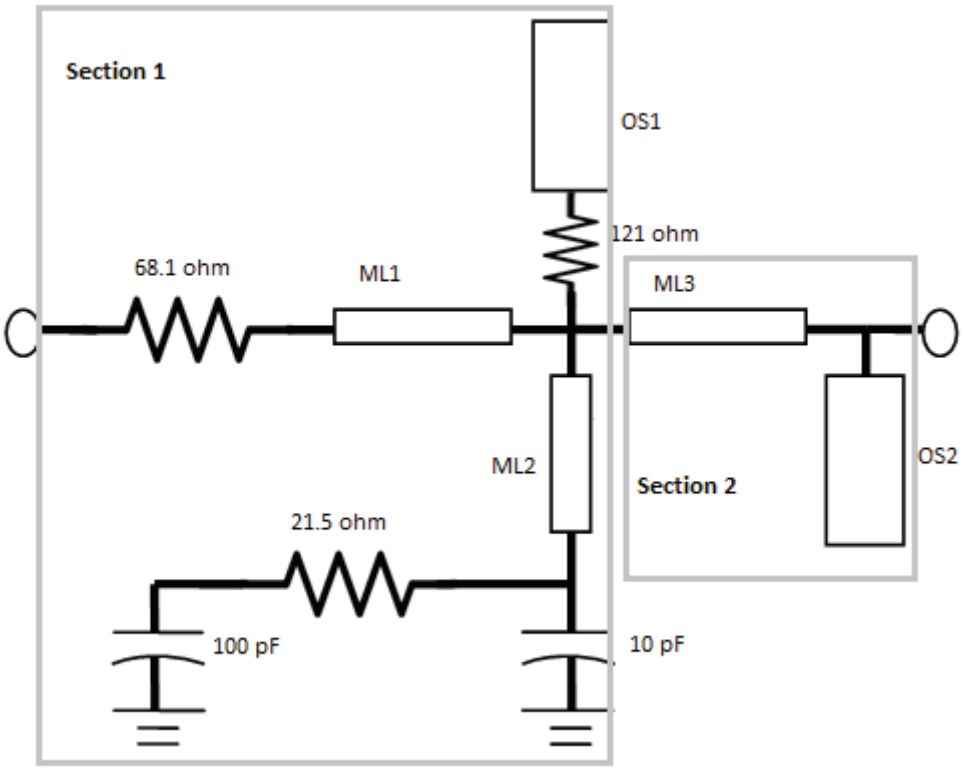


Figure 20 Block diagram of output network

Stability is very important to consider while designing a low noise amplifier. S-parameter data file was available upto 20 GHz for BFY640-04 transistor. Unconditional stability for the circuit was guaranteed by use of a stability network shown in figure 21. For stability, if input is resistively loaded then the noise figure will degrade. Hence, output is selected to be resistively loaded. The stability network consists of a series resistance to improve the stability in the overall simulated frequency band (50 MHz to 25 GHz). This is followed by a microstrip line length of 1.5 mm. The endpoint of this microstrip line, two branches is connected. Both these branches are used to deal with different frequencies. In L-band, the upper branch is almost open circuit. But at 23 GHz, the upper branch will start loading and serves as an absorbing network creating stability. This happens because the open stub presented in the upper branch becomes a quarter wave length at 23 GHz. For L-band frequencies, the stability is assured by having a path for signal to ground (loss) through the lower branch. The curved microstrip line in the lower branch becomes quarter wave at L-band frequencies. Thus, a path for signal to ground is provided by the curved line and

then via capacitor C22=10 pF. It becomes short circuit at L-band frequencies, hence providing loss. While C23 capacitor=100 pF is used as a dc block. P3 is the point of insertion of DC bias to the collector of the transistor. To improve output return loss, a simple matching network consisting of a microstrip line and capacitor connected to ground (replaced by open stub) has been chosen, as shown in Figure 22. All the long microstrip lines are implemented as curved lines to reduce circuit size.

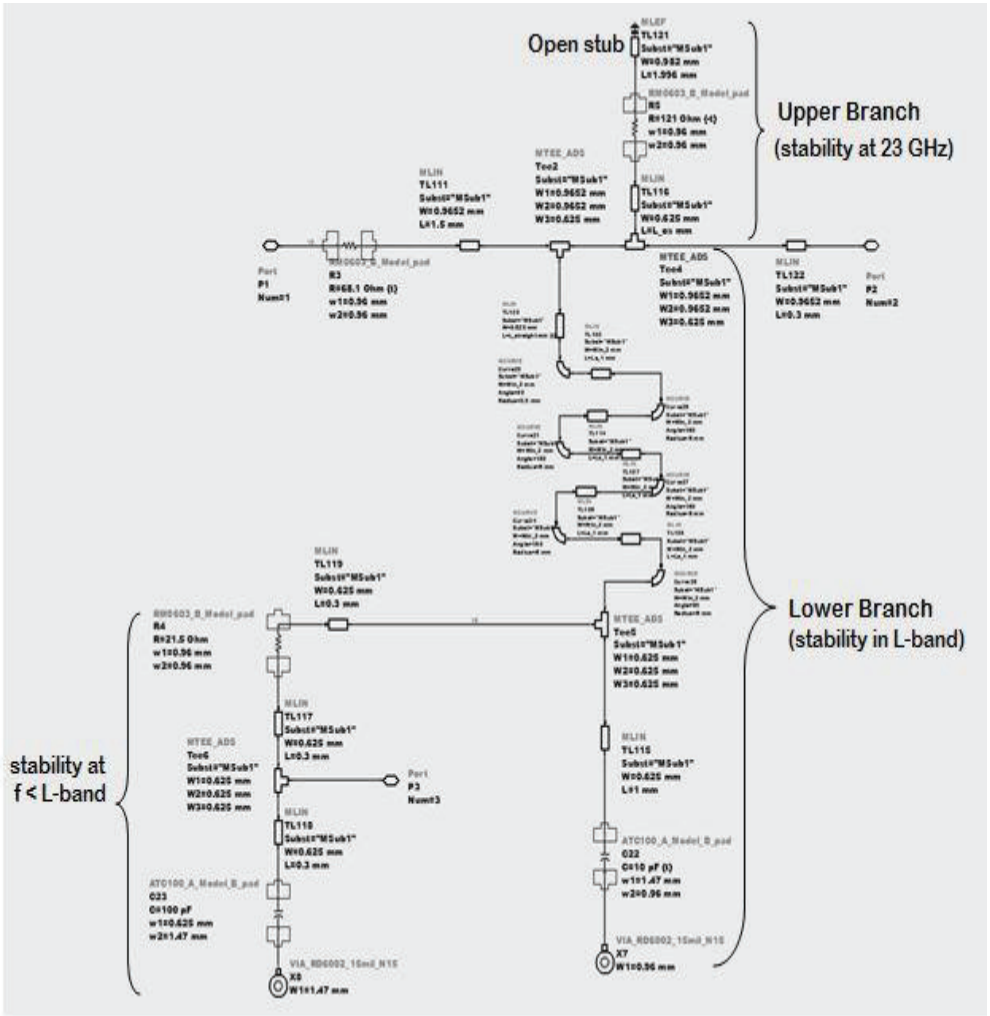


Figure 21 Output network, Section 1

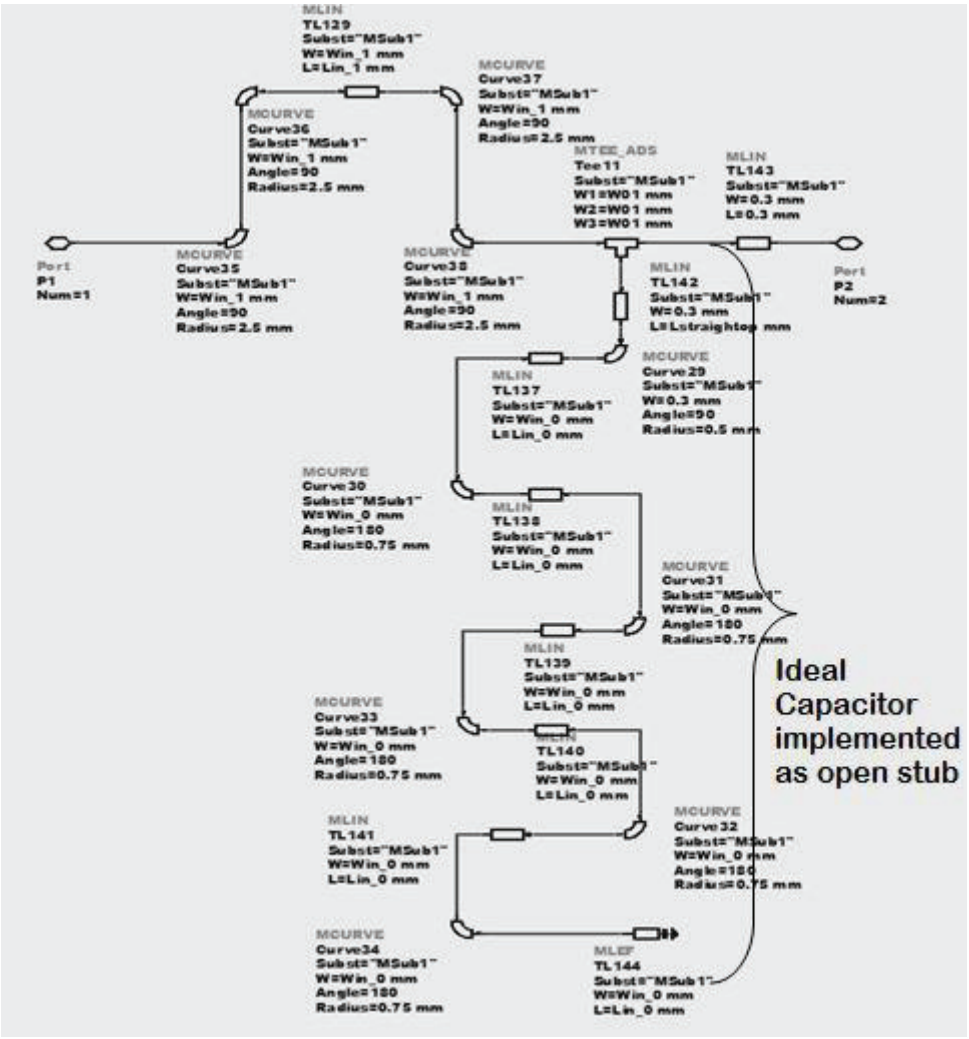


Figure 22 Output network, Section 2

7.4 Input network

A block diagram of the input network is shown in figure 23. The complete network is divided into two sections which are further discussed in detail.

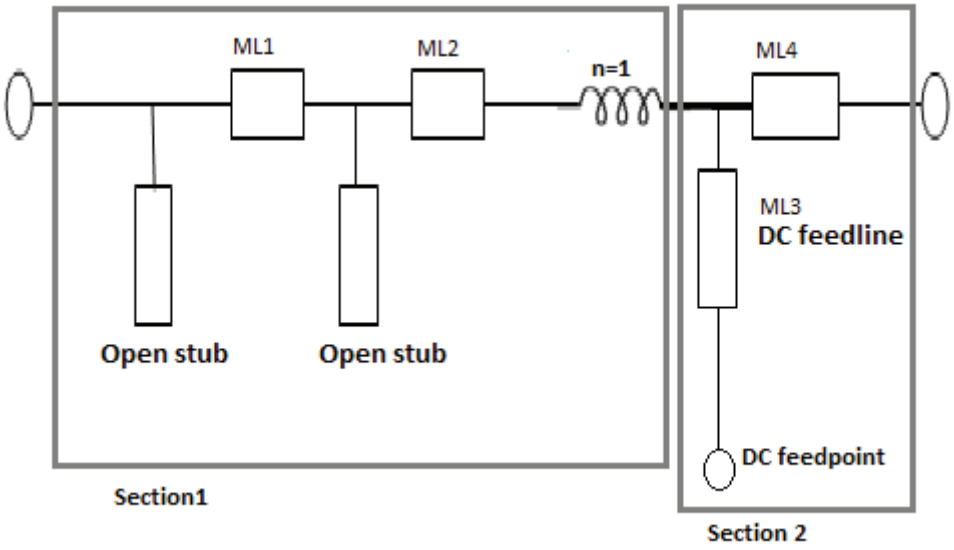


Figure 23 Block diagram of input network

The input matching network is designed in order to obtain minimum noise figure. The implemented input matching network is shown in figures 24 and 25 respectively. Initially, the design was started with ideal components, later the capacitors in both input and output matching network were replaced by open stubs. Optimisation on length and width of each transmission line at the input side is performed to obtain minimum noise figure. The point of inserting the DC bias as shown in figure 25 is carefully selected such that it has high impedance and hence prevents RF to flow through it. This also helps in minimizing the noise figure. The DC feed line helps in obtaining stability at frequencies lower than L-band.

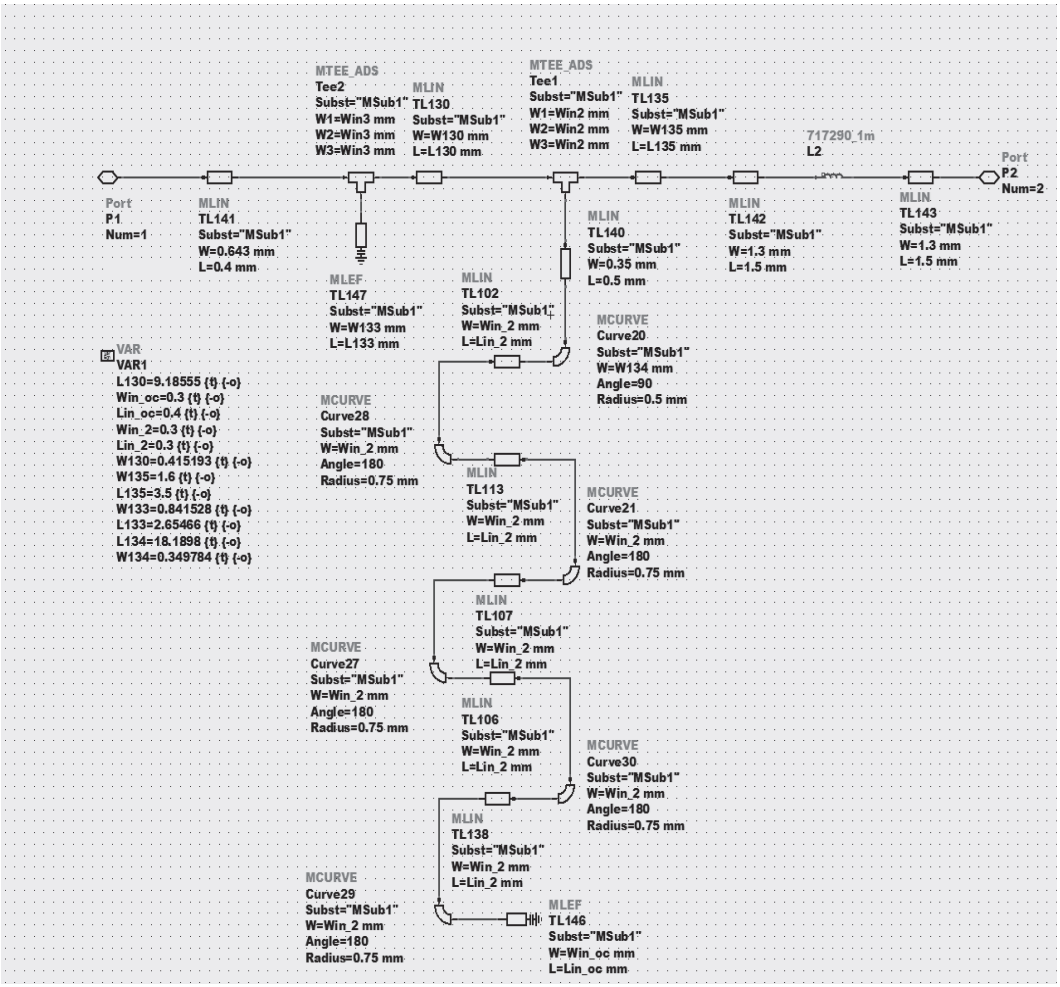


Figure 24 Input network, Section 1

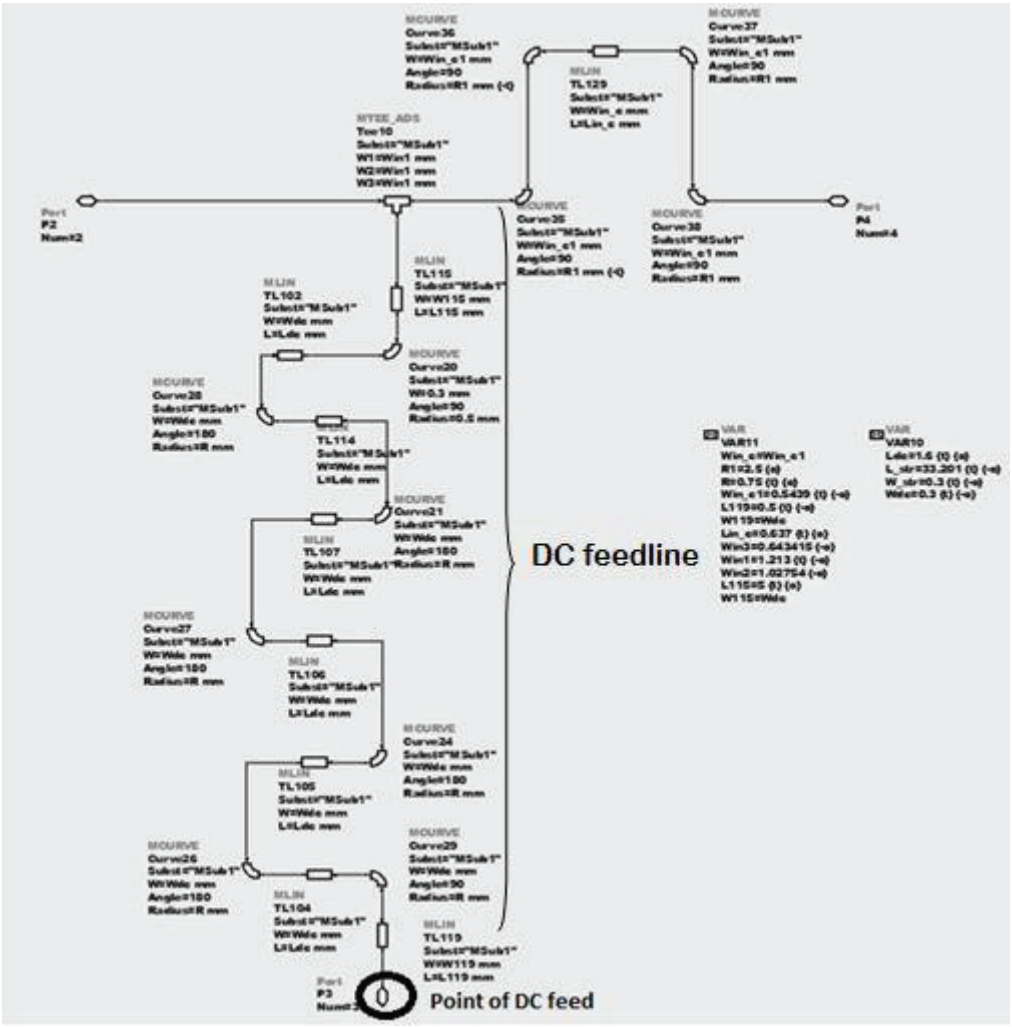


Figure 25 Input network, Section 2

The dc feed network alongwith complete DC bias circuit which is designed in accordance with section 7.2 is shown in figure 26.

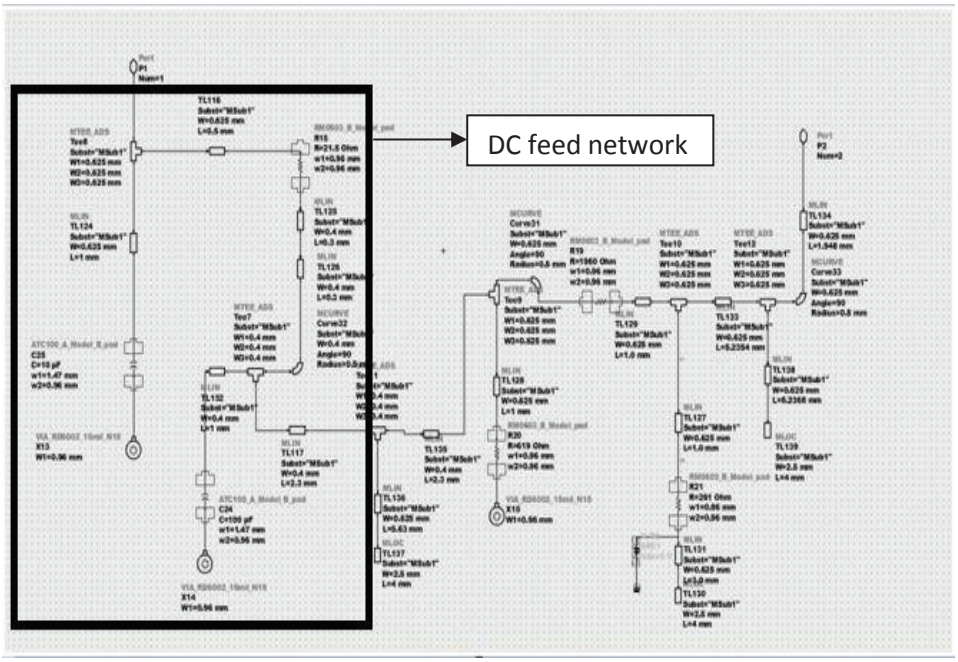


Figure 26 DC bias circuit

The complete LNA structure used for simulation is shown in Figure 27.As we can see, both the input and output sides contain dc blocking capacitors. Their values are chosen to have optimum results with respect to noise figure, gain and matching.

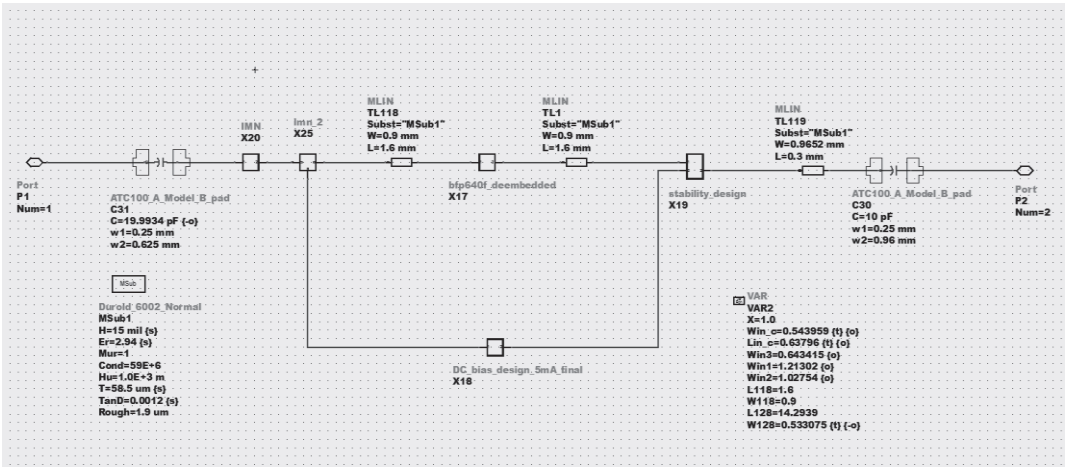


Figure 27 Complete LNA structure

The simulated performance of the designed LNA is discussed in upcoming figures. In figure 28, NFmin indicates minimum noise figure achievable from the designed LNA and nf(2) indicates noise figure obtained at port 2 (output) of LNA. It is good to have low NFmin. In case of an optimum design, a close match exists between NFmin and nf(2).We see that nf(2) varies between 0.70 dB and 0.75 dB in the entire GNSS band.

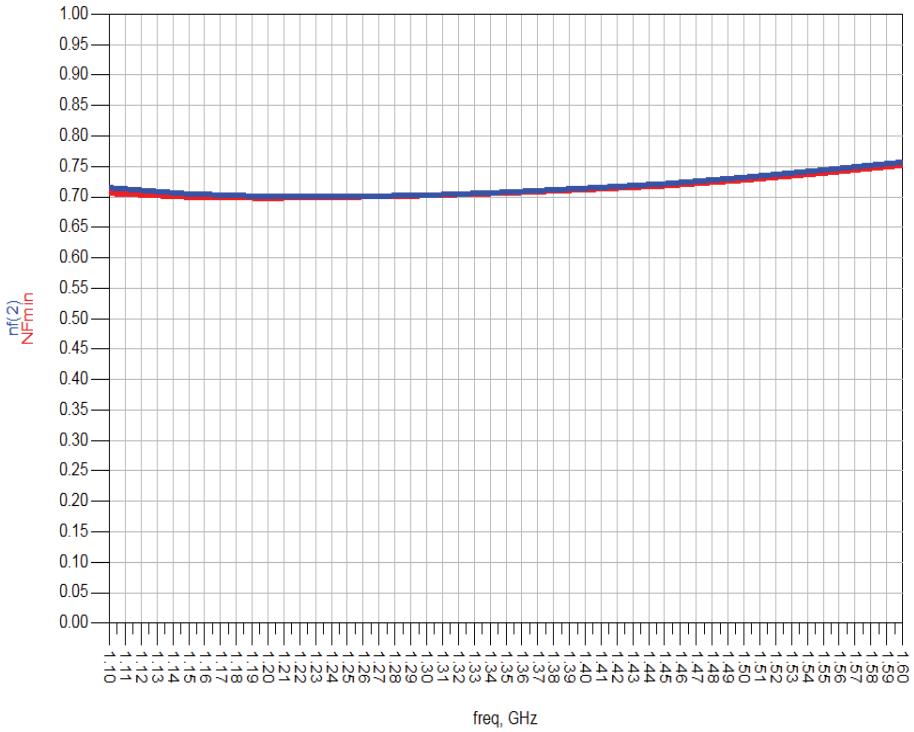


Figure 28 Noise figure

Figure 29 shows that the conjugate of Sopt (source reflection for optimum noise figure) lies very close to 50 ohm as indicated in the Smith Chart. Also, the magnitude of Sopt is well below -20 dB in the complete GNSS band .These two measures are good indications of a very low noise figure.

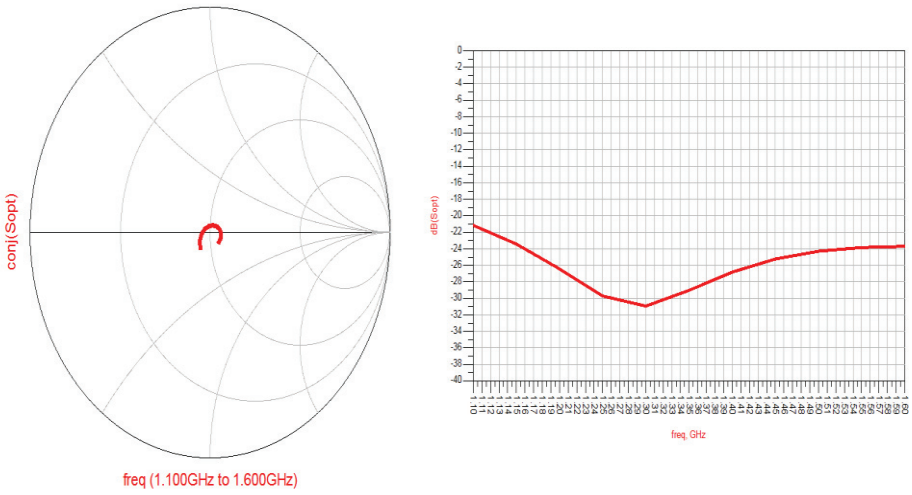


Figure 29 Sopt

In figure 30, we see that the LNA has a simulated gain of nearly 16 dB, input return loss of -5 to -7 dB and output return loss of -3 to -11 dB.

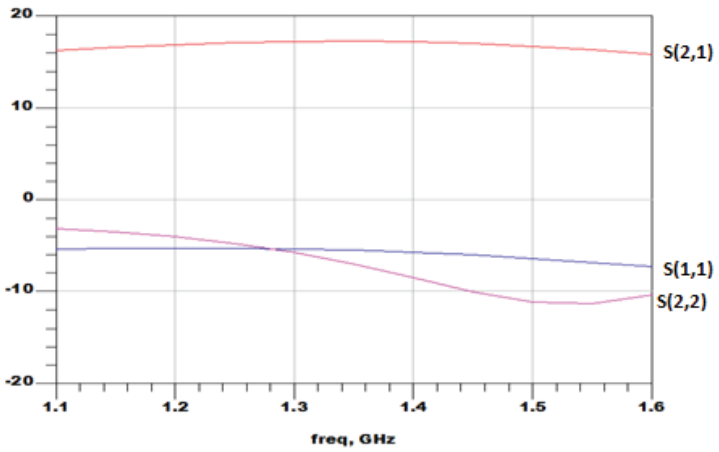


Figure 30 Gain (S21), input return loss (S11), output return loss (S22)

In order to determine if the designed LNA is stable, various simulations were performed in ADS. Firstly, stability factor K was simulated .This is shown in figure

31.We can see that K>1 in the entire simulated frequency range.

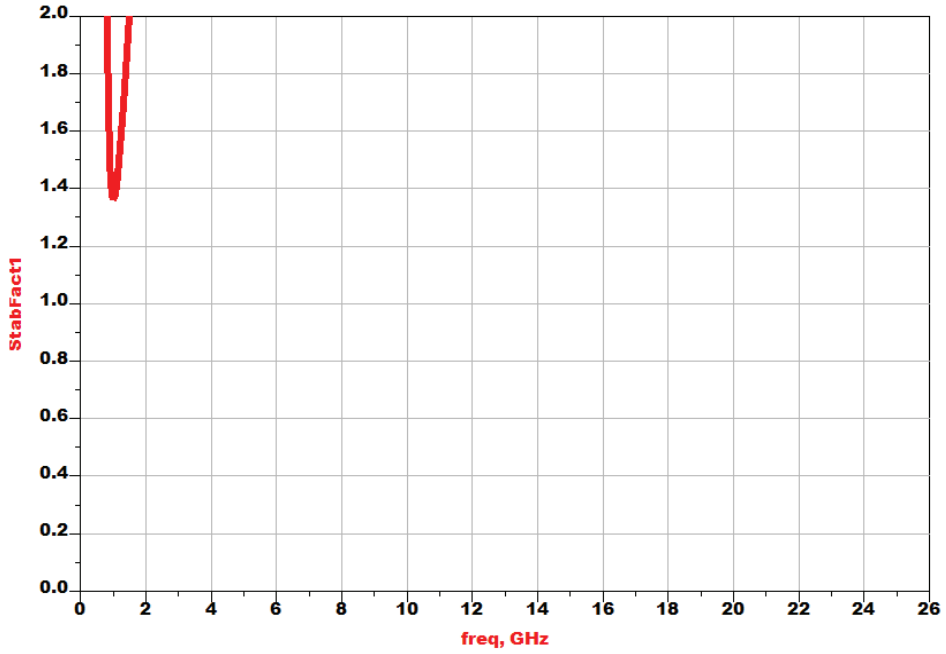


Figure 31 Stability factor, K

Figure 32 shows the results from simulation of $|\Delta|$. We can see that it is less than 1 in the entire simulated frequency range. Hence, both the conditions for unconditional stability (K and $|\Delta|$) are satisfied.

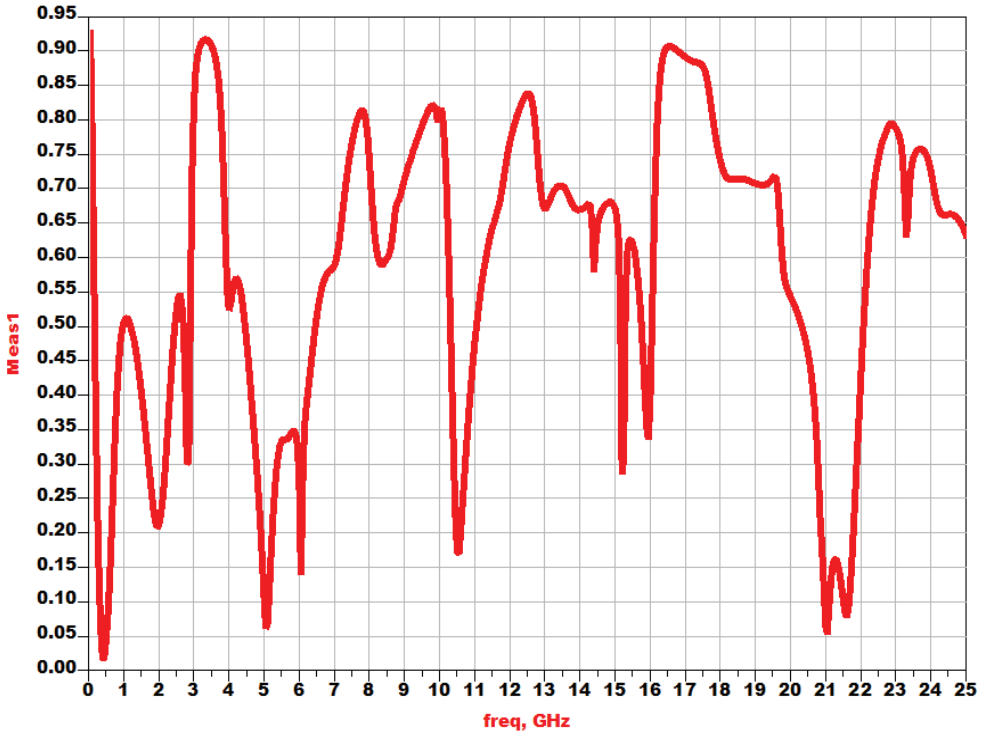


Figure 32 $|\Delta|$

In order to confirm that no loop oscillations exist within the design, S-probe method for stability is used. In this method, s-probes (available in ADS) are connected on the input and output ends of the transistor as it is the only active component in the design. The s-probe simulation calculates the stability index at the input and output of the transistor. It also calculates reflection coefficients Γ_S, Γ_{IN}, Γ_L and Γ_{OUT} corresponding to impedances Z_s, Z_{IN}, Z_L and Z_{OUT}. Here, Z_S is impedance seen outward from the transistor towards the source, Z_{IN} is impedance seen looking into the transistor on the input side, Z_L is impedance towards the load and Z_{OUT} is impedance seen looking into the transistor on output side.

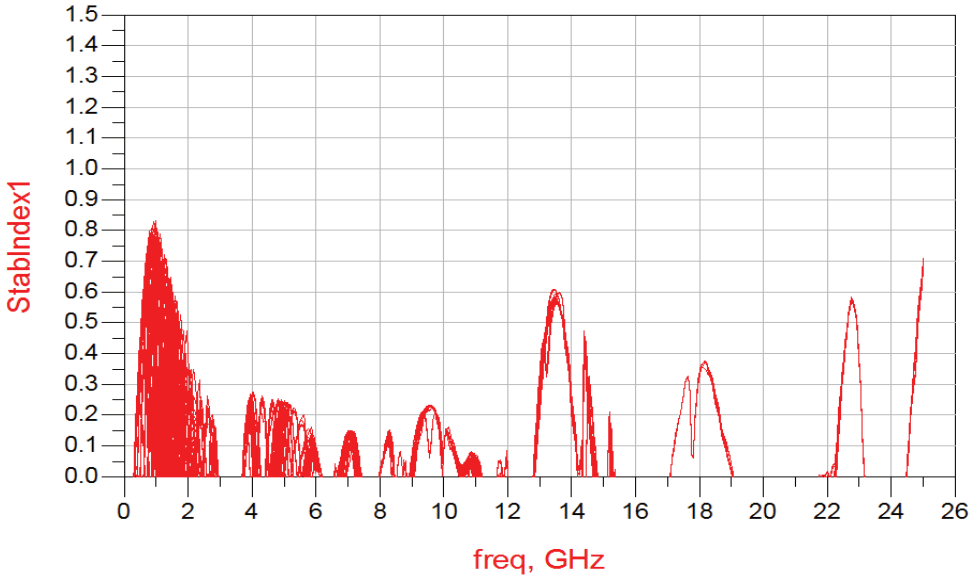


Figure 33 Stability Index (input)

Figure 33 shows the simulation result from S-probe method for the input side of the transistor. The stability index is less than 1 in the entire frequency range which indicates stability of the design.

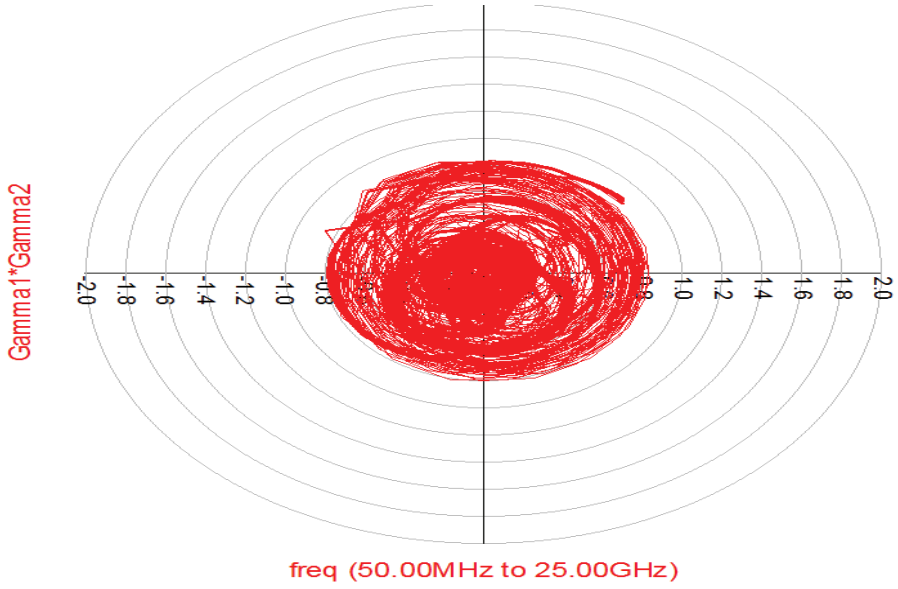


Figure 34 Product of reflection coefficients (input)

Figure 34 shows the polar plot of the product of the reflection coefficients Γ_S(Gamma1) and Γ_{IN}(Gamma2). We notice that the trajectory of |Gamma 1. Gamma 2| does not encircle the point (1, 0) when moving in a clockwise direction versus frequency. This ascertains that no loop oscillations exist on the input side of the transistor.

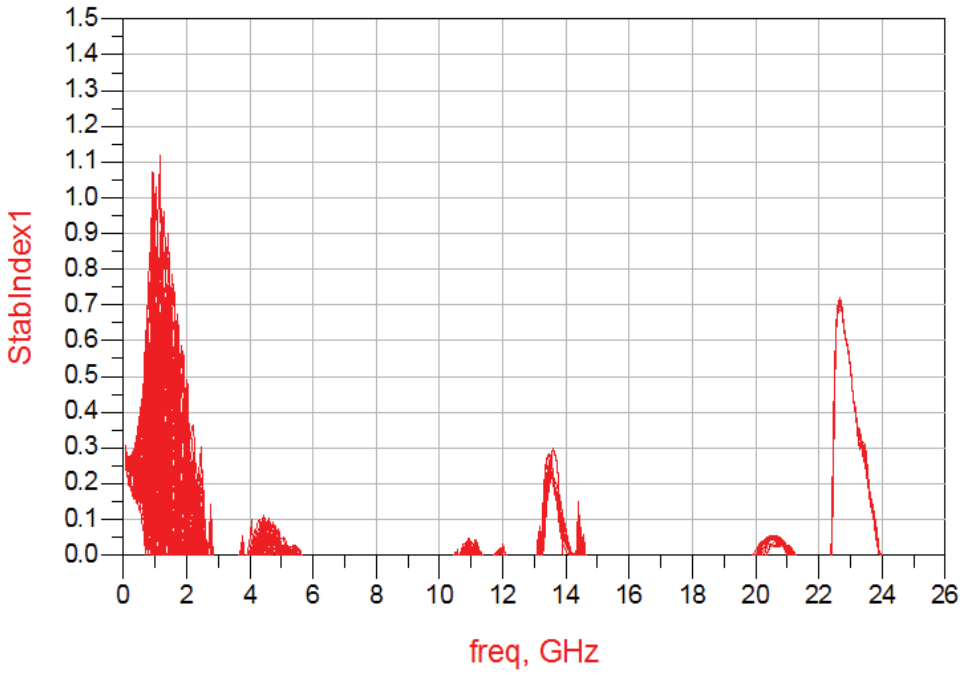


Figure 35 Stability index (output)

In order to check for oscillations on the output side, stability index for the output was checked. As seen in figure 35, stability index becomes >1 at approximately 1.5 GHz. This indicates there could be oscillations in the design. In order to confirm that, polar plot of product of Γ_{OUT} and Γ_L versus frequency was drawn. As seen in figure 36, the polar plot does not encircle (1,0). Hence, as both conditions are not satisfied simultaneously, it is clear that no oscillations exist in the designed LNA.

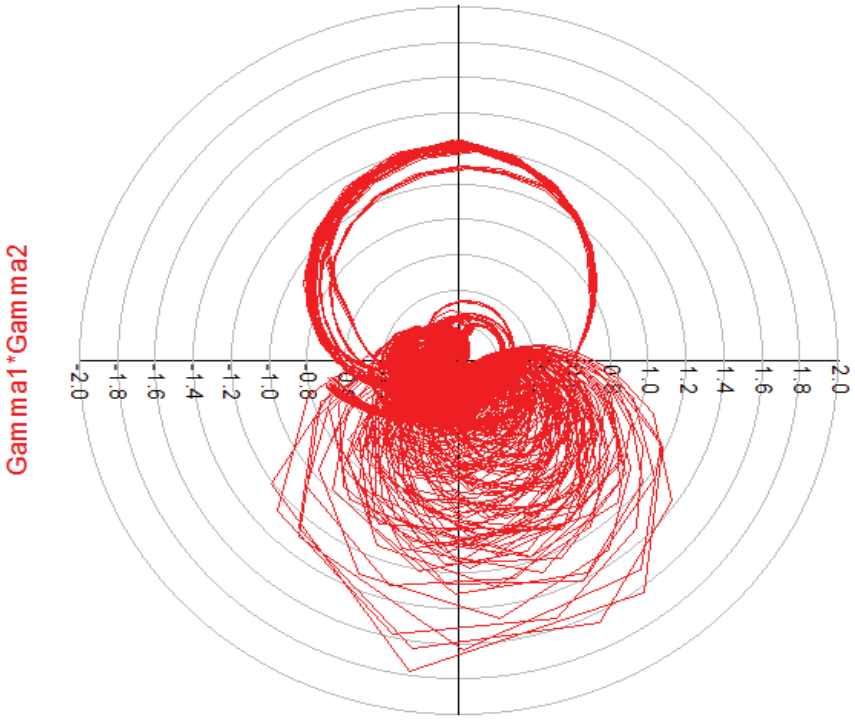


Figure 36 Product of reflection coefficients (output)

7.5 Momentum EM simulation

Electromagnetic coupling is not taken into account in schematic simulation but it happens in reality between adjacent circuits on the PCB. Hence, in order to determine the impact of coupling a 2.5 D planar electromagnetic simulator called Momentum is used. It uses frequency-domain Method of Moments (MoM) technology to accurately simulate complex EM effects including coupling and parasitics. As this design includes both lumped components and distributed lines, it is wise to verify the functionality of the circuit before fabrication. It will prevent us from tuning and optimizing the circuit after fabrication which takes a lot of time. Also, it prevents from going into the whole fabrication loop once again which is costly.

The complete circuit layout is broken into four parts namely input match network, output match network, stability network and DC bias network. Each part is simulated individually in EM environment with the right substrate definition. The S-parameters from these simulations are passed to an intermediate file (test station) where the S-parameters are compared with the

schematic simulation of that part. If differences are found, then the layout is adjusted and the momentum simulation is re-run. The S-parameters obtained from this simulation are compared again with the schematic S-parameters. This procedure is carried out until momentum simulation for each part matches with their schematic simulation. It is to be noted that the schematic fulfills the optimized goals, so any changes needed after comparison is carried out only in layout used for momentum simulation. EM simulation is especially important for the curved lines present in the design which aren't well simulated in simple ADS schematic simulation. The length of the curved lines in the input match network and stability network needed to be tuned to have the performance matched with the schematic performance. Capacitor C22 in figure 21 was changed to 5.6 pF from 10 pF as it was seen to affect the stability of the design.

The performance of the complete LNA after momentum simulation and optimization is shown below:

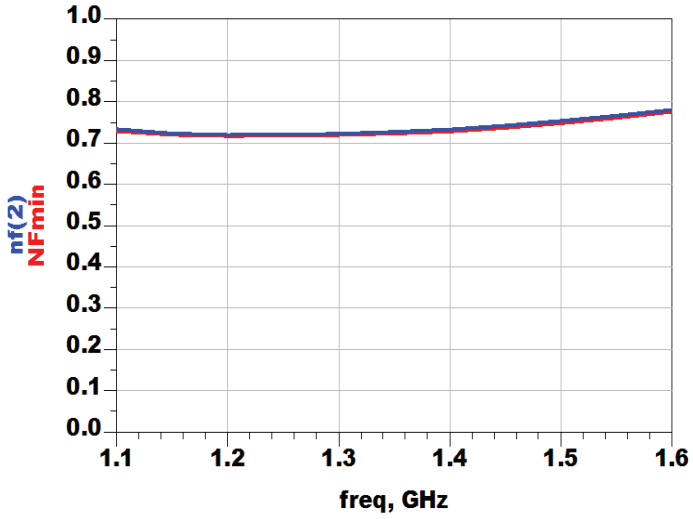


Figure 37 Post-momentum Noise figure

In figure 37 is seen that noise figure, nf(2) varies between 0.74 and 0.78 dB which is slightly increased from the schematic simulations. Still it is closely matched with NFmin indicating it is the lowest possible noise figure obtainable from the design. Also, figure 38 shows that Sopt is less than -20 dB. This further assures that the design has a very low noise figure.

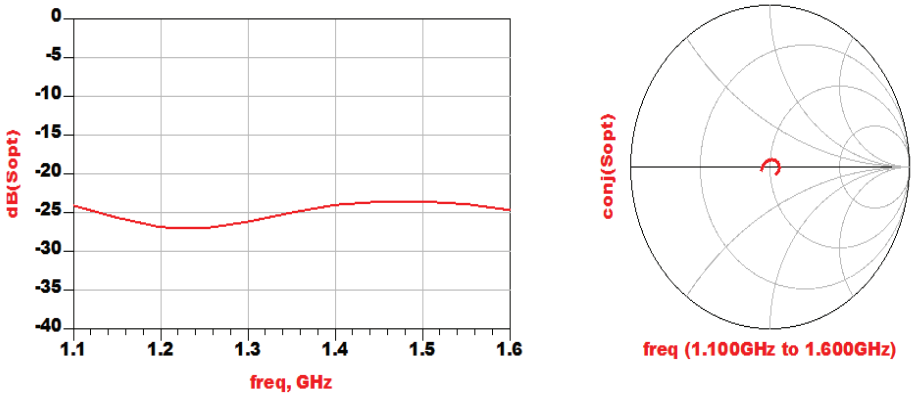


Figure 38 Post-momentum Sopt

Figure 39 indicates that the gain varies between 17.5 dB and 14.5 dB. Unlike schematic simulation, the gain now has a slope. This result is more close to what we would expect in real measurements of the LNA. The output return loss is nearly -9 dB in the entire simulated frequency range while the input return loss varies between -11 and -8 dB. This indicates that in real measurements both input and output return loss will be better than seen in schematic simulation.

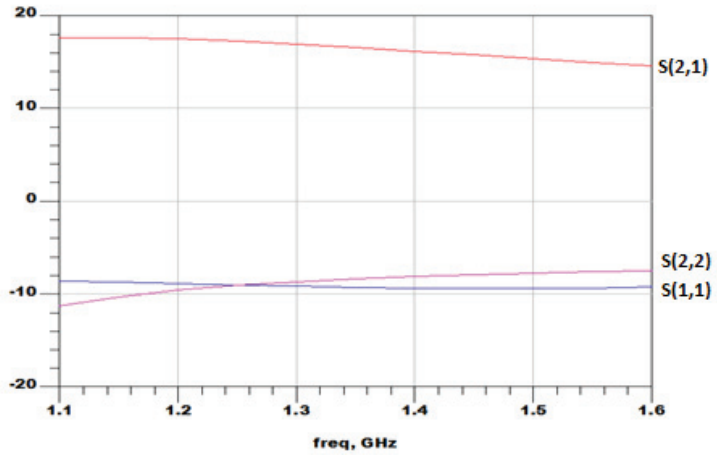


Figure 39 Post-momentum gain (S(2,1)), input return loss(S(1,1)), output return loss(S(2,2))

7.6 Layout:

A layout was generated for the complete LNA schematic as shown in figure 40. 50Ω lines were added at input and output for RF connection to prevent reflection of any RF signal and hence prevent losses. In figure 41, limiter component GG-

77015-01 is also connected in front of the dc blocking capacitor on the input side. Its functionality is verified later in the measurements section.

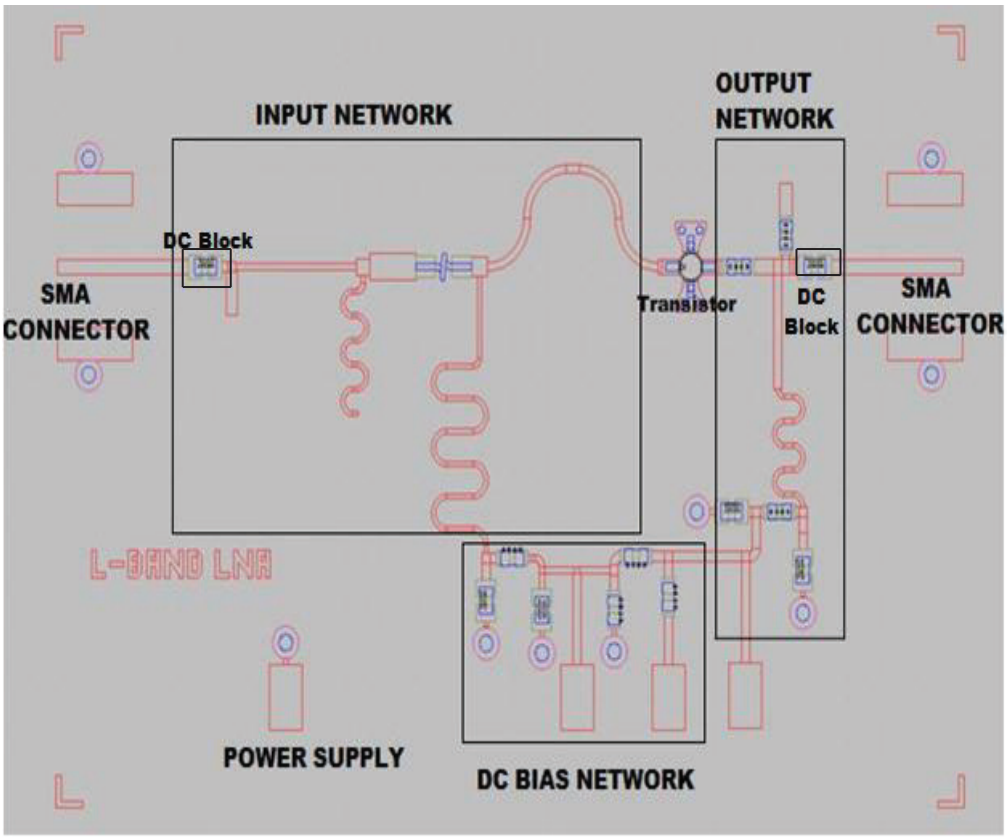


Figure 40 Layout of designed LNA

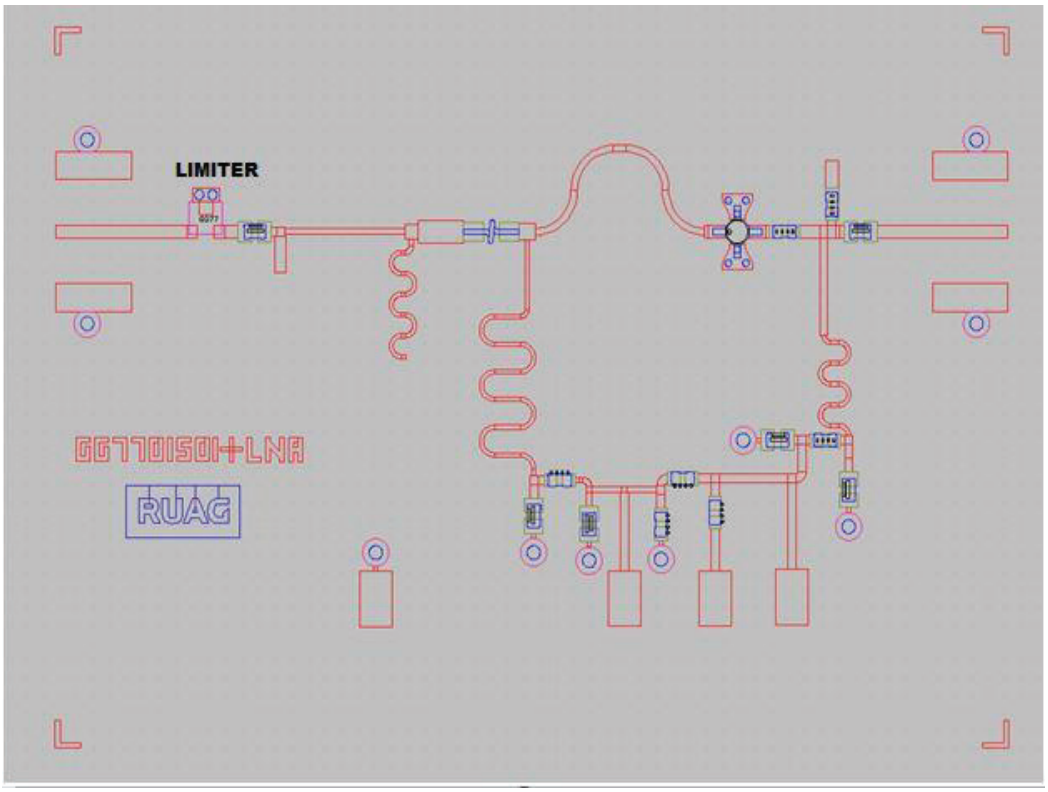


Figure 41 Layout of designed LNA including limiter

The complete circuit was fabricated on Duroid 6002 panel. Layout files were converted to Gerber files and sent along with the panel for etching at Cogra Pro AB.

Once the board was back from fabrication all the lumped components, SMA connectors were soldered and proper DC biasing was obtained. A magnified photograph of the circuit board is shown in figure 42. The physical size of the board is 6.9 x 4.9 cm^2, excluding limiter component.

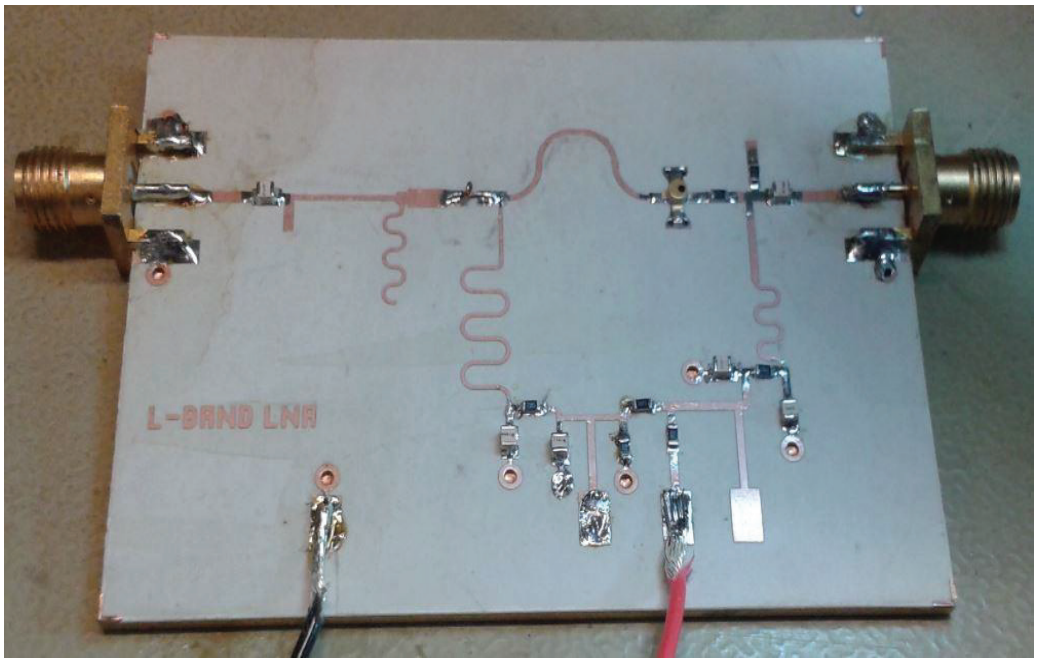


Figure 42 Photograph of fabricated PCB

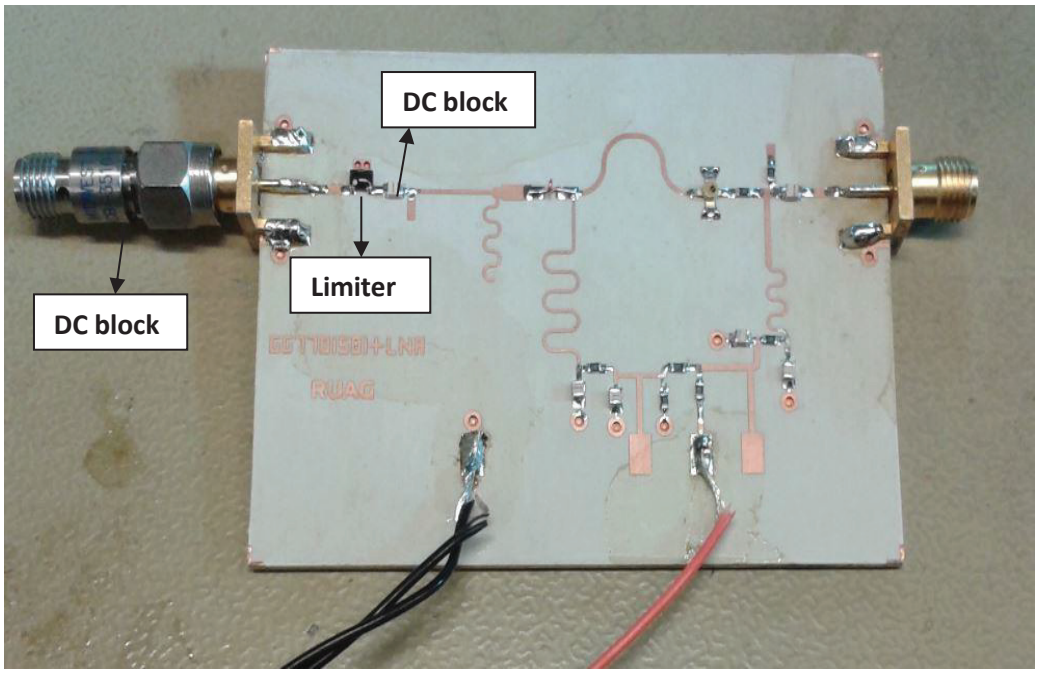


Figure 43 Photograph of fabricated PCB (including limiter)

In figure 43, we see that an external DC block is connected to the design. This is needed as per section 4.4.

8. MEASUREMENT AND RESULTS

8.1 Bias tuning

In order to obtain Ic=5 mA and Vce=3V, right value of resistors R1, R2 and R3 needs to be chosen in the dc bias circuit. Initially, the base and collector side are kept separate by not connecting anything in place of R2. A 5V supply is connected to R1 and value of R1 is chosen so that Vce=3V is obtained. A potentiometer is connected at R2 and it is tuned until 5 mA is obtained at the collector end. Bipolar devices are current driven, so the base current sets the collector current. Once 5 mA is obtained at collector side, values of R2 and R3 are decided by voltage division rule. Obtained values for R1, R2, and R3 are 301 Ω, 28.7 kΩ and 13 kΩ respectively.

8.2 Noise figure measurement

The noise figure of the designed low noise amplifier is calculated by Y-factor method [16]. It is the ratio of two noise power levels, one measured with noise source ON and the other with source OFF.

$Y= N^{ON}/N^{OFF}$

In the first step, calibration of noise figure analyzer N8973A from Agilent was done. The noise source 346A from Hewlett Packard was connected directly to input of the instrument. Next, the DUT is inserted as shown in figure 44 and noise figure was measured.

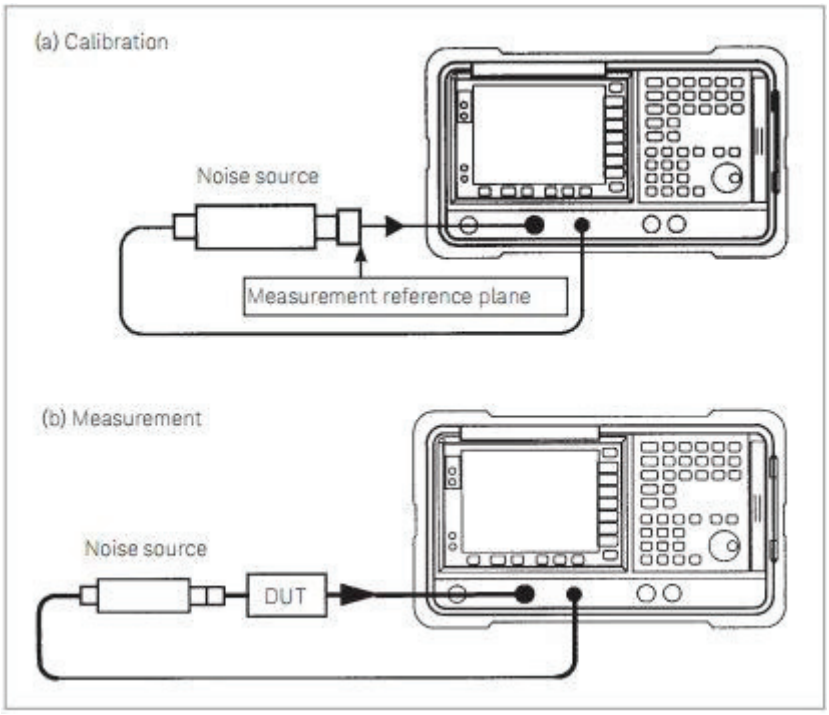


Figure 44 Noise Figure Measurement method

As the device doesn't have a very good input return loss, an isolator was placed in front of the LNA and measurements were done. The loss of the isolator was subtracted by inserting its loss value in the noise figure meter. The measured noise figure for both designs was measured in the frequency range of 1.1 to 1.6 GHz are shown in figures 45 and 46 respectively.

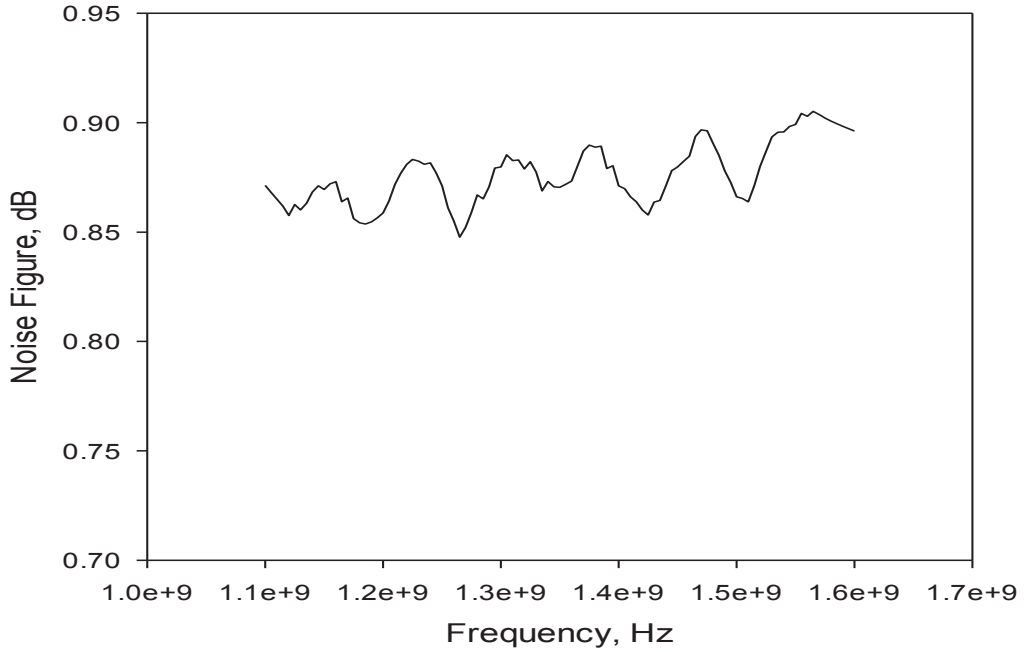


Figure 45 Noise Figure of LNA

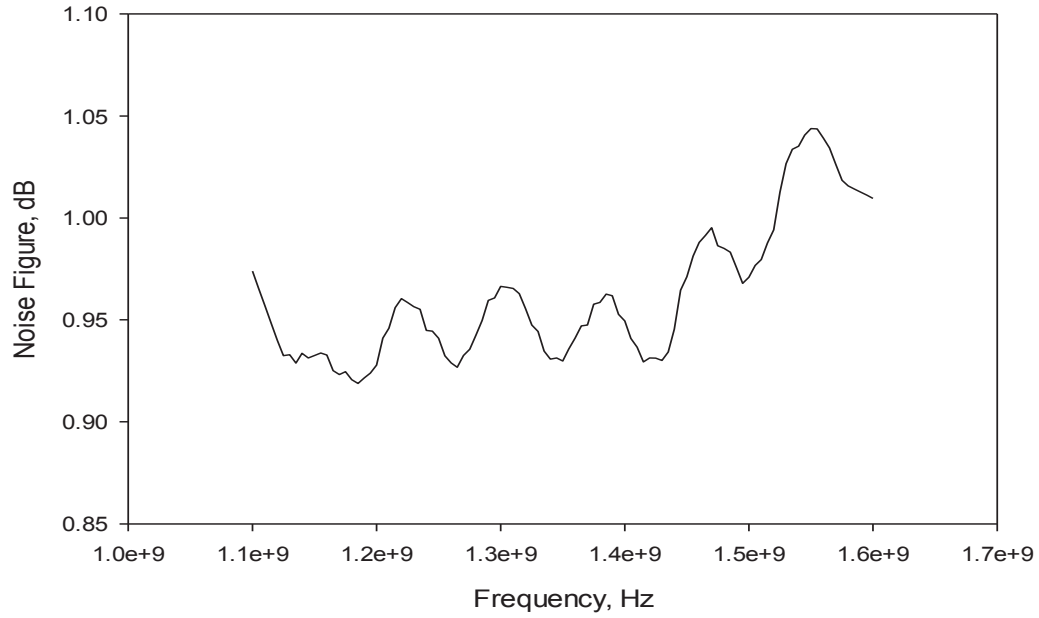


Figure 46 Noise Figure of LNA including limiter

From figure 45, we see that the noise figure for the LNA is 0.84-0.91 dB. And, from figure 46, noise figure for the design including limiter is 0.92-1.05 dB which includes noise from the limiter component (0.1-0.3 dB higher noise figure).We see that the noise figure is more than simulated in ADS. There is clear contribution of 0.05 dB noise due to SMA connectors [17]. Moreover, as the measured devices are not enclosed in a shielded container, there could be interference from stray signals present in the environment which undermine the accuracy of measurement.

8.3 Measurement of s-parameters and stability check

Using Wiltron 37369A (40 MHz- 40 GHz) vector network analyzer, s-parameters were measured for the designed LNA. The s-parameters dataset was then simulated in ADS environment.

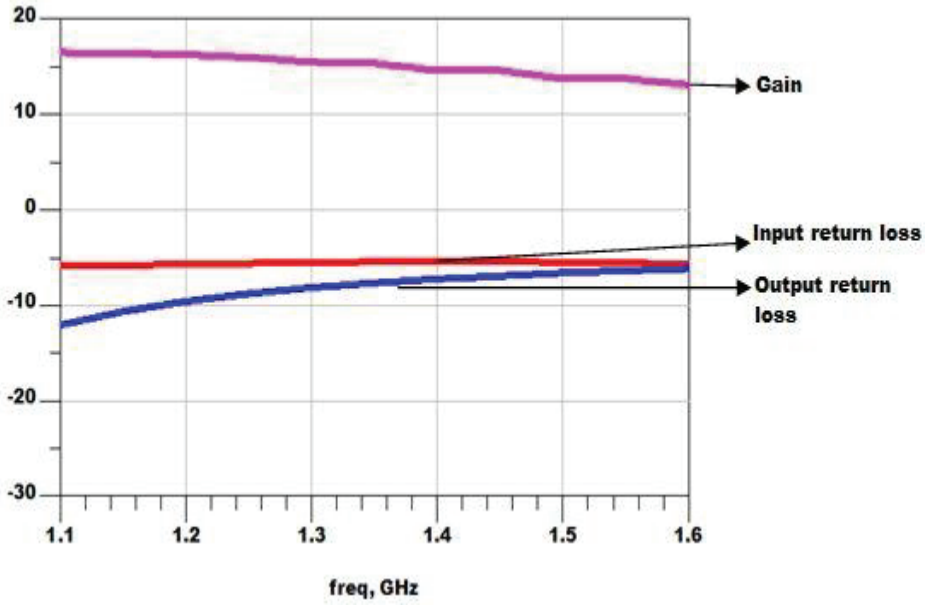


Figure 47 Measured Gain, input return loss and output return loss

In figure 47, we see that the input return loss is nearly -6 dB and output return loss varies between -12 and -7 dB. As was seen in momentum EM simulation, the gain has a slope. This slope can be taken care of in following amplification stages with the help of inter stage matching which is not included in this work.

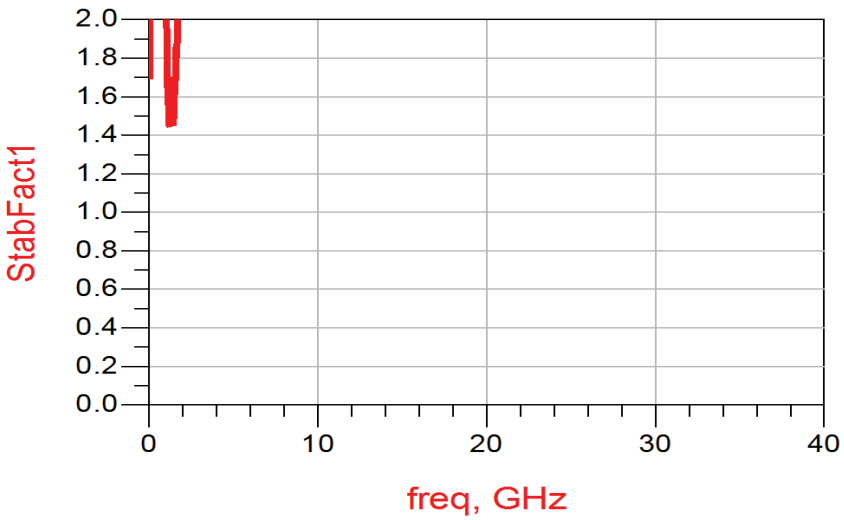


Figure 48 Stability factor, K

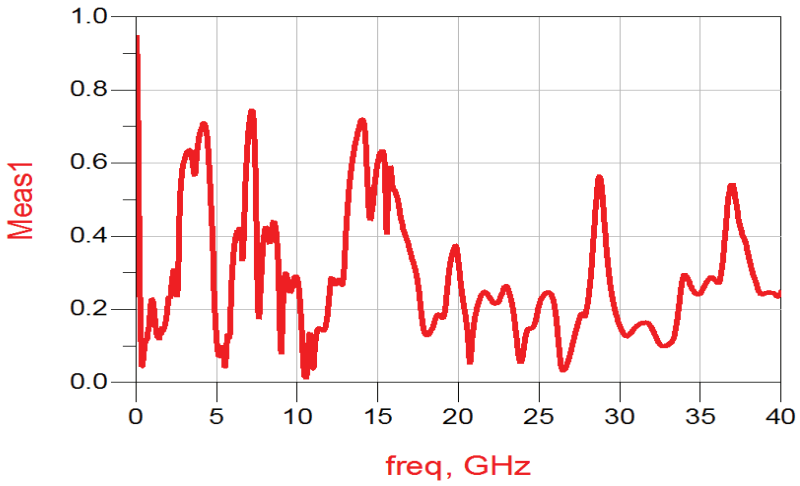


Figure 49 |Δ|

The stability of the fabricated design(excluding limiter) has also been verified. In figures 48 and 49, we see that K >1 and |Δ|<1 in the entire simulated frequency range which indicates that the design is completely stable.

8.4 Overdrive test

The purpose of this test is to check the amplifier's ability to withstand high power. Before subjecting the fabricated devices to high power, the functionality

of the limiter component was tested individually at 1.575 GHz. The result is shown in figure 50.

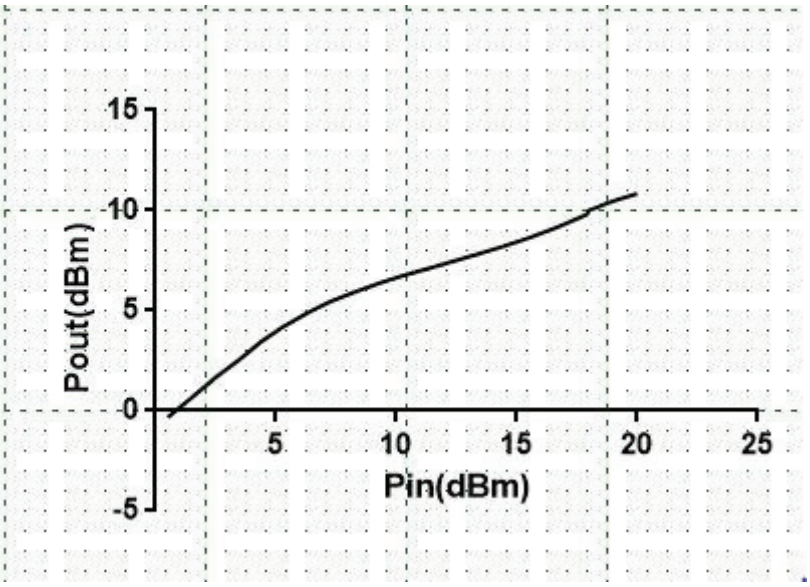


Figure 50 Variation of output power with input power for limiter GG-7015-01

Both LNA and LNA including limiter in front are subjected to high power test. The test setup is shown in figure 51. In order to generate high input power levels (≥ 20 dBm), a pre-amplifier is used along with signal generator. DUT 1 corresponds to LNA and DUT 2 corresponds to LNA including limiter. The voltage level at the directional coupler served as reference. Detectors were connected to monitor the voltage level at the reference and at the output of each DUT. Any major fluctuation in the output power is an indication that the device could not handle a particular input power level.

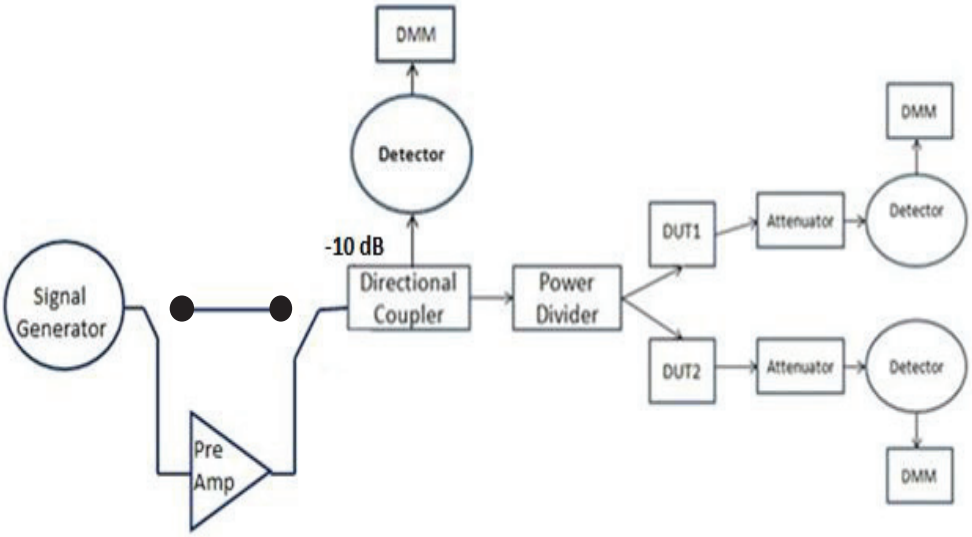


Figure 51 Overdrive test setup

Each device was kept on a particular power level for 24 hours. In order to obtain comparative results, the power level was increased in steps of 2 dB. After subjecting the DUTs to a certain power level for 24 hours or until the point when output power level got declined largely, they were detached from the setup. Then the noise figure and gain was measured using noise figure meter.

Table 3 Overdrive test results

Pin DUT	Time per level	Total time	DUT 1	DUT 2
10 dBm	24 h	24 h	Ok	Ok
12 dBm	24 h	48 h	Ok	Ok
14 dBm	24 h	72 h	Ok	Ok
16 dBm	24 h	96 h	Not ok	Ok
18 dBm	24 h	120 h		Ok
20 dBm	24 h	144 h		Not ok

Table 2 shows that DUT 1 could sustain power levels only upto 16 dB while DUT 2 could sustain power levels upto 18 dB. The variation of output power with input power for DUT 1 is shown in figure 52.

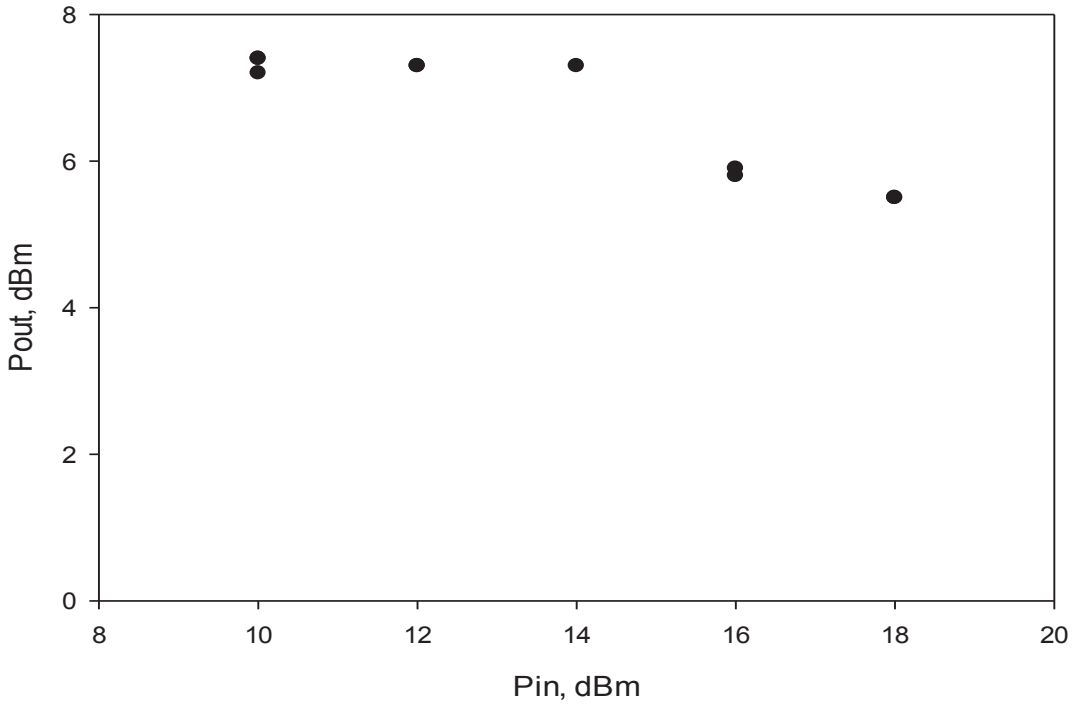


Figure 52 Variation of output power with input power for DUT 1

It can be seen from this graph that the LNA (DUT 1) is already in compression at 10 dBm input power level (starting point). At 16 dBm input power, the output power drops drastically indicating a decline in the performance of the LNA. This was further verified by measuring the noise figure and gain using noise figure meter.

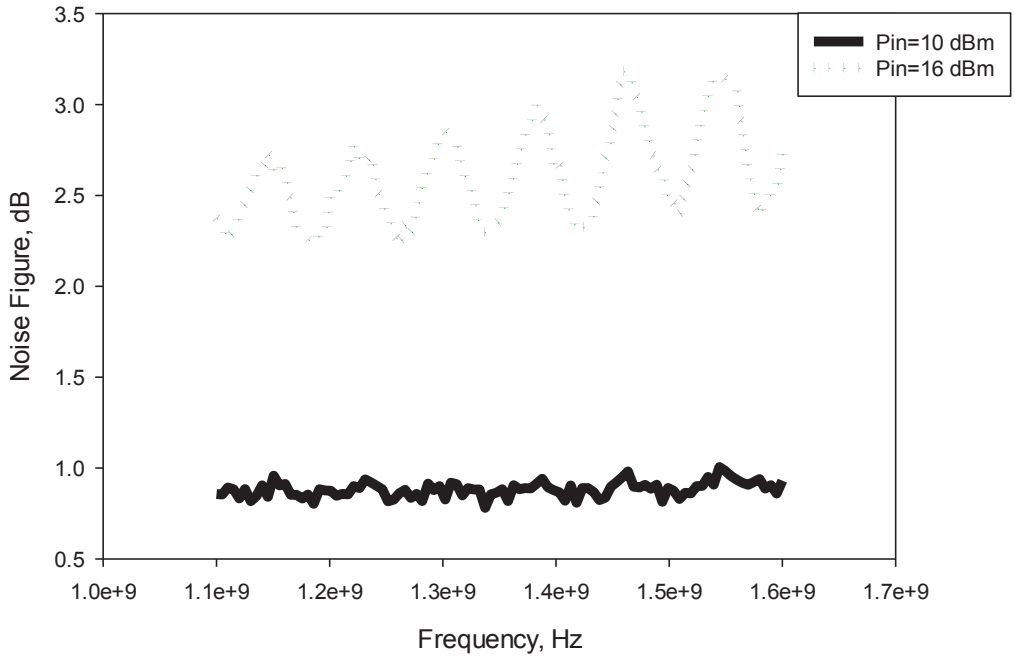


Figure 53 Variation of noise figure with frequency after being subjected to various power levels (DUT 1)

It can be seen that noise figure got deteriorated up to 3 dB at 16 dBm input power. At the same time, gain of the LNA was decreased gradually. The variation of gain is shown in figure 54.

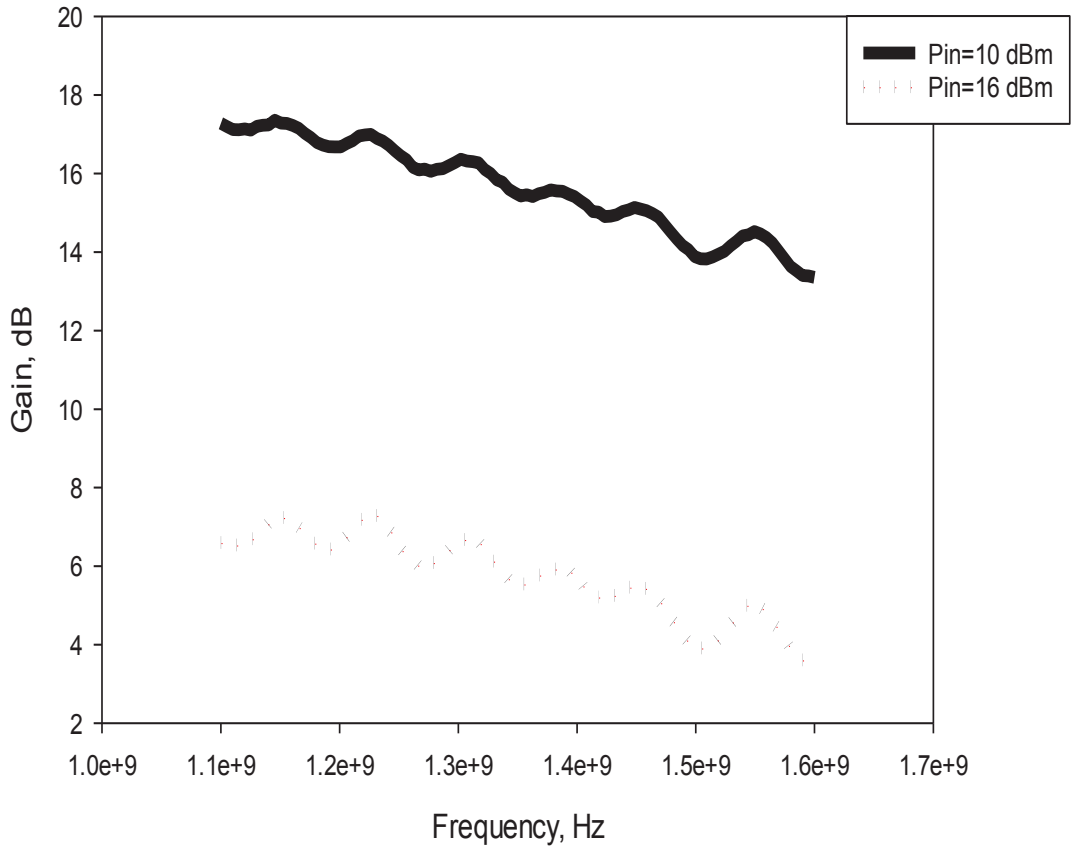


Figure 54 Variation of gain with frequency gain with frequency after being subjected to various power levels (DUT 1)

For the LNA including limiter (DUT 2), variation of noise figure with frequency is shown in figure 55. We see that noise figure gets deteriorated after being subjected to 20 dBm input power. However, this noise levels is still better compared to DUT 1.

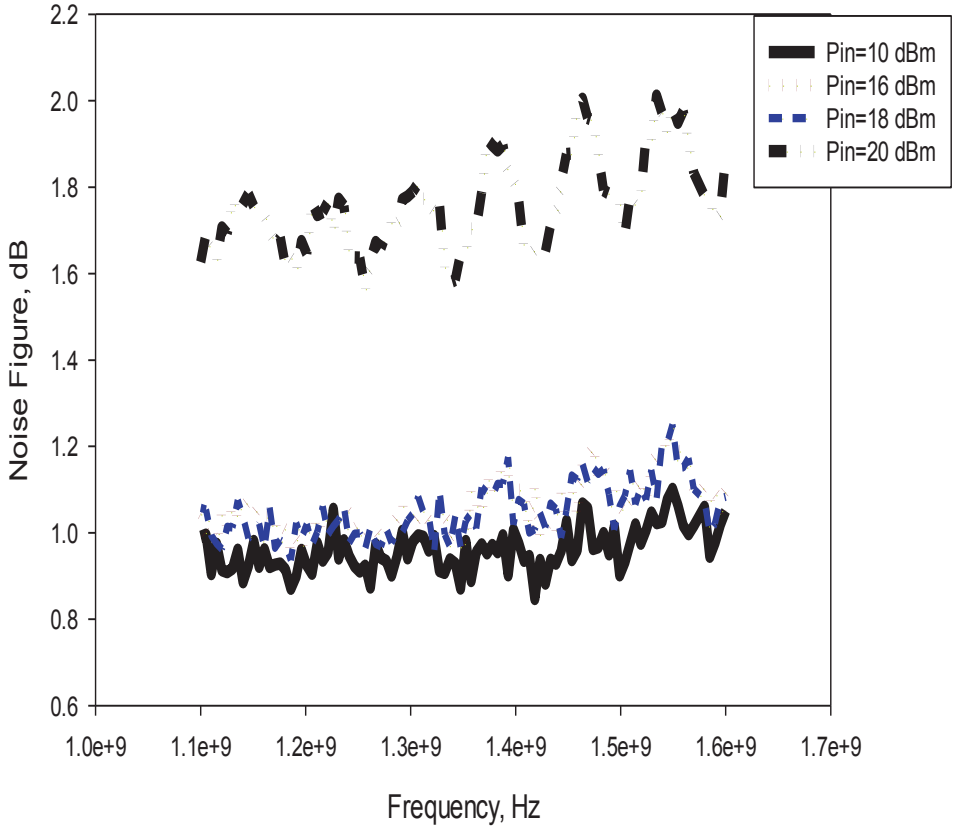


Figure 55 Variation of noise figure with frequency after being subjected to various power levels DUT 2)

The variation of gain with frequency is shown in figure 56. The gain gradually decreases and varies between 13 and 9 dB after 20 dBm input power level.

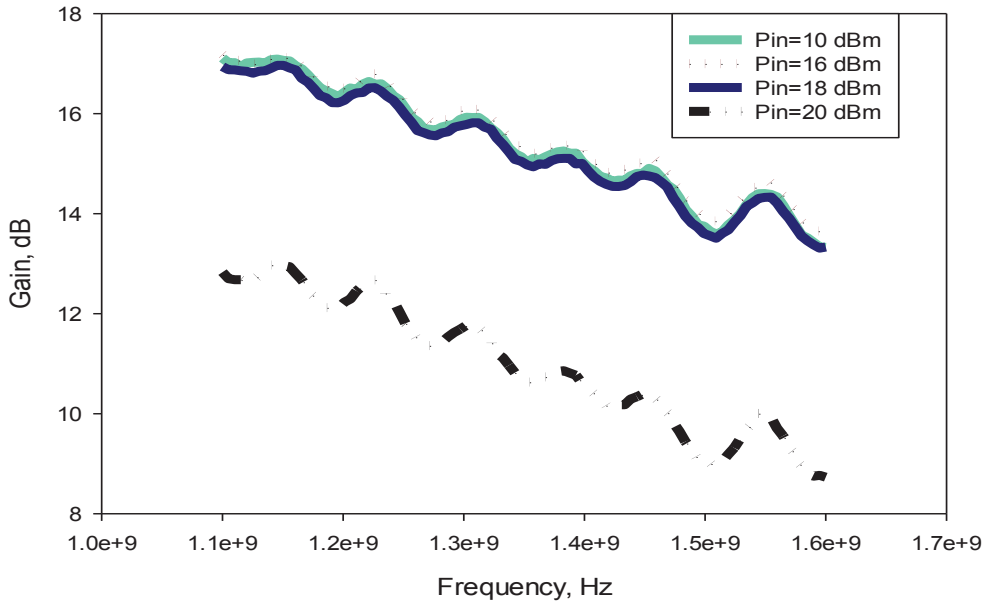


Figure 56 Variation of gain with frequency after being subjected to different power levels (DUT 2)

8.5 Additional tests

a) Single tone test: Using 8596E signal generator from Hewlett Packard, power was fed to the low noise amplifier and it was increased until the gain dropped by 1 dB. The compression point (P_{-1dB}) for the low noise amplifier was found to be at -2.33 dBm. While for the design including limiter, the compression point was found to be -1.91 dBm.

b) Two tone test: Using two signal generators (8643A, Hewlett Packard and E8257D, Keysight), -30 dBm/carrier input signal was fed to the LNA. As expected third order intermodulation distortion was obtained at 1.366 GHz (2f1-f2) and 1.393 GHz (2f2-f1) for f1= 1.375 GHz, f2=1.384 GHz
Output power level, Po= -18 dBm
Third order intermodulation power level, Po_3= -72.44 dBm
Third order intercept point, OIP_3= Po + 0.5*(Po – Po_3) = +9.32 dBm
Similar test was performed for LNA including limiter and the third order intercept point was found to be +12.9 dBm. The results are also shown in table 3.

Table 4 OIP3

	DUT1	DUT2
OIP3 (dBm)	9.32	12.9

Hence, we see that in both cases third order intercept point is at least more than 10dB higher than compression point. Also, for the device with limiter in front, IP_3 is higher indicating that it is more linear and has less interfering signals.

8.6 Comparison between implemented and previous LNA

Table 4 shows comparison between implemented design and previous designs available at RUAG.

Table 5 Comparison between different LNAs designed at RUAG

Parameter	**Implemented design**	**Previous design 1**	**Previous Design 2 (Balanced)**
Process	HBT	pHEMT	MESFET
Operating Frequency Band, MHz	1000-2000	1164-1610	1200.5 +/-40, 1575.42 +/-8
Noise Figure, dB	<1	<1	<2.35(L1), <2.55(L2/L5) (2),(3)
Gain, dB (1)	13(minimum)	20	30.5(minimum in L1 and L5)
DC Power Consumption, W	0.015	0.33	0.99
Current Consumption, mA (1)	5	100	97
Supply voltage	Single	Dual	Dual
Size	Small	Smaller	Large
Input return loss, dB	6	8	15

NOTES:

(1) There is different number of transistors between designs, hence different gain
(2) This is including loss in filters before LNA
(3) Also includes 90° hybrid configuration

9. CONCLUSION AND FUTURE WORK

A LNA using single SiGe HBT transistor has been designed and fabricated. It runs on single supply. It has a measured noise figure of 0.84-0.91 dB and gain is 17-13 dB in the frequency band of interest. Hence, it has been proved that BFY640-04 transistor has potential to provide low noise figure to be useful for GNSS applications. The designed amplifier is very stable compared to the previous design using pHEMT. The input return loss is not optimized in this design compared to the previous designs, which was intentional. One important feature to be noted in the implemented design is that it covers the entire L-band. Measurements showed it had noise figure of less than 1 dB within the frequency range of 1.1 GHz-1.6 GHz while in ADS simulations it has also been noticed that noise figure is about 1 dB up to 2 GHz. This indicates a useful application for future satellite navigations systems which will have increased frequency spectrum within L-band.

As this design was done in a single stage attaining both minimum noise and high gain is cumbersome. In future, efforts can be made to build a multi-stage design with higher gain and improved gain flatness. Also, a balanced configuration in the first stage can help in attaining good input return loss.

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17. Technical.Datasheet http://rosenberger.de/ok/images/documents/db/32K145-400L5.pdf[Cited: July , 2015]

Appendix A

Plots of stability characteristics (μ and μ') obtained from simulation of the designed LNA(excluding limiter)

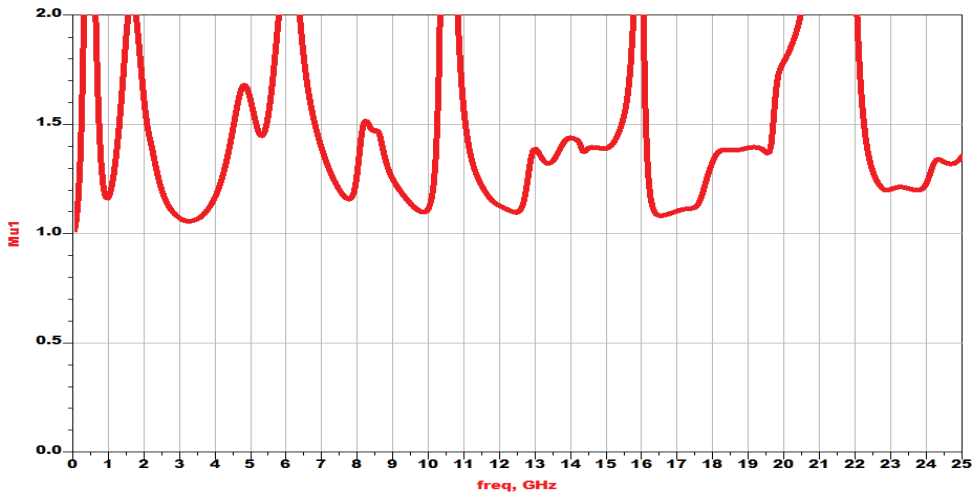

Figure 57 μ

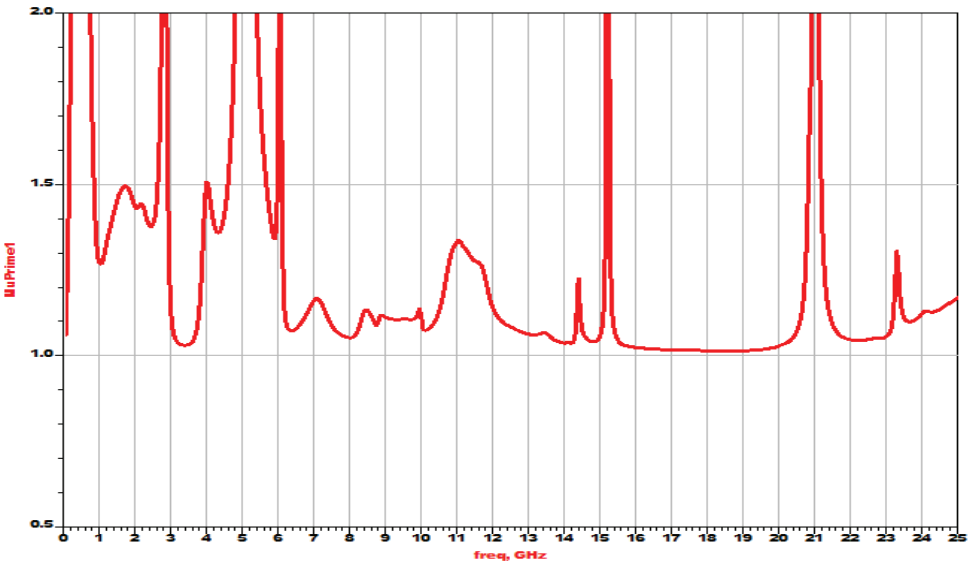

Figure 58 μ'

Appendix B

Plots of stability characteristics obtained after post-momentum simulation of the designed LNA(excluding limiter)

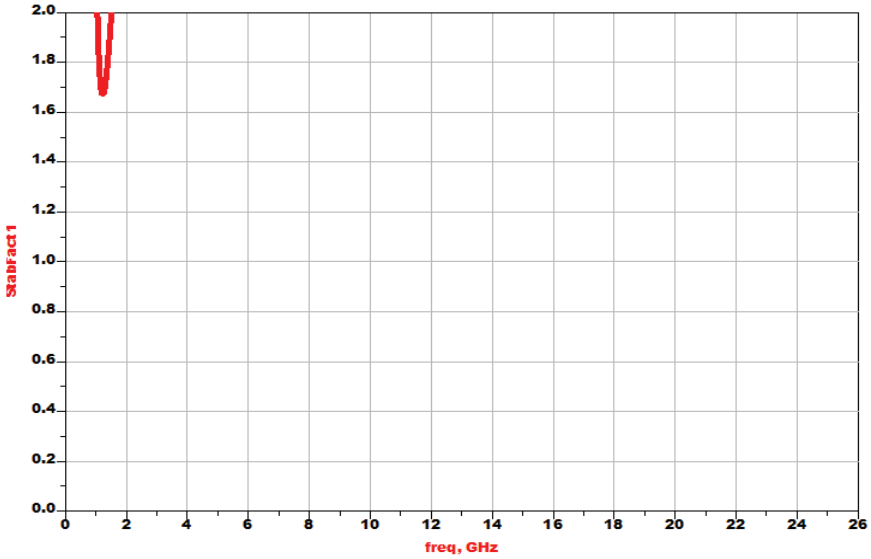

Figure 59 Stability factor K

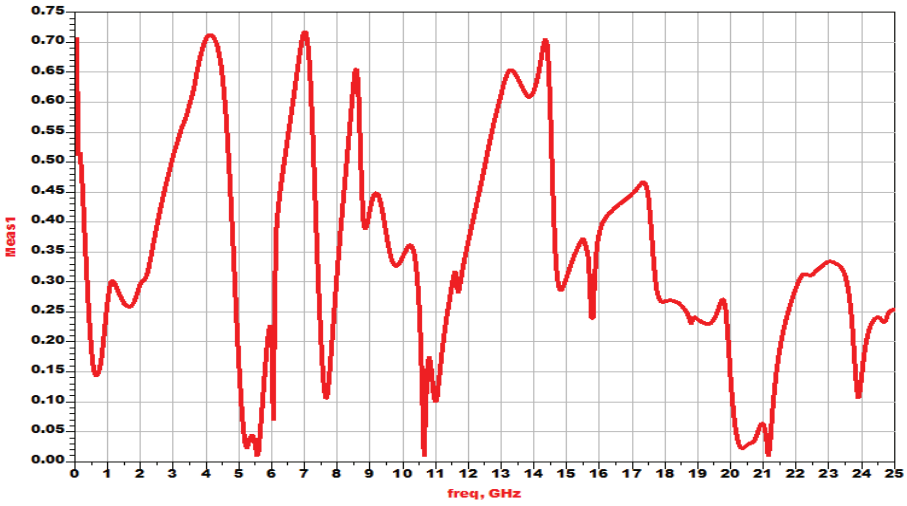

Figure 60 Delta , Δ

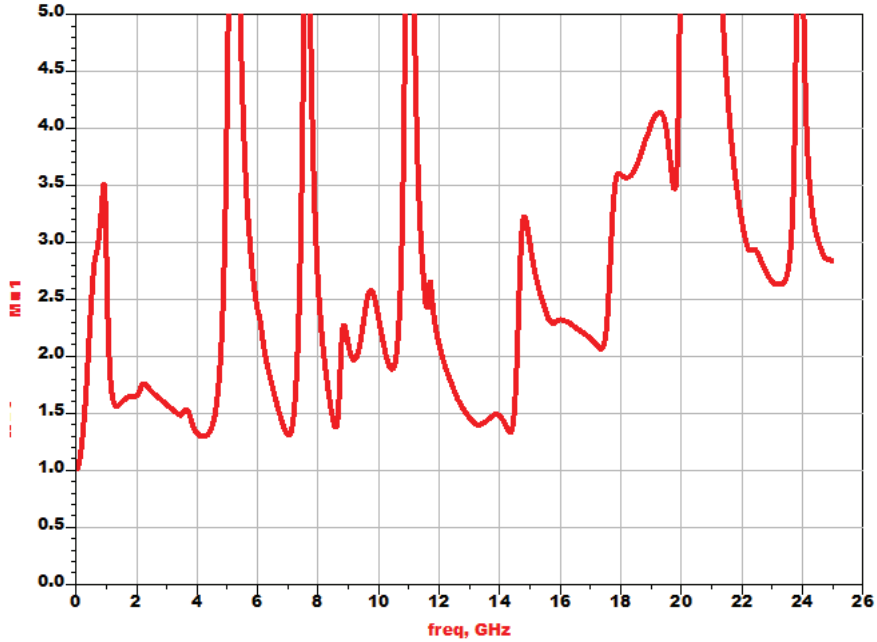

Figure 61 μ

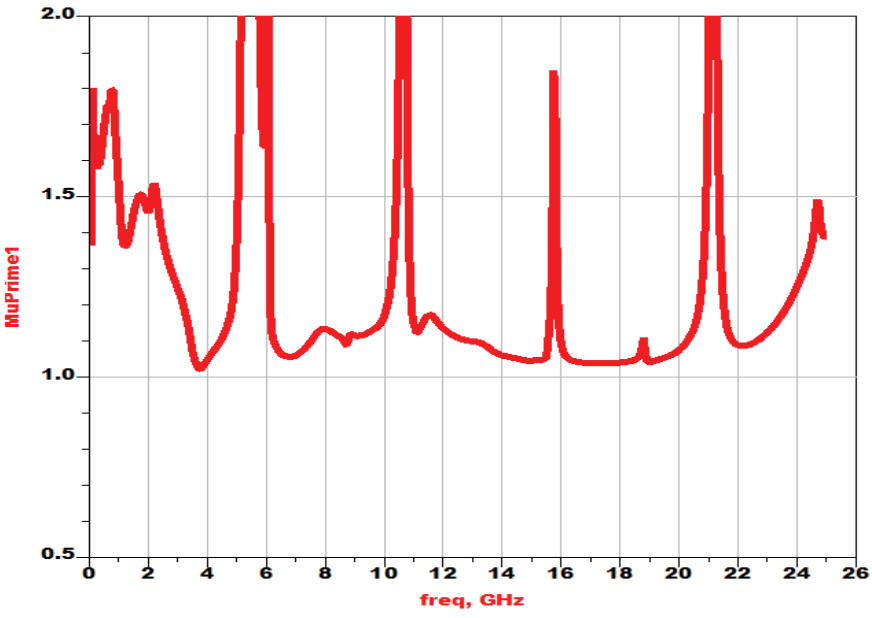

Figure 62 μ'

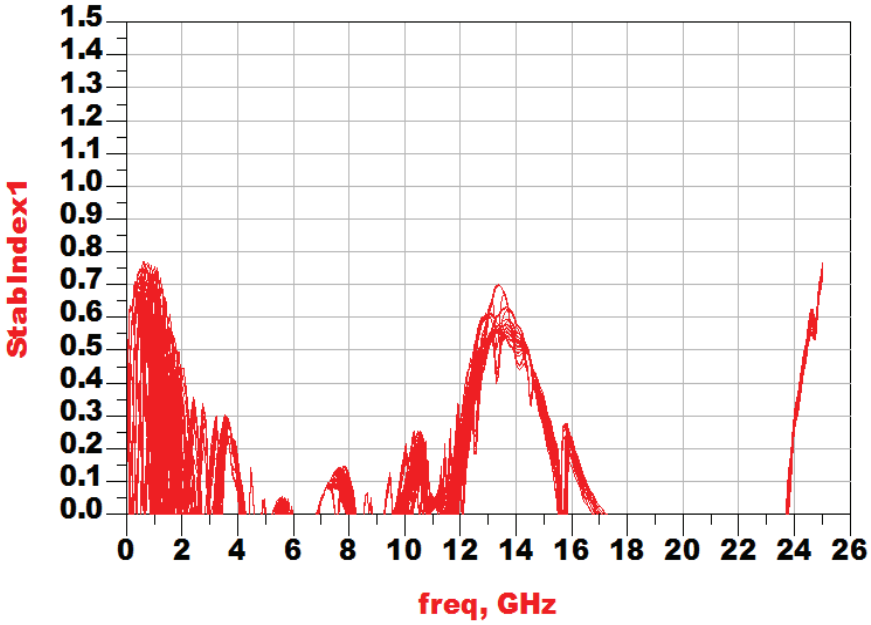

Figure 63 Stability index (input)

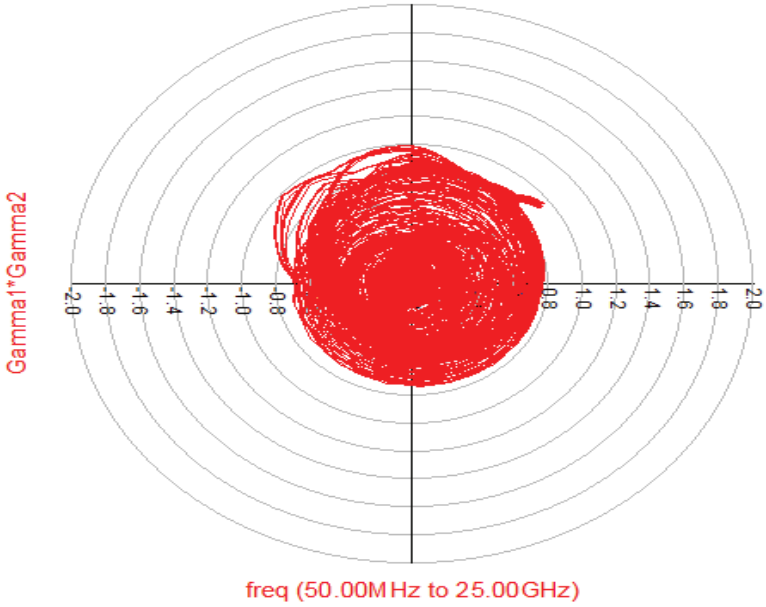

Figure 64 Product of reflection coefficients (input)

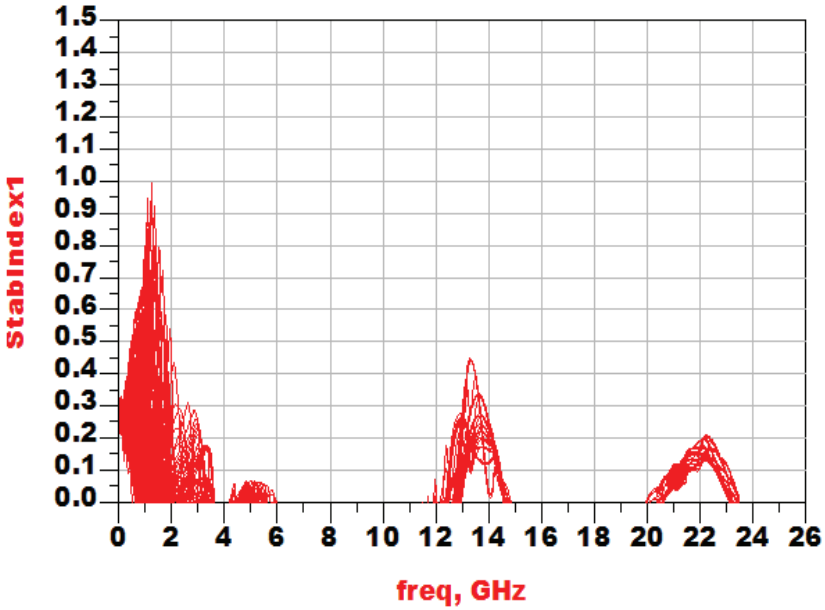

Figure 65 Stability index (output)

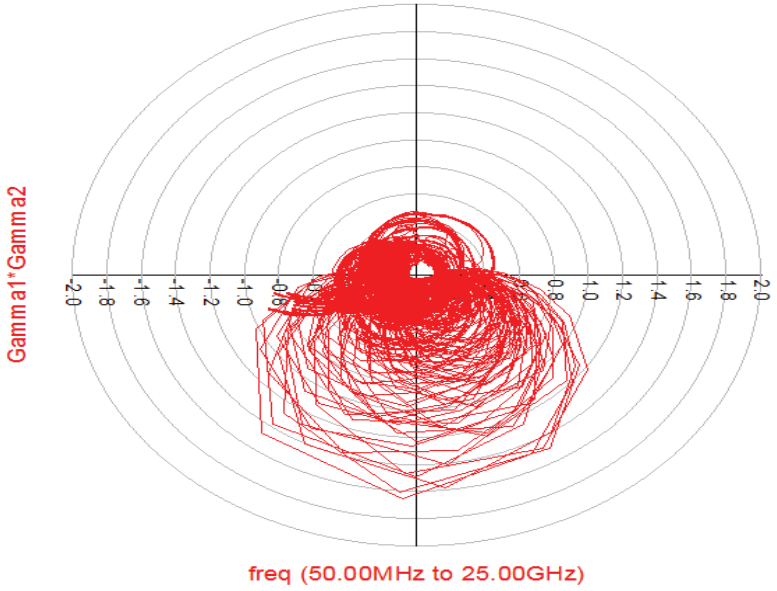

Figure 66 Product of refection coefficients (output)

Appendix C

Plots of stability characteristics obtained from measurements on the fabricated LNA (excluding limiter)

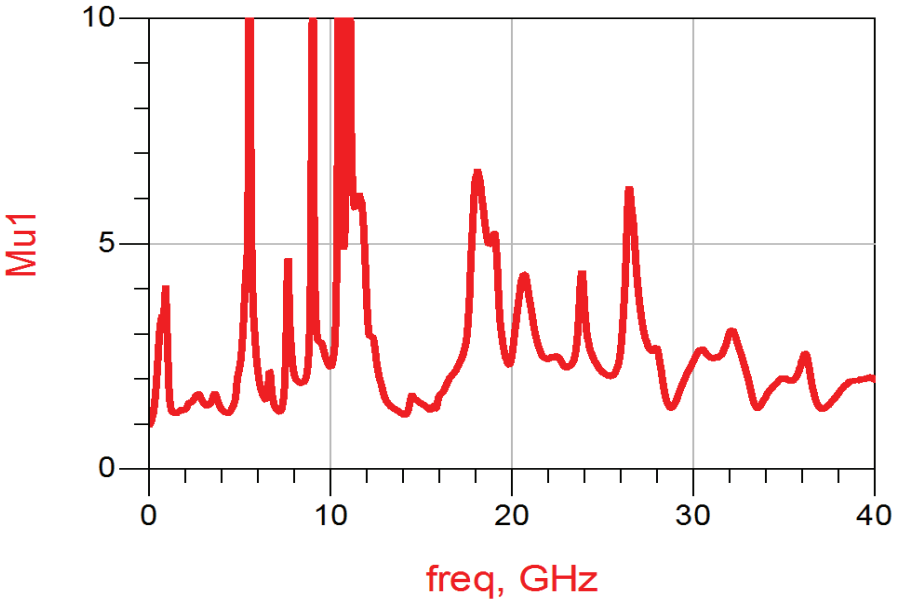

Figure 67 μ

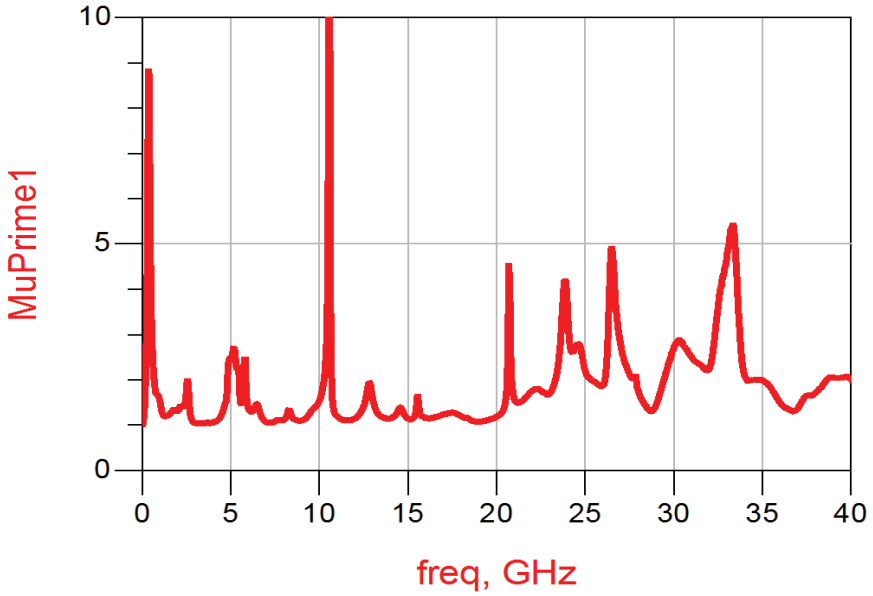

Figure 68 μ'

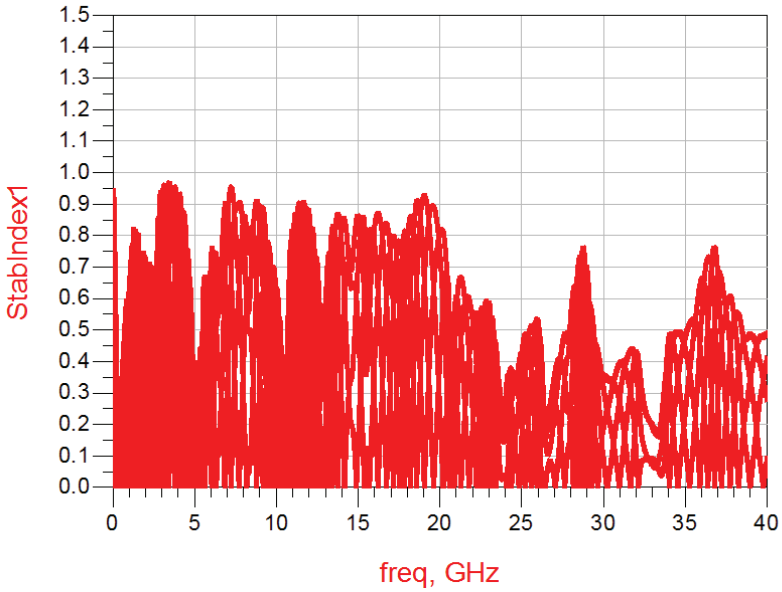

Figure 69 Stability index (input)

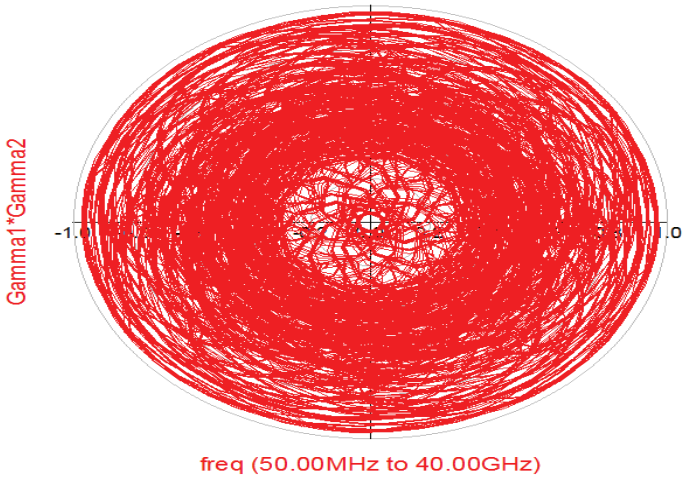

Figure 70 Product of reflection coefficient (input)

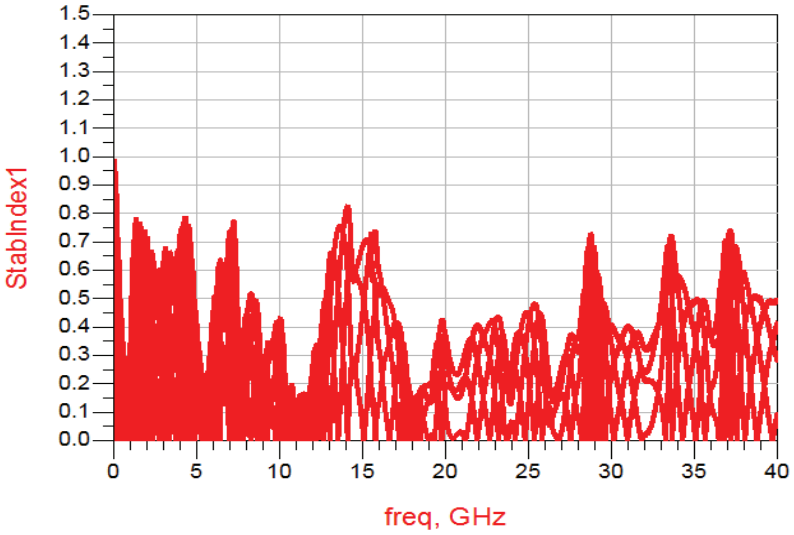

Figure 71 Stability index (output)

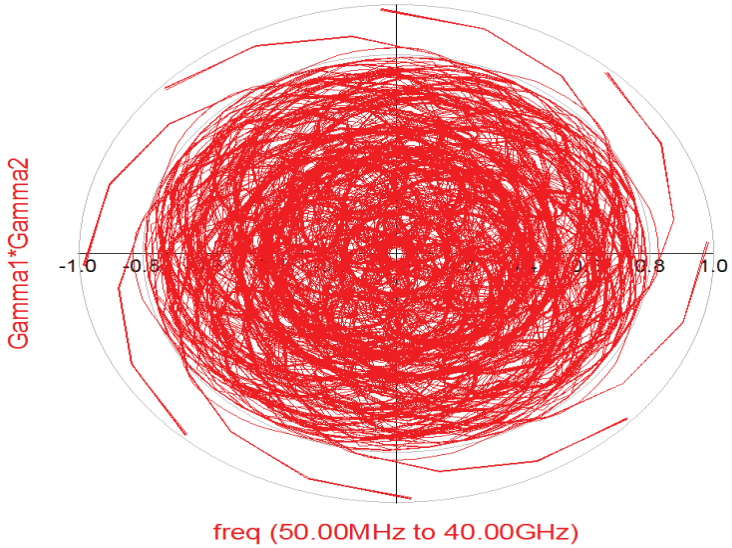

Figure 72 Product of reflection coefficient (output)

Navneeta Deo

Design and Test of an L-Band (GNSS) Low Noise Amplifier and Limiter

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