Master's Thesis

Effect of active load on III-V NWFET Double-Balanced Gilbert Cells

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Department of Electrical and Information Technology,
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Abstract

A center point in the transistor research is to find a successor to the silicon-based transistors that are mainly used in today's industry. III-V Field Effect Transistors (FET) have been the transistor of choice for many researchers for a long time but other options are interesting as well. The aim of this thesis is to show what a mixer circuit based on Nanowire transistors can achieve when combined with active load and current bleeding techniques.

The results achieved in the simulations show how the performance of almost all parameters like gain, noise factor and especially linearity improves. The final values reached was a gain of 4.28 dB, a low noise factor of 9.7 dB, IIP3 of 16.4 dBm and 1dB compression point of 0.17 dBm. The values the linearity reached were very high but they came with the price of an increased power consumption with a factor of five, 40 mW compared to 8.7 mW for the regular Nanowire mixer without the active load implemented.

As the linearity was very good for this mixer at the outset, the improvements of the mixer are mainly in the wrong area making the increased power consumption a disadvantage in the usual case. The design could however still be useful in some specific cases where extreme linearity and low noise factor is of outmost importance.

Acknowledgments

I would like to thank my supervisor Lars-Erik Wernersson, for his guidance and support throughout this thesis and the chance to attend the group's weekly meetings to get some valuable insight on how a research team work and function.

I would also like to thank Niklas Lindblad, whose work I continued to build on with this thesis, for the support and the assistance in the beginning of this project.

Pontus Arvidsson

"Rule No. 11: Be nice to nerds. You may end up working for them. We all could. "

Charles J. Sykes

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The Aim of the Thesis

This master thesis continues to build on the work in the master thesis "Simulations of III-V NWFET Double-Balanced Gilbert Cells with an Improved Noise Mode" [1] written by Niklas Lindblad at the Nano Electronics Group at the department of Electrical and Information Technology (EIT) at Lund University in 2013. The aim of this thesis was to further improve the simulated results reached in 2013 by replacing the load resistors by an active load in the form of PMOS transistors.

The first part of the simulation project was to setup a suitable Nanowire PMOS model that matched the data achieved in the lab here at EIT to have a realistic active load on which to base the rest of the work. The simulations were performed with the SpectreRF component of Cadence Virtuoso, a well-known tool in the semiconductor industry. The components created for the project were created in Veriloga format for easy editing and flexibility while simulating.

The next part of the project was to implement the PMOS Nanowire Field Effect Transistor (NWFET) as active load in the mixer circuit and to find the optimal component parameters and settings. The simulations were automated with an updated version of Niklas's script used in the previous study [1]. The script uses Open Command Environment for Analysis (OCEAN), it is run in Cadence Virtuoso and it is based on the SKILL language.

The final part was to compare the mixer to other published data to find out if this more complex design gives any advantage over the traditional models.

CHAPTER 1

1 Introduction

1.1 The Transistor

When referring to a transistor the type of transistor meant is usually a Metal-Oxide Semiconductor Field Effect Transistor (MOSFET). The MOSFET are in principle two p-n junctions connected to a MOS-diode.
The FET was first demonstrated in 1960 by Bell Telephone even if it was patented already back in 1925 by Julius Edgar Lilienfeld. The transistors have developed rapidly since then to become the most important device for Integrated Circuits (ICs) used in almost all electronic devices that are used today.

The MOSFET have three terminals, the gate, source, and drain as well as a fourth contact in the bulk or substrate that normally is used as ground.

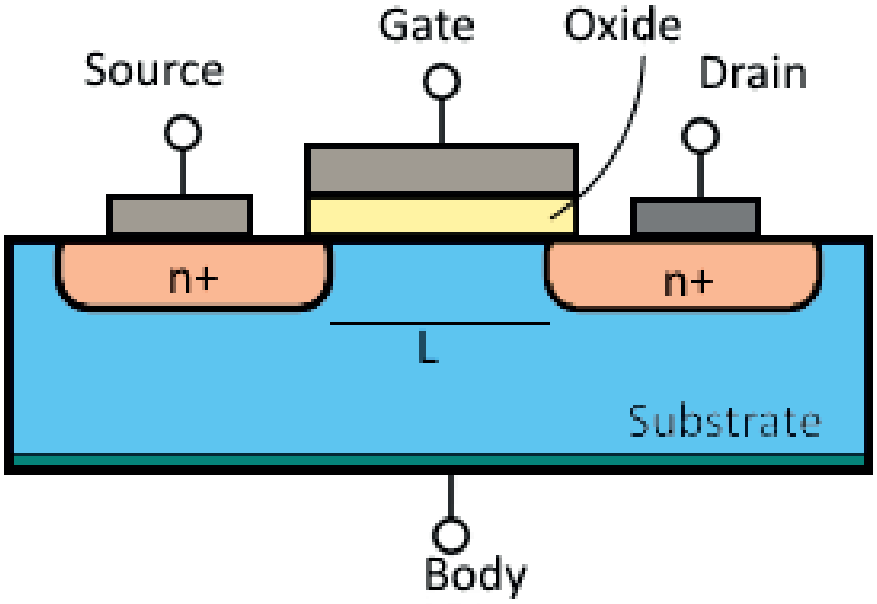

Figure 1: Cross section of a MOSFET of n-type

The transistor works by the gate either opening or closing a channel beneath it depending on the applied voltage over the gate. This is also where the difference lies between the n-type and the p-type transistors. In an n-type it is the electrons that are attracted to the gate and create the channel, as opposed to the negative holes being attracted to the gate in the p-type transistor.

There are several reasons for wanting to make the transistors as small as possible in electronics, a smaller resistor takes less space allowing more

transistors to be included in a chip of the same size and thereby increasing performance and/or decreasing the cost per transistor. Another reason is that the transistors operating speed is based on the length (L in figure 1) of the transistor and a shorter channel allows for a faster transistor. There are, however, not only advantages with decreasing the channel length, today's transistors are so small that short-channel effects have become a major problem.

1.2 FinFET

The result of the downscaling of the MOSFET is that the electric properties of the channel have reached its physical limits and to be able to continue improving the transistors and making them smaller a new method had to be invented. This method is called FinFET and the name comes from the model where the channel is standing up in a 3 dimensional model, so the gate surrounds it on 3 sides instead of just on the top as in a 2 dimensional model. The effect of this is better electrical control over the channel, which helps to reduce the leakage current and overcoming short-channel effects.

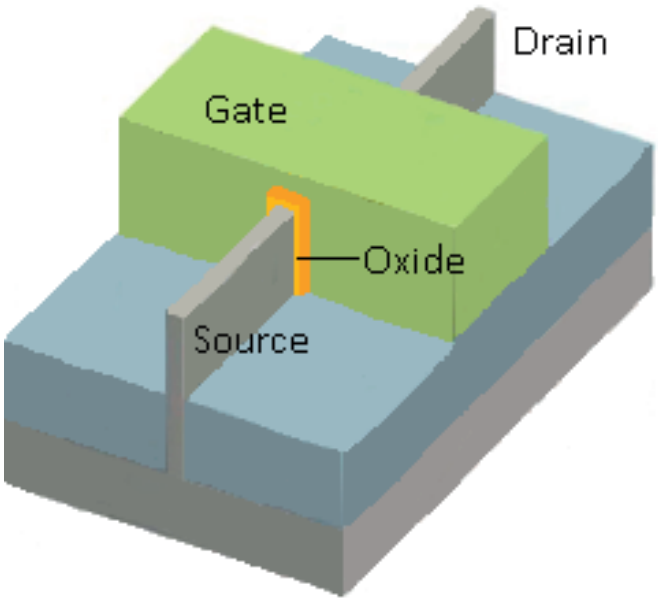

Figure 2: Drawing showing how the channel leaves the 2d plane in a traditional MOSFET as a fin for better electrical control.

1.3 NanowireFET

The next logical step from finFET is to build a structure where the channel is surrounded by the gate on all sides. This further increases the electrical control over the channel. One of the alternatives being researched is the use of thin nanowires (NWs) as the channel, which allows the use of new materials and material combinations as thin NWs can materialize in crystal structures that are impossible for bulk materials to materialize in due to the structure being more flexible for strain in nanometer size than normal bulk size.

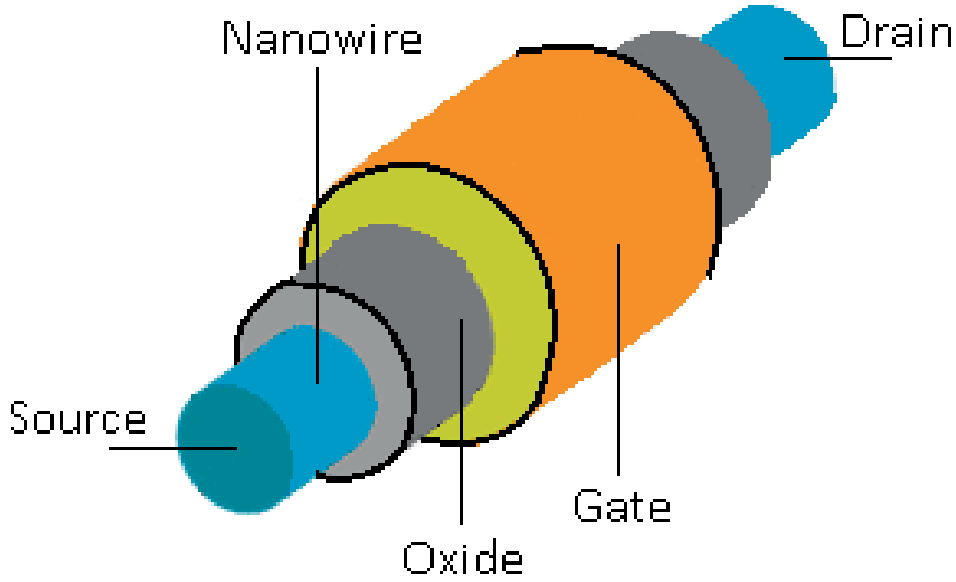

Figure 3: Sketch of a next-generation FET using a nanowire that is surrounded by the gate as channel.

The model shown in Figure 3 illustrates how the gate surrounds the channel completely when using a NW as the channel which leads to better electrical control than in the finFET case. To further improve the control and the channel width, stacks of NWs can be used as shown in figure 4 which leads to a large contact area in relation to the channel area compared to the other methods shown before, this method with lateral NWs was used by the group of EITs when accomplishing the record for fastest III-V MOSFET [25].

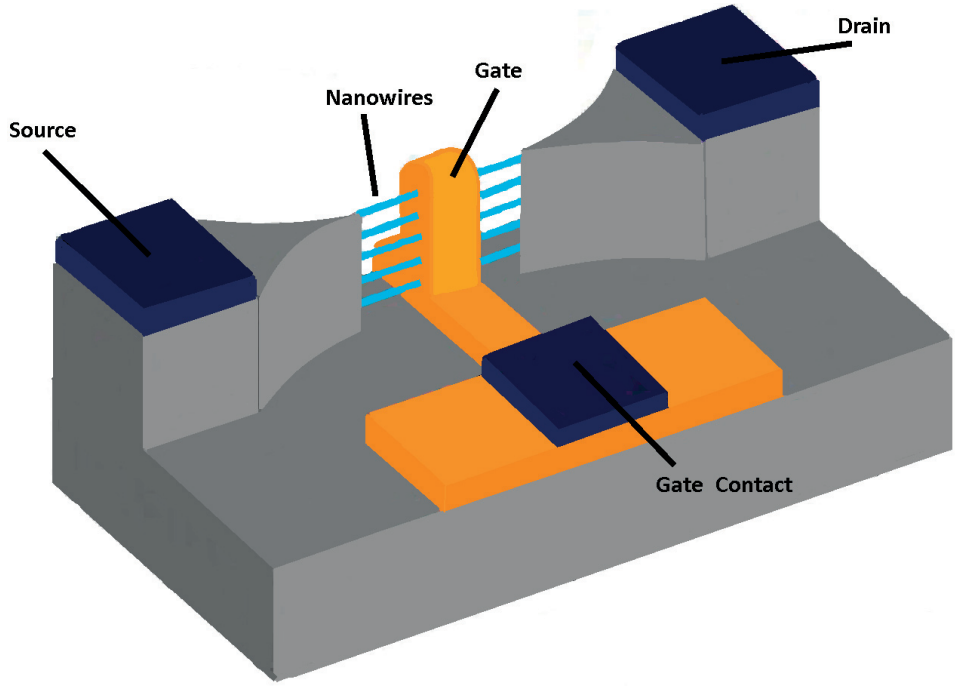

Figure 4: Drawing of stacked nanowire FET based on the concept from [15]

Another interesting application when using nanowires as transistors is to have them standing in a vertical position as they are grown on the substrate instead of removing the nanowires from the substrate and placing them on a new substrate to be part of a transistor. This has the advantage of removing the problem with placing the nanowire as gate between the drain and source contacts as the substrate it is grown on is used as one contact. The next step in the process of creating the transistor is to add a gate along the length of the NWs and finally add another layer as contact at the top.

1.4 RF mixer basics

One of the most important processes in the Radio Frequency (RF) technology and designs is mixing signals. Mixing the signals enables them to be processed more effectively and used for a wider spectrum of application by converting the signal to different frequencies.

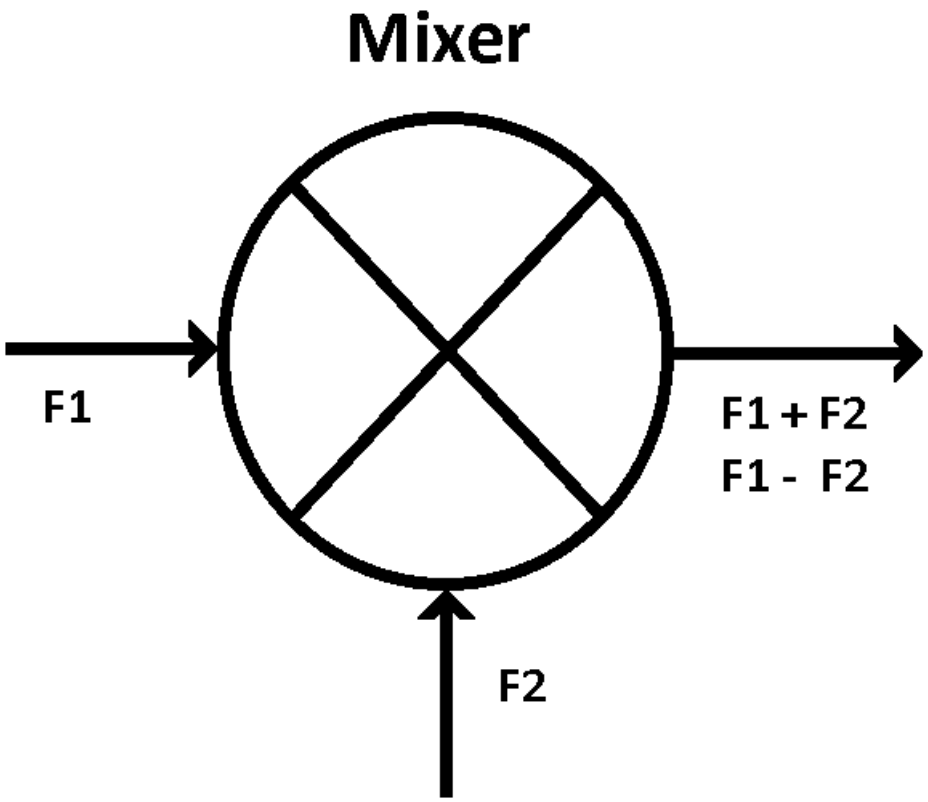

Figure 5: Circuit symbol for an RF mixer,

All RF-mixers are based on three ports, two inputs and one output, the three ports are:

RF input: This is the port that is connected and accepts the incoming signal, which is then converted by the mixer.

LO input: (local oscillator input) this port is the second input that receives an internal oscillator signal that is used as the converting frequency that the RF signal gets multiplied with in the mixer.

IF output: The intermediate frequency output is the output of the mixer and should in the ideal case contain nothing but the mixed product from the two inputs, the sum and the difference.

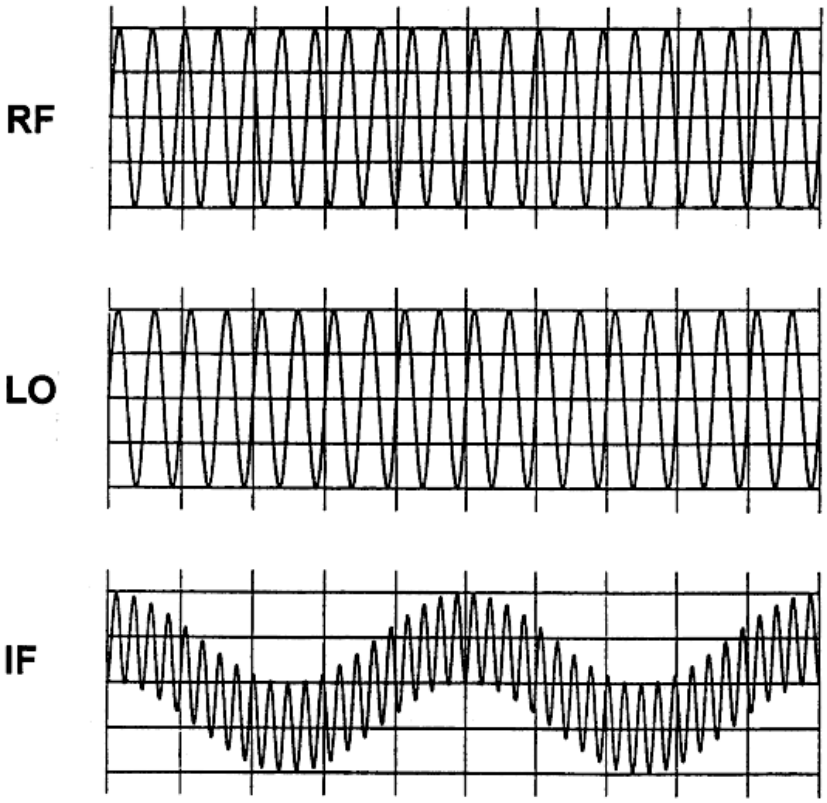

Figure 6: The result of two signals mixed together [4]

RF mixing differs from for example audio mixing where multiple signals are added together linearly. RF mixing however acts as a non-linear process where the instant level of one input signal affects the level of the other input signal at the output. This means that the two signal levels multiply together at any given time resulting in a complex waveform based of the product from the two original signals.

As illustrated in figure 6 the top two signals show the input to the mixer and the bottom signals show the product of the two input signals at the output from the RF-mixer.

Just as shown in the symbol for the RF-mixer in figure 5 the result at the output can be seen as the sum and the difference between the two input signals.

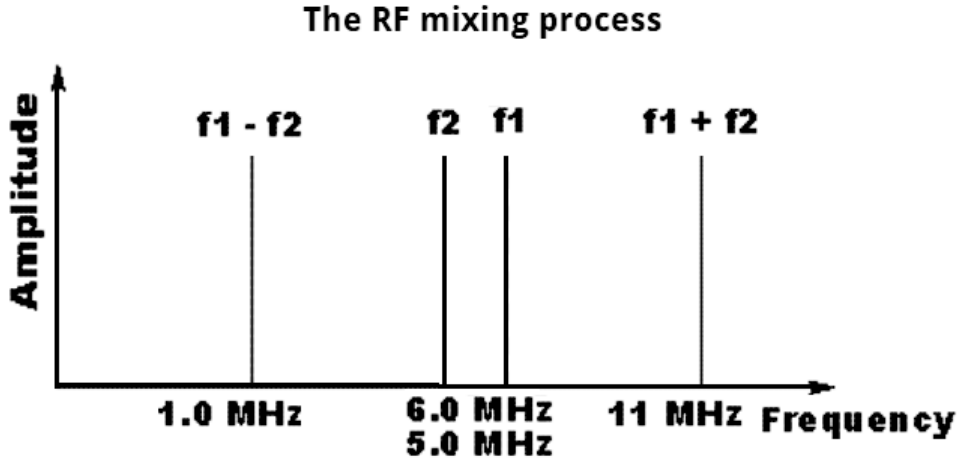

Figure 7: The RF mixing process.

The equation (1) describes the mixing of the two input signals V1 and V2 with the frequencies ω_1 and ω_2:

$$V1 = A \sin(\omega 1 t)$$
$$V2 = B \sin(\omega 2 t)$$

The output from the RF-mixer after multiplying the two inputs with a trigonometrical expression assumes the form of the equation 1 where the terms ω1 - ω2 and ω1 + ω2 can be seen:

$$V1 \times V2 = (A \times B)/2 \ [\cos(\{\omega 1 - \omega 2\} t) - \cos(\{\omega 1 + \omega 2\} t)] \quad (1)$$

1.5 Key RF mixer specifications

- Power Consumption
- Frequency range
- Input levels
- Conversion loss / gain
- Port isolation
- 1 dB Compression Point
- Third-Order Intercept Point (IP3)
- Noise figure

Power Consumption
Depending on the area of usage, the power consumption of the mixer can be of the outmost importance. It is possible to simulate a complete power spectrum for the mixer but this figure is normally only given as power consumption for a specific setting. The most common way to interpret this figure is by showing the DC power consumption as the DC current measured, multiplied with the supply voltage. [14]

Frequency range
Frequency range or bandwidth is the useful frequency range of the RF-mixer as no mixer is able to operate successfully over the full frequency spectrum. The limiting factor for the frequency range is normally the required voltage conversion gain that depends on the frequency.

Input levels
It is important that the level of the input signals is within the specifications of the RF-mixer for it to function correctly. This applies to both extremes, but most notable is the maximum input level as the mixer may become overloaded which results in an increase of unwanted spurious signals, for example intermodulation distortions (IMD) and harmonics, as well as the mixer failing to keep up with the port isolation.

When it comes to the LO input is it necessary to keep reasonably close within the specifications of the RF-mixer, if it goes too low the conversion gain will decrease and if it goes too high more spurious signals will affect the output

result. A typical tolerance of the LO input is a deviation of +/- 3dB from the specified input level [14].

Conversion loss / gain

Conversion gain measures the signal gain in an active mixer, while conversion loss describes the insertion loss in a passive mixer. The conversion loss or gain is measured in decibel (dB).

The conversion loss of a RF-mixer is a description of how efficient the mixer is. The definition of conversion loss is the ratio of the level of one of the two output signals, the sum or difference, compared to the level of the RF-input. Therefore, the ratio can never be higher than half of the RF input as the output power is split evenly between the output bands. This means that the ideal conversion loss is 3dB, typical values range between 4.5-9dB, because of other losses that are present in the non-ideal case [3], for example towards the ends of the allowed bandwidth or as a result of a badly tuned LO signal.

Conversion gain in the active mixer is measured as power conversion gain or voltage conversion gain [2]:

$$Power\ Conversion\ Gain\ (dB) = 10 * \log(\frac{P_{IF}}{P_{RF}})$$

$$Voltage\ Conversion\ Gain\ (dB) = 20 * \log(\frac{V_{IF}}{V_{RF}})$$

The power and voltage conversion gain are equal for matched impedance and the conversion gain is normally measured as a function of LO power with constant RF and LO frequencies or as a function of RF frequency with a set LO power.

Port isolation

The port to port isolation, most importantly LO to RF and LO to IF isolation, is one of the most important parameters of the RF-mixers for most of the RF applications. Port isolation is defined as the ratio between the signal power sent into one port of the mixer and the power of that signal at one of the other ports of the mixer in a 50 ohm system. The isolation that normally receives the highest focus is the LO to RF isolation as the LO signal is often much stronger, increasing the risk that the LO signal is interfering with the RF signal and causing problems such as intermodulation before the mixing can take place. Figure 10 shows the LO and RF inputs and the IF output.

1 dB Compression Point

When plotting output power against input power of a linear amplifier for a specific frequency, you will se a linear relationship where the slope is the gain. The output power is limited and will start to plan out and reach a compression region once the input power is high enough to saturate the amplifier [5]. This region leads to distortions of the signal, as well as harmonics and intermodulation products.

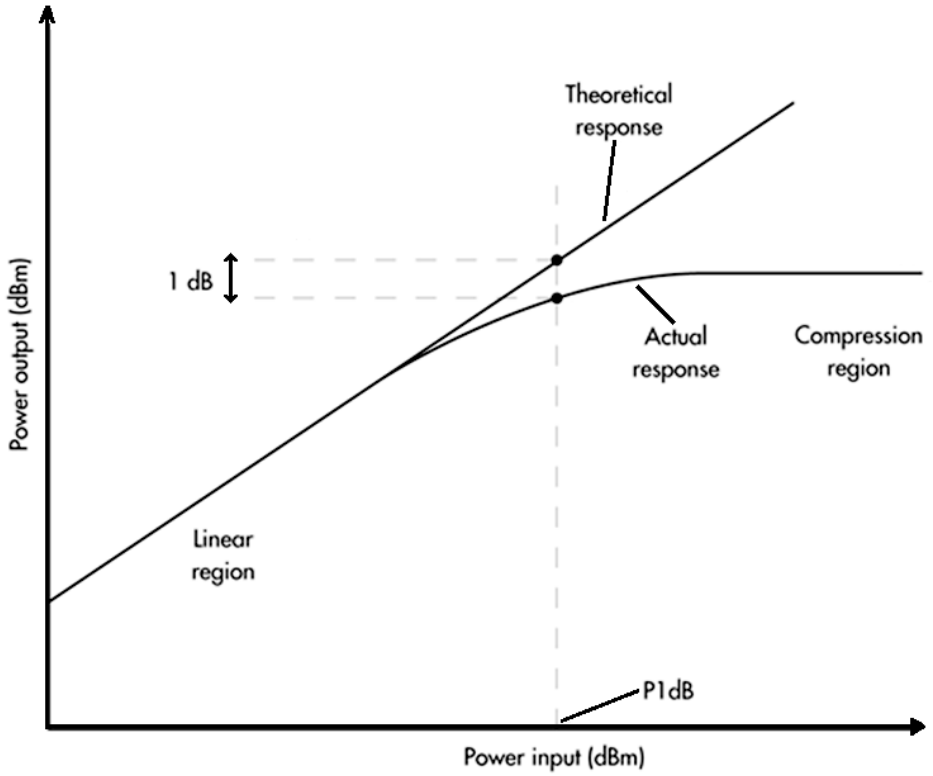

Figure 8: Illustration of the 1 dB compression point.

The 1 dB compression point is a measurement for at what input power level the compression reaches a 1 dB drop between the wanted and the actual response. It is used as a value to show the power limits of the amplifier, or in this case, of the mixer.

Third-Order Intercept Point (IP3)

The third order intercept point is a theoretical point that builds on the response of the mixer when it becomes nonlinear and starts to produce harmonics. The harmonics are normally outside the mixer's bandwidth and usually relatively easy to remove with a filter. One exception is the situation when the signals are close together, especially the third order harmonics can be a problem since they are the products [5]:

$2F_1 \pm F_2$
$2F_2 \pm F_1$

Two of these, $2F_1 - F_2$ and $2F_2 - F_1$ have a high chance to be close to the starting frequencies and therefore most likely to cause a problem.
When plotting the output power against input power as shown in the 1 dB compression point case (figure 8) for both the signal and the third order harmonics it becomes apparent that the third order signal power increases at a 3:1 gain rate compared to that of the intended signal.

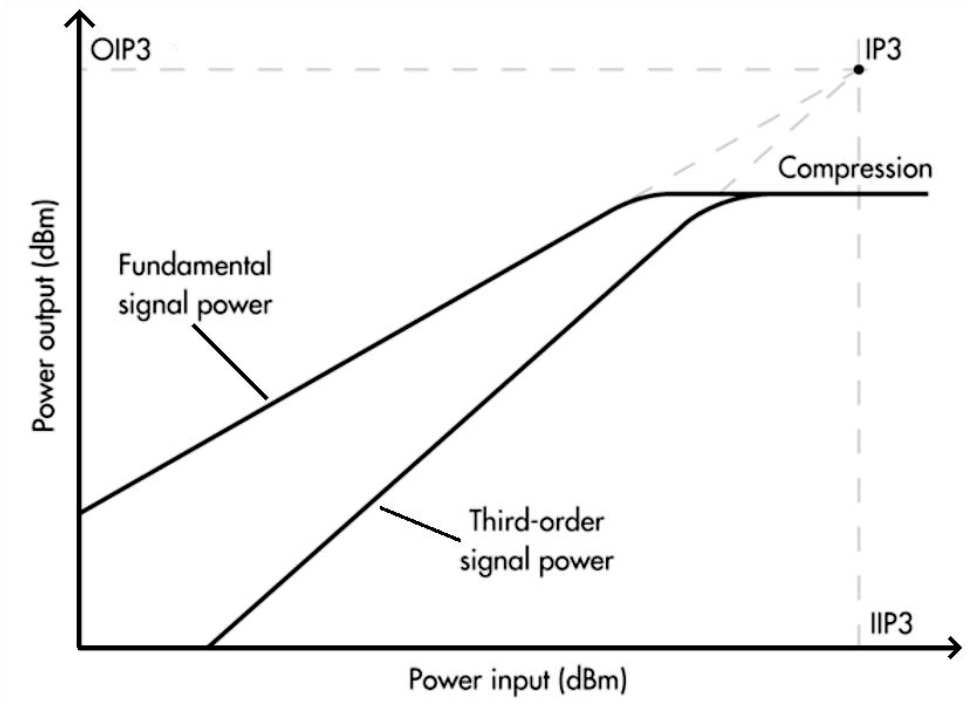

Figure 9: Illustration of the Third-Order Intercept Point (IIP3)

In the normal case the curves will not cross because of the occurring compression when the mixer gets saturated, but when extending the linear portions of the curves they will reach an intersection point where they would have crossed over in the ideal case without saturation. This point is called the IP3. IP3 read as a function of the input is called IIP3 and correspondingly when it is read as a function of the output it is called OIP3. Even if this point is never achieved it is still a useful metric in determining the linearity conditions of the mixer and how good its linearity and IMD are.

Noise figure

Harold Friis Defined the Noise figure (NF) in 1944 [16] as the signal to noise ratio for the output compared to the input.

$$NF = \frac{S_i/N_i}{S_o/N_o}$$

Noise figure is a very useful parameter when describing noise as it is suitable for describing both components as well as characterizing the full system [17]. This makes the noise figure from the RF-mixer important but it gets suppressed in a full receiver system by the gain of the low noise amplifier (LNA) and the noise from the LNA becomes dominant. High noise from the mixer can however still pose a problem, especially if it is at an early stage in the system and it is therefore important to keep the noise figure low.

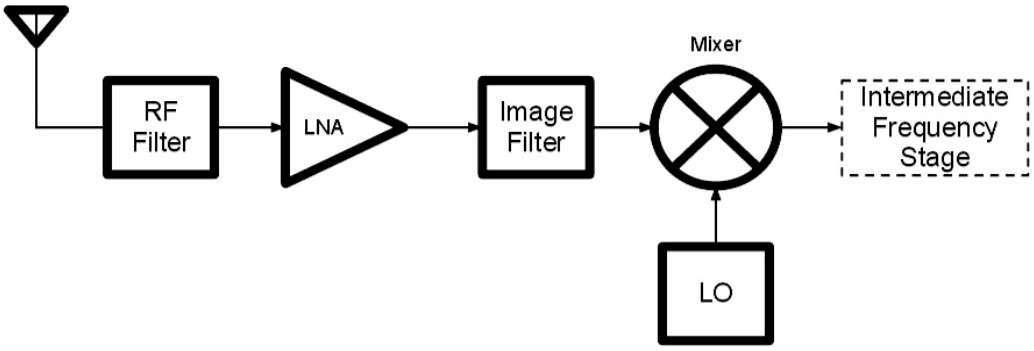

Figure 10: Block diagram of a receiver system.

1.6 Passive or Active Mixers

Figure 5 describes a basic mixer, also called a passive mixer. It is the most widely used type of mixer due to its simplicity in design, its wide bandwidth and high tolerance for spurious signals. One problem with this technique is the need for external baluns that are used to increase the bandwidth. A balun is a component used to convert an unbalanced input to a balance output or a balanced input to an unbalanced output (Where balun is a short from combining the words Balanced and Unbalanced) [18]. The downside of this is the introduction of noise that can be helped by an LNA, although this comes with the price of reduced IMD performance.

The alternative to passive mixers is active mixers. Some advantages are that they can provide conversion gain instead of conversion loss as in the case with the passive mixer. The active mixer requires much less power to drive the LO port, has better port isolation and they are also more suited to be integrated into ICs because of the integrated active baluns. The downside is that it is harder to achieve good IMD performance [24].

1.7 Single Balanced Mixer

The transistor pair showed in figure 11 can be used for multiplications if the transistors are run within appropriate specifications:

$$\Delta I_d = I_{d1} - I_{d2} = I_s \tanh(V_{id} / 2V_T)$$

$$V_{id} = V_{in+} - V_{in-}$$

Approximate that:

$V_{id} << 2V_T$ which leads to $\tanh(V_{id} / 2V_T) \sim = V_{id} / 2V_T$

Then:

$$\Delta I_d \approx I_{EE} (V_{id}/2V_T)$$

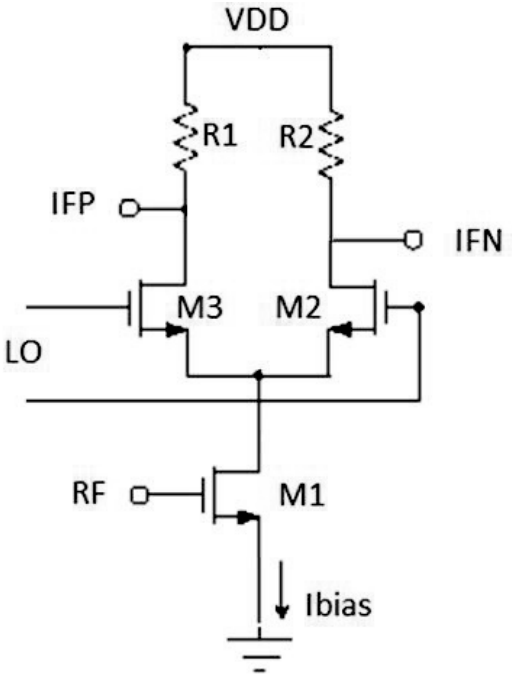

Figure 11: Single balanced mixer

This relationship is plotted in figure 12 and it shows that the transistor pair alone can be used as a multiplier as long as the input signal is kept small enough compared to V_T so it remains in the linear region. If the input signal is large compared to V_T, which results in the transistor working as switches and effectively creating a square wave. This allows the circuit to work as a mixer when the input signal multiplies with the square wave. The single balanced mixer design has a big advantage compared to the single device mixer in that the design gives an infinite port isolation in the ideal case, even if some leakage occurs with real transistors due to parasitic capacitances between gate and drain [24].

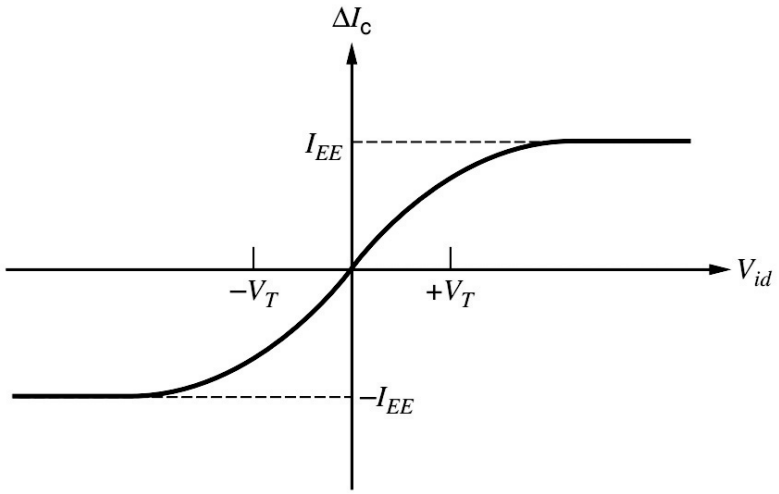

Figure12: Current plot for a transistor pair.

1.8 Double Balanced Mixer / Gilbert Cell Mixer

The double balanced mixer or the Gilbert cell mixer is the next step from the single balanced mixer. It is named after Barrie Gilbert who first described it in 1968 and has been a popular and widely used choice since then. It is also the mixer of choice for this thesis.

The Double Balanced Mixer is basically two single balanced mixers that are connected to each other with the effect that the IF output is now connected to two switching transistors and the LO leakage current cancels out if the two switching transistors are differenced by a π radians phase between their respective LO signal. This leads to better port isolation than the single device and single-balanced mixer. However, an obvious disadvantage is the increased number of transistors used resulting in a larger circuit. The noise figure of the Gilbert cell is also 3dB higher than an equivalent single balanced mixer or in the practical case up to 4dB higher [19].

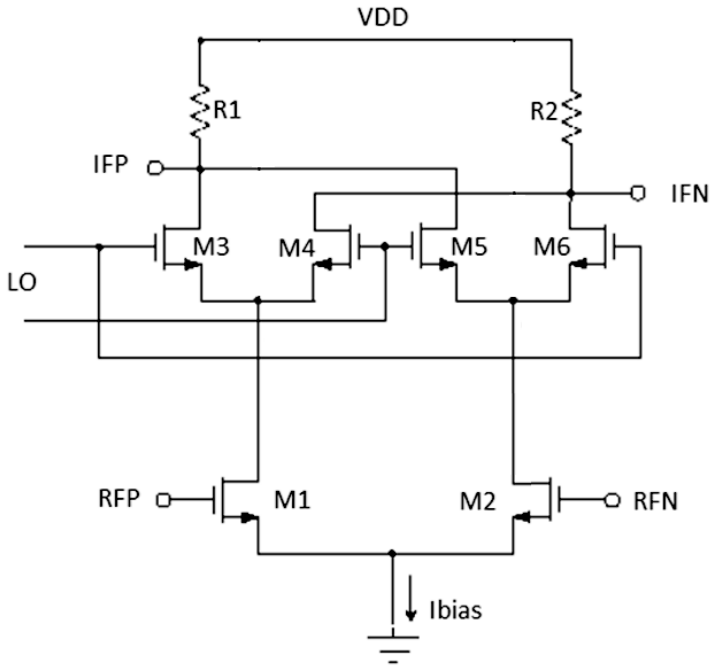

Figure 13: Basic Gilbert cell mixer configuration

Gain

The gain of the mixer needs to be high enough to suppress the noise from the IF stage and since noise factory is a power quantity and it generally is easier to calculate the noise from power gain than the gain normally used when discussing mixers [9].

$$Power\ gain = \left(\frac{V_{out}}{V_{in}}\right)^2 * \frac{R_{Source}}{R_{Load}} = \left(\frac{I_{out}}{I_{in}}\right)^2 * \frac{R_{Source}}{R_{Load}} \quad (2)$$

The voltage gain is adjustable by changing the g_m of the transistors M1 M2 and the load size, it can be calculated by:

$$Voltage\ gain \approx Kg_mR_{Load} \quad (3)$$

The R_{load} is then limited by

$$R_{Load} = \frac{2(VDD-3VDS_{sat})}{I_{Bias}} \quad (4)$$

The transconductance factor g_m of the transistor pair M1 M2 is then:

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{th}) = \frac{2I_D}{(V_{GS}-V_{th})} = \frac{I_{Bias}}{(V_{GS}-V_{th})} \quad (5)$$

Finally, in the case of an active load equation 4 is no longer valid and can be rewritten as:

$$VDD_{min} = 4VDS_{sat} \quad (6)$$

$$R_{Load\ active} = \frac{2VDS_{sat}}{I_{Bias}} \quad (7)$$

Linearity

Linearity is one of the critical design parameters in the mixer and has impact on the noise level of the mixer as higher linearity leads to less distortion. The linearity of the mixer represents a significant part of the linearity of the whole system, resulting in research to improve the design of highly linear mixers being of high priority [11] [12].

CHAPTER 2

2 Theory

2.1 RF Spectre Simulations in Cadence Virtuoso.
2.2 current bleeding
2.3 active load

2.1 RF Spectre Simulations in Cadence Virtuoso.

Periodic steady-state analysis (pss)
The PSS analysis is a RF adapted version of the normal DC analysis in SPICE (Simulation Program with Integrated Circuit Emphasis, a program that is used to simulate the integrated circuits). The difference compared to a DC analysis is that in PSS the circuit is driven by a periodic signal instead of a static voltage and, just as in the DC case, the input signal can be swept over a range of values. The solution gained from the analysis is a periodic operating point that is used for further small signal analysis [23].

Periodic AC analysis (pac)
The pac analysis is run after the pss has determined the periodic operating point. This analysis is similar to the alternating current analysis (AC analysis, the default analysis performed on an AC circuit) with the difference that it linearizes the circuit around the periodic operating point found in the pss analysis. The pac analysis calculates the response of a circuit in steady state when it is affected by a small sinusoidal effect. The frequency of the sinusoidal effect is not locked to the larger system and can be swept as wished. This allows it to model frequency conversion effects accurately.

Periodic transfer function analysis (pxf)
This is the analysis used after the pac analysis and it performs a small-signal analysis on the circuit. The small-signal analysis computes a transfer function from every source in the circuit to the output. The pxf analysis is similar to the normal transfer function analysis with the exception that it linearizes the circuit around the periodical operating point (which is determined in the pss analysis); therefore, the pxf more accurately models the frequency conversion effects.

Periodic noise analysis (pnoise)
The pnoise analysis can be performed after determining the periodic operating point of the circuit. The pnoise linearizes the circuit around the periodic steady state point obtained via the pss analysis and then performs a small-signal analysis. This analysis computes the total noise spectral density at the output.

Quasi periodic steady-state analysis (qpss)
A large signal analysis is similar to the pss analysis with the exception that the qpss uses one or multiple large periodic input frequencies. The steady state point is reached after all transient effects have significantly diminished [23].

Quasi periodic AC analysis (qpac)
The qpac analysis resembles the pac analysis with the main difference that the qpac analyses the quasi periodic steady state point achieved from the qpss analysis. The product from the qpac is frequency dependent transfer functions. The qpac analysis is necessary to perform to be able to achieve data of the linearity of the mixer.

2.2 Current Bleeding

Two important factors for the mixer's performance is the conversion gain and third order intercept point (IP3), both factors are proportional to the square root of the bias current of the driving stage as shown below in Figure 14. To improve the values the simple method is raise the bias current but this results in unwanted effects like increased noise from the switch pair M2 and M3, as well as the need to reduce the load resistance to avoid a larger voltage drop over the resistors M2 and M3 that could affect in which active mode the transistors operate. Reducing the load resistance does however reduce the gain which means simply increasing the bias current of the driving stage is not an efficient way to improve the overall performance.

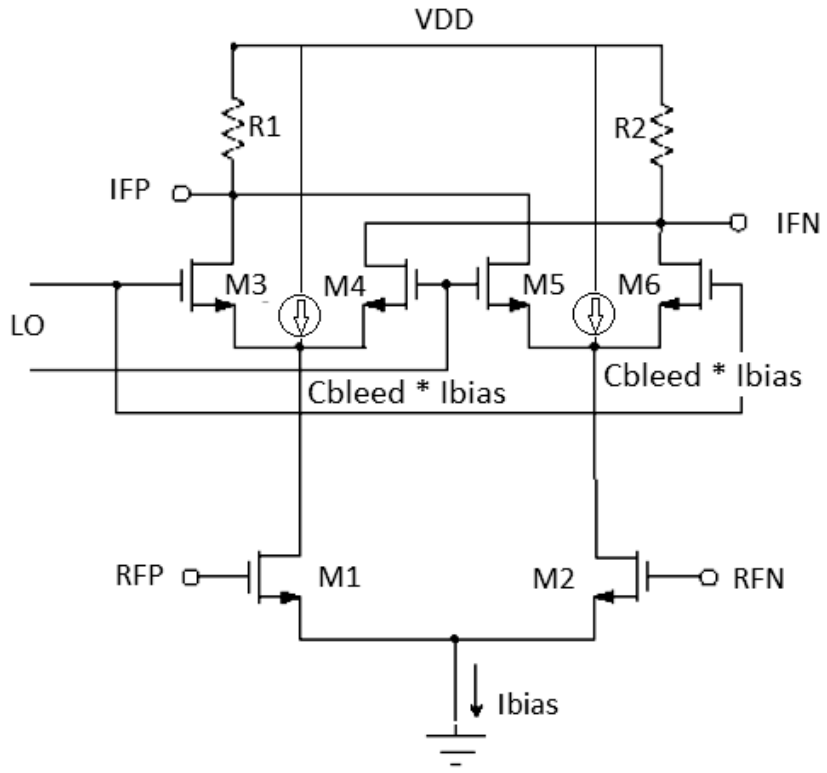

Figure 14: A double balanced gilbert cell with a current source in parallel to the switching pairs used as current bleeding.

This is where the current bleeding [6] technique applies, as it allows for an increase of the current over the bias stage by applying a current source in parallel to the M2-M3 switches and therefore increasing the gain and IP3 without degrading the other parameters as shown in figure 14. Another advantage is that this method allows M2-M3 to operate at a lower voltage leading to a higher efficiency when switching the stage on and off. The lower voltage also allows the utilizing of a smaller and more compact structure, saving space for the mixer.

Another way to implement the current bleeding is by adding two new resistors, R3 and R4, as shown in figure 15. This model allows a smaller part of the current to go through the LO transistors, reducing the requirements of the R_{load}. If, for instance, 75% of the current passes through R3 and R4 instead, the resistance on R_{load} can be increased up to fourfold while maintaining the same voltage drop over the resistors as in the example where no current bleeding is applied, which should result in an increased gain of the mixer [10].

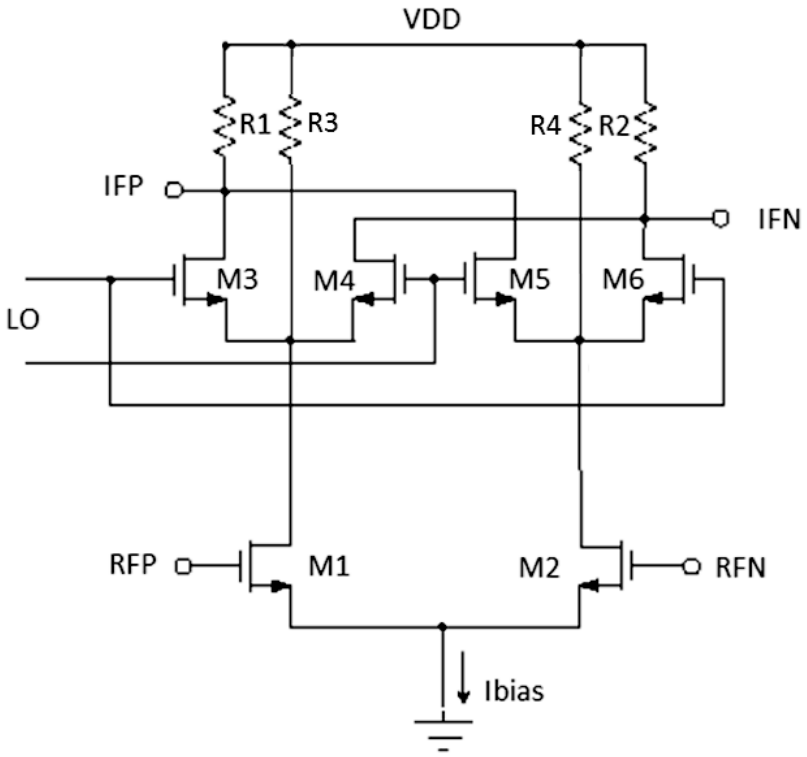

Figure 15: A double balanced gilbert cell with two resistors added, R3 and R4, in parallel to the switching pairs functioning as current bleeding

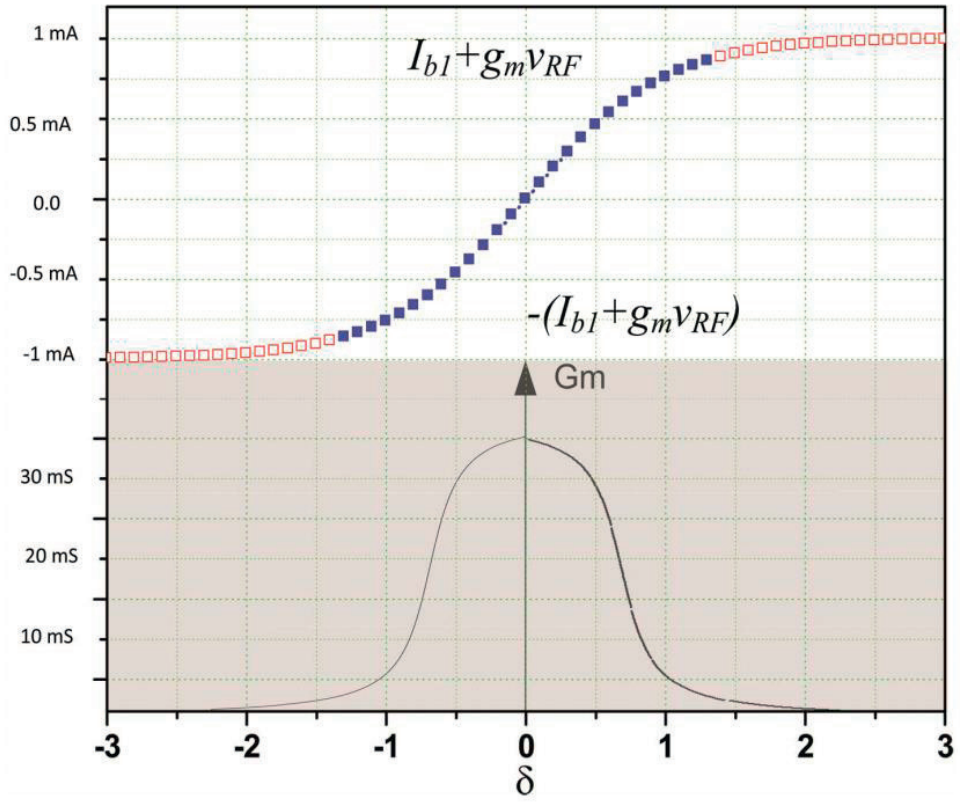

Figure 16 shows the I-V characteristics of M2-M3 with δ = vLO/Vod used as an example in the paper by Wah Ching Lee et al [6].

The G_m showed in figure 16 is given by:

$$G_m\ (V_{LO}) = 2\frac{G_{m2}(V_{LO}) * G_{m3}(V_{LO})}{G_{m2}(V_{LO}) + G_{m3}(V_{LO})} \tag{8}$$

Equation (8) shows that G_m depends on V_{LO}, this dependency is showed in (9) where G_m is derived as a function of V_{LO}:

$$G_m\ (V_{LO}) = 2I_{D1}\sqrt{\frac{1}{V_{LO}^2 + \frac{2I_{D1}}{K}}} \tag{9}$$

This formula and Figure 16 both show that $G_m\ (V_{LO})$ reaches its maximum value when V_{LO} approaches zero as well as how G_m approaches zero as V_{LO} increases.

An important parameter that is affected by the change of G_m is the noise. The noise power spectral density (PSD), a frequency dependent measurement of the noise power per bandwidth. The PSD when both transistors are at the "on" state according to the noise models used in [7] and [8] equals:

$$PSD = 8KT\gamma G_m = 16KT\gamma \left(\frac{G_{m2} * G_{m3}}{G_{m2} + G_{m3}}\right) \quad (10)$$

In which K is Boltzmann's constant, T the absolute temperature and γ the noise coefficient.

At the zero state of V_{LO} the G_m reaches its maximum as shown in equation (8) and figure 16, both M2 and M3 are in the "on" state resulting in non-zero values for G_{m2} and G_{m3} resulting in a high noise according to (10). Another interesting aspect illustrated in (9) combined with (8) is how a high V_{LO} swing will render either G_{m2} or G_{m3} close to zero resulting in a suppression of the noise from M2-M3. Noise PSD can also show the contribution of noise as a function of the Bias current [10]:

$$PSD = \frac{16KT\gamma}{\pi}\frac{I_B}{V_{LO}} \quad (11)$$

Where I_B is the bias current of M2-M3. (11) shows that increasing V_{LO} leads to suppressed noise PSD, as well as how reduced I_B also leads to reduced noise, which verifies that the principle behind current bleeding is relevant in this case. Another important parameter of the mixer is the gain. The conversion gain (CG) of the mixer is given by:

$$CG = c * g_{m1} * re\{Z_L\} \quad (12)$$

Where the multiplier c is given by:

$$c \approx \frac{2}{\pi}\left(\frac{\sin(\pi\Delta / T_{LO})}{\pi\Delta / T_{LO}}\right) \quad (13)$$

Where Δ is the switching interval when both transistors are in the "on" state, equation (12) shows that the best alternative to increase CG is to increase c and/or g_{m1}.

Adding the current bleeding to the mixer design has shown great promise in a previous study by Wah Ching Lee et al [6] when combined with active load.

However, when current bleeding alone was investigated previously in the thesis [1], that this project is built on, the result was inconclusive.

2.3 Active Load

In a similar way to current bleeding, the active load [9] is another alternative to overcome the limits of the classic double Gilbert cell.
The active load adds extra noise and increases the noise figure of the mixer. It also requires a stable bias to keep the load impedance as close to constant as possible, this can be challenging with process, voltage and temperature variations.

A PMOS transistor is used as load because of the lower flicker noise with the PMOS than with a comparable NMOS transistor [9]. The output resistance of the PMOS transistor is set by the gate bias. The active load could receive its own power from an adjustable circuit delivering the gate bias voltage V_{B2} as shown in figure 17, or from the mixer circuit itself. The headroom for the active load is VDS_{min} which depends on how the V_{B2} is tuned. The change to the active load does not remove the upper size limit of the resistive loads' size:

$$R_{Load} = \frac{2(VDD - 3VDS_{sat})}{I_{Bias}} \quad (14)$$

Where I_{Bias} is the tail current of the mixer core. This limit can be lifted combining the active load with a current bleeding approach.

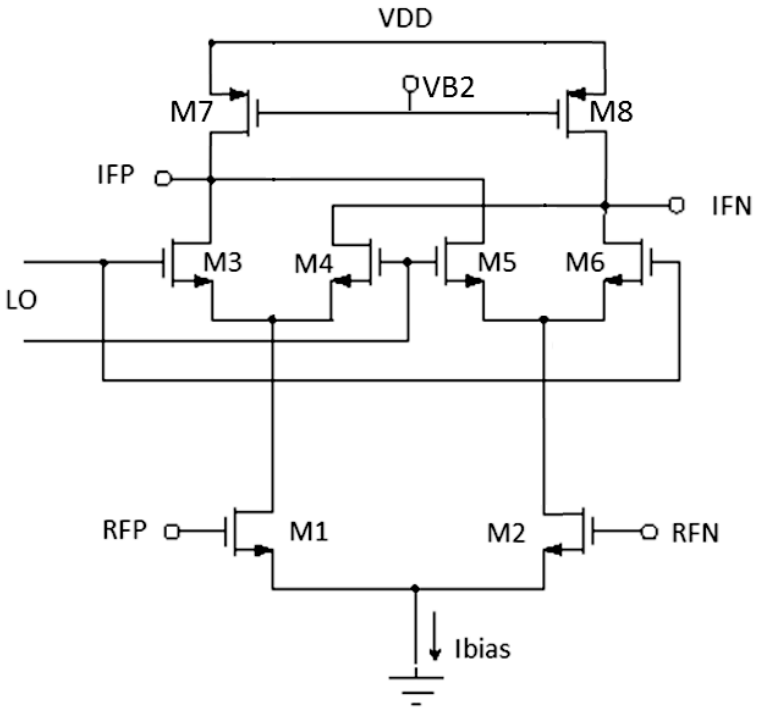

Figure 17: This figure shows a double balanced gilbert cell with active load, M7 and M8, represents a pair of PMOS transistors that are biased by V_{B2}.

The effect of active load was inconclusive in the study by Roghoyeh Salmeh [9], this study however indicates that a big performance increase of the mixer is possible to achieve when combining the two techniques of current bleeding and active load as illustrated in figure 18.

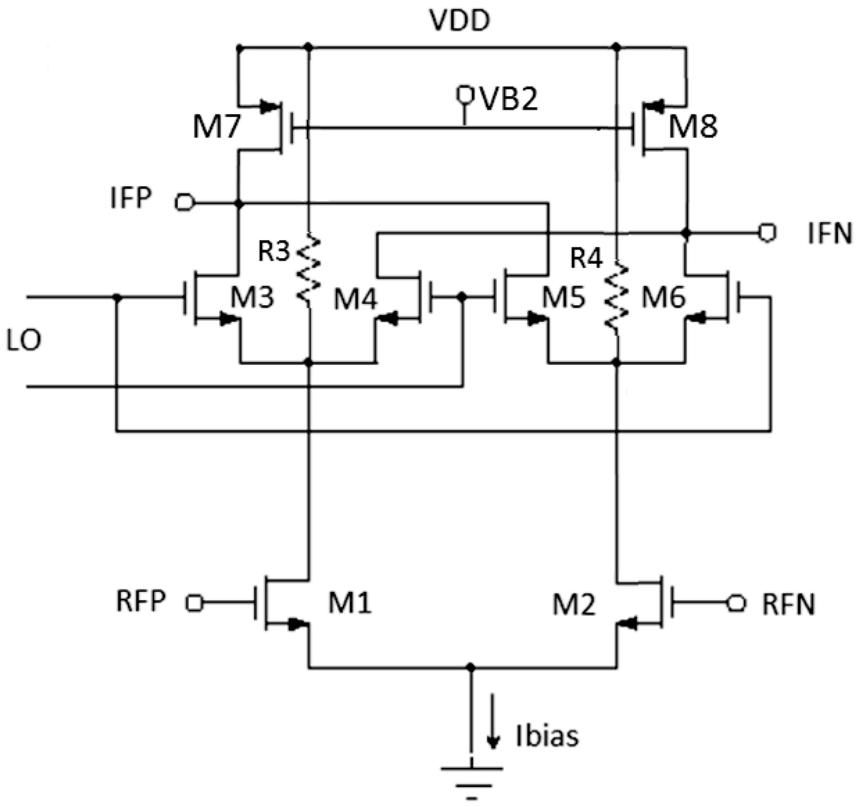

Figure 18: This figure shows a double balanced gilbert cell with active load combined with the two added resistors as shown in the current bleeding version in figure 15.

CHAPTER 3

3 Method

3.1 Transistor model

The project outline included an updated NMOS model similar to the model used in the previous project [1], to better match the improvements that EIT have achieved with their Nanowire transistors since 2013. As shown in the results (4.1), further comparison between the real transistors and the old model shows that the data for the old model fits the real transistors very well. Therefore, an updated NMOS transistor model is not relevant for the project and the use of the old model is adequate.

3.2 PMOS model

The active load used in this thesis is based on PMOS transistors. To find a relevant working PMOS transistor model, the project started with studying the existing NMOS model and comparing what parameters differ between PMOS and NMOS in the real Nanowire transistors. The most notable differences were the change of material from indium arsenide (InAs) to gallium antimonide (GaSb) that are used in the PMOS nanowire transistors fabricated at EIT, as well as the change from electrons to holes as carriers in the transistor.

The first tested PMOS model simply changed the mobility of the NMOS model from 0.135 $cm^2/(V \cdot s)$ to 0.0135 $cm^2/(V \cdot s)$ or 0.0400 $cm^2/(V \cdot s)$ to match the mobility of the holes in a GaSb NWs for the two cases, current data and realistically reachable values of electron mobility (μ). Another important aspect was to update the PMOS transistor model to handle positive carriers instead of electrons by making the gate respond to a negative V_{GS}.

3.3 Implementation active load

The goal was to use the active load PMOS transistors as active components that respond to the changes in the circuit. Therefore, the active load was implemented (as described in 2.4), biased from the circuit without using an external source for gate voltage (since an external source would increase the complexity of the mixer and add the need of another contact on the mixer). The final model of the mixer with active load is shown in the appendix A.1.

3.4 Adding current bleeding

The current bleeding is added to two mixers, both the standard gilbert cell mixer and the mixer with active load. The current bleeding is implemented in the same way as shown in figure 14 with a current source in parallel with the switching pair, and where the total current bleed is set as a fraction of the tail current.

3.5 Simulation layout

The workflow for the simulations starts by verifying that the reference mixer A [1] behaves as expected. It also includes getting the full data necessary for fine-tuning the parameters for the new mixers.

The next step is to continue with Mixer B that will act as a reference passive mixer, which incorporates current bleeding. Mixer C is based on active load in the form of a PMOS transistor instead of a resistor. The last step is mixer D, where mixer B and C are combined, to see if current bleeding can improve the mixer with active load, as the study in [9] shows that current bleeding might be a useful addition when using active load.

Finally, the goal is to see if any of the new designs are an improvement over the traditional double balanced gilbert cell (mixer A) used as reference.

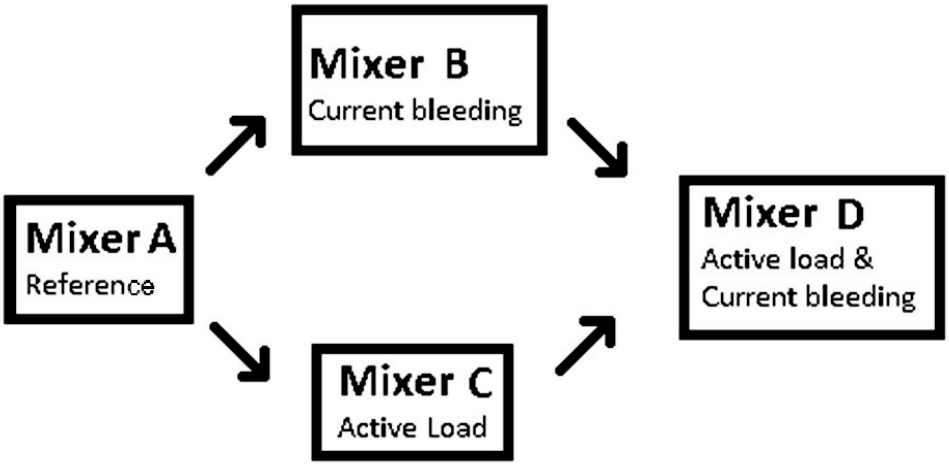

Figure 19: An illustration of the workflow from Mixer A to D via B and C.

CHAPTER 4

4 Results

4.1 NMOS transistor model

The first part of the study was a comparison between an actual nanowire transistor (Figure 20) physically measured at EIT and the NMOS NWFET transistor model used for simulations [1] (Figure 21). The VerilogA data for the NMOS transistor is shown in A.2 in the appendix.

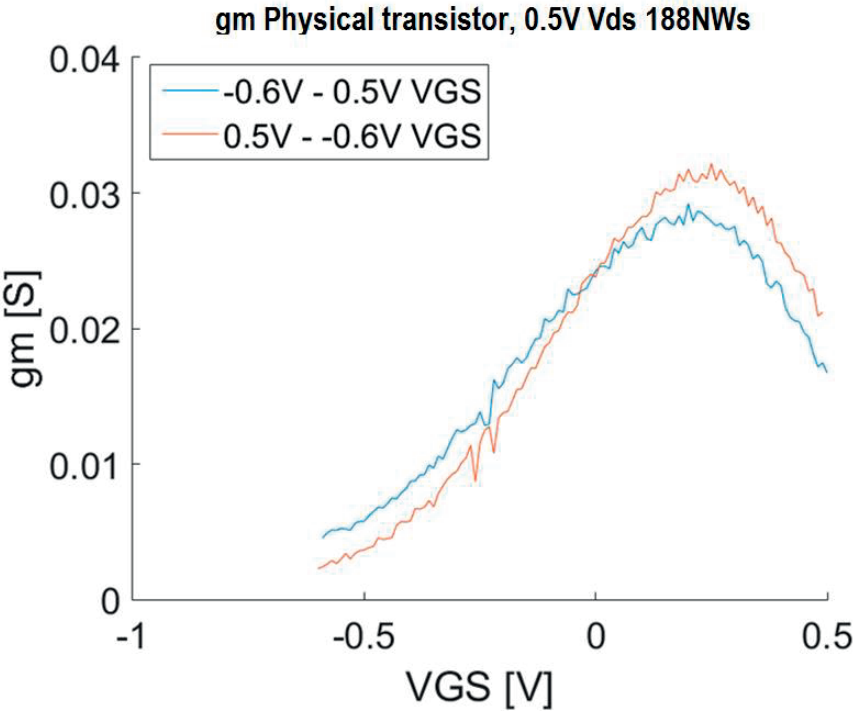

Figure 20: The gm as a function of V_{gs}, with V_{gs} swept over the voltage range starting from both the positive and negative side of the voltage spectrum illustrating the effect of the transistors getting charged during the test.

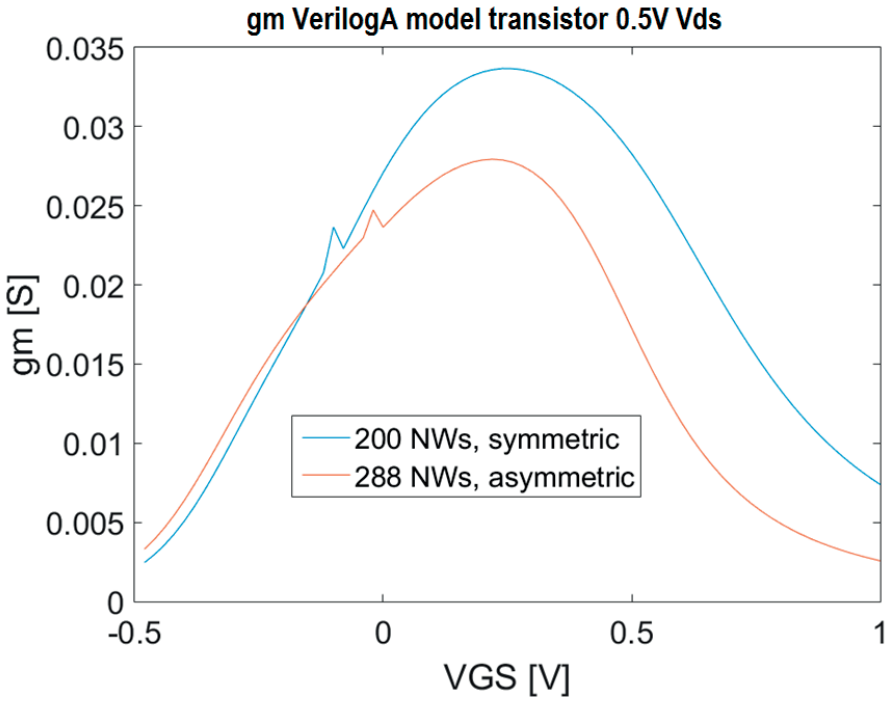

Figure 21: The gm as a function of V_{GS} for the simulated transistor in two configurations showing the advantage of a symmetric design explained in [1].

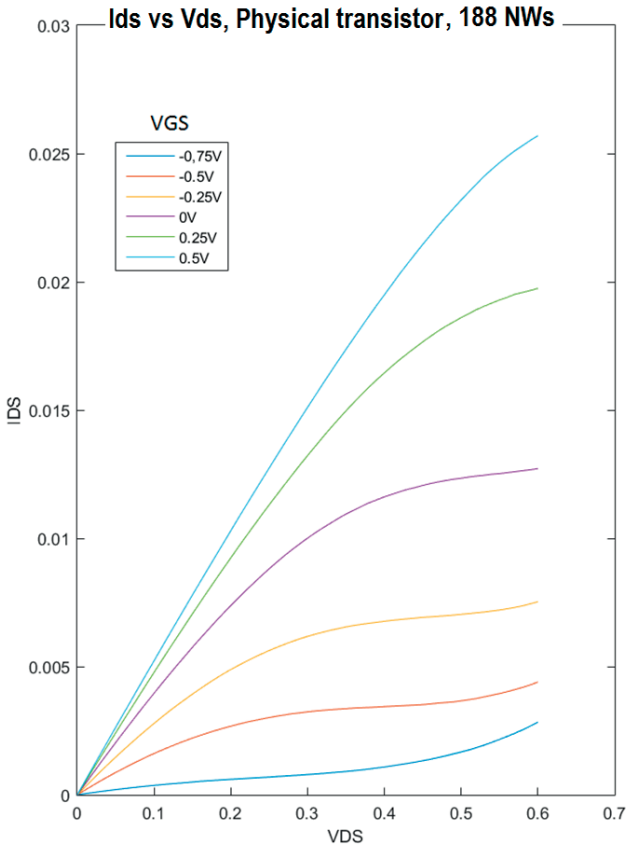

Figure 22: I_{ds} vs Vds curves for different V_{gs} for the real physical transistor.

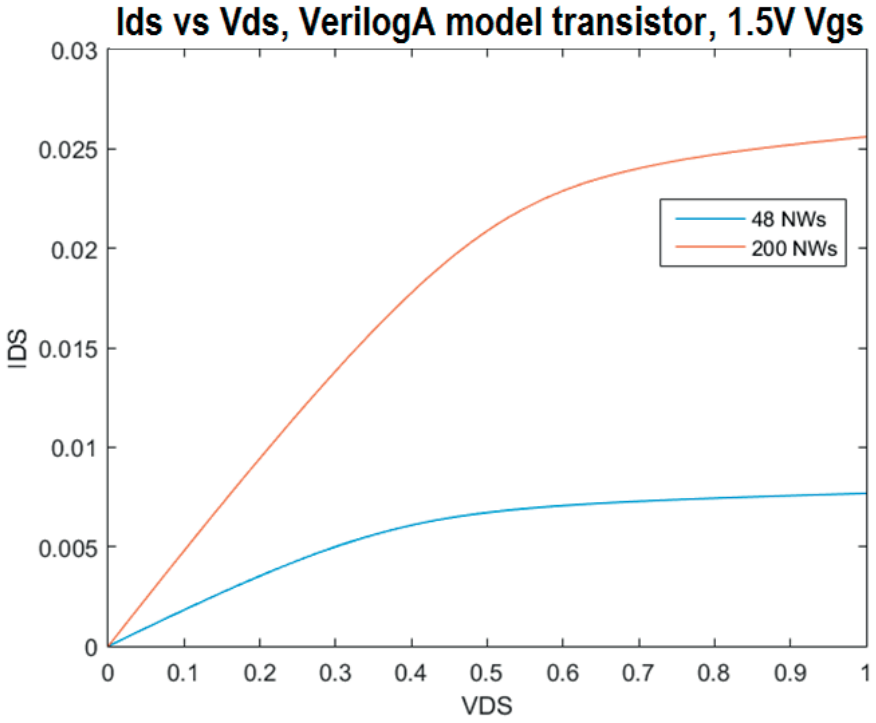

Figure 23: I_{DS} vs V_{ds} curves for 1.5V V_{gs} for the transistor model with 48 and 200 NWs in a symmetrical configuration.

The gm curves shown in figure 20 and 21 as well as the Ids vs Vds curves in figure 22 and 23 show that the transistor model corresponds well with the physical transistor. Therefore, no updated model is required.

4.2 PMOS transistor model

The simulated data for the PMOS model is based on the NMOS transistor model used in 4.1. The PMOS model is setup in two versions, one based on the current data from EIT with a my value of 0.0135 $cm^2/(V \cdot s)$ (which is one tenths of the my value of the NMOS transistor). The other version uses a higher my value of 0.0400 $cm^2/(V \cdot s)$ that is assumed to be the highest

realistically achievable value of my. The VerilogA data for the PMOS transistor is presented in A.2 in the appendix.

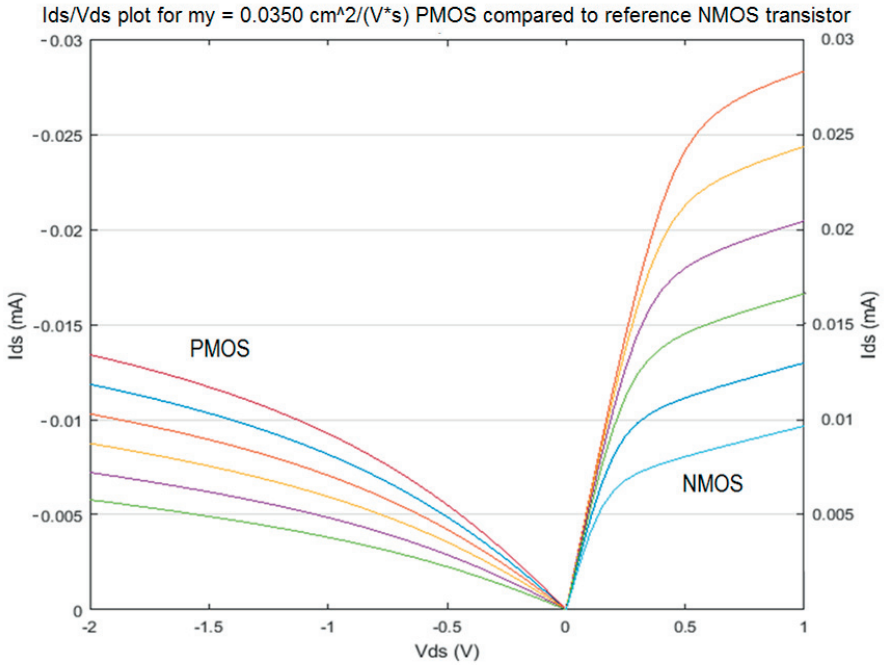

Figure 24: An I_{DS}/VDS plot for the 0.0135 $cm^2/(V \cdot s)$ PMOS transistor compared to the 200 NWs NMOS transistor used as reference. Notice the change of sign for the Ids of the PMOS compared to the NMOS.

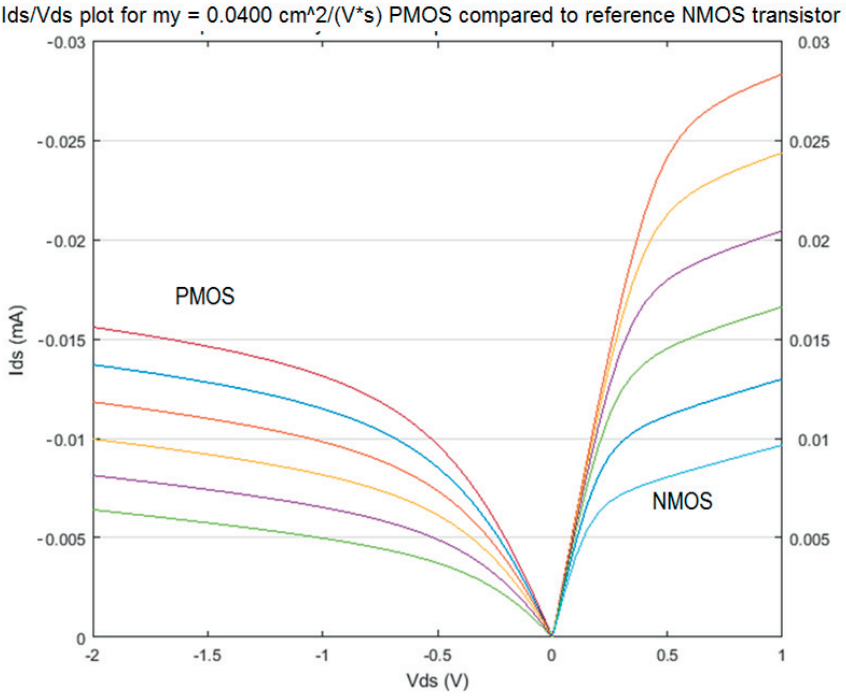

Figure 25: An I_{DS}/VDS plot for the 0.0400 $cm^2/(V \cdot s)$ PMOS transistor compared to the 200NWs NMOS transistor used as reference. Notice the change of sign for the Ids of the PMOS compared to the NMOS.

4.3 Double balanced gilbert cell (Mixer A)

The aim of this study is to improve the normal double balanced gilbert cell mixer based on NW transistors. Here, we first present the settings used and the results achieved for mixer A, which the following mixers will be compared with. All the following mixer simulations were performed with the mixer test bench found in appendix A.1 and with a RF frequency of 59-64 GHz. The test was performed by sweeping the V_{DD}, the R_L and the I_{tail} to find the maximum performance of the mixer. The final parameters used for mixer A were as follows:

$V_{DD} = 1.5$ V
$R_L = 270$ k
$n_{NW} = 288$ (17·17)
$I_{tail} = 5.8$ mA

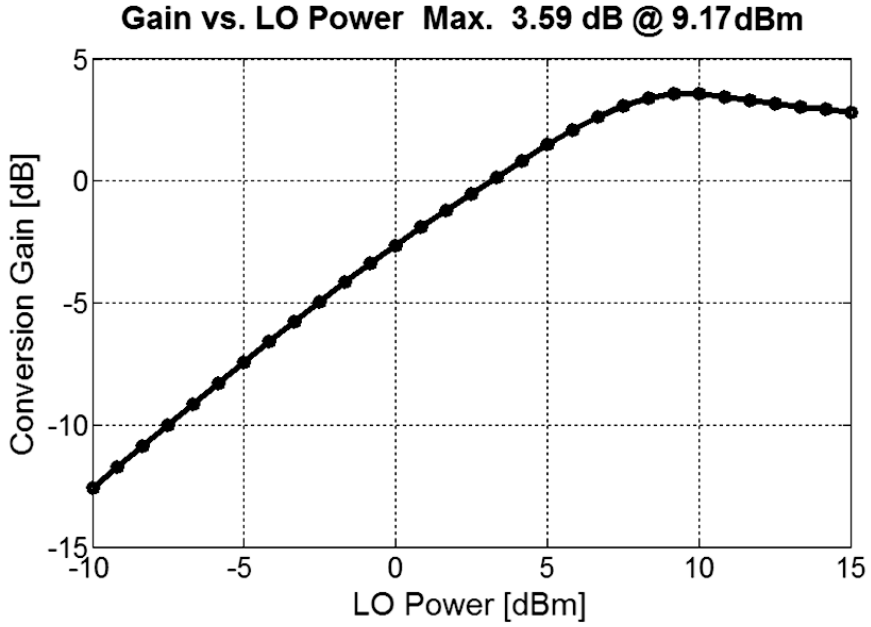

Figure 26: The conversion gain as a function of LO power reaching its maximum value of 3.59 dB for a LO power of 9.17 dBm.

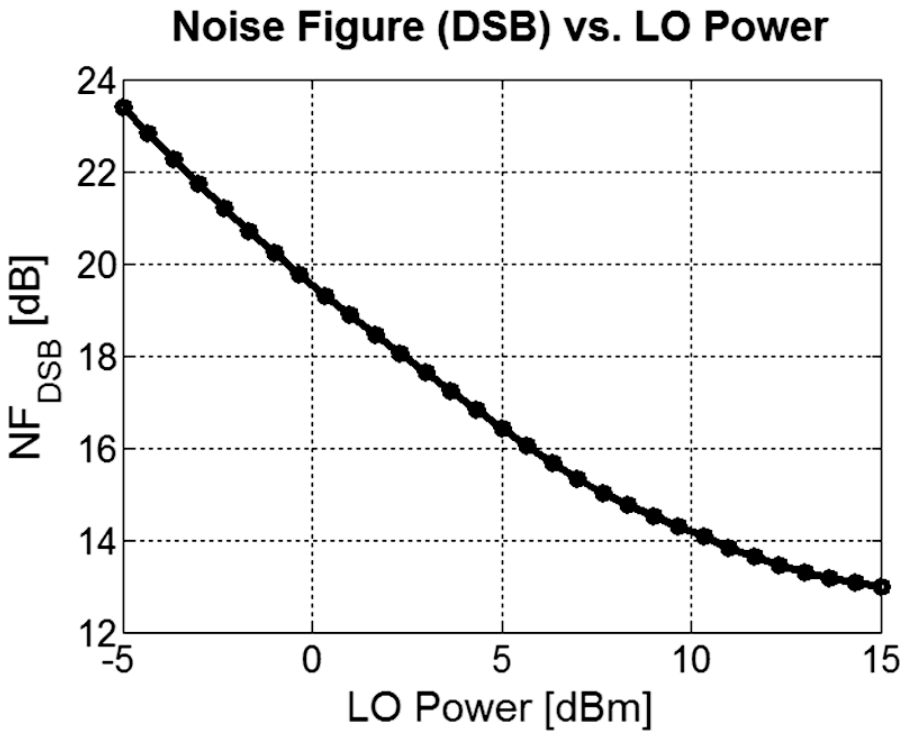

Figure 27: The Noise figure for Mixer A, with a value of 14.3 dB at 9.17 dBm LO Power.

Parameter	Achieved values
Conversion Gain [dB]	3.59
Noise Figure 100MHz IF [dB]	14.3
Power_Consumption [mW]	8.7
1dB Compression Point [dBm]	0.48506
IIP3 [dBm]	10.9565
OIP3 [dBm]	12.3288
LO_to_IF [dB]	-51.63
LO to RF [dB]	-68.63

Table 1: A summary of the data obtained with the double balanced gilbert cell mixer (Mixer A) used as reference in this project.

4.4 Double balanced gilbert cell with current bleeding (Mixer B)

The test with mixer B was performed to determine how current bleeding alone affected the double balanced gilbert cell based on NW transistors. As in the case with mixer A the following parameters were swiped; the V_{DD}, the R_L and the I_{tail}. We also tested how the mixer reacted to different values of current bleeding ranging from zero to 50% of the I_{tail} value. The following design parameters where used for the final Mixer B:

$$V_{DD} = 1.5\ V$$
$$R_L = 270$$
$$n_{NW} = 288\ (17 \cdot 17)$$
$$Itail = 5.8\ mA$$
$$C_{bleed} = 10\%$$

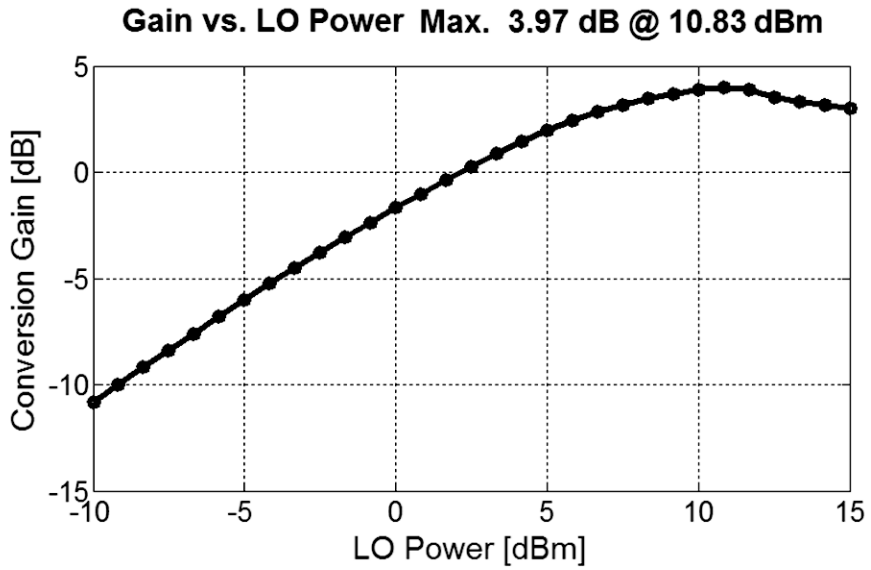

Figure 28: The conversion gain as a function of LO power reaching its maximum value of 3.97 dB at a LO power of 10.83 dBm, with current bleeding set at 10% of the tail current.

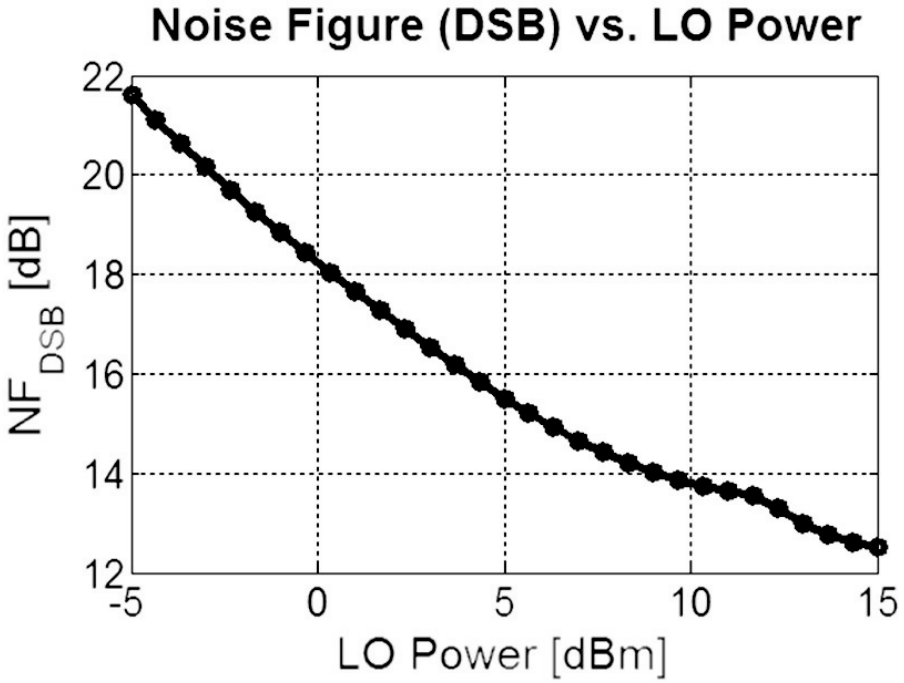

Figure 29: The Noise figure for the current bleeding mixer, with a value of 13.6 dB at 10.83 dBm LO Power.

Parameter	Mixer A	Mixer B
Conversion Gain [dB]	3.59	3.97
Noise Figure 100MHz IF [dB]	14.3	13.6
Power_Consumption [mW]	8.7	8.7
1dB Compression Point [dBm]	0.48506	0.17909
IIP3 [dBm]	10.9565	9.8257
OIP3 [dBm]	12.3288	11.6061
LO_to_IF [dB]	-51.63	-51.87
LO to RF [dB]	-68.63	-69.31

Table 2: Comparison between the reference double balanced gilbert cell and the current bleeding mixer.

4.5 Double balanced gilbert cell with active load (Mixer C)

Mixer C applies active load based on PMOS transistors instead of the resistors normally used as load in the double balanced gilbert cell (Mixer A). The load transistors receive their gate voltage from the circuit on the drain side of the PMOS to achieve an active function of the load. The parameters swiped for mixer C were the V_{DD} and I_{tail}.
The following design parameters where used for the results with mixer C:

$$VDD = 1.5\ V$$
$$n_{NW} = 288\ (17 \cdot 17)$$
$$I_{tail} = 20\ mA$$

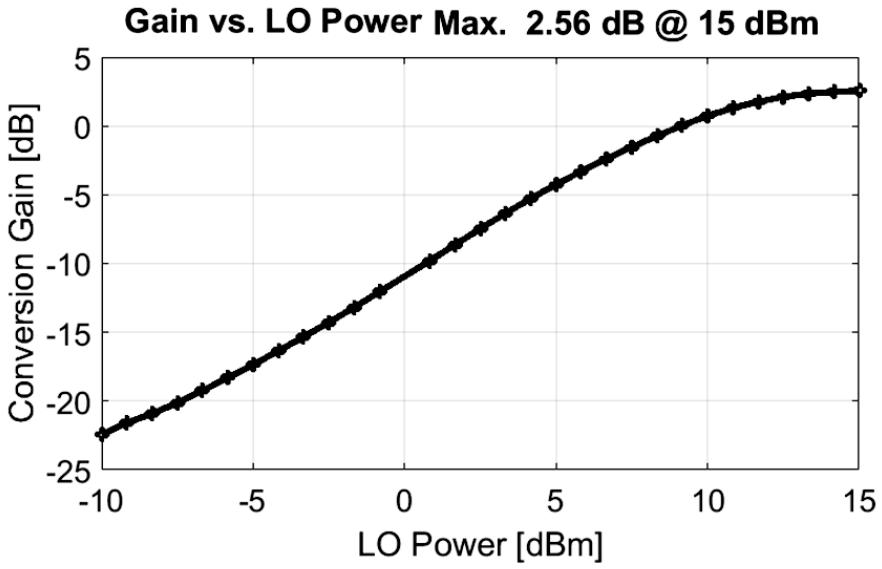

Figure 30: The conversion gain as a function of LO power reaching its maximum value of 2.56 dB at 15dBm LO power, with PMOS transistors used as active load.

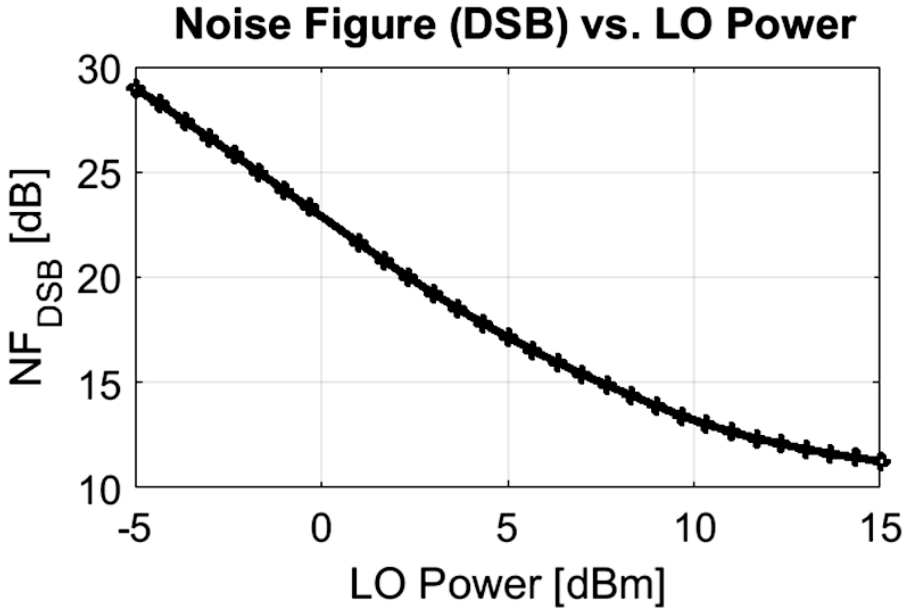

Figure 31: The Noise figure for the active load mixer, with a value of 11.2 dB at 15 dBm LO Power.

4.6 Double balanced gilbert cell with active load and current bleeding (Mixer D)

The final mixer in this project integrated both active load and current bleeding in the same circuit. The problem from mixer C, where a higher I_{tail} value was required to stabilize the mixer, also affected mixer D. Therefore, we decided to aim for the highest possible mixer performance accepting a higher power consumption than the reference mixer.
The parameters swept for mixer D were as follows: V_{DD}, I_{tail}, % current bleeding. In addition, different component parameters for the PMOS were also tested; this included my, carrier injection velocity, $R_{ds,}$ and alpha/beta values.

The following design parameters where used for Mixer D:

VDD = 1.5 V
n_{NW} = 288 (17·17)
I_{tail} = 27 mA
Vinj = 0.400e5 m/s
my = 0.0135 $cm^2/(V \cdot s)$
alpha = 3.5
beta = 1.4
pRds = 24e4 Ω
C_{bleed} = 20%

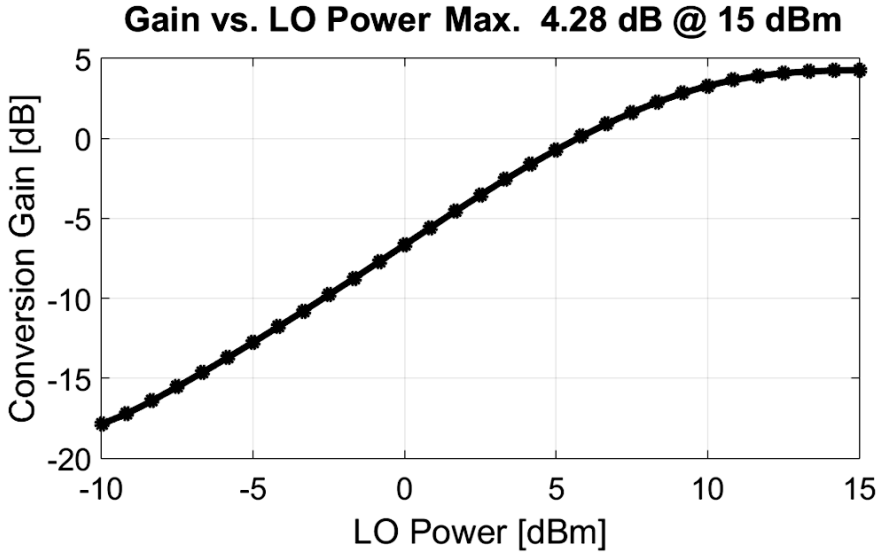

Figure 32: The conversion gain as a function of LO power reaching its maximum value of 4.28 dB at 15dBm LO power, achieved with current bleeding active set at 20% of the tail current.

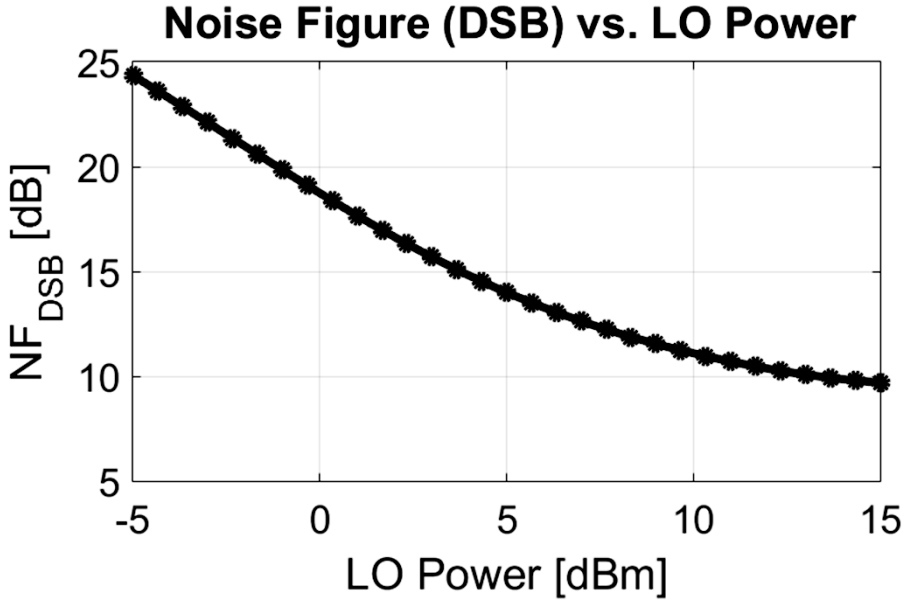

Figure 33: The Noise figure for the active load with current bleeding mixer, with a value of 9.7 dB at 15 dBm LO Power.

Parameter	Mixer A	Mixer B	Mixer C	Mixer D
Conversion Gain [dB]	3.59	3.97	2.56	4.28
Noise Figure 100MHz IF [dB]	14.3	13.6	11.2	9.7
Power_Consumption [mW]	8.7	8.7	30	40
1dB Compression Point [dBm]	0.485	0.179	0.376	0.170
IIP3 [dBm]	10.9565	9.8257	25.92	16.38
OIP3 [dBm]	12.3288	11.6061	24.09	17.65
LO_to_IF [dB]	-51.63	-51.87	-45.73	-43.47
LO to RF [dB]	-68.63	-69.31	-58.94	-61.68

Table 3: A summary of the four different mixers analysed in this project.

Parameter	Mixer D	[20]	[21]	[22]
Conversion Gain [dB]	4.28	15.46	24.6	16
NF 100MHz IF [dB]	9.7	12.8	5.6	7
Power [mW]	40	17	34.4	60
1dB Compression Point [dBm]	0.170	-25	-33	-21
IIP3 [dBm]	16.38	-12	-23.3	
OIP3 [dBm]	17.65			
LO_to_IF [dB]	-43.47	-51.5	>41.9	
LO to RF [dB]	-61.68	-64.7	>-55.9	>-90

Table 3: A table with data of mixer D compared to other 60 GHz mixers from previous published reports.

CHAPTER 5

5 Discussion

The effect when comparing the normal passive double gilbert mixer with the active load mixer combined with the current bleeding technique based on PMOS technology is a performance increase in all aspects as shown in table 3. The gain has increased from 3.59 to 4.28 dB which is a small but useful difference as higher gain is always seen as an advantage. At the same time the noise figure decreased from 14.3 to 9.7 dB, this a quite large change and it actively reduces the risk of noise related problems in the circuit.

Both the IIP3 and the OIP3 also increased substantially in Mixer D compared to the reference mixer A while not reaching the extreme levels of mixer C. This means that the mixer is much more linear in its behavior then the reference mixer. While the reference mixer already has a high level of linearity, even higher linearity can still be a great advantage depending on the application.
The same thing applies to LO to IF port isolation and LO to RF port isolation, they are lower than in the reference case but still at a very high level due to the double balanced gilbert cell design, thereby the decrease is of no concern.

The effect on the 1dB compression point in this study is a massive reduction from 0.485 dBm in mixer A to 0.170 dBm in mixer D. This is a problem related to the current bleeding used, as mixer D responded like mixer B where current bleeding made the sample more vulnerable to higher input powers. Current bleeding is however necessary for good performance when using active load as mixer C shows in table 3.

The greatest disadvantage in this study, depending on the usage of the mixer, is the power consumption. It increases from 8.7 mW in the reference mixer A to 30 mW for mixer C with active load added, and even further to 40 mW in mixer D which combines active load with current bleeding. This was unexpected as no such results were presented in the paper by Salmeh [9] which also focused on combining active load with current bleeding. The power consumption is based on the voltage over and the current through the mixer. The higher required tail current from the current source in the tail of

the mixers in the active load mixers compared to the reference mixer results in this increase of power consumption.

Another interesting aspect concerning the active load mixers from a production perspective, is that the PMOS transistor is more exposed to variations in the component than the resistor as it is more complex to produce. The mixer including PMOS transistors is also more sensitive to variations in the transistor parameters as the effects on the mixer from small changes in transistor parameters are a lot larger than the variations that comes from the resistor.

Limitations to this study

This study is pure simulation work with no actual component being built and tested in reality, even if the model is based on existing components developed and tested by the group of EIT at Lund University. The model for the PMOS has some noteworthy limitations as it is based on a reversed NMOS transistor model. The material parameters for the model are tuned to match the real PMOS transistors and its IV-curve well, but there are other parameters that could receive some attention, in this case mainly the capacitances within the transistor as they are still setup as in a NMOS transistor.

In this study the optimal value for tail current was found to be around 27mW for mixer D, another interesting idea for future research would be to limit this tail current to a lower setting that would better match the power consumption of mixer A and try to find the maximum performance achievable for mixer D with those restrictions. Instead of searching for a maximum conversion gain while maintaining good noise levels and linearity, the idea would be to find a setting with maximum performance at a lower current level.

One parameter that was not investigated in this project but that could be of high interest for a future study is to test how the nanowire count in the PMOS compared to the NMOS would affect the circuit, as a change in the number of nanowires in the PMOS transistor would affect the resistance of the transistor as well as the internal capacitances in it.

Conclusions

The conclusion from this study is that the mixer with active load and current bleeding can be a useful component in the right application as in a sensitive

system with high requirements on linearity and a low noise factor, without the extreme requirements of single digit mW power consumption.

6 References

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7 List of Abbreviations

HBTs	Heterojunction Bipolar Transistors.
IF	Intermediate Frequency.
IIP3	Input-referred Third-order Intercept Point.
InAs	Indium Arsenide.
InP	Indium Phosphide.
LNA	Low Noise Amplifier.
LO	Local Oscillator.
MOSFETs	Metal-Oxide Semiconductor Field-Effect Transistors.
NF	Noise Figure.
NR	Noise Ratio.
NW	Nanowire.
NWFETs	Nanowire Field-Effect Transistors.
OCEAN	Open Command Environment for Analysis.
OIP3	Output-referred Third-order Intercept Point.
PAC	Periodic Alternating Current.
Pnoise	Periodic Noise.
PSS	Periodic Steady-State.
PXF	Periodic Transfer Function.
QPAC	Quasi-Periodic Alternating Current.
QPSS	Quasi-Periodic Steady-State.
RF	Radio Frequency.
VCO	Voltage Controlled Oscillator.

Appendix 1

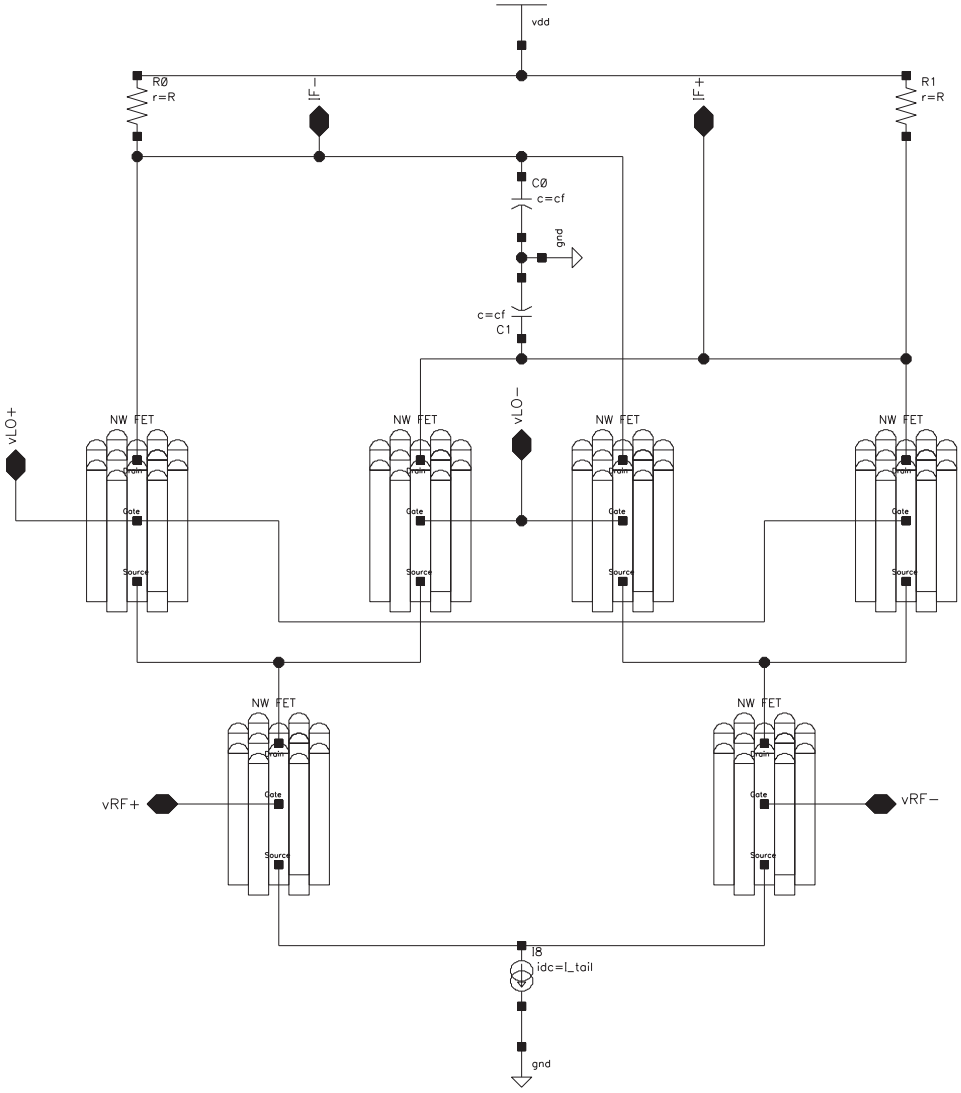
A. Appendix

Some extra information for readers who would like more information

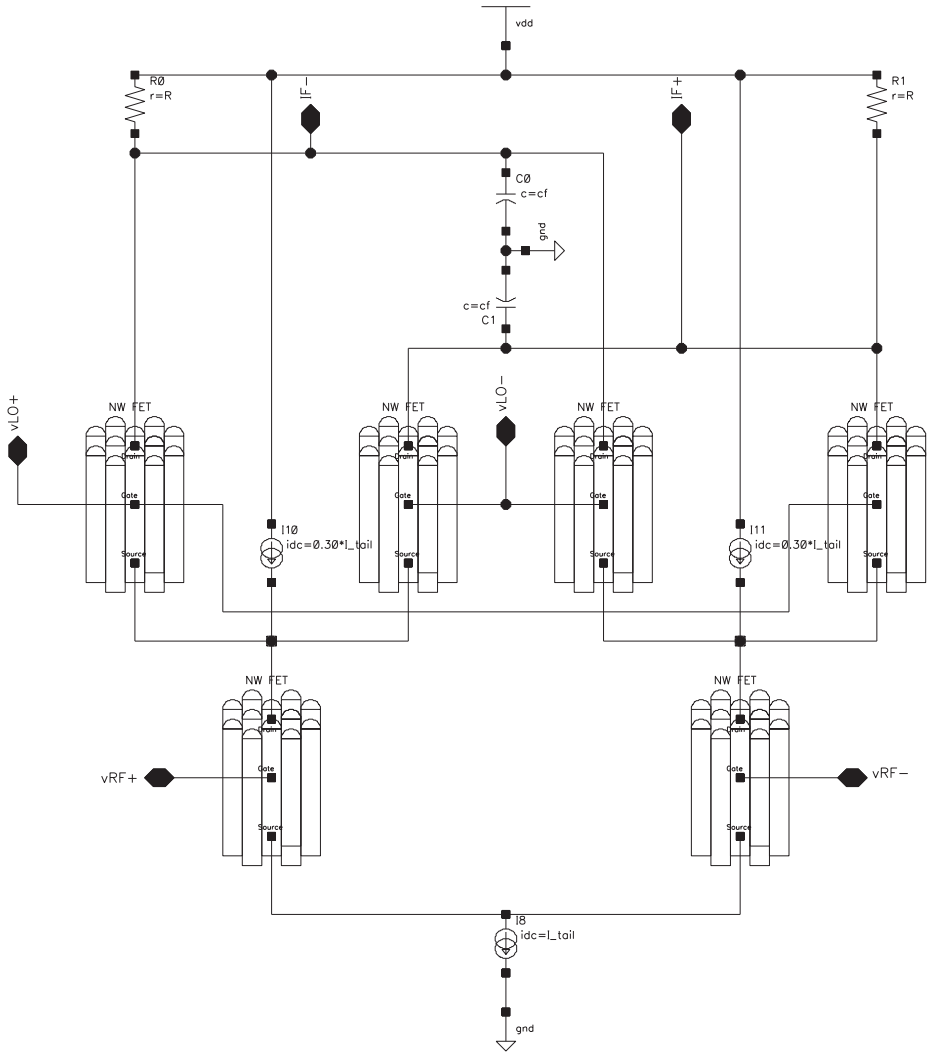
A.1 Schematics
A.2 Code
A.2.1 NMOS NWFET VerilogA.
A.2.2 PMOS NWFET VerilogA.

A.1 Schematics

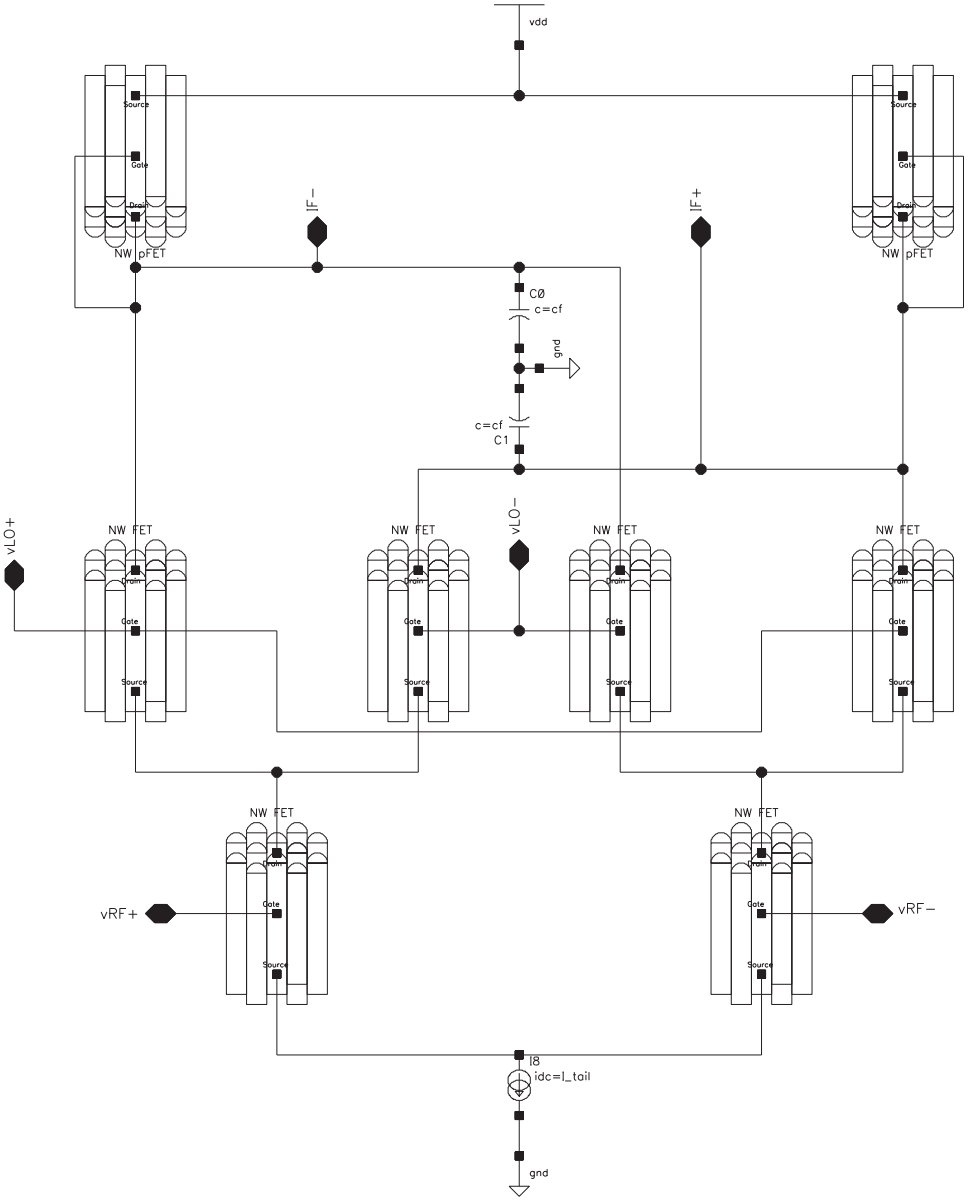
Mixer A (Double Balanced Gilbert cell)



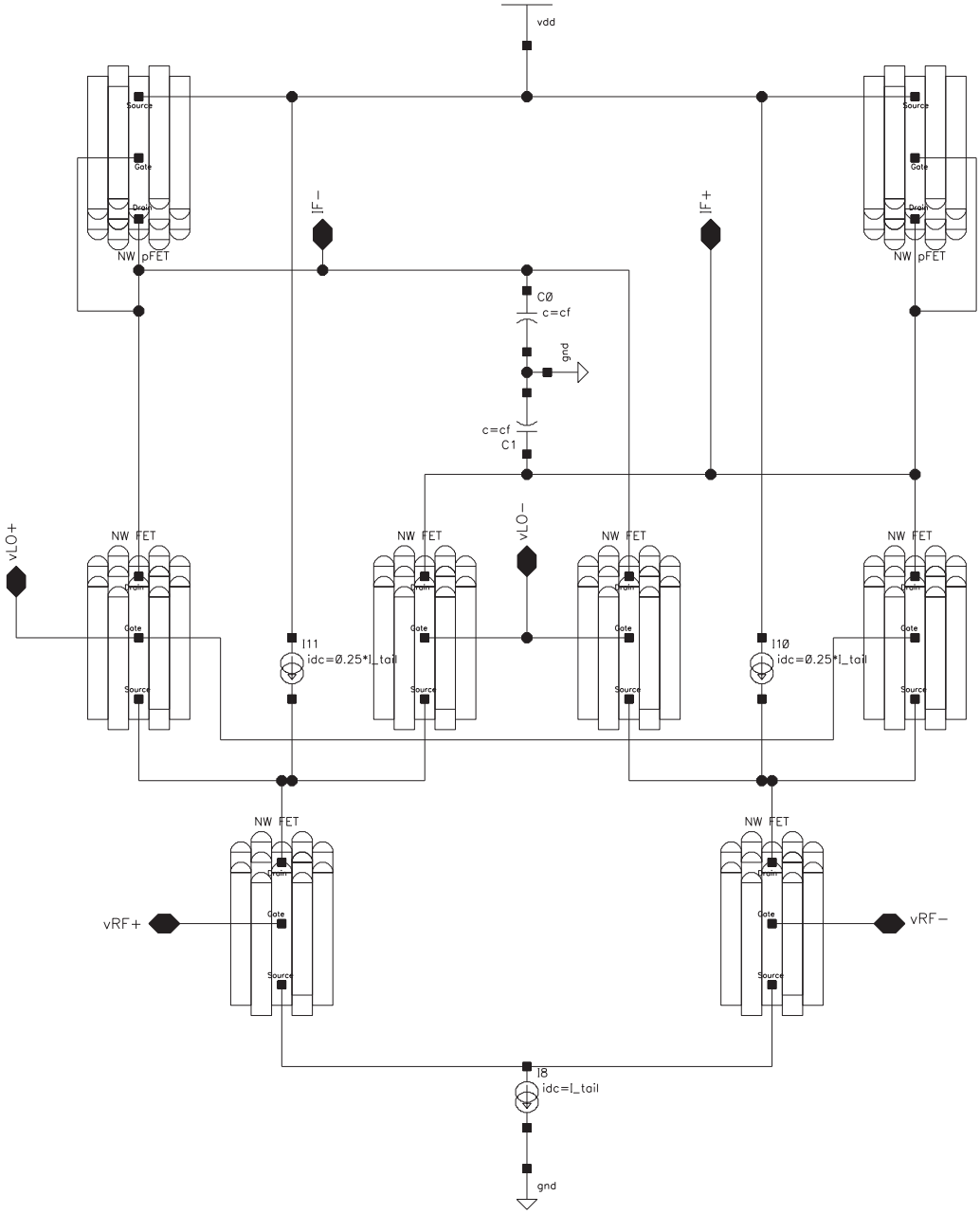
Mixer B (Current Bleeding)



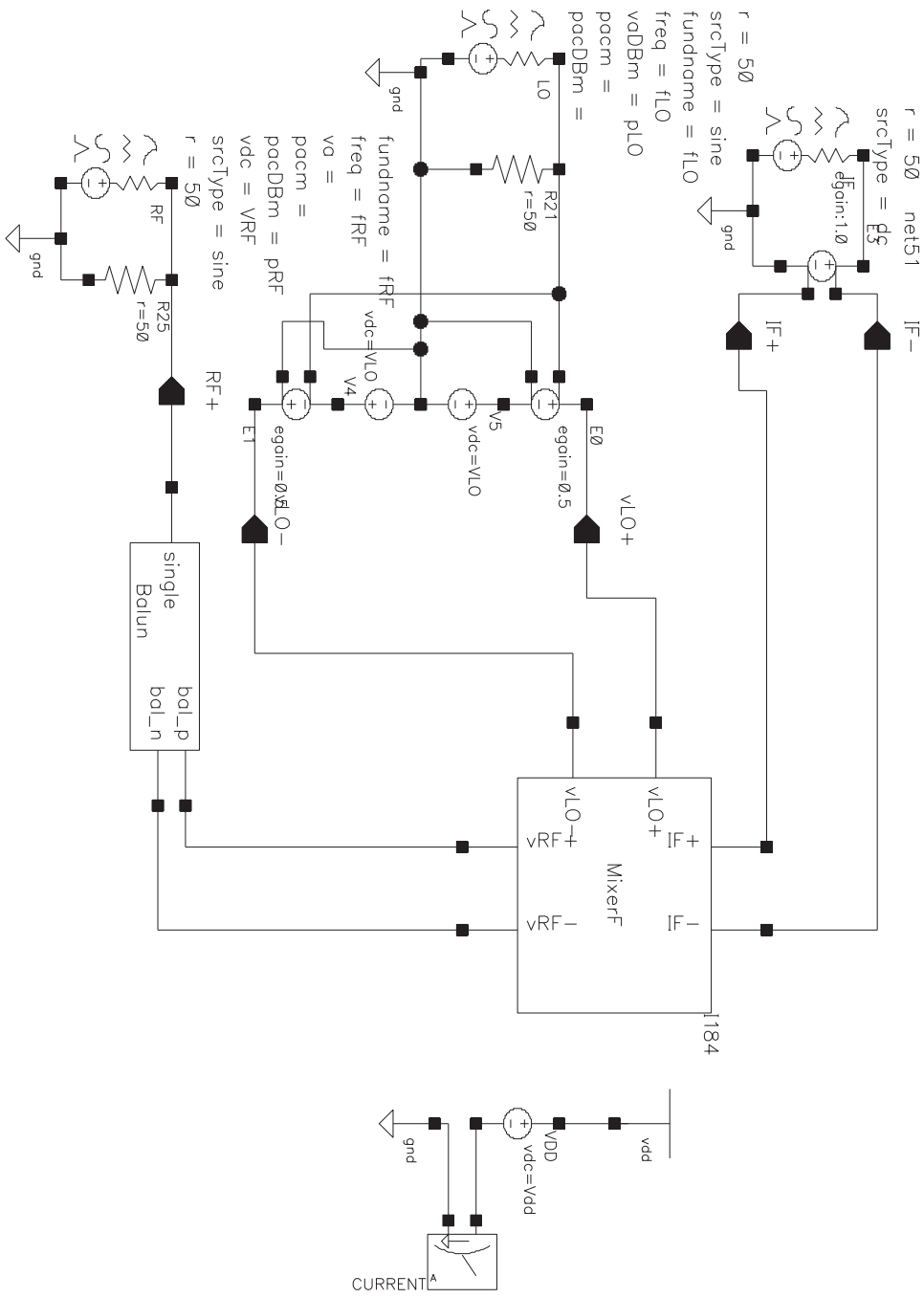
Mixer C (Active Load)



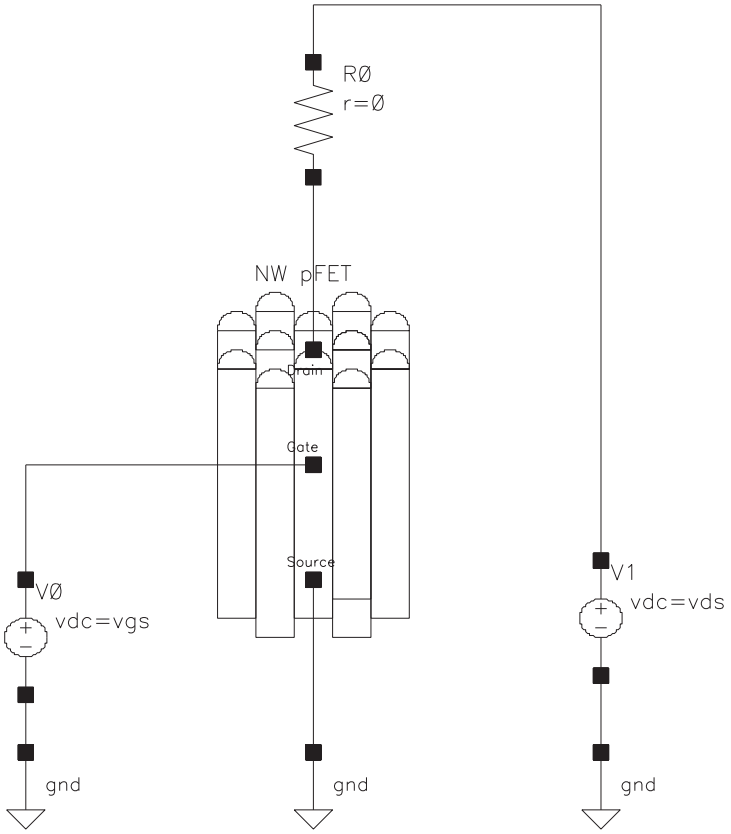
Mixer D (Active load and Current Bleeding)



Mixer Test Bench



Transistor Test bench



A.2 Code

A.2.1 NMOS NWFET VerilogA.

```
// VerilogA for NMOS NWFET, nw_int, veriloga

`include "constants.vams"
`include "disciplines.vams"

module NW_VS_Matrix(g,d,s);
inout g,d,s;
electrical g,d,s;

parameter real pi = 3.141528;
parameter real diam = 45e-9;
parameter real nNW = 192;
parameter real W = nNW*(diam*pi);
parameter real Vt = -0.11;
parameter real DIBL = 0.02;
parameter real tox = 7e-9;
parameter real L = 200e-9;
parameter real epsilon = 8.85e-12;
parameter real eox = 15;
//parameter real Cox =
2*pi*eox*epsilon*L/ln(1+(tox/r))*0.55;
//parameter real Cgg = nNW*Cox;
//parameter real Cinv = Cox/(W*L);
parameter real Wmin = 4.66e-9*eox/14.6;
parameter real Cinv = epsilon*eox/(tox+Wmin);
//parameter real Cmin =
2*pi*epsilon*eox*L/((2*(Wmin+tox)+diam)/diam);
parameter real Vmin = 0.026;
parameter real Vinj = 1.65e5;
parameter real my = 0.135;
parameter real m_elec = 9.1094e-31;
parameter real q = 1.602e-19;
parameter real Vdsats = Vinj*L/my;
parameter real alpha = 3.5;
parameter real beta = 1.8;
parameter real n = 3;
parameter real Rds = 30e3;
parameter real m_star = 0.2;
parameter real gamma = 2;


analog function real Id;
```

```
  input Vgs,Vds;
  real
Vgs,Vds,Vgd,sgn,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,Ids,R
dsv,IdVS;
  begin
            sgn = 1;
         Vg = Vgs;
            if (Vds < 0) begin
                        sgn = -1;
                        Vg = Vgs-Vds;
            end
            Vd = abs(Vds);
            Veff = (Vg-Vt+DIBL*Vd);
            VeffA = Veff+alpha*Vmin/2;
            Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
            VeffB = Veff+alpha*Vmin*Ff;
            Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
            Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
            Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
            Rdsv = Rds/nNW;
            if (Veff < 0) begin
                        Rdsv = (Rds/nNW)*exp(-(Vg-
Vt)/(12*Vmin));
            end
            Ids = Vd/Rdsv;
            IdVS = W*Qix*Vinj*Fs;
            Id = sgn*(IdVS+Ids);
end
endfunction

analog function real Cgs;
  input Vgs,Vds;
  real
Vgs,Vds,sgn,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,m_e,k,k3,
f1,f2,idVg,Cix,Cs,csk,Cfrac,Csmin,Cggmax;
  begin
         Vg = Vgs;
            if (Vds < 0) begin
                        Vg = Vgs-Vds;
            end
            Vd = abs(Vds);
            Veff = (Vg-Vt+DIBL*Vd);
            VeffA = Veff+alpha*Vmin/2;
            Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
            VeffB = Veff+alpha*Vmin*Ff;
            Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
            Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
```

```
           Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
           m_e = m_star*m_elec;
           if (L < 150e-9) begin
                      m_e = (0.05+0.15*(max(20e-9,L)-20e-
9)/(150e-9-20e-9))*m_elec;
           end
           k = 2*q*(Vd+Vmin/2)/(m_e*pow(Vinj,2));
        k3 = asinh(sqrt(k))/sqrt(k)-(sqrt(k+1)-1)/k;
           f1 = VeffB/(n*Vmin);
           f2 = VeffA/(alpha*Vmin);
           idVg = 1/(n*Vmin)*(1-
exp(f2)/pow(1+exp(f2),2))*exp(f1);
           Cix = n*Vmin*idVg/(1+exp(f1));
           Cs = Cix*k3*Cinv*L*W;
           //Cgs = max(Cs,Cmin/2*(1-Fs*(1/3)));
           csk = 0.53-0.262*Vd+0.123*pow(Vd,2);
           Cfrac = 0.17;
           Csmin = Cfrac*(1-Fs*(1/3));
           Cggmax = Cinv*L*W*(0.87-Vd+0.53*pow(Vd,2));
           Cgs = Cs*(1-Cfrac/csk)+Csmin*Cggmax;
end
endfunction

analog function real Cgd;
  input Vgs,Vds;
  real
Vgs,Vds,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,m_e,k,k4,f1,f
2,idVg,Cix,Cd,cdk,Cfrac,Cdmin,Cggmax;
  begin
        Vg = Vgs;
           if (Vds < 0) begin
                      Vg = Vgs-Vds;
           end
           Vd = abs(Vds);
           Veff = (Vg-Vt+DIBL*Vd);
           VeffA = Veff+alpha*Vmin/2;
           Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
           VeffB = Veff+alpha*Vmin*Ff;
           Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
           Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
           Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
           m_e = m_star*m_elec;
           if (L < 150e-9) begin
                      m_e = (0.05+0.15*(max(20e-9,L)-20e-
9)/(150e-9-20e-9))*m_elec;
           end
           k = 2*q*(Vd+Vmin/2)/(m_e*pow(Vinj,2));
```

```
            k4 = (sqrt(k+1)-1)/k;
            f1 = VeffB/(n*Vmin);
            f2 = VeffA/(alpha*Vmin);
            idVg = 1/(n*Vmin)*(1-
exp(f2)/(pow(1+exp(f2),2)))*exp(f1);
            Cix = n*Vmin*idVg/(1+exp(f1));
            Cd = Cix*k4*Cinv*L*W;
            //Cgd = max(Cd,Cmin/2*(1-Fs*(2/3)));
            cdk = 0.47-0.281*Vd+0.150*pow(Vd,2);
            Cfrac = 0.17;
            Cdmin = Cfrac*(1-Fs*(2/3));
            Cggmax = Cinv*L*W*(0.87-Vd+0.53*pow(Vd,2));
            Cgd = Cd*(1-Cfrac/cdk)+Cdmin*Cggmax;
end
endfunction

analog function real VdsSat;
  input Vgs,Vds;
  real
Vgs,Vds,Vgd,sgn,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,Ids,R
dsv,IdVS;
  begin
            sgn = 1;
         Vg = Vgs;
            if (Vds < 0) begin
                        sgn = -1;
                        Vg = Vgs-Vds;
            end
            Vd = abs(Vds);
            Veff = (Vg-Vt+DIBL*Vd);
            VeffA = Veff+alpha*Vmin/2;
            Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
            VeffB = Veff+alpha*Vmin*Ff;
            Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
            Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
            Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
            VdsSat = Vdsat * Fs;
end
endfunction

analog begin
  I(d,s)<+Id(V(g,s),V(d,s));

  // Add noise to the drain current
  // First add white noise (thermal), then flicker noise

I(d,s)<+white_noise(gamma*4*`P_K*$temperature*(Id(V(g,s),V(d
,s))/V(d,s)), "thermal_channel");
```

```
I(d,s)<+flicker_noise(nNW*(diam*pi*1e6)*pow(10,(1.37*(V(g,s)
-Vt)-15.26))*VdsSat(V(g,s), V(d,s)), 1, "flicker_channel");

  // Debug
  //$strobe("%M: nNW = %g, Id = %g mA, Vds = %g V, Vgs = %g
V", nNW, I(d,s)*1000, V(d,s), V(g,s));
  //$strobe("%M: nNW = %g, Cgs = %g", nNW,
Cgs(V(g,s),V(d,s)));

  I(g,s)<+Cgs(V(g,s),V(d,s))*ddt(V(g,s));
  I(g,d)<+Cgd(V(g,s),V(d,s))*ddt(V(g,d));

  //I(g,s)<+Cinv*L*W*ddt(V(g,s));
  //I(g,d)<+Cinv*L*W*ddt(V(g,d));
end

endmodule
```

A.2.2 PMOS NWFET VerilogA.

```
// VerilogA for WFET_VS_pModel, VS_pModel, veriloga

`include "constants.vams"
`include "disciplines.vams"

module NW_VS_pMatrix(g,d,s);
inout g,d,s;
electrical g,d,s;

parameter real pi = 3.141528;
parameter real diam = 45e-9;
parameter real nNW = 192;
parameter real W = nNW*(diam*pi);
parameter real Vt = -0.20;
parameter real DIBL = 0.02;
parameter real tox = 7e-9;
parameter real L = 200e-9;
parameter real epsilon = 8.85e-12;
parameter real eox = 15;
//parameter real Cox =
2*pi*eox*epsilon*L/ln(1+(tox/r))*0.55;
//parameter real Cgg = nNW*Cox;
//parameter real Cinv = Cox/(W*L);
parameter real Wmin = 4.66e-9*eox/14.6;
parameter real Cinv = epsilon*eox/(tox+Wmin);
```

```
//parameter real Cmin =
2*pi*epsilon*eox*L/((2*(Wmin+tox)+diam)/diam);
parameter real Vmin = 0.026;
parameter real Vinj = 0.400e5;
parameter real my = 0.0135;
parameter real m_elec = 9.1094e-31;
parameter real q = 1.602e-19;
parameter real Vdsats = Vinj*L/my;
parameter real alpha = 3.5;
parameter real beta = 1.4;
parameter real n = 3;
parameter real pRds = 24e4;
parameter real m_star = 0.2;
parameter real gamma = 2;


analog function real Id;
  input Vgs,Vds;
  real
Vgs,Vds,Vgd,sgn,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,Ids,R
dsv,IdVS;
  begin
           sgn = -1;
        Vg = -Vgs;
           if (Vds > 0) begin
                     sgn = 1;
                     Vg = Vgs-Vds;
           end
           Vd = abs(Vds);
           Veff = (Vg-Vt+DIBL*Vd);
           VeffA = Veff+alpha*Vmin/2;
           Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
           VeffB = Veff+alpha*Vmin*Ff;
           Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
           Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
           Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
           Rdsv = pRds/nNW;
           if (Veff < 0) begin
                     Rdsv = (pRds/nNW)*exp(-(Vg-
Vt)/(12*Vmin));
           end
           Ids = (Vd/Rdsv);
           IdVS = W*Qix*Vinj*Fs;
           Id = sgn*(IdVS+Ids);
end
endfunction

analog function real Cgs;
```

```
  input Vgs,Vds;
  real
Vgs,Vds,sgn,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,m_e,k,k3,
f1,f2,idVg,Cix,Cs,csk,Cfrac,Csmin,Cggmax;
  begin
        Vg = Vgs;
           if (Vds < 0) begin
                     Vg = Vgs-Vds;
           end
           Vd = abs(Vds);
           Veff = (Vg-Vt+DIBL*Vd);
           VeffA = Veff+alpha*Vmin/2;
           Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
           VeffB = Veff+alpha*Vmin*Ff;
           Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
           Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
           Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
           m_e = m_star*m_elec;
           if (L < 150e-9) begin
                     m_e = (0.05+0.15*(max(20e-9,L)-20e-
9)/(150e-9-20e-9))*m_elec;
           end
           k = 2*q*(Vd+Vmin/2)/(m_e*pow(Vinj,2));
        k3 = asinh(sqrt(k))/sqrt(k)-(sqrt(k+1)-1)/k;
           f1 = VeffB/(n*Vmin);
           f2 = VeffA/(alpha*Vmin);
           idVg = 1/(n*Vmin)*(1-
exp(f2)/pow(1+exp(f2),2))*exp(f1);
           Cix = n*Vmin*idVg/(1+exp(f1));
           Cs = Cix*k3*Cinv*L*W;
           //Cgs = max(Cs,Cmin/2*(1-Fs*(1/3)));
           csk = 0.53-0.262*Vd+0.123*pow(Vd,2);
           Cfrac = 0.17;
           Csmin = Cfrac*(1-Fs*(1/3));
           Cggmax = Cinv*L*W*(0.87-Vd+0.53*pow(Vd,2));
           Cgs = Cs*(1-Cfrac/csk)+Csmin*Cggmax;
end
endfunction

analog function real Cgd;
  input Vgs,Vds;
  real
Vgs,Vds,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,m_e,k,k4,f1,f
2,idVg,Cix,Cd,cdk,Cfrac,Cdmin,Cggmax;
  begin
        Vg = Vgs;
           if (Vds < 0) begin
                     Vg = Vgs-Vds;
```

```
            end
            Vd = abs(Vds);
            Veff = (Vg-Vt+DIBL*Vd);
            VeffA = Veff+alpha*Vmin/2;
            Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
            VeffB = Veff+alpha*Vmin*Ff;
            Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
            Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
            Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
            m_e = m_star*m_elec;
            if (L < 150e-9) begin
                        m_e = (0.05+0.15*(max(20e-9,L)-20e-
9)/(150e-9-20e-9))*m_elec;
            end
            k = 2*q*(Vd+Vmin/2)/(m_e*pow(Vinj,2));
            k4 = (sqrt(k+1)-1)/k;
            f1 = VeffB/(n*Vmin);
            f2 = VeffA/(alpha*Vmin);
            idVg = 1/(n*Vmin)*(1-
exp(f2)/(pow(1+exp(f2),2)))*exp(f1);
            Cix = n*Vmin*idVg/(1+exp(f1));
            Cd = Cix*k4*Cinv*L*W;
            //Cgd = max(Cd,Cmin/2*(1-Fs*(2/3)));
            cdk = 0.47-0.281*Vd+0.150*pow(Vd,2);
            Cfrac = 0.17;
            Cdmin = Cfrac*(1-Fs*(2/3));
            Cggmax = Cinv*L*W*(0.87-Vd+0.53*pow(Vd,2));
            Cgd = Cd*(1-Cfrac/cdk)+Cdmin*Cggmax;
end
endfunction

analog function real VdsSat;
  input Vgs,Vds;
  real
Vgs,Vds,Vgd,sgn,Vg,Vd,Vdsat,Veff,VeffA,VeffB,Ff,Qix,Fs,Ids,R
dsv,IdVS;
  begin
            sgn = 1;
         Vg = Vgs;
            if (Vds > 0) begin
                        sgn = -1;
                        Vg = Vgs-Vds;
            end
            Vd = abs(Vds);
            Veff = (Vg-Vt+DIBL*Vd);
            VeffA = Veff+alpha*Vmin/2;
            Ff = 1/(1+exp(VeffA/(alpha*Vmin)));
            VeffB = Veff+alpha*Vmin*Ff;
```

```
            Qix = Cinv*n*Vmin*ln(1+exp(VeffB/(n*Vmin)));
            Vdsat = Vdsats*(1-Ff)+Vmin*Ff;
            Fs =
(Vd/Vdsat)/pow((1+pow((Vd/Vdsat),beta)),1/beta);
            VdsSat = Vdsat * Fs;
end
endfunction

analog begin
  I(d,s)<+Id(V(g,s),V(d,s));

  // Add noise to the drain current
  // First add white noise (thermal), then flicker noise

I(d,s)<+white_noise(gamma*4*`P_K*$temperature*(Id(V(g,s),V(d
,s))/V(d,s)), "thermal_channel");

I(d,s)<+flicker_noise(nNW*(diam*pi*1e6)*pow(10,(1.37*(V(g,s)
-Vt)-15.26))*VdsSat(V(g,s), V(d,s)), 1, "flicker_channel");

  // Debug
  //$strobe("%M: nNW = %g, Id = %g mA, Vds = %g V, Vgs = %g
V", nNW, I(d,s)*1000, V(d,s), V(g,s));
  //$strobe("%M: nNW = %g, Cgs = %g", nNW,
Cgs(V(g,s),V(d,s)));

  I(g,s)<+Cgs(V(g,s),V(d,s))*ddt(V(g,s));
  I(g,d)<+Cgd(V(g,s),V(d,s))*ddt(V(g,d));

  //I(g,s)<+Cinv*L*W*ddt(V(g,s));
  //I(g,d)<+Cinv*L*W*ddt(V(g,d));
end


endmodule
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