Master's Thesis

Design of a 60GHz Low-Noise Amplier in SiGe Technology

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Abstract

A low noise amplifier is designed for future applications in the 60GHz band, using an existing SiGe technology, BiCMOS8HP from IBM. Different topologies are analyzed and compared. Two different schematics of single ended three stage designs are compared. A differential four stage CE topology is designed and simulated with parasitic extraction. The final design shows a noise figure of less than 6 dB, gain of more than 29dB and input/output return loss of less than -13dB for the entire band. Results show a low-noise amplifier in BiCMOS technology is feasible, but issues such as unconditional stability, better linearity and more efficient biasing would have to be solved.

Acknowledgements

First of all I would like to thank my supervisor Kjell Larsson at Ericsson Göteborg for all the guidance and help. I would also like to thank Björn Albinsson, Magnus Dahlgren and everyone else at the Analog ASIC department at Ericsson Göteborg who has helped me during my thesis.

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Olof Malmodin

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Chapter 1
Introduction

Modern electronic devices are capable of receiving many different kinds of wireless signals. There are mobile signal standards such as GSM, 3G and LTE and short range data standards such as WiFi and Bluetooth to name a few. To handle the weak signal from the antenna in the receiving circuit the signal is amplified to a managable level. Low-noise amplifiers, LNAs, are used as input amplification stage in receiver circuits to reduce the overall noise figure [1, 2]. Receivers of wireless signals can for example be found in mobile phones, computers, routers, radios and wireless links. One example of such a reciever is the superheterodyne reciever [1], see fig 1.1.

In this work an LNA is designed from scratch to almost ready for tape out, an actual production. All the work is done using two different computer programs suites, Agile Advanced Design System (ADS) and Cadence Design Systems (Cadence). The work is presented in chronological order with simulation results in a separate chapter.

Chapter one will cover some basic concepts such as materials, noise, electrical properties and measurement methods.

In chapter two the NPN transistor is examined, as this is the most important component of the circuit. Based on these results a topology for the amplifier was chosen.

In chapter three schematics of two different matching net topologies using ideal lossless components are designed and compared.

In chapter four one of the previous schematics is redesigned using real lossy components. The design is tuned to compensate for the different response from the new components.

In chapter five a layout is designed from the schematic, the last step before a tape out.

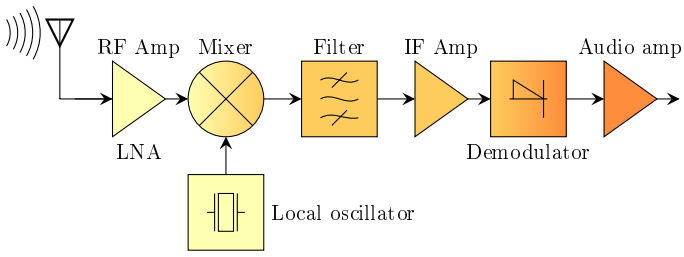


Figure 1.1: Block diagram of a superheterodyne reciever for radio frequencies

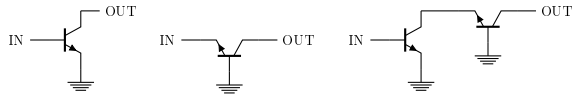


Figure 1.2: Common-emitter (CE), Common-base (CB) and Cascode

1.1 LNA

LNAs in Si or SiGe for frequencies around 60GHz can be designed in several different ways, as single ended two stage cascode [2], single ended three stage cascode [3], single ended four stage cascode [4], single ended CB to cascode [5], single ended to differential cascode-CE [6], differential three stage CE [2, 7, 8, 9], single ended two stage CE two stage cascode [10] and single ended CB to cascode [11]. Common to these designs is the use of one or more of three basic amplifier stages, the common-emitter, the common-base and cascode [12], see fig 1.2.

1.2 SiGe

III-V materials such as GaAs have great RF performance with fast transistors, low noise figure and high output power. However these materials are expensive and not as well suited for mass manufacturing due to high wafer costs and difficult integration with CMOS technology. This is where the SiGe material system has several attractive features for heterojunction bipolar transistors, or HBTs [13]. Contrary to HBTs consisting of III-V materials, the SiGe HBTs can easily be incorporated in the standard silicon process while still maintaining advantages such as band gap difference.

1.3 Noise

There are several kinds of noise in electronic devices, such as thermal noise, shot noise and flicker noise. One way of measuring the noise of a device is to measure the signal-to-noise ratio, SNR

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{1.1}$$

where P_{signal} is the power of the measured signal and P_{noise} is the power of the measured noise [12]. For amplifiers it is however more relevant to know how much noise is being added to the output signal in comparison to how much noise was in the input signal. This is measured as the noise function, F

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{1.2}$$

The total noise of a signal chain can be calculated from

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{1.3}$$

which is known as Friis formula for noise factor, where n is the total number of stages, F_i is the noise function and G_i the available gain of stage i [1]. From this formula it is apparent that the primary stage will contribute the most to the total noise of the signal chain. It is therefore of importance to keep the noise of the input stage as low as possible. In Frii's formula, noise is measured in linear units, this is however not practical in some other cases. Instead F is recalculated as noise figure NF

$$NF = 10\log(F) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{1.4}$$

1.4 S-parameters

Scattering parameters, often referred to simply as s-parameters, is a way of describing electrical behaviour of a circuit at frequencies as high as 60 GHz. At frequencies this high it is not possible to measure voltages and currents with accuracy, therefore how much of the electrical waves are reflected and transmitted is measured instead. For a generic two-port which has an input and an output, there are four possible electrical waves. At the input there are two waves, one in each direction, and similarly at the output [12], see fig 1.3.

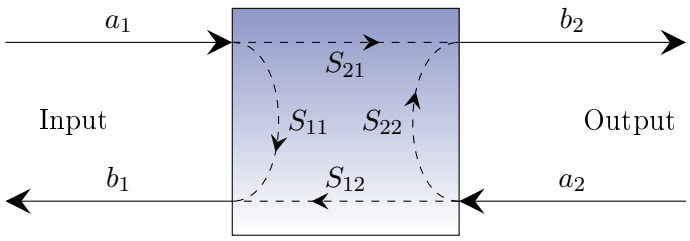


Figure 1.3: Generic two-port

The waves travelling into the two-port can either go through to the other side or be reflected back at the same side, either amplified or attenuated. How much of the incident waves are being reflected or transmitted is determined by

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{1.5}$$

where

S_{11}	is the input port reflection coefficient
S_{12}	is the reverse gain
S_{21}	is the forward gain
S_{22}	is the output port reflection coefficient

For an amplifier the most important s-parameter will be S_{21}, how much the input wave is amplified before leaving at the output.

1.5 Impedance and reflection coefficient

The complex impedance Z of a component consists of real resistive part and a imaginary capacitive or inductive part. This can be expressed as

$$Z = (R + jX)\Omega \tag{1.6}$$

where R is the resistance and X is the reactance, both measured in ohms. Sometimes it is more useful to use admittance

$$Y = \frac{1}{Z} = (G + jB)\mathrm{S} \tag{1.7}$$

which is the inverse of the impedance, where G is the conductance and B is the susceptance, both measured in siemens.

A simple system can be illustrated using a signal source, source impedance and load impedance, see fig 1.4. To achieve maximum power transfer from a signal source to a load, the load impedance should be conjugately matched to the source impedance, $Z_L^* = Z_S$. This can be found from the maximum power transfer theorem

$$P_L = \frac{1}{2}\left(\frac{|V_S|}{|Z_S + Z_L|}\right)^2 R_L \tag{1.8}$$

where P_L is the average power dissipated in the load [14].

To achieve a minimum reflection coefficient the source and load impedances should be equal. Reflection coefficient Γ is the proportion of the signal that is reflected back when encountering an impedance. For the signal going into the load it is given by

$$\Gamma_L = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{1.9}$$

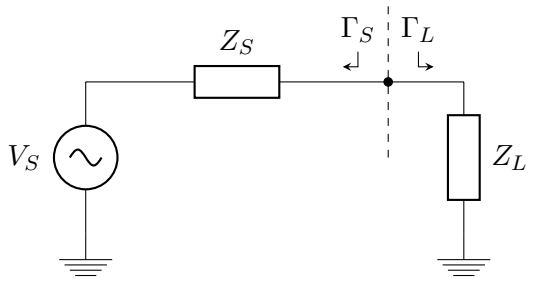


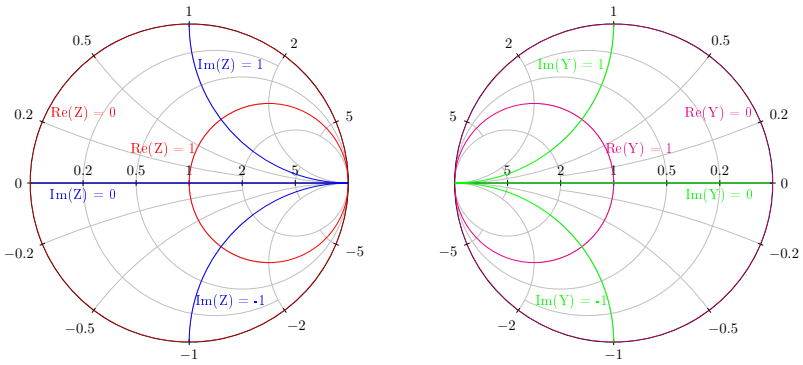
Figure 1.4: Small system

where Z_L is the load impedance and Z_S is the source impedance [12]. If the two impedances are equal Γ becomes zero, wich means no signal is reflected back. A positive Γ will give a reflected wave in phase with the incident wave, a negative Γ will give a reflected wave with a 180° phase shift.

In this case for the amplifier where the source impedance is purely resistive (50 Ω) the load impedance for minimum reflection coefficient and the maximum power transfer will be the same, equal to the source impedance.

1.6 Smith chart

The smith chart is a handy tool where both normalized impedances and reflection coefficients can be plotted with great flexibility [12], a few examples are shown in fig 1.6. The Smith chart is usually plotted with an impedance grid showing constant resistance circles and constant reactance curves, see fig 1.5. It can also be plotted with an admittance grid, with constant conductance circles and constant susceptance curves. In both cases the center of the charts show one, representing the normalized impedance. A pure resistance or conductance will be located along the horizontal line in the middle of the chart, and a pure reactance or suseptance will be located along the outer circle of the chart. It will simultaneously show reflection coefficient, making the Smith chart a very powerful tool. The reflection coefficients are plotted in Cartesian coordinates overlapping the Smith chart, with zero at the center of the chart.



(a) Impedance grid **(b)** Admittance grid

Figure 1.5: Smith charts

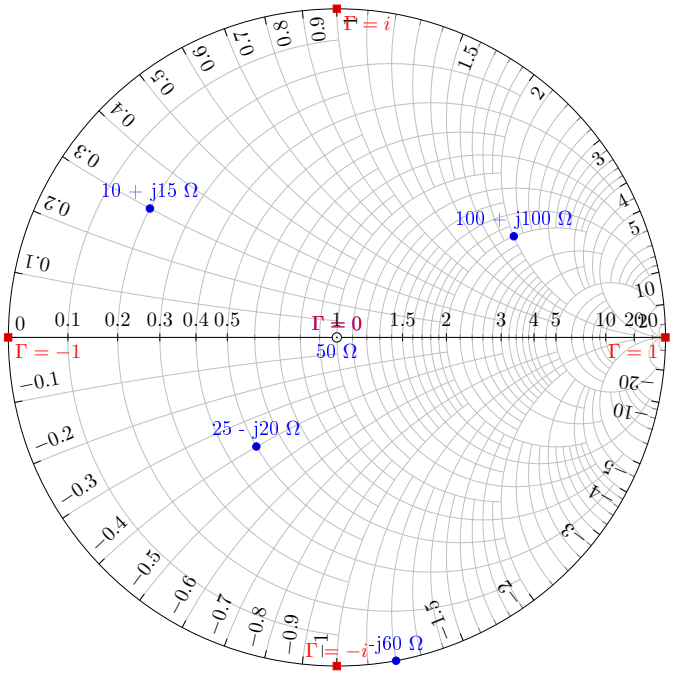


Figure 1.6: Detailed smith chart normalized to 50Ω

1.7 Requirements

The initial specified requirements of the LNA was

Spec	Value
Gain	20 dB
Center Frequency	60 GHz
Bandwidth	7 GHz
Input return loss	<-10 dB
Output return loss	<-10 dB
$IIP3$	>-10 dBm
R_S	100 Ω Differential
R_L	100 Ω Differential
NF	<6 dB

Chapter 2
Initial tests

The initial tests were conducted using ADS (Advanced Design Systems 2012) from Agilent Technologies. The characteristic impedance Z_0 is the standard 50Ω and the ports were 50Ω as well. The process used was the five metal layer version of BiCMOS8HP from IBM.

2.1 The NPN device

The transistor used was the NPN device of the process [15], a heterobipolar junction transistor with n-doped Si emitter and collector and p-doped SiGe base. The option for performance instead of high breakdown was chosen and the suggested drive voltage of $V = 1.2$V was used [16]. The minimum noise figure of the device at 60GHz was found by optimizing the emitter length and base current, see figure 2.1 and 6.1.

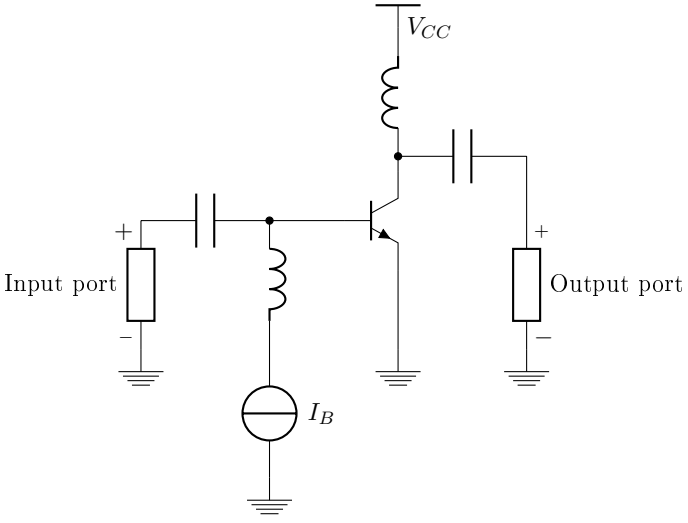


Figure 2.1: Schematic of ADS bias measurements

A decrease in minimum noise figure with multiple devices of a shorter emitter length connected in parallel instead of a single device was also noted, see figure

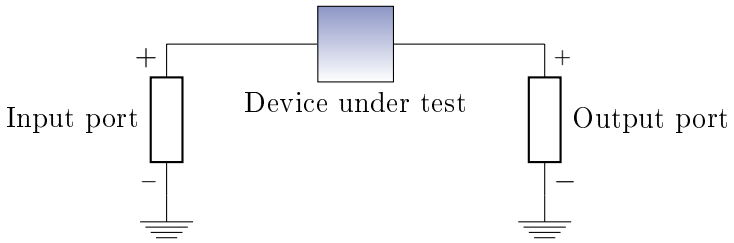


Figure 2.2: Test bench

6.2 and table 6.1. For practical reasons a single device was used in the following measurements.

2.2 Transistor configurations

Three different transistor configurations was considered to be used as stages in the amplifier: CE (common-emitter), CB (common-base) and cascode, see fig 1.2. For the cascode stage the supply voltage was doubled, since it consists of two devices in series to the supply source.

2.3 Input networks

Three different input networks were investigated for the three different stage configurations. The same testbench was used for all measurements, see figure 2.2. The input network to the transistor will determine the transformed source impedance. As seen in section 1.5 the input impedance can effect properties such as gain, noise figure and return loss. The output network will also affect these properties, but not as much.

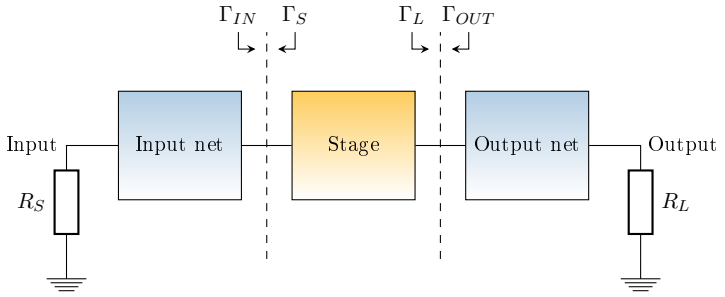


Figure 2.3: Block diagram of a single stage with surrounding nets

2.3.1 No input network

The three stages were designed using large ideal inductors and capacitors to separate the bias- and RF-networks. S-parameters of the three different stages were

plotted up to 70GHz, see figure 6.3. Studied parameters were also noise figure NF, maximum available gain MAG and stability factor K [12].

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right) \tag{2.1}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.2}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.3}$$

The minimum noise figure NF_{min} is the noise figure that would be achieved if the input network reflection coefficient seen from the stage was conjugate matched to Γ_{OPT}. This gives is the input network impedance resulting in the least possible increase in noise from the stage. Γ_{OPT} is a function of the transistor design and it is provided by the manufacturer.

The maximum available gain MAG is the gain of the stage if both input and output were conjugate matched to S_{11} and S_{22} respectively.

Unconditional stability is achieved when

$$Unconditional\ stability \begin{cases} K & > 1 \\ |\Delta| & < 1 \end{cases} \tag{2.4}$$

Since both the common-base and the cascode stage had a stability factor of less than one, they are not unconditionally stable, see table 6.2. Therefore the expression for maximum available gain is not valid. Instead it is replaced by the maximum stable gain MSG, which is the maximum gain available when the stability factor is set to one [12].

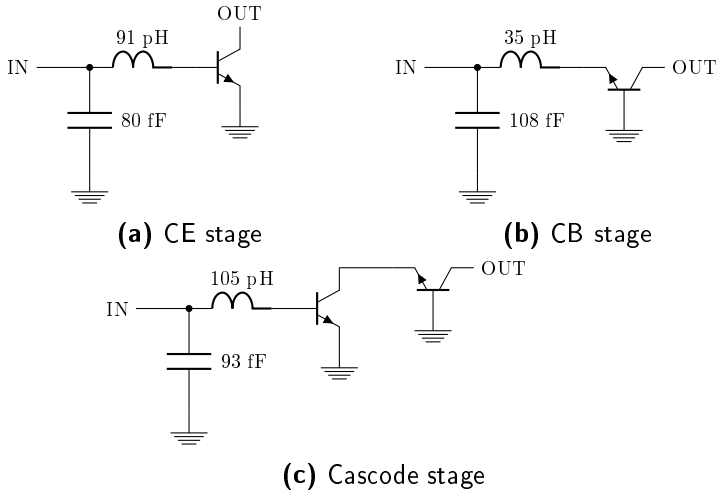
$$MSG = MAG|_{K=1} = \frac{|S_{21}|}{|S_{12}|} \tag{2.5}$$

The stability factor K is not valid for stages with several devices, in this case the cascode. This is because there may be a instability between the stages which is not seen when measuring at the input of the first stage and at the output of the second. The maximum stable gain MSG is directly dependent of K and is therefore not valid for the cascode either. This becomes very apparent since the cascode achieves a higher gain than the combination of the highest possiblie gain of both common-emitter and common-base.

The minimum noise measure M_{min} could be determined from

$$M_{min} = 1 + \frac{F_{min} - 1}{1 - \frac{1}{G_{max}}} \tag{2.6}$$

where F_{min} is the minimum noise factor and G_{max} is the linear maximum available gain or maximum stable gain, see table 6.3. M_{min} is a way of benchmarking the noise of a stage by putting an infinite number of stages in series [17]. As previously, the maximum stable gain of the cascode is not valid and therefore the value of M_{min} is not valid either.



(a) CE stage **(b)** CB stage

(c) Cascode stage

Figure 2.4: Gain matching input networks

2.3.2 Gain matching input network

The input reflection coefficient Γ_{IN} of the amplifier stage is defined as

$$\Gamma_{IN} = S_{11} + S_{12}S_{21}\frac{\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.7}$$

and similarly for the output

$$\Gamma_{OUT} = S_{22} + S_{12}S_{21}\frac{\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.8}$$

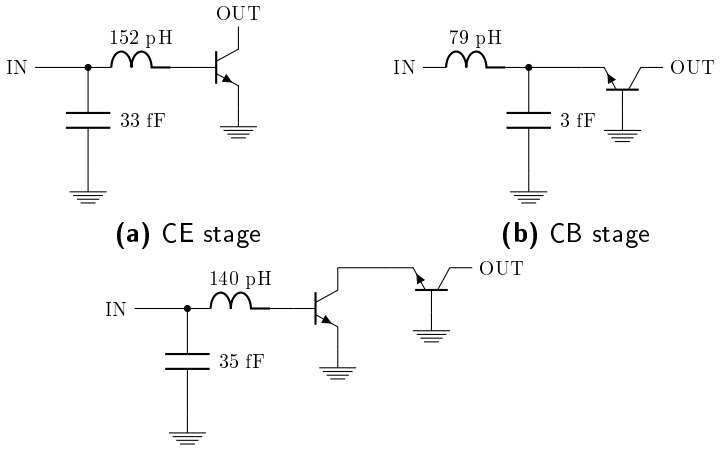
where Γ_L is the reflection coefficient of the load and Γ_S is the reflection coefficient of the source [12], see fig 2.3. If there is no coupling between the input and output port it can be considered unilateral, then equation 2.7 reduces to

$$\Gamma_{IN} = S_{11} \tag{2.9}$$

A conjugate match of S_{11} in the input network will reduce S_{11} and therefore increase S_{21}, see table 6.4. The networks were realized as L-networks, using a shunt capacitor and a series inductor, see figure 2.4.

2.3.3 Minimum noise matching input network

The minimum noise figure is achieved when conjugate matching the input network to Γ_{opt}. The common-emitter and cascode networks were designed using the same method as the conjugate matching to S_{11}, a shunted capacitor to ground followed by a series inductor. The common-base network was designed in the reversed order, a series inductor followed by a shunted capacitor. The networks optimized for NF_{min} reduced S_{21} of the common-emitter and common-base stage, but actually improved the cascode, see table 6.5.



(a) CE stage **(b)** CB stage

(c) Cascode stage

Figure 2.5: Minimum noise matching input networks

2.4 Inductive feedback

Inductive feedback, also called emitter degeneration, was introduced by adding an inductor between the emitter and ground of the common-emitter and cascode stages with no input networks, see figure 2.7. This is in this case done to counter the effect of the capacitance C_{be}, which is the parasitic capacitance between the base and the emitter of the transistor. When introducing an inductor in series a band-stop filter is created which increases the impedance at the base and therefore reduces the voltage lost at higher frequencies. The inductance L of the inductor was tuned to move S_{11} in the smith chart as close as possible to Γ^*_{opt}. With this emitter degeneration both stages achieved a reduced return loss as the input is better matched to 50Ω, but had also a reduced gain. The common-emitter minimum noise figure was reduced.

2.5 Two-tone tests

For all the amplifier stages a two-tone test was performed using a similar test bench as previously. This test was conducted to determine the interpolated 1 dB compression point CP_{1dB} and the third order intercept point IP_3. The 1 dB compression point is where the gain has 1 dB less power that what is to be expected, at this point the amplifier is no longer considered to operate linearly. The third order intercept point is the projected point where the amplified signal would have a fundamental tone and a third order harmonic of the same output power, see fig 2.8.

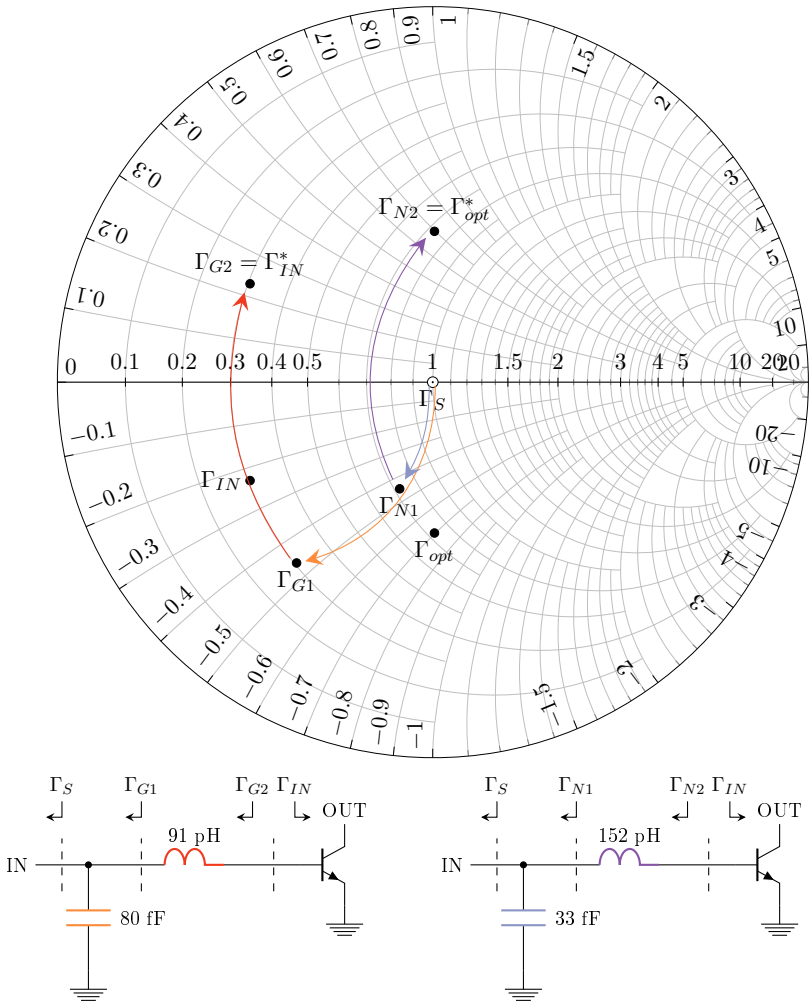


Figure 2.6: Smith chart paths for CE stage input matching nets

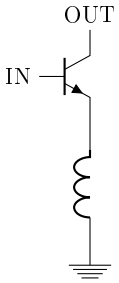


Figure 2.7: CE stage with inductive feedback

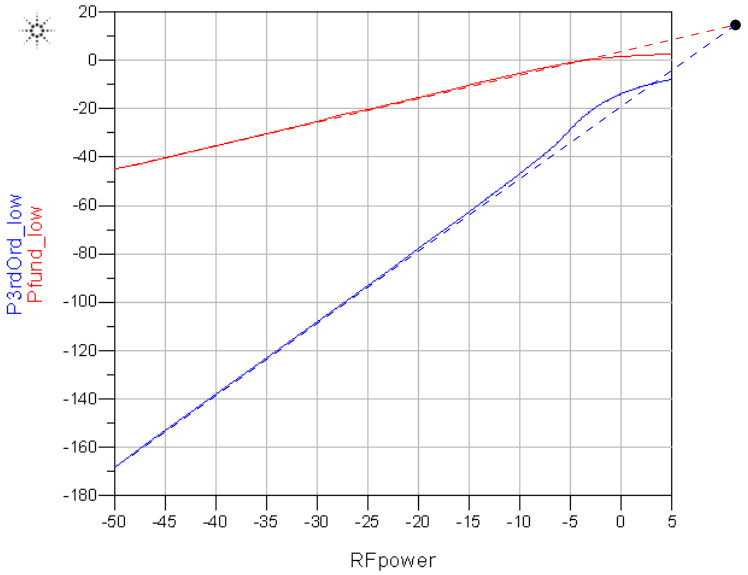


Figure 2.8: Fundamental and third order harmonic of CE stage with no input network

Chapter 3
Ideal schematic

Based on the results of the initial tests a three stage design with common-emitter stages was chosen, see figure 3.1. This was mainly because the CE stage had the lowest noise figure and did not show any stability issues, see table 6.2. For the first stage a degenerated common emitter was used to reduce the noise figure. The biasing current, emitter length and inductor value was tuned to minimize the input reflection coefficient Γ_{IN} by matching the input impedance Z_{IN} to the source impedance Z_S of 50Ω, and to match Γ_{OPT} and S_{11} as good as possible. This was done using a test bench with only stage one in the signal path between the input and output ports, and observing in the Smith chart how the parameters could be moved to more favourable values. Both stage two and three were designed as common emitter stages without any emitter degeneration, see figure 3.2.

To get an estimation of the lowest achievable NF of the amplifier, M was calculated for stage one. As a comparison, NF was calculated using Friis formula with three identical stage one components connected in series. This suggested a NF of 4.0dB. One needs to keep in mind however that this value is only valid for a schematic using ideal components.

3.1 Designing nets using modules

Using only CE-stages means that the matching nets will affect not only the following stages but also the previous to some extent. Therefore a test bench showing all the intersections of the amplifier was used with modules of each stage and net. With all stages and nets implemented as individual design blocks, it was possible to see all the internal s-parameters of the entire amplifier, see fig 3.3. It was also possible to see the noise contribution and gain for each stage added to the chain.

With this modular setup the design could be tweaked and tested in a lot of

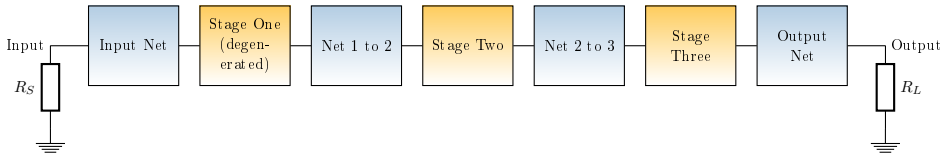


Figure 3.1: Three stage LNA block diagram

(a) Stage one **(b)** Stage two and three

Figure 3.2: Small signal scematic of stages

different ways, with the result seen in real time. The nets could be altered to individually give the transistor stages maximum gain, minimum noise figure or minimum return loss. Since the later stages in the chain affected the previous to some extent, this was an iterative process. Starting with the input net to the first stage, then the second, then the third and finally the output net and repeating this process as many times as needed.

A first coarse design of the nets was realized using series transmission lines in the interstage nets and a series inductor in the output net. The biasing of the stages and DC-blocks were realized separately with ideal DC-feeds and DC-blocks. Since the input impedance of stage 1 is so close to 50Ω no input net was used. Using this network design, NF ended up at 5.0dB which is not acceptable considering the calculated minimum of 4.0dB.

A second design was realized using shunted inductors to ground and series capacitors. The nets were designed for optimum noise figure of stage one and two, and maximum gain of stage three. The biasing current was fed through resistors from V_{CC}, the capacitors provided needed DC-blocks. With this new design all of the requirements were met, apart from the input return loss. NF was reduced to 4.1dB.

A third design used a current mirror to provide the biasing through an inductor, with nets consisting of shunted inductors and series capacitors. A current mirror replicates the current passing through transistor to other transistor. Signal ground was introduced at V_{CC} and V_{BIAS} through large capacitors.

A fourth design used a current mirror as well to provide the biasing, but with nets consisting of transmission lines and capacitors. The drive voltage source was isolated using quarter wavelength transmission lines, signal ground was introduced at V_{CC} and V_{BIAS} through large capacitors.

3.2 Full schematic

The third and fourth design were extracted from the modules into single design blocks, see figure 3.4 and 3.5. These were simulated and confirmed to show results coherent with their modular based counterparts. The large capacitors and inductors are not part of the matching nets, they only serve as DC-blocks and DC-feeds. Both designs using ideal components were implemented in Cadence as well as ADS. This would provide a validation of the results.

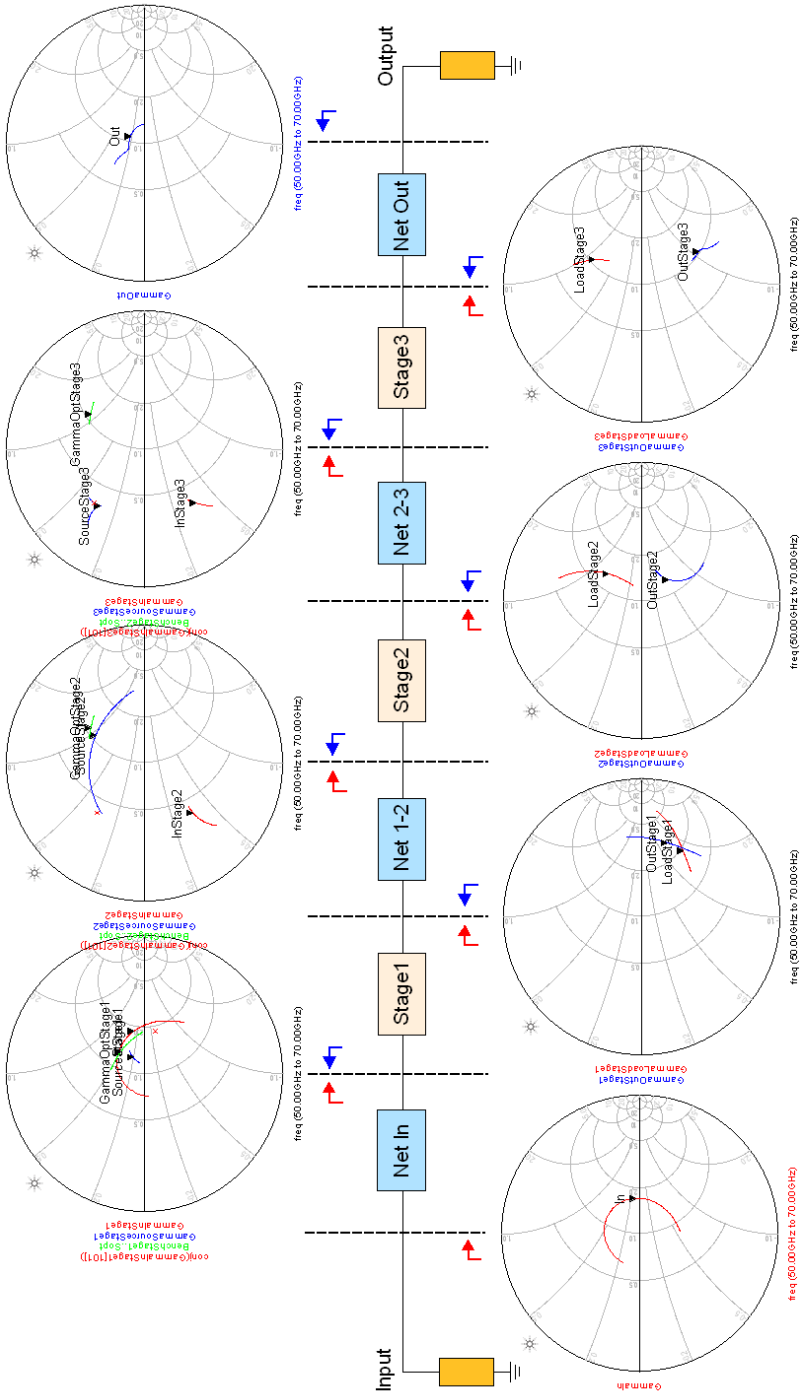


Figure 3.3: Signal chain with s-parameters

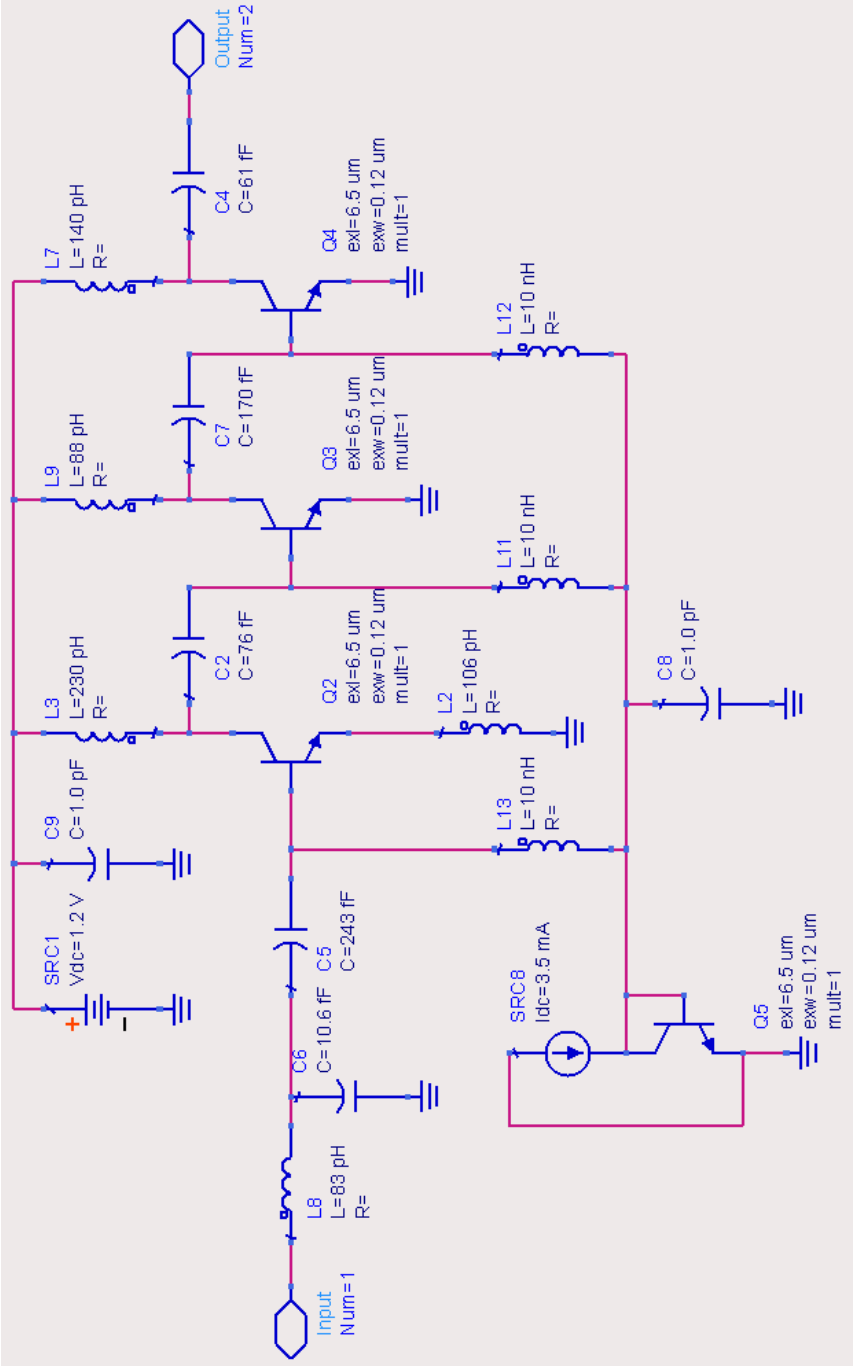


Figure 3.4: Full schematic using LC networks

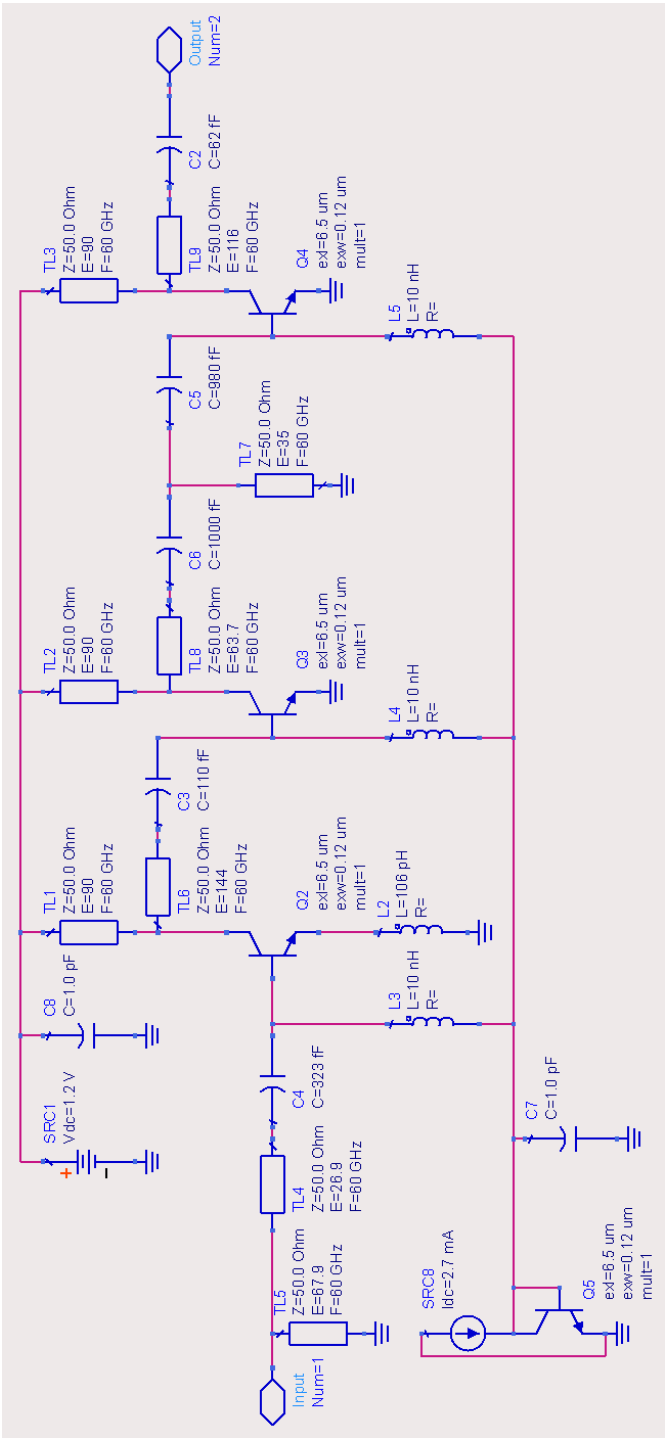


Figure 3.5: Full schematic using transmission line networks

Chapter 4

Real schematic

Previously components such as capacitors, inductors and transmission lines were considered ideal. A more realistic model of the components includes parasitics, which are always present in all components. These realistic components, also from the BiCMOS8HP design kit, would later be used in the layout process.

Integrated circuits are constructed in different layers on top of one another, called a stack. For the simulations in ADS the five metal layer version of IBM8HP process was used, and for the simulations in Cadence the six metal layer version [16], see fig 4.1. The six layer version has one more thick top layer, preferably the six layer version would have been used in the ADS environment as well, but there was unfortunately not any design kit available.

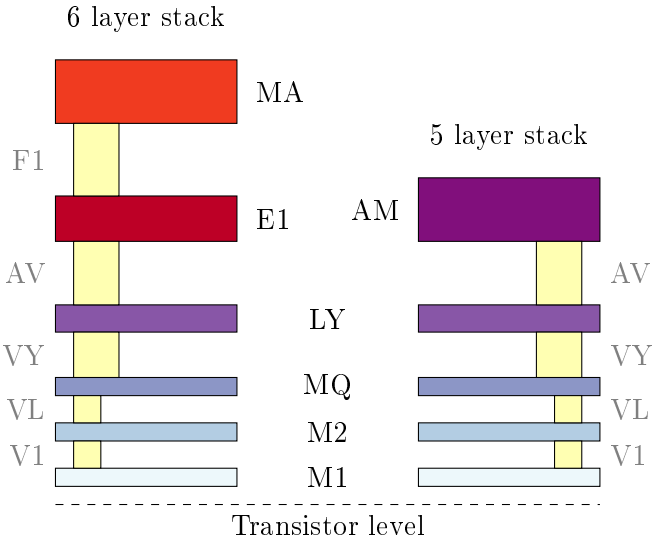


Figure 4.1: Simplified cross section of the 5 and 6 layer stacks also showing vias between layers, not drawn to scale

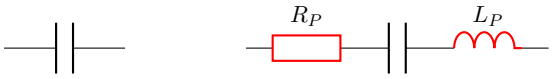


Figure 4.2: Ideal capacitor and capacitor with parasitics

4.1 Components

When using real components there is always parasitic resistances and impedances which has to be accounted for. For example, a capacitor has both a parasitic resistance and a parasitic inductance, see fig 4.2.

4.1.1 Transistor

The transistors used in the design were high performance SiGe heterojunction bipolar transistors, see fig 4.3. The device layout consists of a single emitter stripe with a fixed width of 0.12μm, with the length scalable for different currents. To avoid a long signal path and inconvenient geometries, long transistors were split into several shorter transistors.

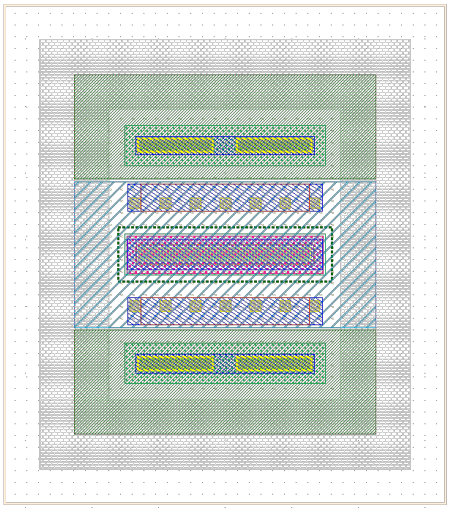
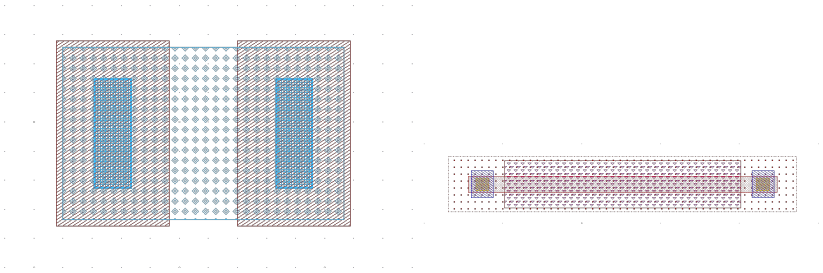


Figure 4.3: Layout of transistor

4.1.2 High-Ω Resistor

The resistors for several kΩ were P+ poly OP resistors in the PC layer, a layer at the bottom, below the metal stack. These were contacted from the M1 layer. So far down there was a high capacitance to the substrate and the resistors could not be used in the signal path, only for biasing.



(a) Low-Ω resistor **(b)** High-Ω resistor

Figure 4.4: Layout of resistors

4.1.3 Low-Ω Resistor

The resistors in the range of 100 Ω were KQ BEOL resistors located in the KQ layer, between LY and MQ. These were contacted from the LY layer.

4.1.4 Transmission line

For both the design in ADS and in Cadence, transmission lines were located in the the top layer of the stack. For the AM layer of the five layer stack in the ADS simulations the minimum width of the line was 2μm, the height is the same as the layer thickness. Adjusting the width of the line will affect the characteristic impedance, the length will affect the phase of the signal. The transmission lines had a ground plane at MQ, a middle layer.

4.1.5 Capacitor

The capacitors used were metal-insulator-metal, or MIM-capacitors. The correct capacitances were achieved by adjusting the size of the capacitor, since

$$C = \frac{\epsilon A}{d} \tag{4.1}$$

where ϵ is the dielectric constant of the insulating layer, A is the area of the metal plates and d is the thickness of the insulator. The length and width of the capacitors was kept as equal as possible during the design process, as the capacitor preferably would be square shaped. In the layout with the six layer stack the capacitors were located between the LY and E1 layers, see fig 4.5. The E1 layer was used to contact both input and output. The capacitor itself was formed in LY and QY, where QY is a layer just above LY. Between QY and LY was a thin dielectric. Both the LY and QY layers were contacted by vias to the E1 layer.

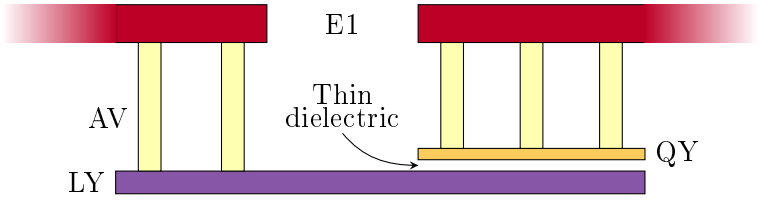


Figure 4.5: Cross section of a capacitor, not to scale

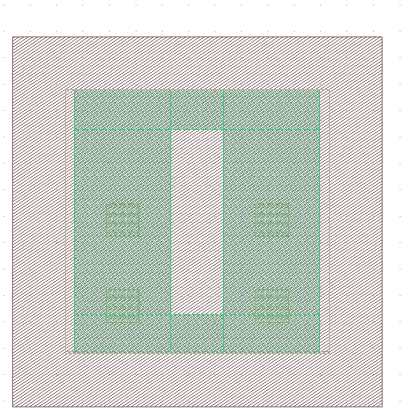


Figure 4.6: Layout of capacitor

4.2 Design with modules

As previously, the circuit using real components was also designed with nets and stages in separate modules to see all relevant internal s-parameters. $\lambda/4$ transmission lines were used as RF-blocks to the base and collector. The first stage was degenerated using a short transmission line. RF-ground was connected at V_{CC} and the current mirror through large capacitors. All interstage nets and the input net were designed using a transmission line stub shorted by a capacitor to ground, a series transmission line and a series capacitance, see figure 4.7. The output net was designed in the same way but without the series transmission line.

4.3 Full schematic

A full schematic was extracted from the individual modules as previously with the ideal design. The three stages were all connected to the same drive voltage, ground and biasing current mirror.

4.4 Optimizer

The full design was tuned using the ADS optimizer with control over all relevant component parameters. The design goals were a high S_{21} with good linearity and low NF, S_1 and S_{22}. The specified goals increased in difficulty as the optimizer managed to meet them. Finally a goal was set which the optimizer after many iterations could not meet, this was chosen as the best possible design configuration.

4.5 Cascode comparison

A similar three stage design was made with a CB configuration in the second stage, making it from a small signal point of view a Cascode-CE design. This design was tuned and optimized in the same manner as before. This configuration did not surpass the triple CE design, and was therefore discarded.

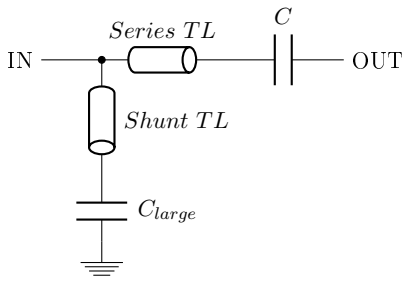


Figure 4.7: Net topology

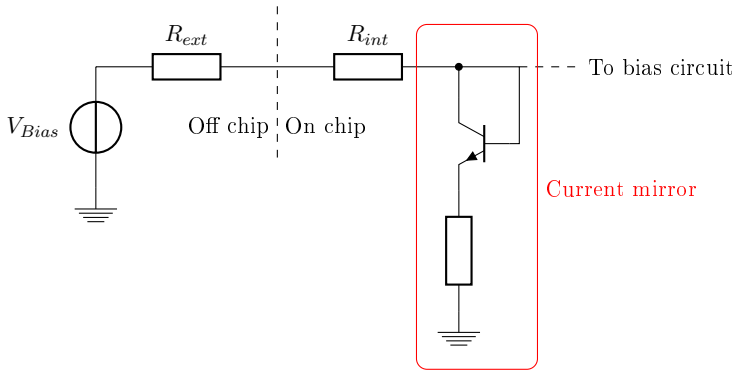


Figure 4.8: Design of current mirror

4.6 Current source

The current source driving the current mirror for the biasing was implemented as a two resistances to a diode coupled transistor, see fig 4.8. The resistance was divided into one resistor on-chip and one off-chip, this to enable tuning of the bias.

The current through the current mirror is set by

$$I \approx \frac{V_{Bias} - V_{be}}{R_{ext} + R_{int}} \tag{4.2}$$

where V_{be} is the voltage drop from the base to the emitter. A fraction of the current is lost to the bases of the stages the current is mirrored to.

4.7 Differential design

The full schematic using three CE stages was mirrored into two identical amplifiers using the same drive voltage and biasing current mirror. A current source was introduced for each transistor pair, keeping the current constant through the pair and introducing a virtual ground at the emitters, see fig 4.9. To compensate for the loss in voltage swing over the differential stage due to the current source, the supply voltage was increased.

To verify the performance using the same s-parameter measurements as previously, ideal transformers were used to transform the signal from unbalanced to balanced, see fig 4.10. The number of turns in the secondary coil is calculated from

$$Z' = \left(\frac{N_P}{N_S}\right)^2 Z \tag{4.3}$$

where Z is the actual impedance, Z' the transformed impedance, N_P the number of turns in the primary coil and N_S the number of turns in the secondary coil. To transform the 50 Ω source and load impedances to 100 Ω a turn ratio of 1:1.414 was used since $\sqrt{2} \approx 1.414$.

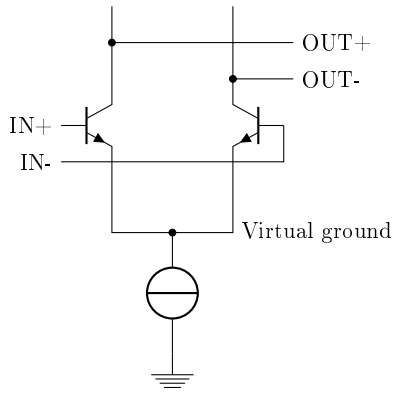


Figure 4.9: Differential stage

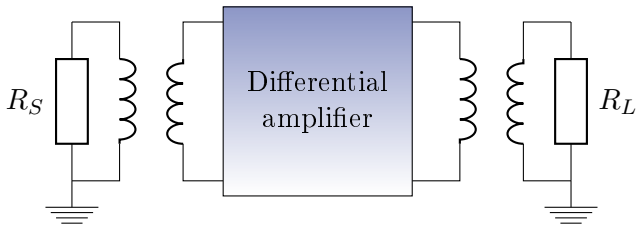


Figure 4.10: Bench with ideal transformers

4.8 Test Stage Layout

To approximate the losses from the parasitics in the layout of the full design, a small layout of a single stage was made. This layout was made with very little effort to minimize the parasitics, thus resulting in a worst case scenario design. From the results of the comparison between schematic and layout, it was obvious that a better performance was needed.

4.9 Four stage design

To improve the performance of the amplifier a fourth stage was added. With an additional stage, the four stages could be tuned for less noise with a manageable loss in gain.

The four stage design was replicated from ADS into Cadence. Since the six layer stack was used in Cadence, the width of the transmission lines would have to be recalculated to achieve the correct impedances.

Unfortunately the results from the same design in ADS and Cadence did not match. It turned out the ADS version of the design kit was outdated and had to be updated. When this was done the results of the design were not very good so the values of some components had to be adjusted. With the design satisfactory again in ADS, it was once more replicated in Cadence. This time the results matched.

Chapter 5
Layout of final design

The layout of the design is when all the limitations of the physical world are accounted for. Previously in the schematic, any number of components could be connected side by side without any parasitics to each other. The layout is what the design actually will look like when processed.

5.1 First layout

When designing the layout it became obvious that the biasing nets would have to be changed since the width of the transmission lines made it impossible to fit everything to the much narrower signal chain. Another realization was that the use of $\lambda/4$ lines opposing each other made the size of the amplifier go above $\lambda/2$. This would most likely induce an unwanted resonance. For these reasons the biasing nets were redesigned.

Instead of using $\lambda/4$ transmission lines, current was fed to the bases of the differential stages through large coils with a capacitance to ground. Current to the collectors was fed through the already existing path of the matching nets, see fig 5.1.

The signal chains were kept as short as possible to reduce noise and avoid phase errors. Where possible, the MQ layer was added as ground plane. No bondpads were placed in the design since it was not decided yet what the bonding method would be. An RCL extraction was made for the full differential amplifier layout using Assura Parasitic Extraction (RCX) [18] and the resulting component was simulated. The simulations showed the amplifier working as intended, see fig 6.5. However, stability simulations showed potential instabilities for 16GHz in differential mode and 65GHz for common mode. This was determined from the K factor being below one for those frequencies.

5.2 Stabilized layout

To suppress the common mode signal and eliminate the instability, low value resistors were added between the differential stages and the current mirrors, see fig 5.4. This way the common mode signal would have to pass the resistor but the differential would not, see fig 5.3.

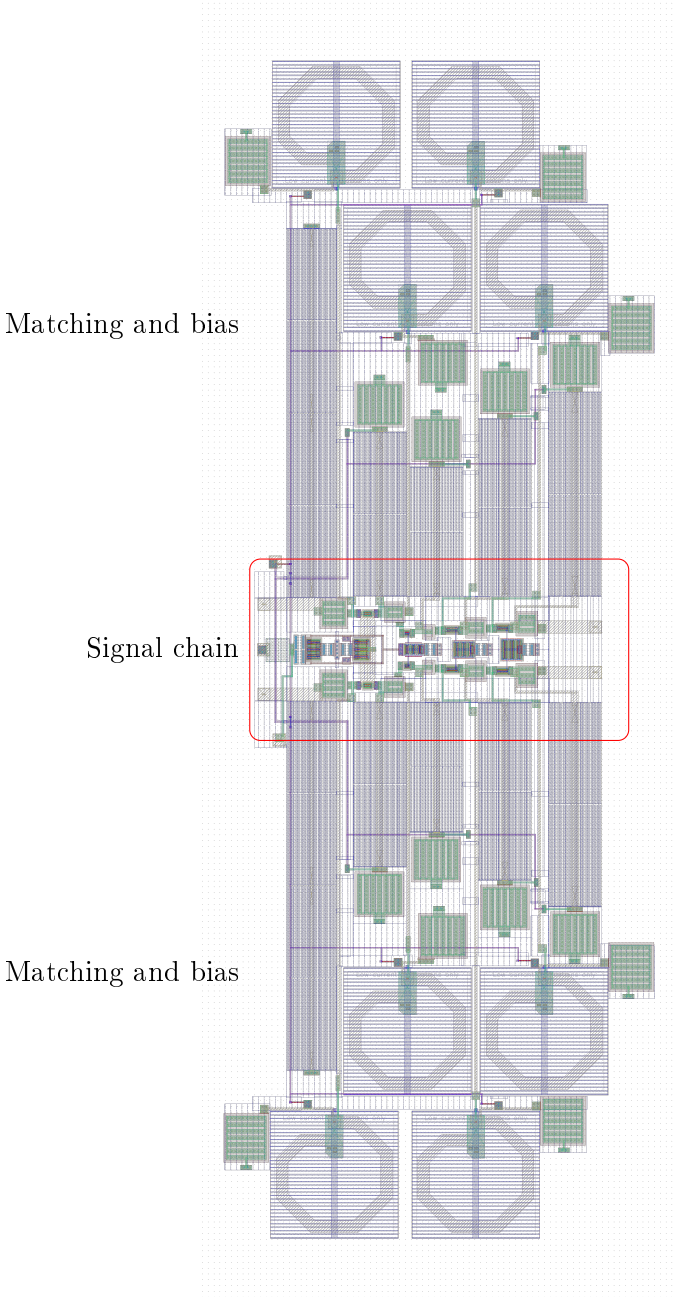


Figure 5.1: First layout

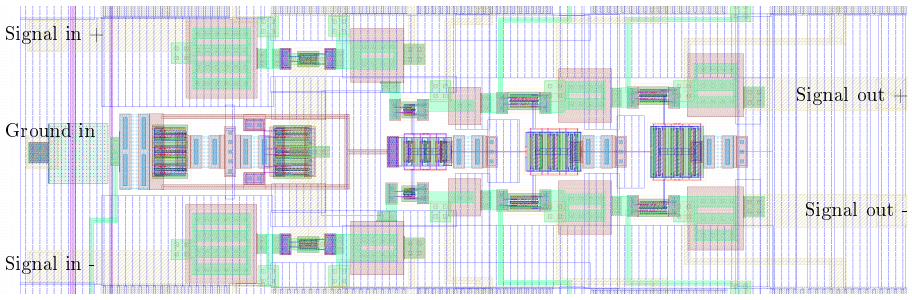


Figure 5.2: First layout, signal chain

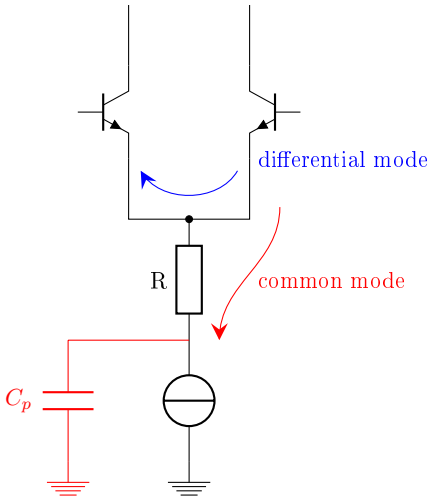


Figure 5.3: Differential stage with common mode suppression

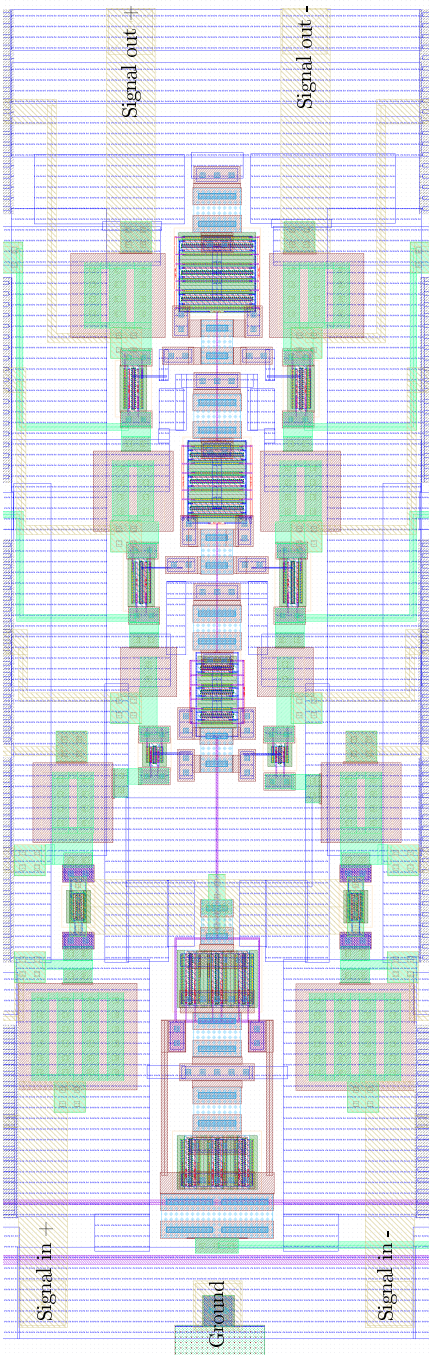


Figure 5.4: Improved layout signal chain with added resistors

Chapter 6
Results

The relevant results of the various measurements are presented in chronological order, with separate sections for each of the previous chapters.

6.1 Initial tests results

The initial tests were conducted to get an understanding of what the technology was capable of. These results were to determine the topology for the later schematic.

6.1.1 The NPN device

The transistor is the most important component in the entire amplifier. The behaviour is highly influenced by the operating point set by the biasing as well as the physical dimensions. In fig 6.1 the effects of different emitter lengths and biasing currents to the noise figure can be seen. The minimum noise figure is located at 7.4 μA for the 10 μm emitter. In fig 6.2 the difference between a single transistor and two transistors in parallel is shown. The decrease in NF with multiple transistors in parallel is shown in table 6.1.

n	NF [dB]	I_B [μA]	I_C [mA]	L_{em} [μm]	L_{TOT} [μm]
1	3.53	7.4	3.15	10	10
2	3.49	7.7	3.46	5.5	11
4	3.46	6.6	3.22	2.5	10
8	3.43	6.0	2.97	1.1	9
16	3.40	5.3	2.56	0.5	8

Table 6.1: Minimum noise figure with multiple devices of different emitter lengths

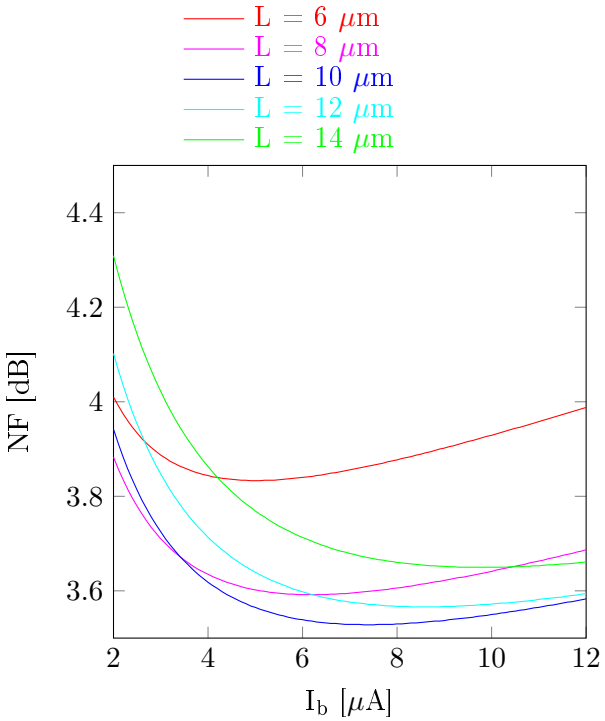


Figure 6.1: Noise figure versus base current at 60GHz for different emitter lengths

Figure 6.2: Comparison with multiple devices

6.1.2 Transistor configurations

The different configurations of the transistors in the amplification stages all have their own advantages and disadvantages. In fig 6.3 the four s-parameters are shown for the three configurations. The input reflection coefficient is roughly the same for all three configurations, the cascode stage has the lowest reverse transmission and the highest forward transmission and the CE stage has the lowest output return loss.

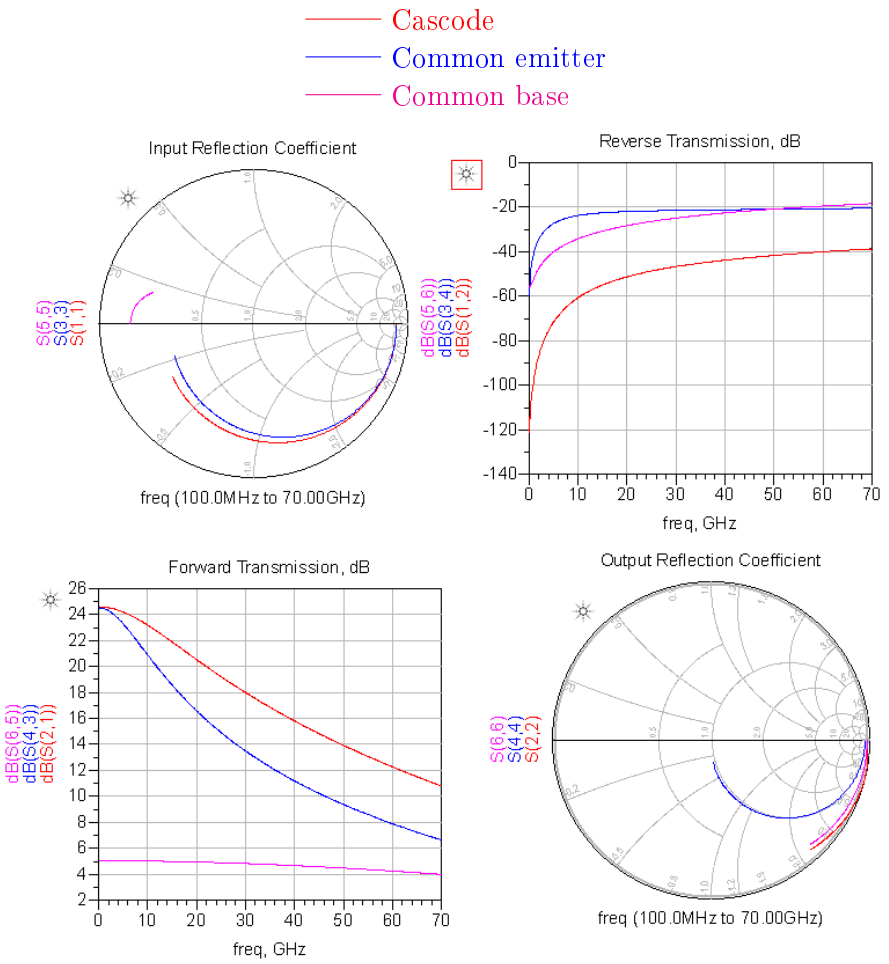


Figure 6.3: S-parameters of the cascode, common emitter and common base stages with no input networks from DC to 70GHz.

In table 6.2 the possible minimum noise and maximum gain values are shown for the three stages. Maximum gain is not shown for the cascode stage due to stability issues. These results show a better noise and stability performance for the CE stage. In table 6.3 the noise measure is shown for the CE and CB stages, the CE stage showing better noise performance here as well. In table 6.4 and 6.5 the change in gain is shown with different input matching networks.

Measurement	CE	CB	Cascode
NF_{min} [dB]	3.123	3.336	3.635
K	1.394	0.474	*0.027*
MAG [dB]	10.018		
MSG [dB]		11.894	

Table 6.2: Parameters of the three stages with no input networks

Configuration	F	G	M_{min}
CE	2.05	10.0	1.17
CB	2.16	15.5	1.24

Table 6.3: Noise measure results

Configuration	S_{21} [dB]	S_{21} matching network [dB]
CE	7.69	9.27
CB	4.13	6.78
Cascode	11.8	14.2

Table 6.4: S_{21} increase with gain matching input network

Configuration	S_{21} [dB]	S_{21} matching network [dB]
CE	7.69	7.66
CB	4.13	2.87
Cascode	11.8	12.8

Table 6.5: S_{21} change with minimum noise matching input network

6.1.3 Two tone tests

The two tones were centred around 60GHz with a spacing of 1 MHz. The total input signal power was swept from -50 dBm to 5 dBm. For all three configurations the CB stage shows the highest compression point and third order intercept point, except for the gain matching net where the CE stage shows a slightly higher third order intercept point. The gain however is lower for the CB stage in all three configurations.

Configuration	G [dB]	CP_{1dB} [dBm]	OIP_3 [dBm]	IIP_3 [dBm]
CE	6.90	2.63	16.4	9.47
CB	3.26	4.14	16.9	13.7
Cascode	11.3	2.73	15.0	3.74

(a) No input network

Configuration	G [dB]	CP_{1dB} [dBm]	OIP_3 [dBm]	IIP_3 [dBm]
CE	8.48	2.54	16.1	7.65
CB	6.23	2.91	13.6	7.35
Cascode	13.5	2.47	14.8	1.29

(b) Gain matching input network

Configuration	G [dB]	CP_{1dB} [dBm]	OIP_3 [dBm]	IIP_3 [dBm]
CE	6.76	2.62	16.5	9.77
CB	1.96	4.23	18.0	16.0
Cascode	12.1	2.56	15.0	2.88

(c) Minimum noise matching input network

Table 6.6: Compression point and third order intercept

6.2 Ideal schematic results

Measurements from the two single ended three stage schematics with ideal components are presented in table 6.7 and 6.8. Gain drop is measured as the difference between maximum and minimum gain between 56.5 GHz and 63.5 GHz. Input return loss is measured for the entire bandwidth as well.

Program	ADS	Cadence
NF at 60GHz	3.52	3.65
Gain at 60GHz	23.4	23.1
Gain variation inside BW	3.58	3.59
Input return loss	<-11.5dB	<-11.5dB

Table 6.7: Results from ideal LC schematic

Program	ADS	Cadence
NF at 60GHz	3.41	3.71
Gain at 60GHz	22.3	23.0
Gain drop inside BW	5.34	5.58
Input return loss	<-11.0	<-10.6

Table 6.8: Results from ideal transmission line schematic

6.3 Real schematic results

Measurements in ADS from the four stage differential amplifier schematic with real components are presented in table 6.9. Measurements in cadence for the similar schematic is presented in fig 6.4.

NF at 60GHz	6.18
Gain at 60GHz	27.9
Gain drop inside BW	0.60
Input return loss	<-11.8

Table 6.9: Results of four stage differential amplifier schematic simulations in ADS

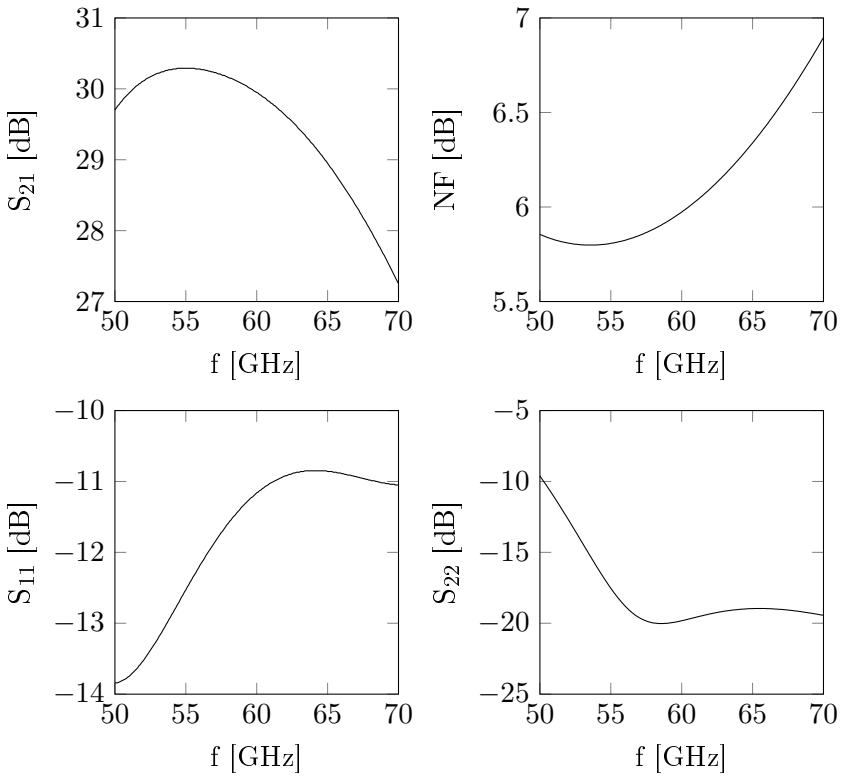


Figure 6.4: Results of four stage differential amplifier schematic simulations in Cadence

6.4 Layout results

The two layouts were simulated after RCL extraction using Assura Parasitic Extraction (RCX) [18]. Results from simulations of the first layout and the stabilized layout is presented in fig 6.5 as well as the previous schematic for comparison.

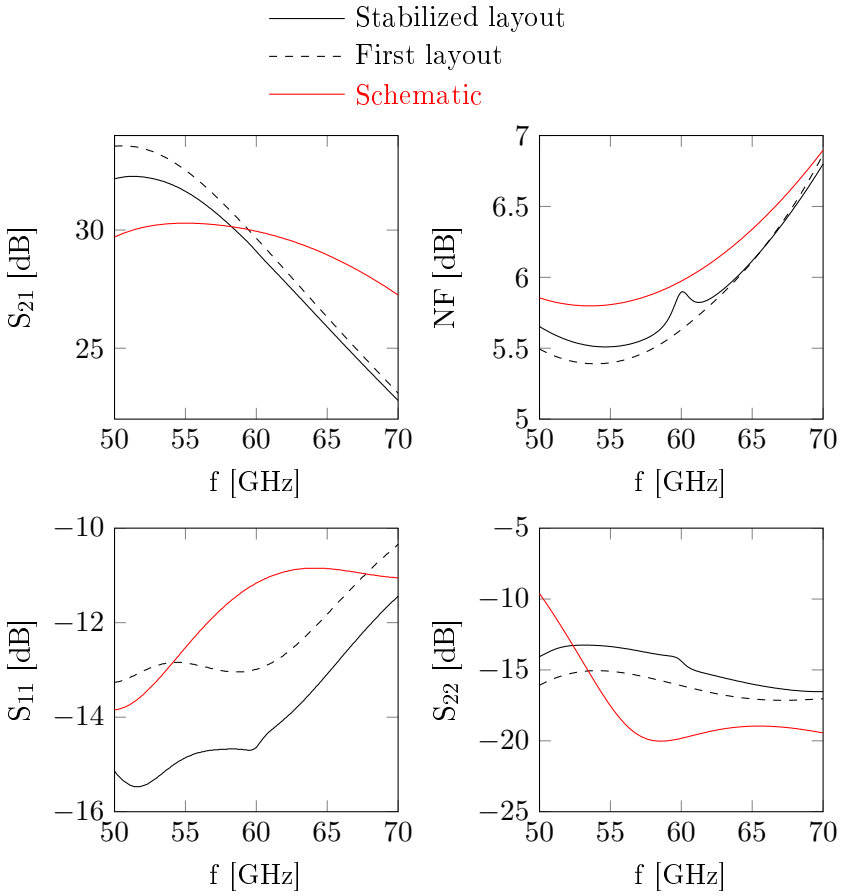


Figure 6.5: Results from the parasitic extraction of the two layouts, schematic results also shown for reference

6.5 Comparison with other work

The simulated results in this work is presented in comparison to the measured results from tape out in other publications.

Ref	f [GHz]	NF [dB]	$Gain$ [dB]	$IIP3$ [dBm]	CP_{1dB} [dBm]	S_{11} [dB]	S_{22} [dB]	I [mA]	V [V]
[8]	49-71	*6.8*	18dB			<-15	-7	30	2.2
[10]	59-64	<6.2	>20		-29	<-12	<-12	10	2.7
[11]	61.5	4.5	17	-9	-20	-14	-12	6	1.8
This work	56.5-63.5	<6	29	-25	-35	<-13	<-13	45	3.2

Chapter 7

Conclusions and discussion

The results of the simulations show that a 60GHz LNA in currently available, relatively inexpensive SiGe technology is indeed feasible. In this study the simulated layout met the requirements for noise figure, gain and return loss.

In the later stages of the design process the center frequency got shifted to a lower frequency than 60GHz when striving for a lower noise figure and return loss. This resulted in a poor linearity of the amplifier gain, which will have to be addressed.

The design has not been simulated for varying temperatures. Since the transconductance in a bipolar transistor can be expressed as

$$g_m = \frac{I_C}{V_T} \tag{7.1}$$

where I_C is the collector current and V_T is the thermal voltage, the transistor will show a varying gain with varying temperature.

The parasitic extraction tool RCX [18] enabling simulation of the layout may not be accurate at 60 GHz. This tool does not take into account currents in the substrate which would be present at such frequencies. There may also be some coupling between the transmission lines of the bias and DC-feed nets. Even though the lines are shielded with a 46 μm wide ground plane and are fairly separated from each other, there may be relevant parasitics in between since some of them run in parallel several hundred microns. No electromagnetic simulations were run on the final design, this would determine if there is any coupling that has to be accounted for.

For real world applications the design would need to include ESD protection, to avoid the circuit being damaged or destroyed by electrostatic discharges. Static charges can easily be built up when there is friction between two materials, for example when walking on a rug or rubbing a plastic comb against dry hair. When statically charged, a single touch on the circuit could potentially destroy it.

No bondpads were included in the design at this stage since the desired bonding method was not known. Including bondpads will result in some parasitic capacitances. These can to some extent be reduced by the connected inductive wiring, but the overall effect will still be negative to the performance of the amplifier.

With the specified source and load impedances the design was stable for all frequencies. However it would be favourable if it could modified to be uncon-

ditionally stable, for a more flexible and useful component to be used in other surroundings.

The best way to verify the design would of course be a tapeout, which has not been done.

Appendix A

Full schematic

The full schematic shown in fig A.1 represents the stabilized design. The transistors used are presented in table A.1. The supply voltage V_{CC} was 3.2V.

Transistor	L_E [μm]	Multiplicity	Use
Q1/Q2	5.3	1	Stage one
Q3/Q4	3.2	1	Stage two
Q5/Q6	8.9	1	Stage three
Q7/Q8	8.6	1	Stage four
Q9	10.8	3	Current source one
Q10	6.6	3	Current source two
Q11	11	3	Current source three
Q12	15	3	Current source four
Q13	10	3	Current mirror

Table A.1: Transistors used in the stabilized design

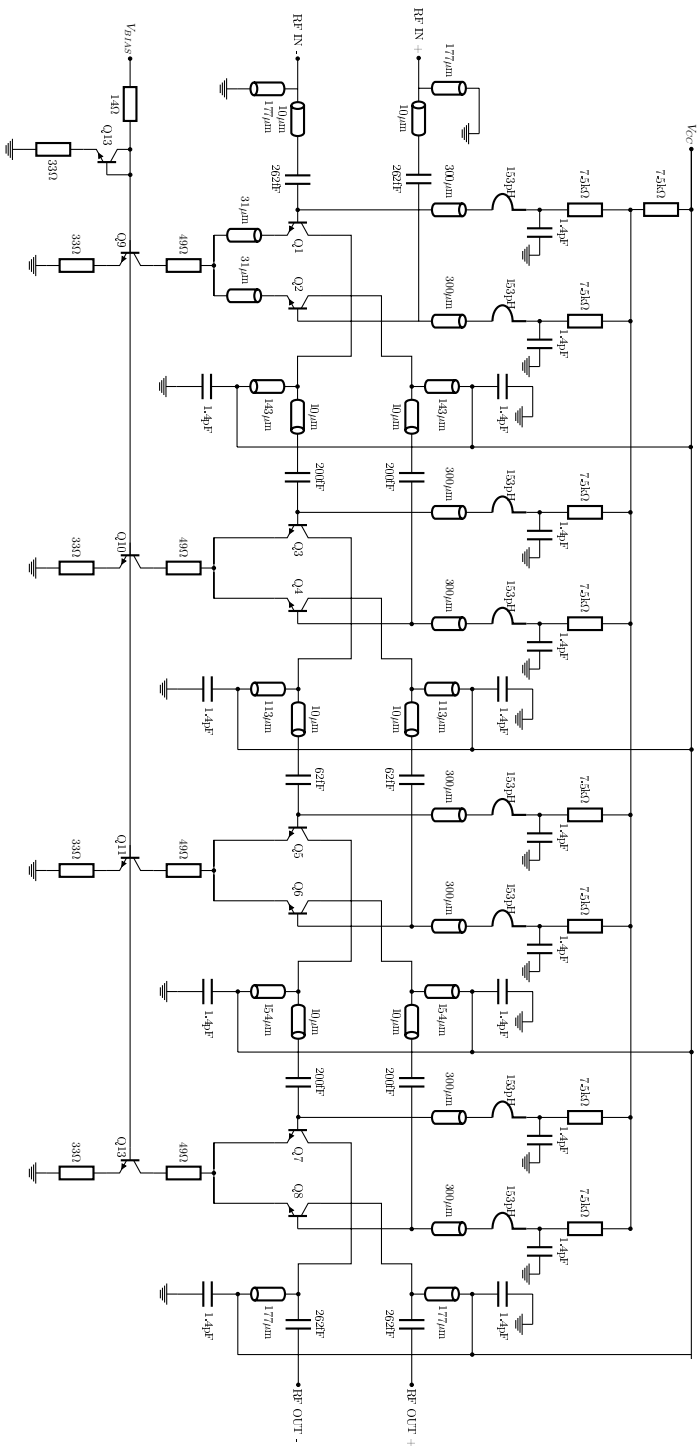


Figure A.1: Four stage differential amplifier in Cadence

Appendix B

List of components

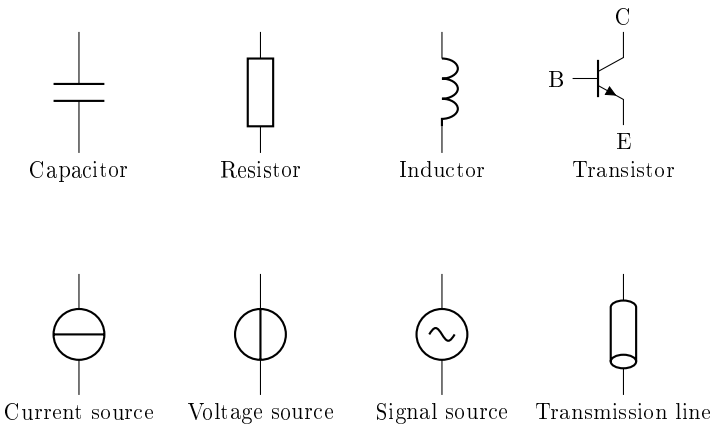


Figure B.1: Components used in schematics

Appendix C

List of symbols and abbreviations

Symbol	Unit	Name
B	S	Suseptance
C	F	Capacitance
CP_{1dB}	dB	1 dB compression point
F		Noise factor
G	dB	Gain
G	S	Conductance
I	A	Current
IIP_3	dBm	Input third order intercept point
K		Stability factor
L	H	Inductance
M		Noise measure
MAG	dB	Maximum available gain
MSG	dB	Maximum stable gain
NF	dB	Noise figure
P	W	Power
R	Ω	Resistance
S		Scattering parameters
S_{11}		input port voltage reflection coefficient
S_{12}	dB	reverse voltage gain
S_{21}	dB	forward voltage gain
S_{22}		output port voltage reflection coefficient
V	V	Voltage
V_{CC}	V	Drive voltage
X	Ω	Reactance
Y	S	Admittance
Z	Ω	Impedance
Z_0	Ω	Characteristic impedance
Γ		Reflection coefficient
ϵ	Fm^{-1}	Dielectric constant
λ	m	Wavelength

References

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