Review and upgrade of a sensor interface system for airfield automation

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September 26, 2013

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Abstract

Increasing demand of power efficient products has led Safegate Group International AB to decrease system current from 6.6 A to 2.0 A . This decrease requires upgrade and review of their existing product portfolio. The master thesis focal point was to renew one of their products; a Sensor Interface Unit, a SIU, for use in the 2.0 A system.

After examining the existing unit, the conclusion was that a new version of SIU had to be developed, not only to meet present specifications in the new 2 A system but also to satisfy future needs. Due to the scope of the project, this master thesis only focused on product planning, prototype development and prototype evaluation.

An existing Safegate platform, an airfield light controller developed for the 2 A system, was used to create a new SIU prototype. SIU functionality was achieved by developing a hardware extension board including surge protection, filters, level conversions and a variable voltage power supply.

Due to requests by Safegate, software was written in a platform and hardware independent fashion resulting in modular and encapsulated architecture.

Evaluation of the prototype suggests that the concept, with a few adjustments, can be developed into a stable and useful product for Safegate Group International AB.

Abbreviations

Abbreviation	Description
ASP	Airfield Smart Power
CCR	Constant Current Regulator
CPU	Central Processor Unit
DLR	de LaRoche, the first woman flying solo in a powered heavier-than-air craft
EMC	Electromagnetic compability
EMI	Electromagnetic interference
I^2C	Inter-Integrated Circuit, communication protocol
IO	Input/Output (data direction)
$JTAG$	Standard Test Access Port (Used for programming MCU)
LED	Light emitting diode
LMS	Light Monitoring System
LPU	LMS/SIU Programming Unit
MBD	Microwave barrier detector
MCU	Microcontroller
MQX	A RTOS developed for embedded MCU:s
PCB	Printed circuit board
PSU	Power Supply Unit
$R\&D$	Research and Development
$RTOS$	Real Time Operating System
$Q-factor$	Quality factor
SCM	Series Circuit Modem
SIU	Sensor Interface Unit

Acknowledgements

We would like to thank our advisors, Bertil Larsson at LTH for his knowledge of electronics and Andreas Wirandi at Safegate International AB for his expertise on the ASP system and general support. We would also like to specially thank a number of Safegate employees. Björn Hammarberg for his insights on the software and control aspects of the Yeager platform. Johan Forssén for clarification of the hardware design principles of the SIU 2.0 and Yeager-platform. Alexander Strandberg for being acting advicor during Andreas annual leave and for supplying product related data. Ola Håkansson for his valuable comments regarding both past and future projects. Also Mårten Kjellson, Joakim Arnsby and Jörgen Persson for help and tips on PCB design.

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Chapter 1

Introduction

1.1 Safegate Group AB

"Safegate Group is an international company with headquarters in Malmö, Sweden and representatives in more than 50 countries around the world. The main objective for Safegate Group is to provide the airport industry with efficient solutions for more and safer aircraft movements. The solutions include operations, control and handling of aircraft on the ground, airborne aircraft close to the airport and ground vehicles at the airport. As a result of dedicated research and development throughout the years Safegate Group is today considered a specialist in its field of business. " - Safegate Group AB [4]

1.2 Project description

The master thesis was issued by Safegate Group International AB in collaboration with the institute for electrical and information technology at Lunds Tekniska Högskola, Lund University.
Safegate's product the Airfield Smart Power, ASP, system has been a part of their product portfolio for over 20 years and is constantly updated in order to maintain standards compliance and global competitiveness. Modern light sources such as the LED has enabled Safegate to develop a new ASP system with system current decreased from 6.6 A to 2 A. In order to ensure operation in this low current environment Safegate is upgrading all products in their ASP system. The focal point of the master thesis is to review and upgrade one such product, a sensor interface unit, a SIU.

1.2.1 Project primary premises

A current decrease to 2 A means that functionality concerning power availability and communication has to be examined. If the existing SIU does not meet the requirements a prototype for the 2 A system was to be designed and produced. The main goal with the prototype was to prove that creating a product which has the functionality of the existing SIU but works in the 2 A system is possible. The workflow of the master thesis can be chronologically viewed as following:

- Analyse the existing SIU and its sensors in order to collect knowledge on how its electronics and software work.
- Set-up the requirements for the SIU regarding standards, market demands, benchmarking etc.
- Evaluate if the existing SIU meets the requirements and what the best suitable solution would be.
- Risk analyze of sourcing of the components, future availability needs to be considered.
- Design a prototype and create documents such as CAD and BOM files.
- Evaluation of the prototype.

Chapter 2

Background

2.1 Implications of constant current systems

Constant current systems can be surprisingly alien to electrical engineers and the implications of such a system can feel slightly reversed.

In a constant current system a series circuit is fed with a constant current source connected to a variable load, see Figure 2.1. If the series resistance R is increased the resulting voltage V will increase in order to maintain the current I. This means that in contrary to a voltage controlled circuit where a circuit break is regarded as safe it is in the constant current case extremely dangerous, especially since the constant current regulator unit can output very high voltages.

If the current I is alternating the voltage V will alternate with a voltage amplitude of $I \cdot Z$. This means that an AC/DC converter going from constant current AC to constant voltage DC needs to control the load in order to maintain a constant voltage. [7]

2.1.1 Transformers in constant current

Connecting transformers in a series circuit creates a solution to the Christmas-lights problem where one broken light in a series circuit will stop the current in all lamps. This is because a transformer's only power losses, when the secondary side is left open, are iron core losses. This allows a series circuit current to flow even though peripherals connected to secondary sides are broken or disconnected.

An additional benefit of a series circuit with constant current is that the distributed circuit resistance, otherwise problematic in long parallel configurations,has no effect on power transformed to the secondary sides. The problem is displayed in Figure 2.2, the circuit is resistive in nature and voltage drops in the cabling results in uneven power

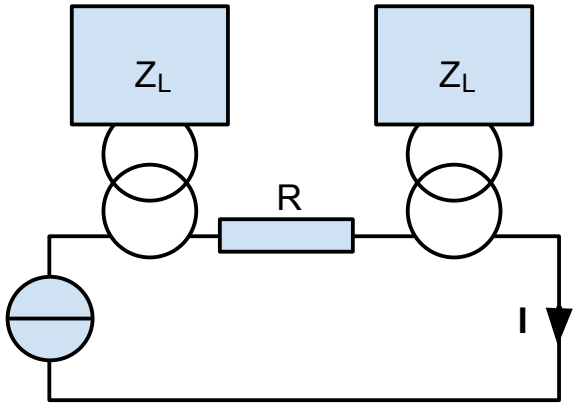


Figure 2.1: Series circuit with two identical loads Z_L connected via isolation transformers. Even if one load is disconnected the other load functions the same. The series resistance does not disrupt power distribution and only increases system power consumption.

distribution. This is especially true at airfields where cable length can be in the order of kilometers and is solved in the constant current case as the resistive cable will only increase power losses at the source.

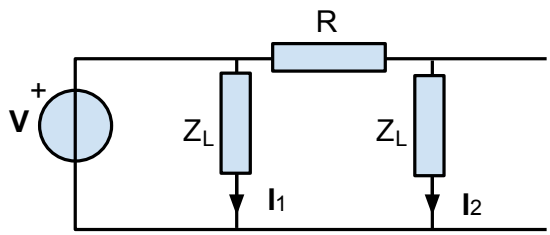


Figure 2.2: Parallel circuit with two identical loads Z_L connected. If one load is disconnected the other load functions the same but the voltage across the series resistance R results in uneven power distribution and $I_1 \neq I_2$.

2.2 The ASP System

The ASP, Airfield Smart Power, system is a product of Safegate Group which powers, individually controls and monitors a runway's airfield lighting and sensors. It consists of a constant current regulator, CCR, a serial circuit modem, SCM, and airfield units; light units and sensor units, see Figure 2.3 which illustrates the concept of a typical ASP system.

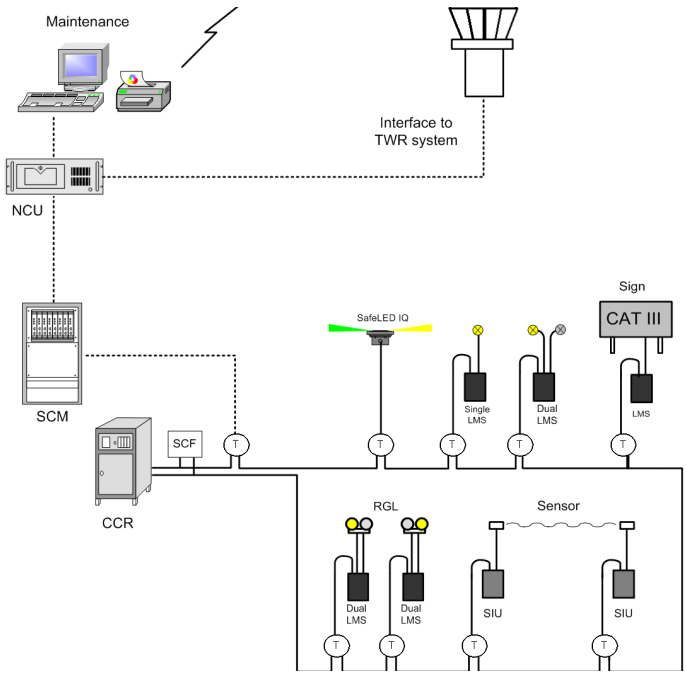


Figure 2.3: An example ASP system with interface towards control tower shown.The constant current regulator, CCR, feeds power to the units on the series circuit while the SCM is modulating the current waveform and transmitting data to and from the control tower. Picture from Safegates Reference list document.

The CCR, SCM and the airfield units are connected by an underground cable in a series circuit fed by a constant alternating current with amplitude adjustable in the interval 2 - 6.6 A and with the same frequency as the mains electricity. Between the airfield sensor, lighting units and the power cable an isolation transformer is located, it isolates sensitive electronic equipment and human contact from power line and allows current to flow through faulty equipment.

The SCM communicates with airfield units in the ASP system by sending out a signal with high frequency at each peak of the 50 Hz, in EU, power sinusoidal signal. Each such signal is decoded as either a one or a zero, depending on its frequency. A long combination of these signals translates into a message which gives directions to the units in the ASP system. The receiving units respond by modulating the supply current and the modulator frequency translates to specific answers.

The SIU, Sensor Interface Unit, controls and powers sensors on the airfield and is connected to the serial circuit via an isolation transformer. This device also handles communication between airfield sensors and the SCM.

LMS units, Light Monitoring System, has the same function as the SIU but it monitors and controls airfield lighting devices instead of sensors.

The customers of systems such as the ASP system want low cost, high reliability, high efficiency and fast response times on their airfields. There are also regulations specifying airfield system response times and therefore are both soft and hard constraints limits the system. Since the ASP system is made up of a number of large inductive and resistive loops which carries high currents, optimizing the power transfer is critical and lowering the circuit current is an appealing approach.

2.3 SIU 2.0

2.3.1 Function

A Sensor Interface Unit, SIU, powers and handles communication for sensors located on airfields. Up to four sensor units can be connected to one SIU at the same time but often one unit demands two slots and then only two units can occupy one SIU. The SIU is connected to the power cable through an isolation transformer and the sensors are connected to the SIU through one of four connectors. A picture of the unit can be seen in Figure 2.4.

The most common sensor used together with the SIU is the microwave barrier detector, MBD. The MBD consists of a microwave transmitter and a microwave receiver, they are placed on each side of e.g. an airstrip and if the microwave signal does not reach the receiver, an airplane is presumed to be located between the transmitter and receiver. Each MBD pair needs two connectors, one with an input pin and the other with an output pin. The SIU signals the MBD through the output pin and that triggers the transmitter to send a microwave signal and the receiver to listen for it. If the receiver senses the signal it will change the input pin and the SIU will signal that no airplane was detected. If the microwave signal detection times-out, the SIU will assume that an airplane is blocking the signal and will send a detect message.

Figure 2.4: A sensor interface unit. The long cable is the connector to the isolation transformer and the four connectors are sensor ports.

Power converter

The connector to the isolation transformer has two pins which are directly connected to the secondary side of the transformer. In order to obtain a stable DC voltage the constant current is fed through a second transformer and is then rectified. This rectified voltage is then controlled to a constant level by shorting the second transformer when a desired voltage is reached. As the time constant of the control system is long, large bulk capacitors are used as current buffers. A SIU can provide 7.5 W of power to external sensors.

2.3.2 Connectors

The SIU has five connectors; four sensor connectors and one connected to the isolation transformer.

The power line is also used by the SIU to communicate with the ASP system. The SIU high-pass filters the power signal to remove the 50 Hz carrier signal and detect the signal with high frequency received from the ASP system. To send an answer back the SIU uses the DC voltage load hardware and switches between loading the capacitance and short circuiting the transformer in the desired frequency, this will modulate the carrier signal enough to be noticed by the receiver in the ASP system.

IO-connectors

The IO connectors have 8 pins each and the connectors' pins are connected in parallel, i.e. pin 1 on the first connector is connected to pin 1 on the fourth connector. The 8 pins are:

1. ground pin
2. power source pin
3. input
4. input
5. input/output
6. input/output
7. output pin
8. not connected

The power source pin can vary between 12 V / 15 V / 24 V and this can only be configured in the software. The input/output pin direction is configured in software. The IO pins are pull-up configured and not constructed for high frequency use, see Figure 2.6 for a SIU output sketch and Figure 2.5 for an input sketch. The usual set-up is that a sensor reciever/transmitter pair is connected to a SIU using two ports. As each port is connected to the same pins internally configuration is required to set pin direction.

2.3.3 Software and Flashing

The SIU enclosure is filled with electronic potting material in order to ensure that it will not come in contact with moisture or dust. Because of this there is no support for upgrading the firmware. Each unit is programmed and tested before being sealed, which also means that the functionality of the SIU is final for each unit. Therefore extensive troubleshooting is necessary to avoid faulty software in unupgradable units.

The configuration of each ASP system is unique and a number of software parameters in the SIU can be changed to accomodate for this. By shorting the power source pin to ground, the SIU is placed in parameter configuration mode and the user can change all the parameters. Some of the parameters can be configured during operation by the user. The parameters are unique for each individual SIU. All parameter changes are made by sending out a message on the power line.

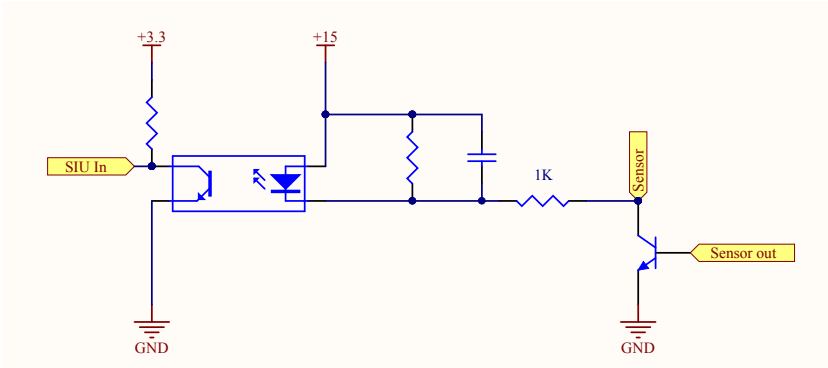


Figure 2.5: Simplified sketch of a SIU 2.0 input connected to a sensor output. The node marked with Sensor *illustrates the physical connection of the two units. By connecting the* +15 V *supply to ground via the NPN transistor data can be sent to the SIU.*

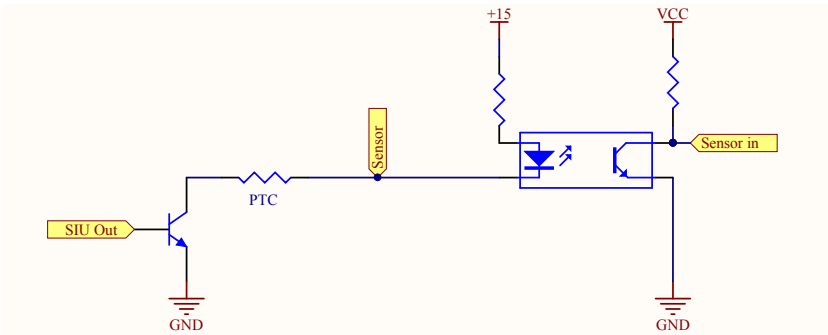


Figure 2.6: Simplified sketch of a SIU 2.0 output connected to a sensor input. The node marked with Sensor *illustrates the physical connection of the two units. The SIU grounds the signal which drives a current through the opto-isolator on the sensor side. This transmits data to the sensor.*

2.3.4 Essential Specifications and functions

A future version of SIU has to be backwards compatible, but not all features are essential to keep. Indispensable features of the existing SIU are listed in the bullet list below.

- **IO functionality**, a future version of SIU has to be able to interact with sensors in a similar way as the existing SIU and with at least the same communication speed.

- **SCM communication**, the SIU has to be able to communicate with the SCM in the same way as today.
- **Power supply**, the voltage level and maximum power output can not be decreased in future versions.
- **Power efficiency**, the power loss of the SIU should not increase.
- **Product cost**, the cost of producing the SIU can not increase.

2.4 Yeager platform

Safegate International AB has developed a new platform codenamed the Yeager platform, which function is to control and monitor the lighting units in the ASP system. The platform is an upgrade in both hardware and software for the lighting units.

Other functions of the platform include controlling and powering LED and upgradable firmware.

2.4.1 Communication

The ASP communication in the Yeager platform follows the same principle as the SIU. Sending high frequency signals on the peaks of the power signal by switching between loading the power source capacitance and short circuiting the power input pins will output a signal on the power cable. By filtering the AC current signal on the power cable, the signal sent by the ASP system can be detected.

2.4.2 Power supply

The AC current between the power pins is transformed and switched into a stable 48-60 VDC power source. This voltage source is used to power the lighting unit and the LED drivers it is connected with.

2.4.3 MQX

The software in the Yeager platform uses the real time operating system MQX, a product from Freescale Semiconductor Inc, supporting threading with components such as events, logs, timers and semaphores. MQX also has a full USB and ethernet stack and a number of high level features such as a FAT-like filesystem. A different version of MQX called MQX-lite contains only RTOS essential parts such as a scheduler, semaphores, mutual exclusions and low level tools for concurrent programming.

Chapter 3

Product planning

Product planning was done by first identifying what a SIU was in terms of a product. Questions like why the SIU had to be upgraded was at the core of the planning phase and finding strengths and weaknesses of the current design was crucial. Many simulations were done on the SIU 2.0 in *LT-Spice*, a simulation tool for analog electronics, in order to understand the product from a hardware point of view.

Other questions were answered by people using and installing SIU:s on airfields. When problem areas was found they were all weighed together and assigned priorities in order to outline the product development. After the main points up for upgrade was identified, a concept generation phase where features of a future SIU and different implementations with the same functional goal went through a process of elimination. Here some features requested by the earlier more general investigation was scaled down or removed in order to contain the project within the original master thesis scope.

3.1 Review and target specification

After identifying weak points of the SIU 2.0/2.1 in the 2 A-system a number of tests was conducted, all of which can be found in detail at Appendix A. Tests concluded that the SIU 2.0 did function in a 2 A environment, at least under laboratory conditions. Though, when interviewing SIU 2.0 installers and technicians they noted that there were situations when the SIU underperformed, both in the 2 A system and the 6.6 A systems. Key points touched upon was:

- Native 2.0 - 6.6 A support due to reported problems in field
- Increase the supply power well above the current 7 W, reports indicated that a new SIU would require at least 10 W
- Add status indicators for the different outputs.
- Firmware upgradeable on sealed unit.
- Upgrade electronics to modern surface mounted components.
- Serial protocol to extend what the SIU can interface against

After interviews with people at the Safegate R&D department's hardware engineers working on a similar upgrade of the ASP light monitoring units noted the similarities of the two systems. The platform for light monitoring, codenamed the Yeager platform, could work as a base for the SIU 3.0.

As this platform was developed for 2 A output from the CCR, having modern electronics and already had gone through thorough testing it was deemed the only suitable direction for the project.

3.2 Concept generation

Only the concept deemed relevant are included and discussed in this report.

3.3 Concept selection

3.3.1 Communication

Concepts

- Only SIU 2.0 IO mode
- Serial communication protocol and SIU 2.0 IO
- Serial communication protocol and SIU 2.0 IO with hub

Review

When reviewing the need for a serial protocol, considering that the bandwidth of the ASP system is limited, the use of bandwidth has to be strongly motivated. The need for a serial protocol seemed most important for sensors measuring analog signals, such as temperature and wind. These sensors could as easily be implemented with a wireless protocol and then use the SIU PSU and still save the same amount on the installation costs and lower ASP overhead.

As Safegate's sensor units does not use any serial protocol a message routing hub would be required to interface towards them. This increases installation complexity but makes the SIU a more generic IO unit.

3.3.2 Power supply - rating

Concepts

- Marginal increase to 12 W
- Large increase to 25 W
- Great increase to 60 W

Review

After reading the reports there were incidents where the current 7 W was barely enough. When using two pairs of sensors and heating kits the SIU loaded around 10 W of power which is above the current rating. Also, late into the project a new specification came for a related product. The need to draw 60 W at 24 V which no other product can supply.

A marginal increase of 12 W would allow the SIU 3.0 to use cheap small fully integrated buck converters operating at less than 1 A.

A large increase to the region of 25 W would require a buck controller with dedicated switching MOSFET and diode or two fully integrated converters at 1 A each. This would set a high limit for future needs.

60 W of power would still only require one buck controller converter with dedicated switching MOSFET and diode but the ratings of all switching components, inductors, capacitors, MOSFET and diode would have to be able to carry currents of up to 3-4 A. Also the PCB wires conducting these currents would take a larger footprint. Switching losses would also double requiring thermal design considerations.

3.3.3 Power supply - converter

Concepts

- Controlling the Yeager DC level using software
- Buck converter controlled by MCU
- Buck converter controlled by dedicated IC

Review

The Yeager platform has an onboard AC/DC converter set to 48V-55 V for internal use. This DC voltage could be controlled down to a lower voltage directly by changing the DC control loop. This would however impact other systems that may or may not be developed to work at the 48 V level. Also, as the CCR is running at 2 A setting the AC/DC converter to 12 V would limit total board supply power to 24 W which may be too little.

MCU controlled buck converter saves on IC costs but would require CPU resources to measure current and voltage in order to keep current ripple low. Also, in order to minimize cost, footprint size and communication disturbance the switching frequency should be well above the ASP communication frequency. High frequency switching could however make the feedback loop sensible for disturbances and care would have to be taken during wire tracing.

Buck converter controlled by dedicated buck controller IC would increase reliability at the expense of footprint area and component cost. However, thanks to controllers operating at close to 1 MHz inductor sizes and capacitor sizes decrease and become cheaper. Also built in short circuit protection is a common feature useful in this application [1].

3.3.4 Input indicators

Concepts

- External LED indicators
- Internal LED indicators
- Graphical display

Review

An external LED indicator would increase cost as it would have to uphold the protection class of the enclosure itself. Socket mounted IP67, [8] LED indicators were found to be expensive, according to retailers such as FARNELL et cetera, and this limits the number of indicators to one or few. However, multicolored units could still signal input status of all ports in a slightly clumsy way.

Both internal indicators and a display would require transparency of the enclosure. Also due to Safegates policy to pot all electronics in protective black molding plastic a way to lead light through this needed.

A display would thus require a transparent molding plastic and an enclosure with a transparent lid. Transparent potting material was found but as Safegate has done extensive tests on the currently used plastic this was not a tempting solution.

Internal LED indicators would require a box with transparent lid, but the problem of potting material could be circumvented by using lightguides higher than the electronics reaching above the molding mass.

3.3.5 Firmware flashing

Concepts

- Additional pins for JTAG
- Shared JTAG/IO pins
- Separate external JTAG connector

Review

Adding pins to the connector would increase the number of pins needed by five. This means that a connector with at least 11 pins would have to be used. The existing connectors have only one spare pin making a connector change necessary if the number of pin where to be increased. This also decreases backwards compatibility as special cables would be needed in this situation.

Shared JTAG/IO pins enables the use of existing connectors using the spare pin as a JTAG 3.3 V supply and the rest of the pins changing function depending on use. The problem would be enabling the pins to be used both in 12-24 V IO and 3.3 V IO. This increases hardware complexity at the electrical level but decreases connector and compatibility costs. Using the same pins also enables the input filters to be the same and this will possibly reduce costs compared to the first solution.

Adding an external JTAG connector enables the SIU to both be backwards compatible and externally flashable. The disadvantage is additional costs related to adding a high quality connector.

3.3.6 Software

Concepts

- Extending current Yeager software
- Writing new software

Review

Software currently written for the Yeager platform is using the proprietary MQX real time operating system. The software works well and the algorithms are efficient but lacks architectural design, a problem brought up by software developer Björn Hammarberg. A request from him was to oversee possible improvements.

3.4 Final specification

3.4.1 Communication

Only SIU 2.0 IO Because backwards compatibility with sensors are important and bandwidth is limited on the ASP system, SIU 3.0 will only use SIU 2.0 type of IO. In order to comply with FAA regulations IO surge protection is necessary [3].

3.4.2 Power supply - rating

60W PSU Due to a customer request of a 50W PSU connected to the ASP grid, 2.5 A was chosen as the max current which corresponds to 60 W at 24 V. The final specification was therefore set to 30W at 12 V, 37.5 W at 15 V and 60 W at 24 V.

3.4.3 Power supply - converter

A buck controller IC with dedicated mosfet A buck controller IC makes the design more robust than a software solution. It also frees up CPU cycles. Due to the power supply rating a discrete switching MOSFET is required.

3.4.4 Input indicators

LED:s and lightguides The requested feature was IO indicators and adding a graphical display over-complicates the design. Surface mounted LED:s together with light guides which transport light through the potting material was chosen as the configuration to be implemented.

3.4.5 Firmware flashing

Shared JTAG/IO In this prototype shared JTAG/IO pins will be implemented. The increase in hardware complexity will be evaluated to see if it is a better solution than the JTAG port which introduces a higher cost. Also as the IO has to comply with FAA regulations using the same IO filter for JTAG and sensor IO reduces costs.

3.4.6 Software

New software on new architecture Creating new software for Safegate International AB seemed the most interesting and rewarding solution. A new architecture based on the following design philosophies was to be created:

- Encapsulation
- Loose dependencies
- Platform independence

Application code will be limited to sensing inputs and communication over serial bus.

3.4.7 Costs

Not more costly than SIU 2.0 As this is a prototype development focus lies on reducing total component costs and to minimize risk of component shortages. Secondly all prototype features will be implemented with producibility in mind but concepts such as connector mounting, enclosure type and board mounting are left out. SIU 3.0 will have increased functionality and as such a cost decrease is over-ambitious and cost reduction measures could be a separate project. Instead target cost will be defined as *not more costly than SIU 2.0*.

3.4.8 Standards compliancy and protection

IPC, FAA-STD-019e In order to later comply with IPC standards and FAA regulations a few precautions has to be taken. The main regulatory body is the FAA-STD-019e paper which states that hardware must be able to withstand surge currents of 10 kA up to 1000 times on the supply line and 1 kV / 1 kA on data lines at least five times.[3]

EN 61000-6-4: 2001 Electromagnetic compatibility must also be taken into account and the project goal is to comply with generic emission standard EN 61000-6-4: 2001 which states allowed radiated emissions from 30 to 1000 MHz as per EN 55011 class A. [2]

Short circuit protection Short circuit of the output protection is also required as it is used as a feature in the existing SIU for entering parameter update mode.

Chapter 4

Product development

4.1 System level design

4.1.1 Hardware

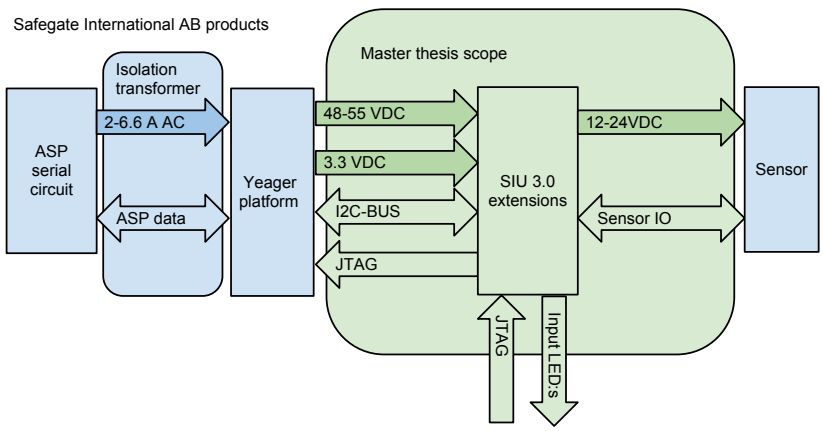


Figure 4.1: Hardware design sketch using arrows indicating data/power transitions. Green areas displays the scope of the master thesis. In order to reduce the number of IO pins required of the Yeager CPU an I^2C IO-expander is used.

The decision to build the SIU 3.0 on top of the Yeager platform ment connecting new peripherals to existing hardware. By matching the PCB area, mounting holes and

connecting a female header on the back facing the Yeager the cards are physically stackable. The purpose of this is to enable a combined unit capable of SIU 3.0 functionality without creating a new PCB with the combined components.

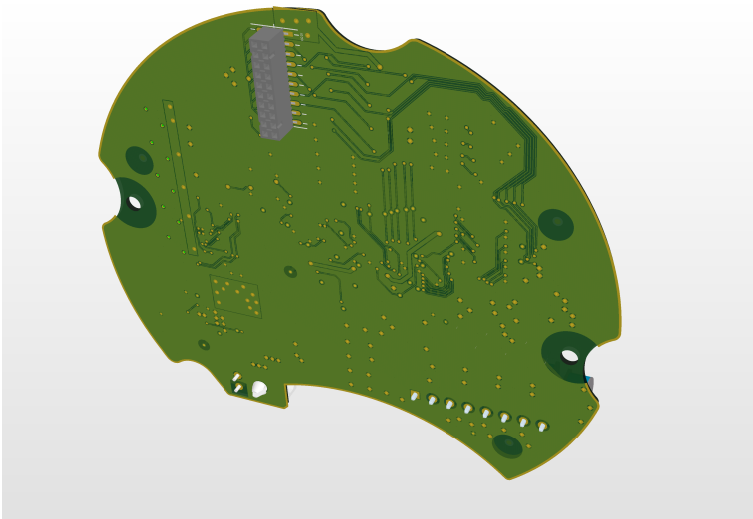


Figure 4.2: Female header used to slot the two cards together.

The female header is the JTAG port on the Yeager platform. According to Figure 4.3 additional ports have to interface between the Yeager platform and the SIU.

The 3.3 V and I^2C bus are connected by a ribbon cable previously used for interfacing LED drivers on the Yeager platform. The bulk DC voltage is soldered onto the Yeager PCB and connected to the SIU expansion.

The Yeager circuit is controlled by a MCU produced by *Freescale Semiconductors*, K10P144M120SF3, 120 MHz. The controller has support for all features required by the new design for the SIU such as I^2C and a RTOS, *MQX*.

4.1.2 Software Architecture

The software architecture of the SIU 3.0 was completely rewritten to improve the expandability of application code. This was achieved by encapsulating code and create loose dependencies between modules. Due to the limited computational power of embedded CPU:s and requests of Safegate the code was to be written in C even though design philosphies such as loose dependacies and encapsulation more easily achieved in object oriented languages such as C++.

Encapsulation in C is achieved by following strict convensions and containing code in modules that preform specific tasks. To simplify design code patterns developed by Adam Petersen were used as a base for the architeture. [5]

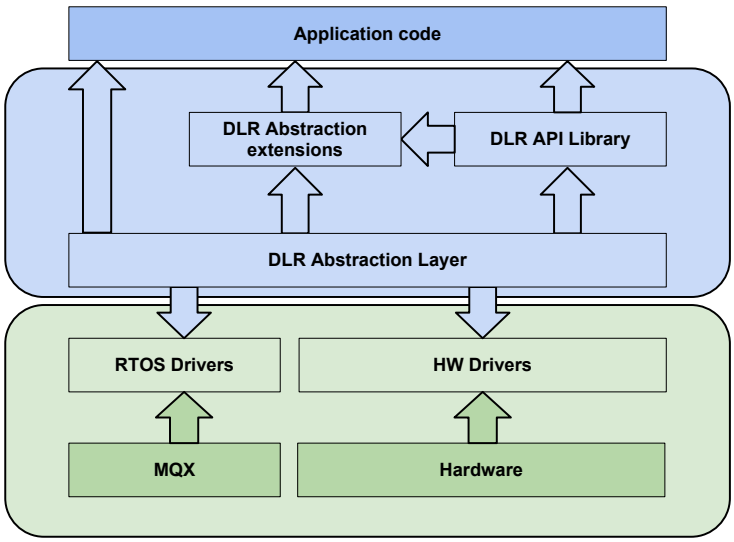


Figure 4.3: Software architecture, DLR or de LaRoche is the name of the prototype platform. Arrows indicate include directions, note that no code written in the blue layer includes code of the lower layer.

The driver subsystem was created by using structures defining function pointers to functions associated with a platform specific operation, such as thread creation or IO toggling. This abstraction of functions nested in structures creates code can be compiled and run on any system. The abstracted structures and functions are labeled as the DLR layer which is an abbreviation for de LaRoche which was the first woman flying solo in a powered heavier-than-aircraft. This in contrast to the Yeager platform which was the first man to break the sound barrier. A typical DLR abstraction structure can be seen in code section below, in this case the *DLRTask* module:

```
#include "DLRTask.h"
struct DLRTask
{
uint32_t stackSize;
uint32_t priority;
DLRIndex index;
TASK_LIST task;
TaskEntryCallBack taskEntryCallBack;
DLRData param;
};
// Function pointers to driver implementations
static TaskSetPriority setPriority;
static TaskGetTickTime getTickTime;
static TaskSleepUntil sleepUntil;
```

In this section the function pointers setPriority, getTickTime and sleepUntil are abstractions of functionality required by the application layer, the struct in this case, has only one function pointer taskEntryCallBack. The callback function is a function pointing to the entry-point of the thread and the module handles communication between the abstracted level and the underlying OS to ensure expected operation.

In order to not include hardware/OS related code in the *DLRTask.h* the binding of the function pointers are called from the low-level subsystem, this means that, if not configured correctly, code can compile and run but the behavior will be undefined. This problem is solved by using error messages notifying the user about configuration problems.

By abstracting the hardware/OS a generic framework can be created which enables code from related products in the Safegate portfolio that might not share hardware and/or RTOS but do share functionality to be reused. Using the abstraction layer an API, application programming interface, was created to simplify application programming and further encapsulating commonly used objects such as buffers, hash tables and events.

4.1.3 Software Application

Application code will be limited to software keeping the Yeager platform operational and sensing the SIU 3.0 IO extension ports. No ASP communication will be implemented as the focus on the software was mainly architectural and in a prototype stage.

4.1.4 Costs

Throughout the design process concepts have been weighted mostly on robustness as this have been the main priority. However as concepts are chosen measures to minimize component price and as importantly maximize component availability has been undertaken. Wherever possible generic component series have been used. In order to minimize production costs the components chosen are of surface mounted types placed on a two layer PCB.

Due to the stackable board design total manufacturing costs might be decreased if a board was developed merging the Yeager platform with the new extension. But the total costs may also be lower for the stackable design due to mass manufacturing of the airfield controller. Either way it is deemed to be outside the scope of this master thesis and thus not further discussed.

4.2 Detailed design

Implementation of hardware and software has been a highly iterative procedure where much time was spent first realizing a solution and then checking for components online to verify feasibility. Here detailed design of the most critical modules of the SIU 3.0 and a short motivation of the actual implementations are collected.

4.2.1 Power supply

Goals

- Supplying in excess of 50W of power at 24V.
- Short circuit protection.
- Surge protection.

Problems

High voltage of bulk DC Because the Yeager platform DC can reach 60V all components on the high side of the converter needs to be able to handle this voltage.

Relatively high current As the rating was set to *in excess of* 50 W at 24 V the product was developed with a safety margin of 20% resulting in a 3 A maximum current.

Switching interference Interference from switches must not interfere with buck regulator feedback nor ASP communication.

Fast short circuit protection If shorting the converter should be used as a feature to enter programming mode no damage can be taken when tripping it.

Solution

A buck controller IC was implemented together with filter components controlling a MOSFET switch.

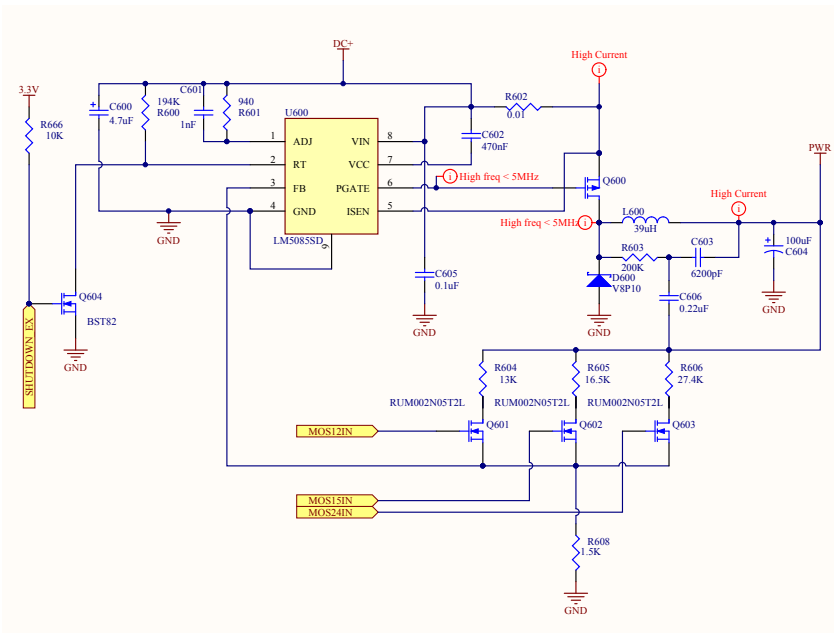


Figure 4.4: Buck controller IC and filter components. Feedback division is either by a digital potentiometer or by a MOSFET-resistor array but only the array configuration is shown in the picture. DC+ marks the high voltage DC and PWR the output. Q604 and signal $SHUTDOWN\_EX$ is used to turn off the buck controller.

Output voltage from the controller is regulated by feedback from the output voltage itself. The voltage reference level is set by dividing down the feedback voltage in a voltage divider, see Appendix B for a detailed description. As this voltage division needs to be dynamic in order for the output voltage to be able to change at least one of the feedback resistors must change resistance. Two implementations of this was done on the prototype, one where a digital potentiometer acted as the top feedback resistor and one where a MOSFET array was used to change which resistor the feedback current was led through. Only the MOSFET implementation is seen in Figure 4.4 here R608 is the low side feedback resistor and R604, R605 or R606 the upper feedback resistor depending on software configuration.

High voltage of bulk DC A high voltage version of Texas Instruments buck regulator, LM5085, was used. This together with high voltage ratings on high side capacitors, rated at 100V and a high voltage switching MOSFET capable of isolating up to 100V ensures safe operation.

Relatively high current Using a MOSFET with low enough on resistance paired with relatively low gate capacitances was essential to limit switching losses and conduction losses.

The switching p-MOS used has a approximately 0.625W of conductive losses and 0.3W of switching losses at average frequency of 450 kHz. See details in Appendix B.

Switching interference In order to reduce communication interference and decrease switching inductor and capacitor sizes the average switching frequency was set to 450 kHz. This is because the switching frequency is proportional to output voltage and changes depending on output configuration. See details about the switching circuit and related calculations in the Appendix B.

To minimize feedback interference the switching components were grouped together in order to shorten potential antennae length. Also the feedback wire was traced perpendicular to the switching inductor's magnetic field. In order to further minimize emission a shielded inductor was used with limited frequency response. See Appendix B for more details.

Surge and short circuit protection The integrated buck controller has a built in short circuit protection scheme but due to shorting the power supply is used as a means to set the SIU in parameter update mode a second system was implemented on top of the other.

By using an operational amplifier U502A to measure the voltage drop over shunt resistor the current is measured. If the current reaches 2.7 A the comparator U501

triggers thyristor SCR500 which in turn grounds the gate of n-mos Q500 causing the gate of Q502 in p-MOSFET to reach *PWR* voltage. This increases the gate-source voltage of Q502 to 0V which causes the p-MOS to break the current.

Surge protection is achieved by using gas discharge tubes for high current surges and transient suppression diodes for smaller currents with higher on time.

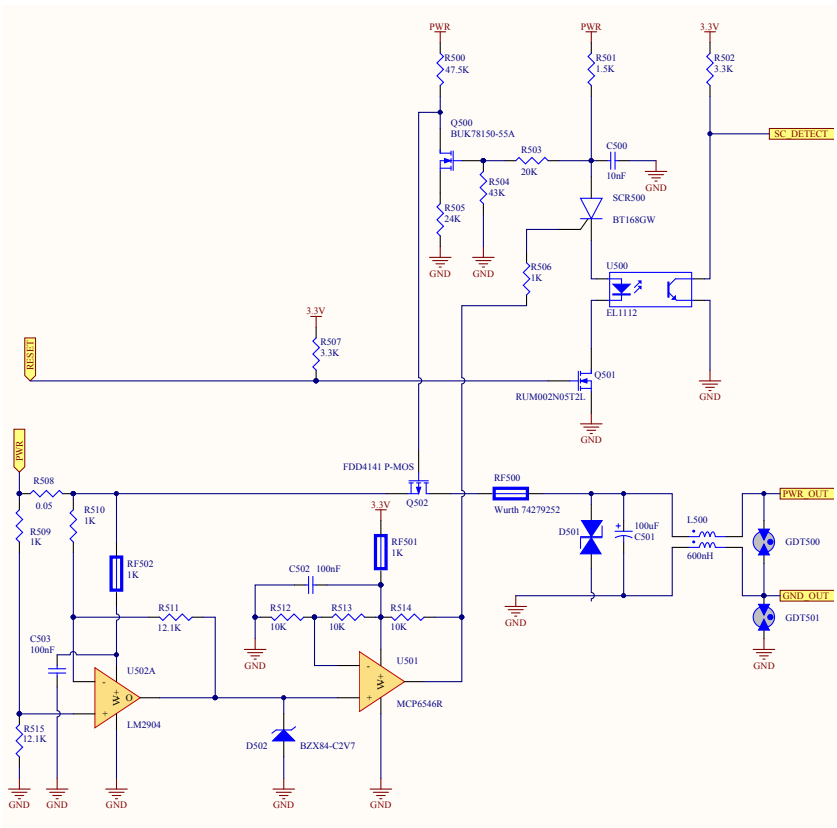


Figure 4.5: By sensing current through a shunt resistor a comparator triggers a thyristor if the current reaches 2.7 A. As the thyristor grounds the gate of n-mos Q500 the voltage at the p-MOS Q502 increases to PWR*, which is the PSU voltage. This means that the gate-source voltage stops being negative and break the current through it.*

4.2.2 JTAG module

Goals

Providing a JTAG connector through pins shared with higher voltage IO.

Problems

Overvoltage protection As the IO pin is shared between JTAG and higher voltage IO there must be hardware protection against enabling JTAG while 12-24 V pull up is enabled.

Low impedance for high frequency JTAG signal The impedance path towards the CPU must be low for high frequency JTAG signals. Filter time constants must be significantly higher than the period of the JTAG signal. This is a problem since many protection devices are of capacitive nature.

Solution

Surge protection filters had to be of low capacitive nature, this was achieved by methodology described under the IO protection section below.

Also the over voltage protection had to be of low pass nature in order to not corrupt the JTAG clock and data signal.

Because a zener diode's capacitance increases when the voltage V_Z decreases, for *BZX84* it is 450 pF for $V_Z = 4.3\,V$, care was taken not to disrupt the signal by adding impedance between the zener diode and ground. The protection circuit triggers when the voltage level on the node PIN_PROT exceeds 4.3 V, as this causes the zener diode D703 to conduct the voltage across C700 increase causing Q706 to ground the *PROGRAM* node once reaching above V_{th}. Zener diode D705 is placed to protect Q706 from over-voltages and R710 together with C700 determines the time constant of when the protection resets.

All MOSFET:s in the design with a connection to the PIN_PROT node (the shared sensor IO and JTAG node) are chosen to have low capacitance between drain and ground. If *PROGRAM* is high the Q705/Q707 MOSFET pair will provide a low impedance bidirectional path to the CPU pin for the JTAG signal.

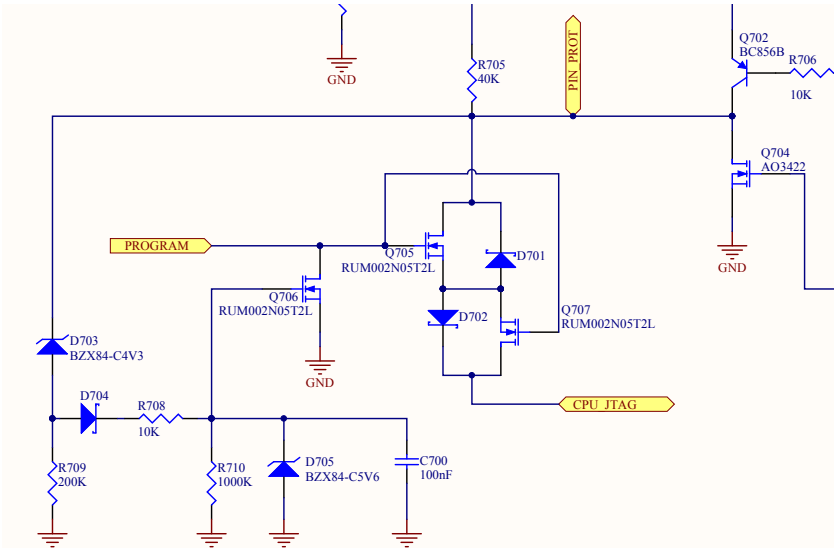


Figure 4.6: JTAG pass through circuit and protection. Q706 is used to ground the program signal if a excessive voltage is sensed on the PIN_PROT node. Q705 and Q707 together with diodes D701 and D702 pass the JTAG signal if node PROGRAM is high.

4.2.3 IO level conversion

Goals

Providing a SIU 2.0 compatible IO interface towards MBD:s and other sensors. A way to sense if an IO is input or output.

Problems

Voltage level conversion Creating a robust voltage level conversion between 12/15/24 V and 3.3 V levels.

Sensing the IO type and plug and play By using the input to sense if an external device is trying to access the pin as an input or as an output.

Solution

In order to sense IO type the old method of SIU 2.0 which used an opto-coupler to sense current when used as an input could not be used. Instead a transistor stage using the 3.3V as reference was used to separate low and high voltages. By using a silicon transistor and diode, D700 and Q701 in Figure 4.7, the temperature dependant voltage drops cancels each other.

A low pass filter on the collector of the Q701 PNP-transistor cancels high frequency noise on the signal path. The filtered output is used to ground the voltage on the CPU_INPUT by using the Q700 NPN transistor.

When configured as output Q704 is used to ground a voltage applied by an external device. The input/output pair matching works by sensing if a PIN is currently expected to be an output by sensing for an external pull up. Using the output pin to send a signal the SIU will then wait for an response on any of its remaining IO lines. This pairing process will be done for all inputs.

4.2.4 IO Protection and filter

Goals

- Repeated ability to suppress surges of 1 kA or 1 kV surges without permanent damage to hardware.
- ESD protection suppressing surges according to human body model without disrupting functionality of the SIU.
- Protection should not disrupt a 1000 kHz JTAG signal.
- Protecting against short circuit during IO grounding.
- Minimizing EMI from long signal cables

Problems

High power surges Protecting against high power surges requires a low impedance path for the disturbance past sensitive electronics.

ESD protection The human body model is less demanding than the real world situation but still requires adequate filters in order to divert transients.

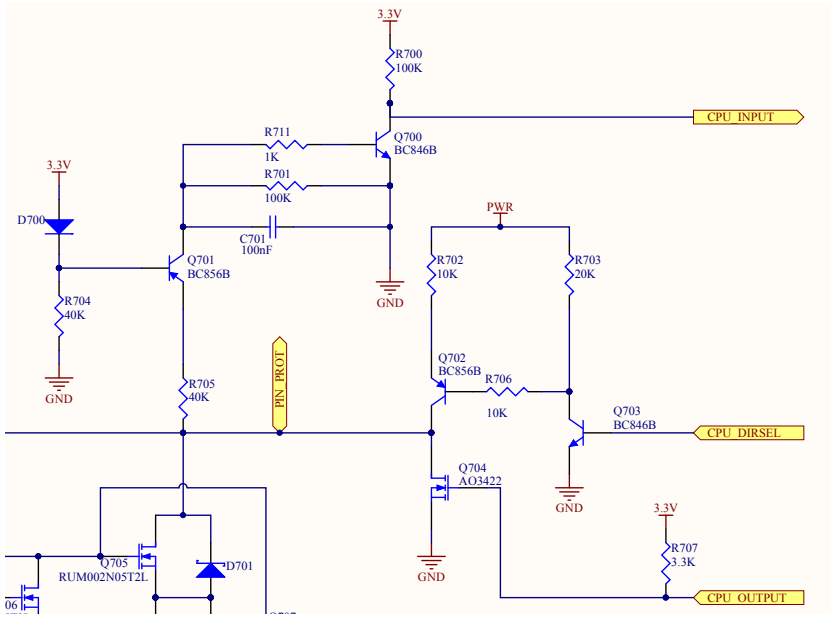


Figure 4.7: When the SIU is configured for output Q704 grounds the PIN_PROT node and an external device senses the resulting current increase or voltage drop. When configured as input Q703 pulls a current through Q702 pulling up the voltage on the PIN_PROT node. When an external device pulls the voltage below 3.3 V Q701 stops conducting and Q700 as well resulting in a level change on the CPU_INPUT node.

Capacitive implications Surge protection devices must be designed with the high frequency JTAG signal in mind. This limits the inductance and capacitance that can be added to the filter. More importantly, as connected IO cables can be of any length, from 5m to 15m, measures to decrease these cables acting as antennae must be taken and a balance between added capacitance to ground and JTAG signal deterioration must be found.

Solution

By using gas discharge tubes together with integrated transient blocking units, TBU:s, surge currents and over-voltage is handled. The chosen TBU:s have a trip time of $1\ \mu s$ and trips when sensing more than 200 mA. Small transient currents managing to pass through the circuit breaker are led to ground via a transient voltage suppression diode.

In order to limit emission due to capacitively coupled VH-frequencies and above a 220 pF EMI filter is installed.

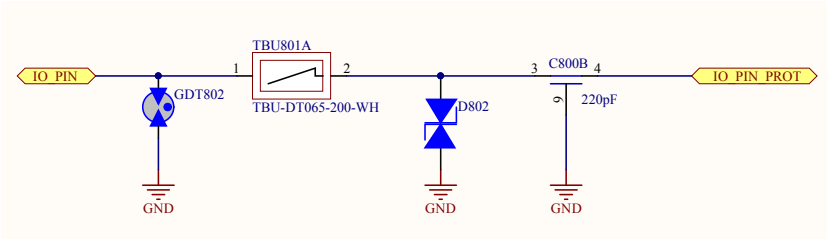


Figure 4.8: The transient blocking unit limits current to 200 mA which causes a surge increasing the voltage on the input. When reaching the GDT arches the current to ground.

4.2.5 LED indicators

Goals

- To see the LED indicators outside the enclosure
- Display error codes and IO status

Problems

The LED:s need one pin controlling them each, either by multiplexing or direct CPU access. As CPU pin access is constrained on the extension board this is a problem. Also, many LED modules with light guides takes up large footprint area.

Solution

In order to decrease the number of needed LED:s two-colored modules are used. One color will be used for active and one for a passive IO state. The third color, when the two individual colors are active, will be used to encode binary status messages.

Surface mounted diodes will be enclosed by light guides taller than all other components and will thus appear through the potting material.

4.2.6 Software

A detailed software description would describe the inner workings of the ASP-system. This section is deliberately leaving low level information out.

Goals

- Keeping the Yeager platform operational
- Sensing the SIU 3.0 IO extension ports
- Ability to set the protorype to programming mode

Solution

The application code will be divided in to the following modules:

- DirectCurrentRegulator
- PhaseTracker
- PowerFactorControl
- PowerSupplyUnitControl
- SensorInputOutput
- SensorInterfaceUnitStateHandler

DCRegulator Will control the bulk voltage to a desired level with a simple PI controller.

PhaseTracker Synchronizes a timer with the mains frequency for use in other modules. This is done by correlating a sinus table to the sampled data and iteratively adding lag to one signal. The lag corresponding to the largest correlation is used as an error term in order to lock the internal phase to the external mains phase.

PowerFactorControl Safegate AB has specified all their converters to have a Q factor above 0.99. This requires control of the current/voltage phase-angle and code related to this is found in the *PowerFactorControl* modules.

PSUControl Sets the SIU 3.0 output voltage to desired level by controlling either the I^2C potentiometer or the MOSFET array (see Figure 4.4). Also monitors the overcurrent protection device and resets it if necessary.

SensorIO Handles the IO bridge extensions, will later be where inputs from sensors will enter the software.

SIUStateHandeler Sets the SIU in programming mode or firmware flashing mode depending on external events.

API In order to decrease rewriting of code a number of libraries were built on-top of the produced DLR abstraction architecture. Some of the more important modules created are listed below:

- Hash Map
- Event
- IIRFilter
- PIDController
- Ring Buffer

Chapter 5

Product evaluation

5.1 Hardware tests

In order to evaluate hardware functionality on the extension board a number of tests were conducted. To decrease tested variables the amount of software required to conduct tests were kept at an absolute minimum. By testing isolated parts of the hardware cascaded modules become easier to debug. The detailed testing method of all the peripherals can be found in Appendix C.

All hardware tests were done on the same circuit and all voltages were measured with the oscilloscope LeCroy waveace 234.

5.1.1 Level conversion

To ensure operational ability, tests were conducted verifying frequency behavior on communication both in to and out from the SIU extension. The tests conducted were:

- Frequency sweeps on the IO ports configured as outputs at 10 - 500 Hz with low duty cycle to study the resulting waveform.
- Frequency sweeps on the IO ports configured as inputs at 10 - 500 Hz with low duty cycle to study the resulting waveform.
- 12 and 24 V IO conversion to 3.3 V CPU IO to ensure good high and low logic levels.

5.1.2 JTAG pass-through

The JTAG pass-through has two critical points. Frequency behavior, as JTAG signals can be in the megahertz region, and over-voltage protection. The over-voltage protection is not designed to react to transients occurring while programming, but for ensuring that an active high level IO port will not couple the 12-24 V IO directly to the CPU pin. Lastly the feature to power the board over a pin and simultaneously set the SIU to programming mode was tested on hardware level.

JTAG ports frequency behavior was tested by applying a 100 to 1000 kHz symmetric square wave on the pin and observing the internal response. The over-voltage protection was tested by applying a high voltage low frequency signal to the IO port. The filter is designed to keep blocking JTAG pass-through for a second after an over-voltage is detected. As such the duty cycle was set low and the frequency decreased until a measurable portion of the high voltage signal passed through.

Due to errors in calculating the zener voltage for diode D703 the over-voltage protection supressed voltages down to 3 V. As such tests were done with lower amplitude.

5.1.3 Power converter

The power converter was tested by using a current limited DC source at 30 - 48 V connected to the extension board. As the configuration of the converter is normally done in software the different logic states had to be set by connecting test points to 3.3 V sources. A $15\ \Omega$ load was used and tested in 15/24 V configurations. Voltage and current ripple was logged during the tests and compared to theoretical expectations. By logging a load change from $15\ \Omega$ to a circuit break the load step-response of the converter was found.
An IR-camera was used to capture component surface temperature while the power converter was connected to a $15\ \Omega$ load. The IR picture was captured both initially and after the temperatures had stabilized.

5.1.4 Short circuit protection

Short circuit protection was to be tested by feeding the current sensing resistor with a current controlled source and increasing the current until the short circuit protection tripped. However during testing the power converter a problem in the short circuit protection was found hindering current to reach the output pin. The protection MOSFET Q502 in Figure 4.5 was not conducting. Through throubleshooing the problem was identified and corrected by disabling the short circuit protection.

5.2 Results

5.2.1 Hardware

Designed hardware resulted in the manufactured PCB, see Figure 5.1.

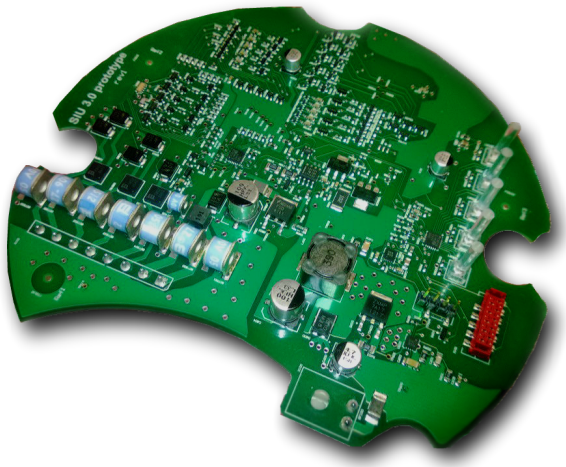
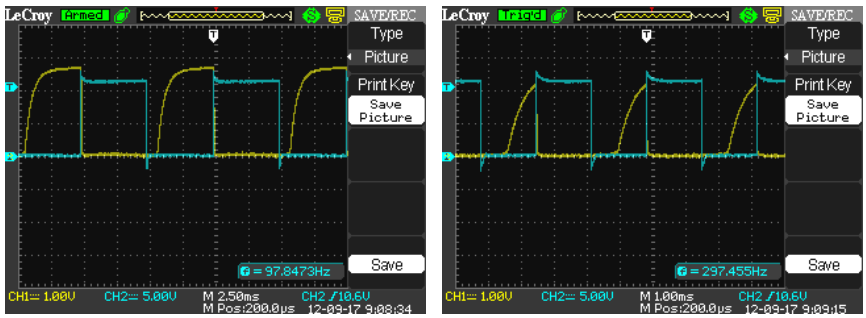


Figure 5.1: Finished hardware SIU 3.0 prototype PCB with components.

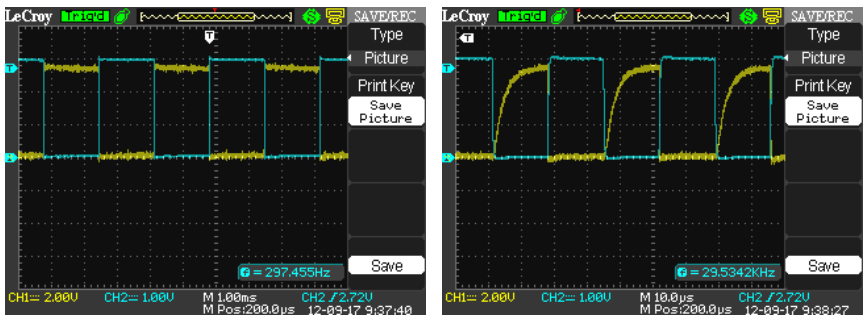
Level conversion

Test results on the 12V voltage sensor input and the level conversion can be seen in Figure 5.2a and in Figure 5.2b where the only difference is frequency, 100 Hz and 300 Hz. With the same pin configured as output the response can be seen in Figure 5.3a and Figure 5.3b for 300 Hz and 30 kHz respectivly. The rise time was much faster for the output than for the input. It was also noted that the voltage level for the internal pull-up was too low, 5-6 V instead of 12 V.



(a) 100 Hz *(b) 300 Hz*

Figure 5.2: The input conversion for two frequencies at 12 V, the blue signal is the raw input and the yellow is the converted input which will later be read by the MCU through an IO expander.



(a) 300Hz *(b) 30 KHz*

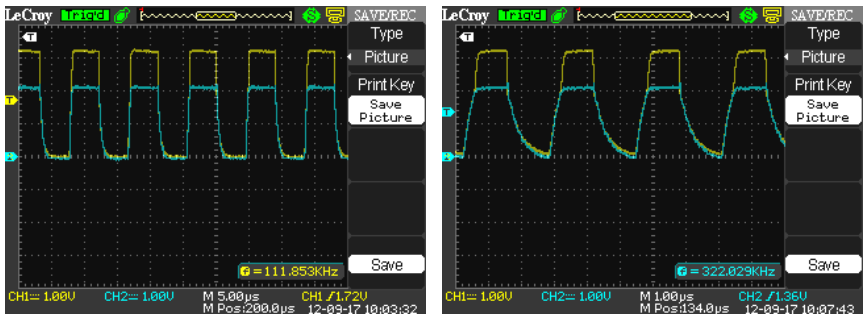
Figure 5.3: The converted output at two frequencies at 12 V, the blue signal is the output and the yellow is the measured converted output. The converted output should reach 12 V.

JTAG pass-through

The emulated JTAG output, from the SIU, had acceptable response at 100 kHz, see Figure 5.4a, and started to detoriate around 400 kHz, Figure 5.4a.

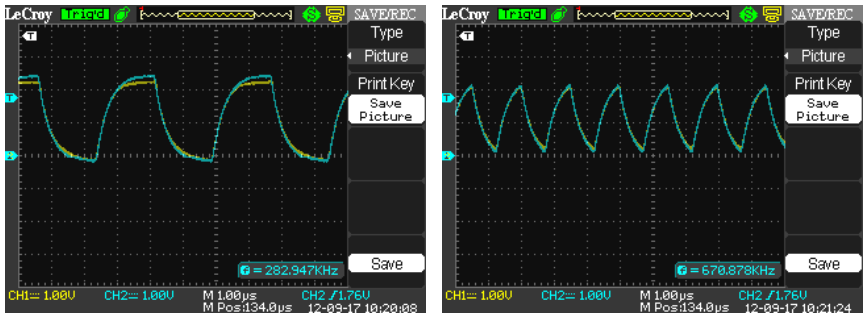
When JTAG was configured as an input to the SIU the response was similar with acceptable response below 400 kHz and a cut-off frequency above 600 kHz see Figure 5.5a and Figure 5.5b.

The JTAG over-voltage protection successfully supressed a 15 V square wave see figure Figure 5.6, highest voltage recorded on the CPU pin was 2.7 V.



(a) 110kHz *(b) 370 KHz*

Figure 5.4: JTAG output test for two frequencies. The yellow signal is a 3.3 V square wave emulating JTAG output from a CPU, the blue signal is the output response measured at the IO port. Note the voltage clipping by the over-voltage protector at 2.1 V.



(a) 280KHz *(b) 670KHz*

Figure 5.5: JTAG output test for two frequencies. The yellow signal is a 2.1 V square wave emulating JTAG output from a CPU, the blue signal is the output response measured at the IO port.

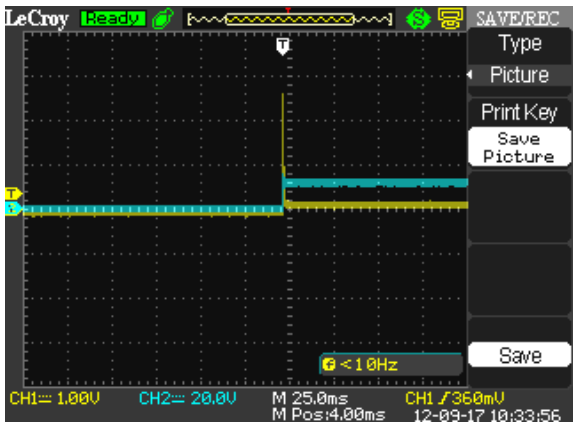


Figure 5.6: 1 Hz signal with high rise time from 0 to 15 V (blue signal). Yellow signal is the CPU pin measured during the step change. Note the voltages per division 1 V for the yellow signal and 20 V for the blue signal.

Power converter

Firstly 15 V without load was tested and the output was stable at 15 V regardless of input voltage in the tested range. With a 15Ω load connected the output was still 15 V DC. The voltage ripple was measured at this configuration and the result can be seen in Figure 5.7, picture taken with oscilloscope on peak detection, and was calculated to +/-200 mV peak.

The converter was tested for 32.6 W at 22.13 V, the converted voltage was 48V and the current from the DC voltage source was 0.751 A which corresponds to 36 W.

When the converted voltage was 35.3V with 40.9 W, the output voltage was 23.75 V with 37.6 W.

This gives an efficiency of:

$$\frac{32.6W}{36W} = 0.905 = 90.5\%,\ V_{out} = 22.13V \tag{5.1}$$

$$\frac{37.6W}{40.9W} = 0.919 = 91.9\%,\ V_{out} = 23.75V \tag{5.2}$$

The resistance of the load was 15Ω which gives the currents:

- 1.48 A for 22.13 V
- 1.58 A for 23.75 V

In Figure B.9 the theoretical efficiency is plotted compare the two real values (1.48, 0.905) and (1.58, 0.919) with the curve for 24 V.

During the power converter tests, the temperatuere of the circuit was documented. The maximum temperature measured was $59.8\,^{\circ}\mathrm{C}$ and it was on the capacitor C600. The switching MOSFET Q600 also got warm, $54.5\,^{\circ}\mathrm{C}$. In Figure 5.8a the whole circuit can be seen during high power output and in Figure 5.8b the hot part is zoomed in on. To simplify orientation Figure 5.9 are pictures taken with the same field of view with a normal camera.

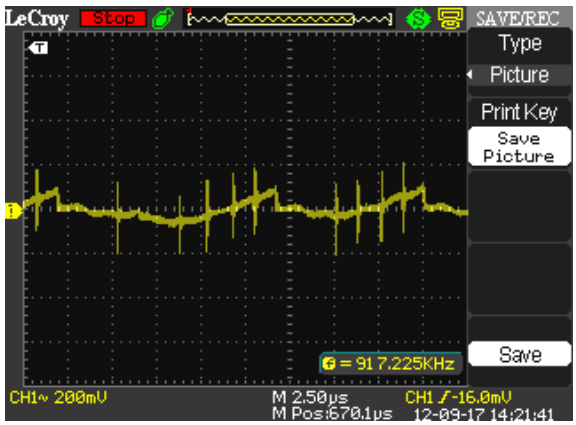
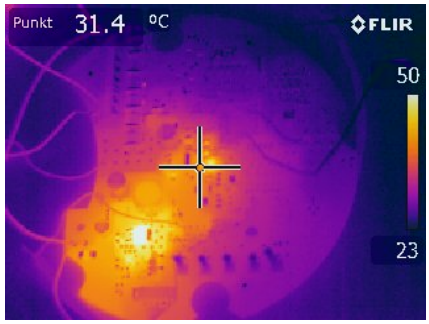
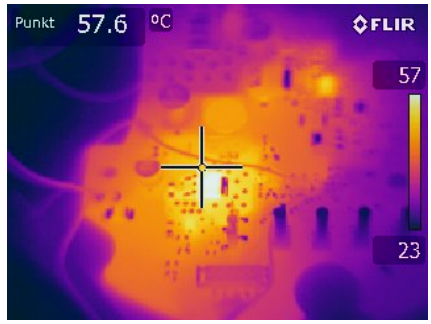


Figure 5.7: Voltage ripple on output pin during a 15W load at 15V. Oscilloscope set to peak detection and AC coupled. Ripple measure to 200 mV peak.

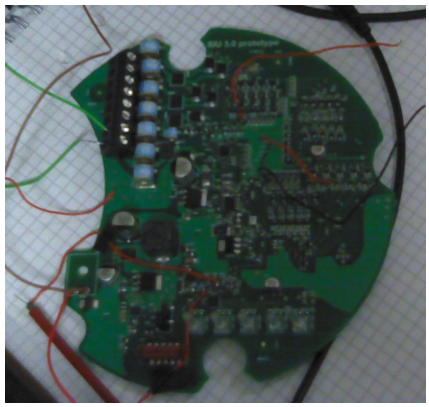


(a) Output power is 35 W. Bright yellow is $50\,^{\circ}\mathrm{C}$ *and deep purple* $23\,^{\circ}\mathrm{C}$

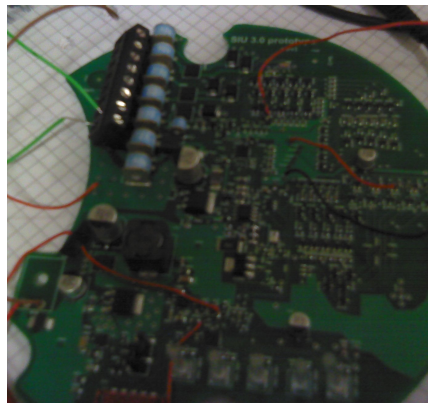


(b) Zoomed on critical area. Bright yellow is $57\,^{\circ}\mathrm{C}$ *and deep purple* $23\,^{\circ}\mathrm{C}$

Figure 5.8: Temperature for the circuit during heavy load for 10 minutes.



(a) Figure 5.8a



(b) Figure 5.8b

Figure 5.9: Reference pictures for circuit during heavy load

5.2.2 Discussion

The level conversion in input configuration worked satisfactory and the limited IO bandwidth of about 300 Hz , Figure 5.2a, was a design choice and the low pass filter time constant could easily be changed if a faster system is required.

The output configuration also worked well but the 12/15/24 V pull-up was poorly designed as the voltage division through the base of PNP-transistor Q702, see Figure 4.7, was not considered which resulted in half the desired pull-up voltage. This is however easily fixed by increasing the value of R706 to $200\ k\Omega$.

JTAG pass-through frequency response was acceptable but not impressive and based on the preliminary test will probably be limited to a 200 kHz JTAG clock, this means that programming would be possible, but not at high speeds. The over-voltage protection was meant to be triggered by anything above the zener voltage of 4.3 V but due to the design, small currents leaking through the diode trigged the protection circuit at 2.2 V, and a small redesign of the circuit would be necessary if it was to enter production.

Due to limited time the *buck converter* was not thoroughly tested but preliminary test results were positive. Although the circuit was not tested for the maximum rated output power it was tested for about 35 W which is 5 times the power output of the existing SIU and the question whether a new version of SIU could power sensors when the powering current is lowered to 2 A is answered, yes.

A MOSFET in the *short circuit protection* was designed with the *gate* as the *drain* pin and vice versa and it had to be removed from the circuit board. The protection was therefore not tested properly, but the internal short circuit protection of the buck converter controller was tested when a load of $0.63\ \Omega$ was mistaken for $63\ \Omega$. The result was a current through the load which would have reached 19 A but only reached 3 A before the controller shut down.

The PCB was designed to emit as little noise as possible but EMC tests was not in the scope of the project. A common problem with buck converters are high frequency switching and in our design the current can have a ripple amplitude of 200 mA and be up to 1 MHz but as the inductor is shielded this will hopefully not be a problem. Tests concerning the power surge protection should be done before the SIU 3.0 enters production but due to such extreme tests are expensive and hard to realize they are also put on hold. Still, by choosing to implement the complete protection circuits impedance test concerning the IO and JTAG could be done.

As the prototype board was manufactured and delivered late in to the project time was limited and a full test with created software was thus not done. The software was however tested on a rapid development board and the basic functions does work, in theory. The software design, as a design philosophy, have already spawned response from Safegate and a document regarding future coding standards and practices have been created together with Safegate software engineer Björn Hammarberg.

5.2.3 Further development

Future development consists of several parts. Next step would be to prepare an Yeager platform with the SIU software and use the hardware as the external add-on it was meant to be used.

When the prototype works with current hardware a second revision of the SIU 3.0 prototype should be produced fixing found hardware errors and improving design where better solutions are found. Such improvements consists of: A small improvement on the input level conversion to use the configurable voltage source as IO reference instead of the fixed 3.3 V source, placing the logic high and low levels in between the max range. The stackable design is not fully stackable as the mounting holes were milled way too large and the JTAG header is also off-center. The incorrectly oriented MOSFET preventing the short circuit protection to function needs to be fixed and tested again.

After the prototype stage the SIU needs to become a product by mechanical design of an enclosure and long term tests in the harsh environments a SIU can find itself in.

5.2.4 Conclusion

This master thesis project has been a great experience in product development and design thanks to the open premises of the project. A theoretically solved problem is just a small step in a long chain of development and this was something strongly realized here. We were given a list of both hard and soft constraints where we would need to ask questions like: "Why would this product need a such feature?" These questions did not have one but many, more or less, correct answers where the weight deciding the best solution or answer was decided by many parameters. We have not faced this kind of product development reasoning to a large extent in our courses at LTH.

Although the planning and designing phase of the project was theoretically demanding, the implementation of the circuit into Altium Designer and implementation of the software was a major part of our project and we gained much experience in how to execute a large scale project.

The largest reward during the time working on this master thesis came when we confirmed that the prototype circuit board was functional and that each module, except the short circuit protection, worked as it should.

Appendix A

SIU 2.0 functionality in 2.0 A system

A.1 Introduction and materials

The following tests evaluate the SIU functionality in the 2A environment. This appendix is written for engineers knowing the details of the ASP system and can otherwise be ignored. The materials used for the experiments were:

- Oscilloscope type LeCroy WA234
- Regular low frequency 10x probe Current measurement probe
- 20, 30 and 75 Ω power resistors
- CCR, thyristor based IDM8000 and switch based IDM9000
- LPU, SCM
- SIU Ver. 2.1 Part No. 591855
- Insulation transformer 200W for IDM9000 and 100W with IDM8000
- 50 mH and 12.5 mH line inductance

The measurements were then compared to the SIU 2.1 data sheet voltage ratings which are represented in table A.1.

Voltage	Min	Typ	Max
12VDC	10.5	12.0	12.5
15VDC	13.8	15.0	15.6
24VDC	23.0	24.0	25.0

Table A.1: Voltage specification SIU 2.1

A.2 Method

The SIU was programmed to respond 4 times on the same sync separated by 19 timeslots each. Another sync was added to the SCM which the SIU did not respond to. Otherwise the SIU was in the *defualt* mode except for the change in output current. The CCR was connected with SCM and SIU surrounded by two SCI:s of 50 mH and 12.5 mH. The SIU was connected to the LPU in order to add a load to the SIU OUT4.

Two CCR:s were used, first a switched sinus CCR and then a standard, thyristor based one. All tests were conducted at room temperature and the following settings were tested for both the thyristor and the switched CCR.

Test	1	2	3	4
SIU output voltage	12 V	24 V	12 V	24 V
CCR output current	2 A	2 A	6.6 A	6.6 A
SIU resistive load	$20.12\ \Omega$	$75.10\ \Omega$	$20.12\ \Omega$	$75.10\ \Omega$

The maximum power rated for the SIU is 7.5 W and the closest resistive loads found were $20.12\ \Omega$ for 12 V and $75.10\ \Omega$ for 24 V configuration.

Other parameters, 4 A and 15 V settings were also tested but proved to add nothing to the conclusion and are as such not discussed in the report.

A.3 Results

Important statistics of the SIU supply is collected in the table A.2 and A.3 and the corresponding plots can be found in Table A.2 through Figure A.10.

Configuration	12 V 2 A	12 V 6.6 A	24 V 2 A	24 V 6.6 A
Ripple	1005 mV	912 mV	744 mV	648 mV
Max/Min	12.1 V/11.0 V	12.3 V/11.3 V	24.7 V/24.0 V	25.1 V/24.4 V
Recovery time	100 ms	75 ms	80 ms	75 ms

Table A.2: Thyristor CCR test results

Configuration	12 V 2 A	12 V 6.6 A	24 V 2 A	24 V 6.6 A
Ripple	784mV	868 mV	720 / 1660 mV	760 / 1760 mV
Max/Min	11.9 V/11.2 V	11.9 V/11.0 V	24.9 V/24.7 V	23.9 V/ 24.7 V
Recovery time	75 ms	65 ms	65 ms	30 ms

Table A.3: Switched sinus CCR test results

The larger values are the extra detected spikes present in both the 2 A and 6.6 A configuration. See figure A.8,A.6 for a detailed view.

A.4 Discussion

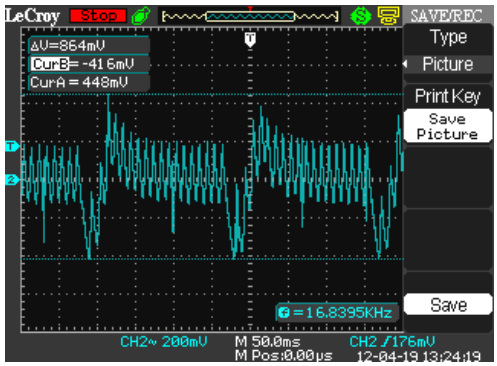
When considering the data collected above it is clear that the specified maximum values for voltage and current in the characteristics page for the SIU is fulfilled, although with less than ideal margins and with a passive load under laboratory conditions at room temperature.

The only apparent difference between the 2 A system and the higher current systems is the recovery time during transmission and recovery overshoot. The value of the ripple is however still within the specified values. The longest recorded recovery time was for the 2 A thyristor based configuration at 12V and was 100 ms, figure A.3.

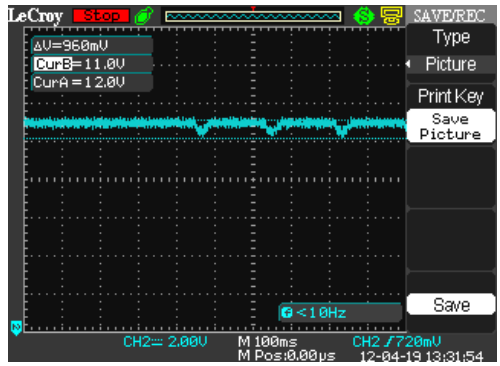
An unexpected occurrence is the large voltage spikes on the output when using the switched CCR with either 2A or 6.6 A current see figure A.8 , A.6 and more detailed in figure A.10. This implies that something in the designed hardware is not working as intended for the newer type CCR. But as this is outside the scope of this report the phenomena remains uninvestigated.

Also the communication seems to be largely unaffected by the change in current, this is probably due to designers having low currents in mind when designing the circuit due to costumers requesting operation in the "dark current" region below 2 A, dubbed dark current due to it not lighting halogen lights. Measurements from the AMT circuit monitor showed values around 29 for the switched CCR at 6.6 A and around 19 for 2 A because the switching frequency and the default SIU response frequency was barely separated. The values for the thyristor based CCR was almost independent of current and was around 49 for both 6 A and 2 A with 6 A performing slightly better.

A.5 Figures

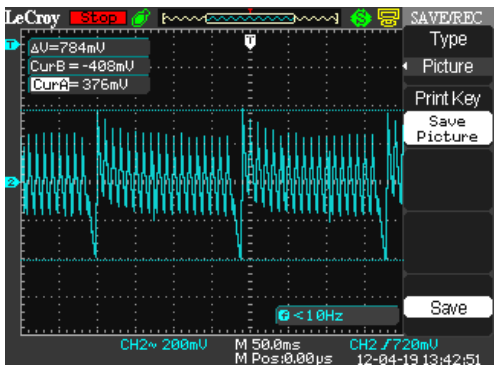


(a) AC coupled

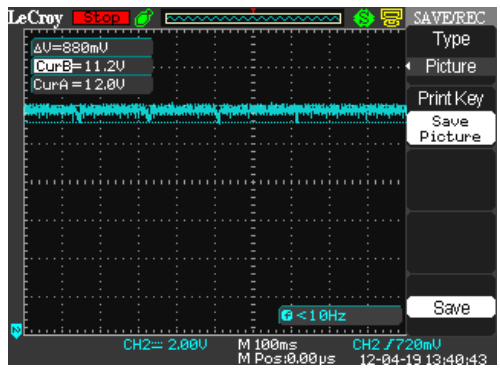


(b) DC coupled

Figure A.1: 12 V 2 A studied in AC and DC mode on the switched CCR

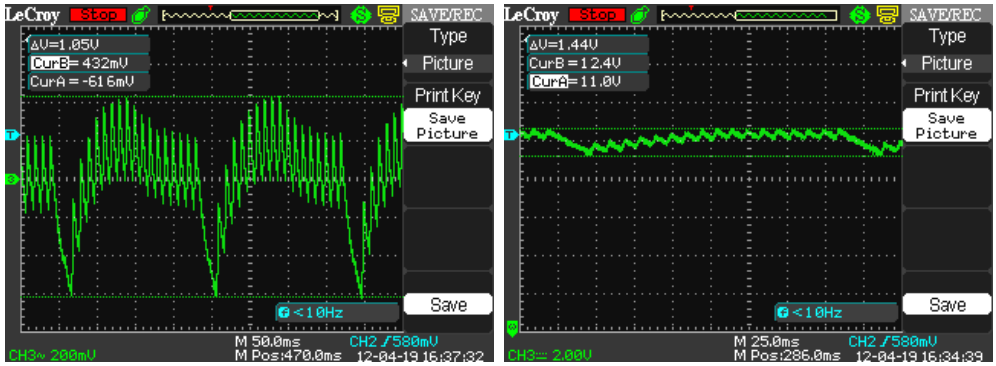


(a) AC coupled



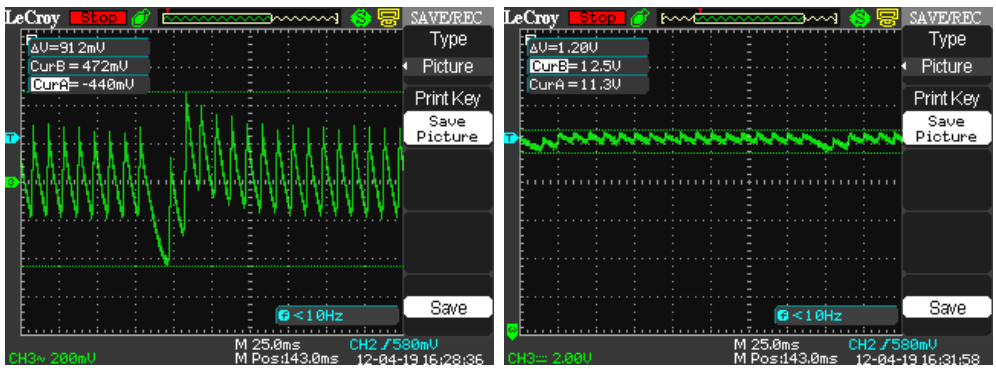
(b) DC coupled

Figure A.2: 12 V 6 A studied in AC and DC mode on the switched CCR



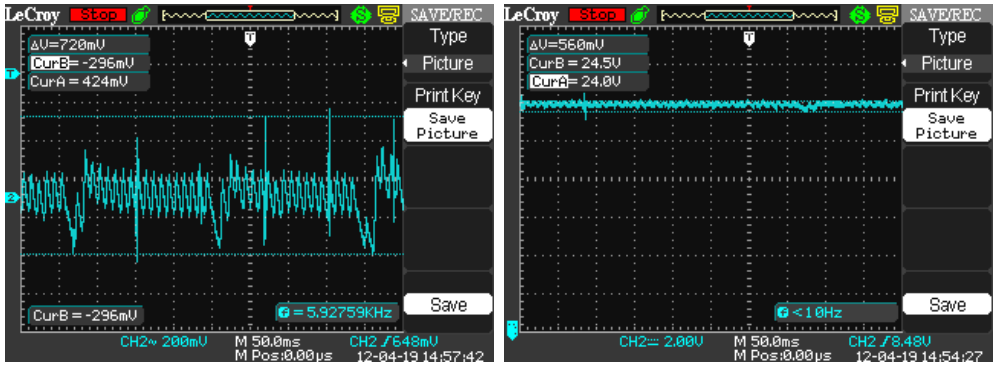
(a) AC coupled *(b) DC coupled*

Figure A.3: 12 V 2 A studied in AC and DC mode on the thytistor CCR



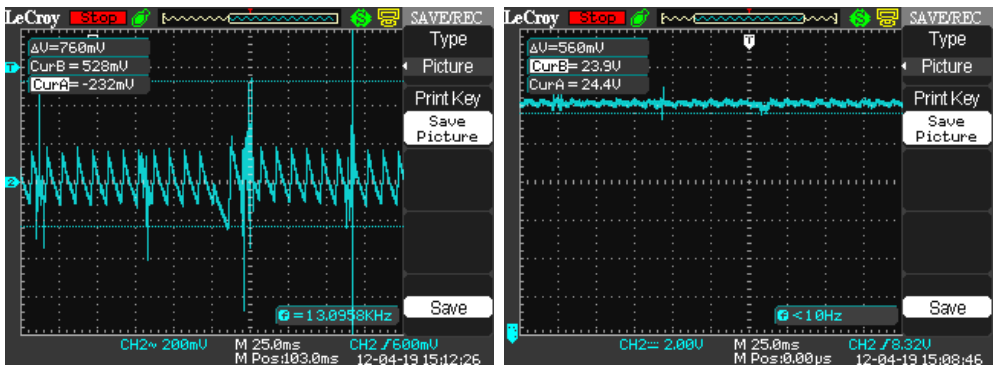
(a) AC coupled *(b) DC coupled*

Figure A.4: 12 V 6 A studied in AC and DC mode on the thytistor CCR



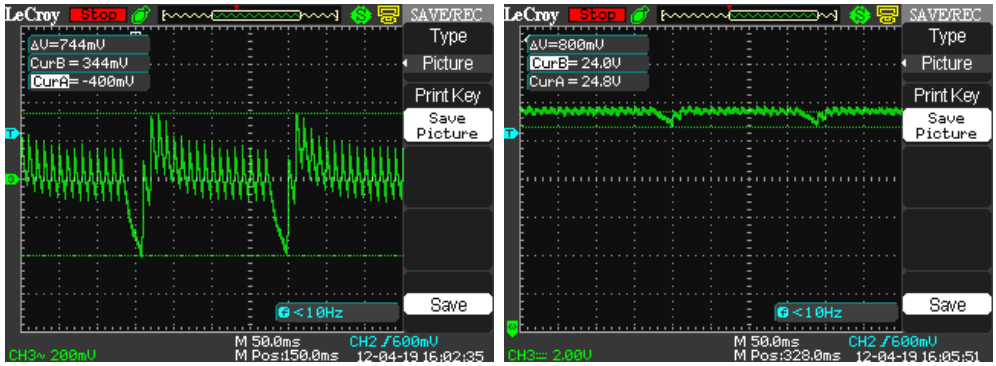
(a) AC coupled *(b) DC coupled*

Figure A.5: 24 V 2 A studied in AC and DC mode on the switched CCR



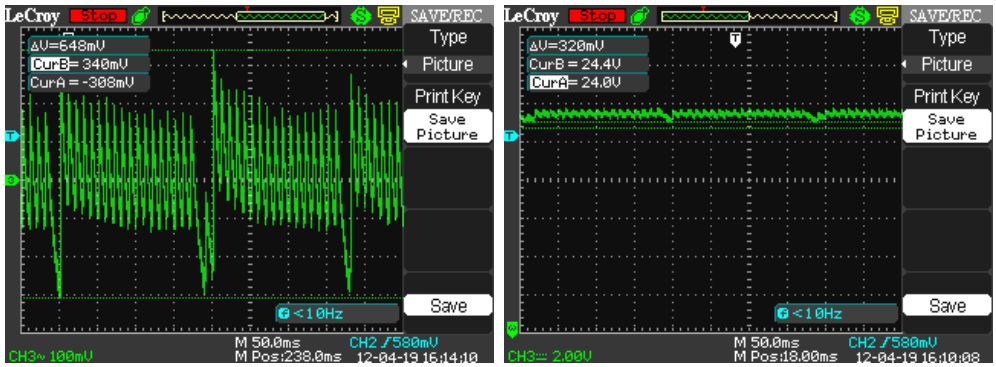
(a) AC coupled *(b) DC coupled*

Figure A.6: 24 V 6 A studied in AC and DC mode on the switched CCR



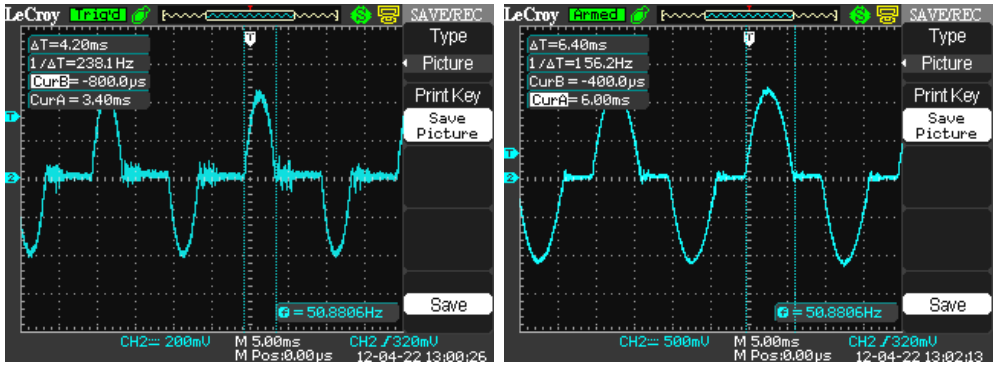
(a) AC coupled *(b) DC coupled*

Figure A.7: 24 V 2 A studied in AC and DC mode on the thytistor CCR



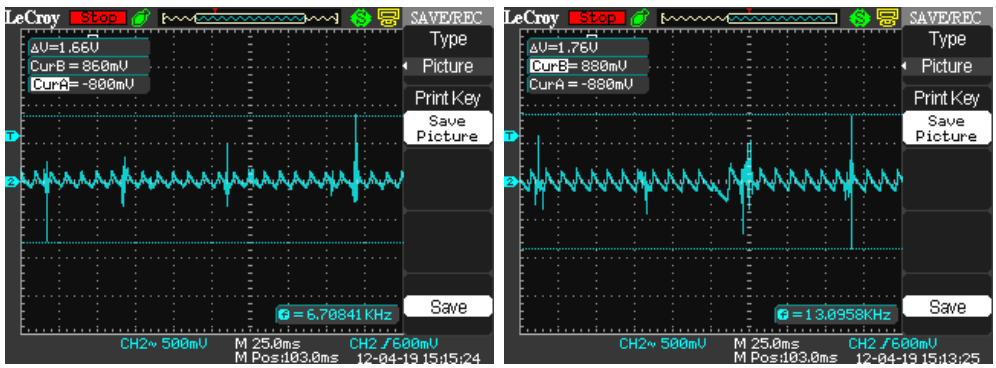
(a) AC coupled *(b) DC coupled*

Figure A.8: 24 V 6 A studied in AC and DC mode on the thytistor CCR



(a) 2A current from CCR *(b) 6.6A current from CCR*

Figure A.9: The tyristor CCR on time for the different current configurations measured with a current clamp



(a) 2A current from CCR *(b) 6A current from CCR*

Figure A.10: 24 V 2 A studied in AC mode on the switched CCR to study the spikes

Appendix B

Converter Calculations

B.1 Buck converter controller

The Yeager platform has a stable DC voltage source, in the Yeager schematics called DC+, which has a maximum value of 60 V and is normally 48 V. The current charging the Yeager platform is the ASP system current which in modern ASP systems is 2 A, this means that the maximum power from the DC+ voltage source is $2 \cdot 48 = 96W$ neglecting power losses in the circuit. The SIU's voltage supply powering the sensors is required to be adjustable between at least 12 V, 15 V and 24 V. By using a buck converter the voltage level is switched down to the desired value, an integrated circuit was chosen to control the buck converter. The converter circuit can be viewed in Figure B.1 and all calculations obtaining component values are supported by the data sheet for the buck converter's IC controller, a *Texas Instrument* product, LM5085.

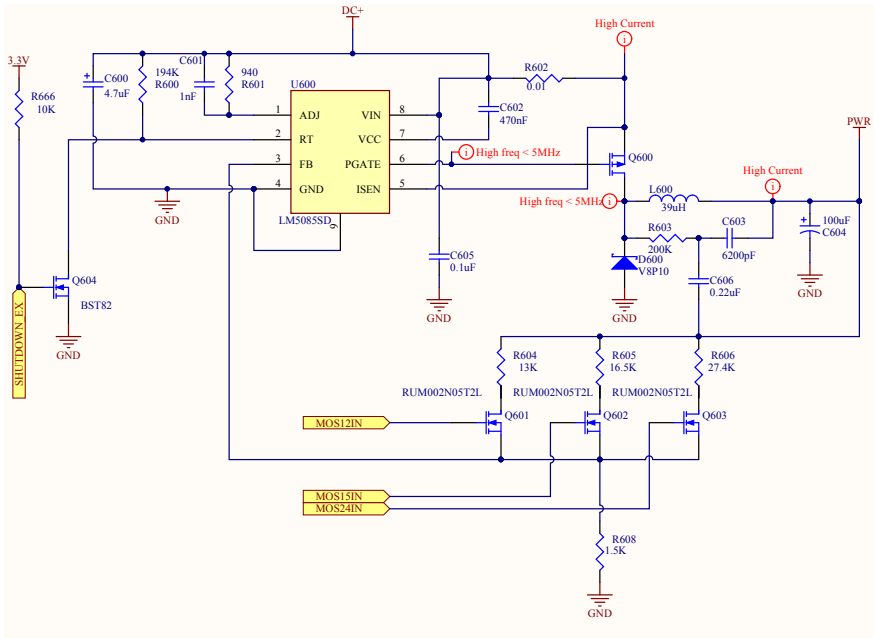


Figure B.1: This circuit contains the buck converter which switches the DC+ voltage to the voltage level needed for the output voltage in the SIU. The circuit contains the buck converter, the buck converter controller and a potentiometer which controls the controller's reference level. To the circuit the DC+ voltage is connected and also some discrete inputs from the MCU, which controls the reference level of the controller. From the buck converter the switched voltage supply is connected to a short circuit protection unit before it connects with the power output pin. The short circuit protection can be seen in figure Figure B.2

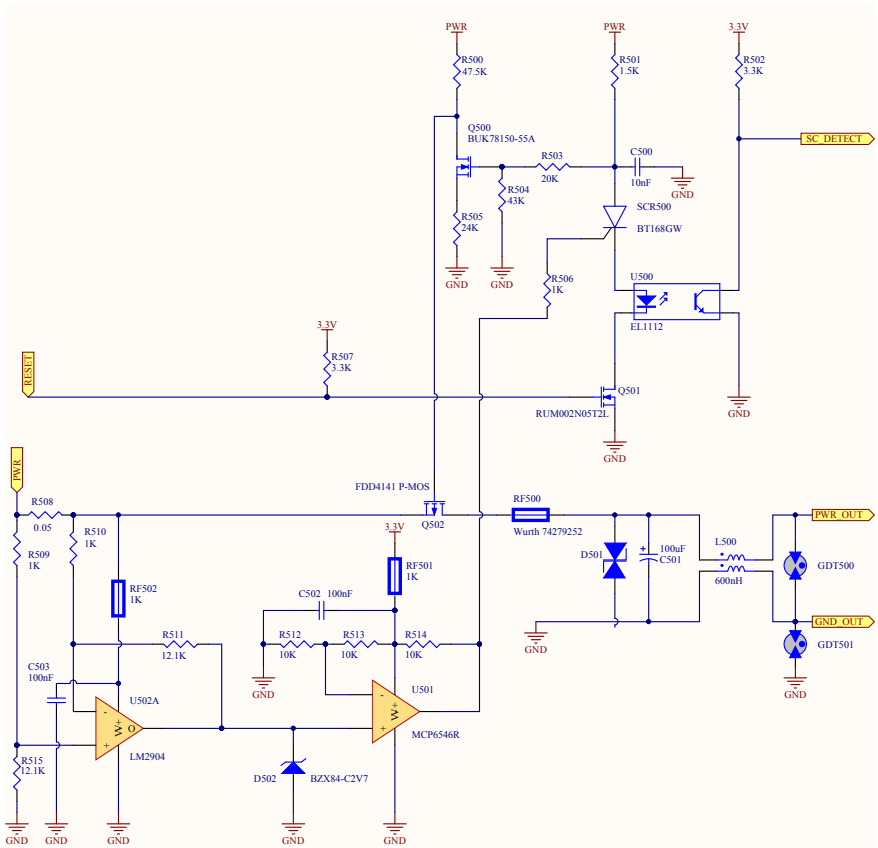


Figure B.2: This is the short circuit protection unit which protects the output voltage supply from overcurrent.

Primarily there are two different configurations of buck controllers [6]; an integrated circuit using an internal switching MOSFET as switching device or a controller circuit which is connected to an externa switching MOSFET. The latter have the benefit that the user can set the restraints in e.g. power output and input voltage by choosing a suitable MOSFET. The configuration with external MOSFET was chosen due to the increased flexibility and also because it's easier to replace in the future because a controller without internal MOSFET is more generic. The properties and features considered when the controller was chosen was:

- Switching frequency - minimal noise on the carrier signal is desirable.
- Current limiter - since the power supply pin will be short circuited to ground when the user wants to program the parameters, a current limiting in the circuit is desirable.
- Input and output voltage constraints - the input and output voltage levels have to be in range of the specified constraints.

The best chose was the LM5085 from *Texas Instruments*[9] and connected to this IC a MOSFET with sufficient qualities has to be chosen. The requirements for the MOSFET was:

- Voltage rating above 60 V.
- Low R_{DS} resistance.
- Bandwidth above the switching frequency.
- The MOSFET has to be of doping type P-MOS.

A MOSFET which met these constraints was found, a product of *ZETEX Semiconductors* with product number ZXMP7A17K.

B.2 Choosing components

The values of the other components associated with the LM5085 buck converter controller is normally calculated for a specific output voltage. In the SIU configuration the output voltage level was adjustable and the values of the components were therefore calculated using an approximative mean value of the output voltage. The input voltage is the DC+ voltage from the Yeager platform which is between 48-60 V but the only input voltage that needs to be taken into account when calculating the component values are the maximum input voltage, i.e. 60 V.

$$V_{in} = 60V$$
$$V_{out} = 18V$$

The switching frequency for the controller reaches as high as 1 MHz and the controller changes frequency but keeps on-time constant, thus changing duty cycle and uses this as the control action controlling the output voltage level. The resistor R_{600} in figure

Figure B.1 scales the switching frequency by changing t_{ON}. The output voltage has multiple settings and because the resistor R_{600} value is constant, the switching frequency differ depending on which level the output voltage source is set to. One factor when choosing the switching frequency is to not disturb the communication signal between the SIU and the ASP system, therefore the switching frequency was chosen to be quite high, 400 kHz for 12 V, 500 kHz for 15 V and around 800 kHz for 24 V. Some components are sensitive to which switching frequency is used and these components are designed for a frequency around 600 kHz, i.e. 18 V.

The LM5085 does have an internal short circuit protection which will cut off the current through the switching MOSFET when sensing a current level higher than allowed. The maximum allowed current is chosen to:

$$I_{CL} = 3.0A$$

Also the minimum load current was chosen to:

$$I_{min} = 0.02A$$

The LM5085 uses feedback in the form of the voltage output divided by impedances on a feedback pin, *FB*-pin. The voltage level at *FB*-pin is compared with controlled to be equal to a reference voltage of 1.25 V. In order to control the voltage level at the *FB*-pin to reach 1.25 V, action is taken which changes the duty-cycle on the switch MOSFET and thus the output voltage as well. The output voltage is controlled to be proportional to the *FB*-pin voltage by a factor determined by voltage division. In the case of the SIU; 12 V, 15 V and 24 V needs to be implemented as output voltage which is solved by connecting resistor and MOSFET in series and three such series connection in parallel. The parallel connection is connected to a resistor to ground and to the output voltage, see figure Figure B.1. By having one of the three MOSFETs conducting, voltage division between the two resistors conducting results in a voltage level proportional to the output voltage at the *FB*-pin. By having one voltage division for each voltage level the MOSFET:s are used to set the output voltage to either 12 V, 15 V or 24 V.

A solution with a digital potentiometer setting the feedback factor was also implemented in order to evaluate which is the better solution. A resistor is connected to the output voltage and to the digital potentiometer which is connected to another resistor

to ground, see figure Figure B.1. The resistor between the output voltage and the potentiometer puts a bias on the voltage division in order to use all of the range of the potentiometer. The potentiometer is controlled by the MCU on the Yeager circuit using I^2C to set the impedance.

The advantages of the solution with the potentiometer is that the output voltage level can be varied in much smaller steps. This can be used if a load disturbance is present or if the conditions changes and another voltage level is needed than the predetermined voltage levels. For the latter instance only a software change is needed in comparison with the MOSFET solution where the hardware has to be changed in that to get a voltage level not predetermined. The drawback of the potentiometer solution is that the hardware is more complex and expensive. Another drawback is that the software and communication taxation is higher. To sum it up, the solution with digital potentiometer is more versatile but also more demanding .

The solution with MOSFET:s one of the voltage divider resistors for all three voltage levels. The other resistor was unique for each voltage level:

$$V_{FB} = \frac{R_2}{R_1 + R_2} \cdot V_{OUT} \iff \tag{B.1}$$

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \cdot V_{FB} \tag{B.2}$$

$$\begin{aligned} V_{FB} &= 1.25V \\ R_{1_{12\ V}} &= 13.0\ k\Omega,\ (R_{604}\ in\ schematic) \\ R_{1_{15\ V}} &= 16.5\ k\Omega,\ (R_{605}\ in\ schematic) \\ R_{1_{24\ V}} &= 27.4\ k\Omega,\ (R_{606}\ in\ schematic) \\ R_2 &= 1.5\ k\Omega,\ (R_{608}\ in\ schematic) \end{aligned}$$

Thus the output voltages for the different settings is:

$$V_{OUT_{12\ V}} = \frac{13.0\ k\Omega + 1.5\ k\Omega}{1.5\ k\Omega} \cdot 1.25\ V = 12.08\ V \tag{B.3}$$

$$V_{OUT_{15\ V}} = \frac{16.5\ k\Omega + 1.5\ k\Omega}{1.5\ k\Omega} \cdot 1.25\ V = 15\ V \tag{B.4}$$

$$V_{OUT_{24\ V}} = \frac{27.4\ k\Omega + 1.5\ k\Omega}{1.5\ k\Omega} \cdot 1.25\ V = 24.08\ V \tag{B.5}$$

The MOSFETs controlling which voltage level should be set was chosen to meet voltage and current ratings, other constraints are insignificant. The on-impedance and the bandwidth of the MOSFET are not very important to consider when choosing MOSFET since the impedance of the MOSFET is much less than the voltage division's impedances and the change of voltage level happens seldom enough to not even consider the bandwidth constraints.

The digital potentiometer was implemented following the datasheet[10] for the product *AD5274* made by ANALOG DEVICES.

The switched DC+ voltage source is low-pass filtered to make the ripple on the output voltage as low as possible. The filter consists of an inductor and a bulk capacitor; the inductor is chosen to decrease the current ripple and the capacitor is chosen to decrease the voltage ripple. The value of the inductor is obtained from the following equation:

$$L = \frac{t_{ON(min)} \cdot (V_{IN(max)} - V_{OUT})}{I_{OR(max)}} \tag{B.6}$$

- $t_{ON(min)}$ is the minimal on-time for the gate at the switching MOSFET.
- $I_{OR(max)}$ is the maximal current ripple.

To achieve high accuracy when limiting the current, a sense resistor, R602 in figure Figure B.1, is placed between the DC+ voltage source and the drain on the switching MOSFET. This resistor is chosen to be $10m\Omega$ as recommended in the data sheet for the LM5085. A resistor and a capacitor, R_{601} and C_{601}, is used as a reference for the voltage level at the DC+ voltage and compared with the voltage level after the sense resistor in order to sense over-current at the output voltage source. The capacitor is recommended to be 1000 pF and the value of the resistor is calculated from the following equation:

$$R_{ADJ} = \frac{I_{CL} \cdot R_{SEN}}{40\ \mu A} \tag{B.7}$$

I_{CL} is the maximum current limit for the output voltage, in this application the limit was chosen to 3.0 A, when this limit is exceeded the buck converter controller LM5085 will hold the switching MOSFET off and will regularly try to start the switching process up.

B.3 Switch power losses

The power output current goes through:

- two resistors, R_{602} and R_{508}
- the switching MOSFET, Q_{600}
- the switching inductor, L_{600}
- the switching diode, D_{600}
- the Short circuit break MOSFET, Q_{502}
- a ferrite bead, RF_{500}
- a common mode choke, L_{500}
- the buck converter controller, U_{600}

The power source current goes through these components which will introduce a non neglectable power loss. For the resistors the power loss is easily calculated:

$$P_R = R \cdot I_{OUT}^2 \tag{B.8}$$

The power loss for the inductor can be divided into three power loss addends; core, DC and AC losses. The AC loss is so small it can be neglected, the DC loss appears because of the impedance in the inductor. Since the power source current runs through the inductor and it is resistive, the DC loss is calculated by modeling the inductor as a resistor:

$$P_{L_{DC}} = R_{L_{DC}} \cdot I_{OUT}^2 \tag{B.9}$$

The core loss was given by the product specifications and is not higher than $300\ mW$ which is added to the DC loss in order to estimate the total power loss. The power losses for different output currents can be seen in figure Figure B.3 for the resistors and for the inductor.

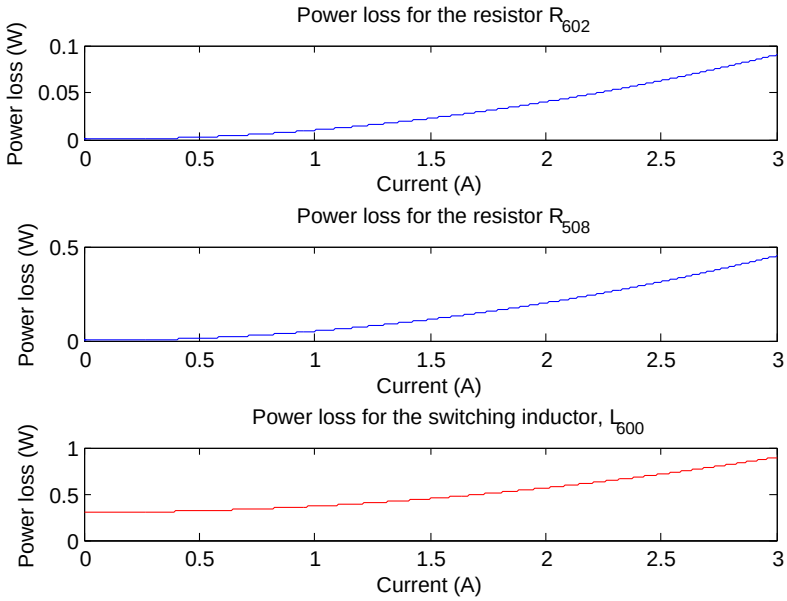


Figure B.3: The power loss of the two resistor R_{602} and R_{508}, see figure Figure B.1 and Figure B.2. Also the power loss of the inductor L_{600} in figure Figure B.1.

The power loss for the ferrite bead can be calculated by modelling that the bulk capacitor and switching inductor, *C604* and *L600* from figure Figure B.1, removes the current ripple and the power loss can be calculated by modelling the ferrite as a resistor.

The common mode choke can also be modelled as a resistor due to the same reason as for the ferrite bead, figure Figure B.4

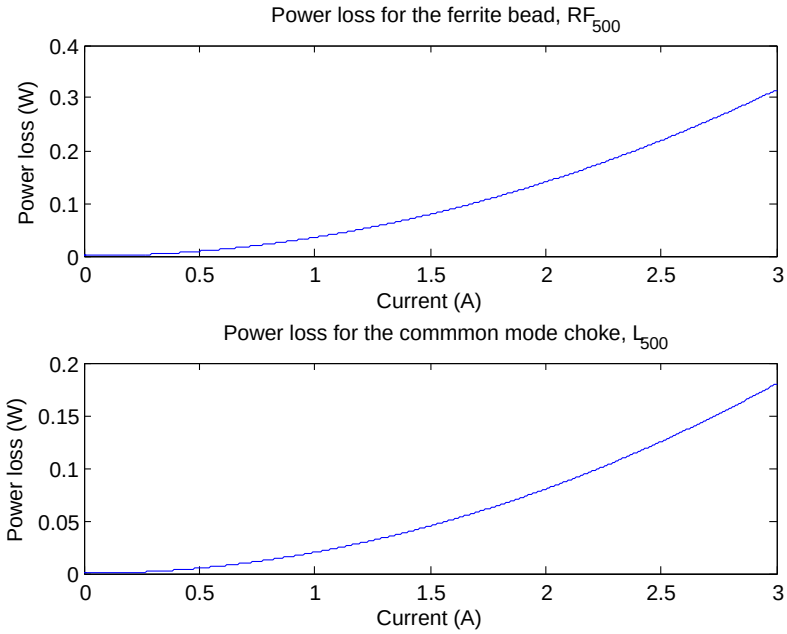


Figure B.4: The power loss of the ferrite bead RF_{500} and the common mode choke L_{500} in figure Figure B.2.

The calculations of the power loss in the switching diode is not as obvious as the calculations above. When the switching MOSFET is turned on, the power supply drives a current through the inductor and magnetic energy is then charged up. When the MOSFET is turned off, the stored magnetic energy tries to maintain the current and the only way this is done is by driving a current from ground, through the switching diode and the inductor. The current through the inductor decreases as the stored magnetic energy is used to drive the current. But before the magnetic energy has dissipated, the MOSFET is turned on again and the currents is once more driven through the inductor by the DC power supply. This means that the only time the switching diode loses power is when the MOSFET is turned off. The mean value of the diodes power loss is therefore calculated from the duty cycle of the switching signal:

$$P_{D_{600}} = (1 - D) \cdot R_{D_{600}} \cdot I_{OUT}^2 \tag{B.10}$$

where D is the duty cycle of the switching signal.

Since the on-time for the switching signal is constant, the duty cycle is changed when the frequency is changed. When the period is increased the on/off-time ratio is also changed, this is true because the on-time is constant which means that the off time has to increase as much as the whole period. By this logic, the duty cycle increases when the frequency is increased and it decreases when the frequency decreases. The duty cycle can be calculated as following:

$$(1 - D) = \frac{\frac{1}{f} - t_{ON}}{\frac{1}{f}} = 1 - \frac{t_{ON}}{\frac{1}{f}} \tag{B.11}$$

Since the frequency is decided by which voltage level the output source should have, the figure Figure B.5 shows the power loss for the three voltage levels.

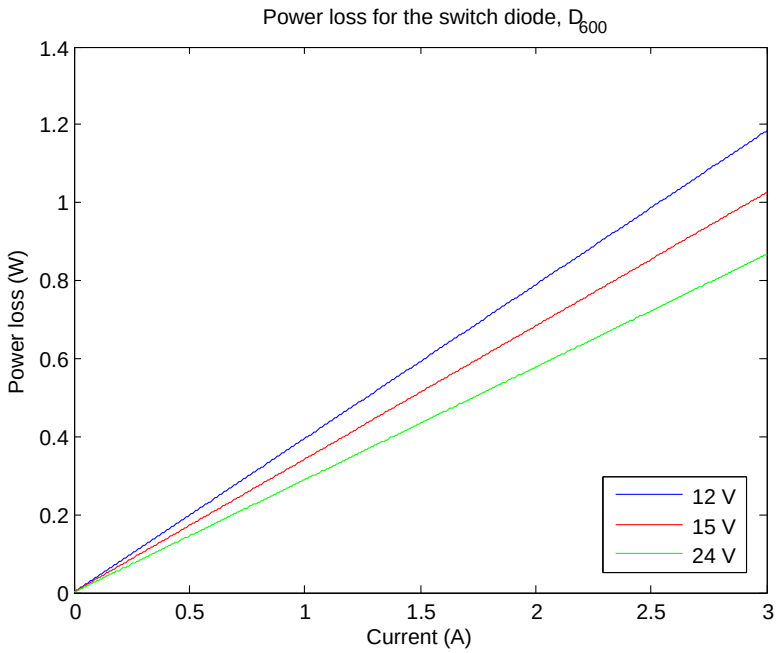


Figure B.5: The power loss of the switching diode D_{600} in figure Figure B.1, the blue curve is the power loss for 12 V, the red is for 15 V and the green is for 24 V output voltage level.

The buck converter controller's power losses are, according to the data sheet for the *LM5085*, mainly related to the charge up of the switching MOSFET's gate. The equation

expressing the power loss of the controller is:

$$P_{DISS} = V_{IN} \cdot (Q_G \cdot F_S) + I_{IN} \tag{B.12}$$

$V_{IN} = 48\ V,\ the\ input\ voltage\ level.$
$Q_G = 18\ nC,\ the\ gate\ charge\ for\ the\ switching\ MOSFET.$
$F_S = [400, 600, 800]\ kHz,\ the\ switching\ frequency.$
$I_{IN} = 1.3\ mA,\ the\ operating\ current\ opening\ and\ closing\ the\ switching\ MOSFET.$

The power loss is independent of the output current but increases as the output voltage increase:

$$P_{U600-12} = 0.4\ W$$
$$P_{U600-15} = 0.58\ W$$
$$P_{U600-24} = 0.75\ W$$

The two MOSFETS has power losses, but since the current at the MOSFET Q_{500} can be modelled as a DC, the power losses will not be frequency dependant and the MOSFET can be modelled as a resistor as the other components, the power loss for the MOSFET Q_{502} can be seen in figure Figure B.6. The DC related power loss for the other MOSFET Q_{600} can also be seen in figure Figure B.6.

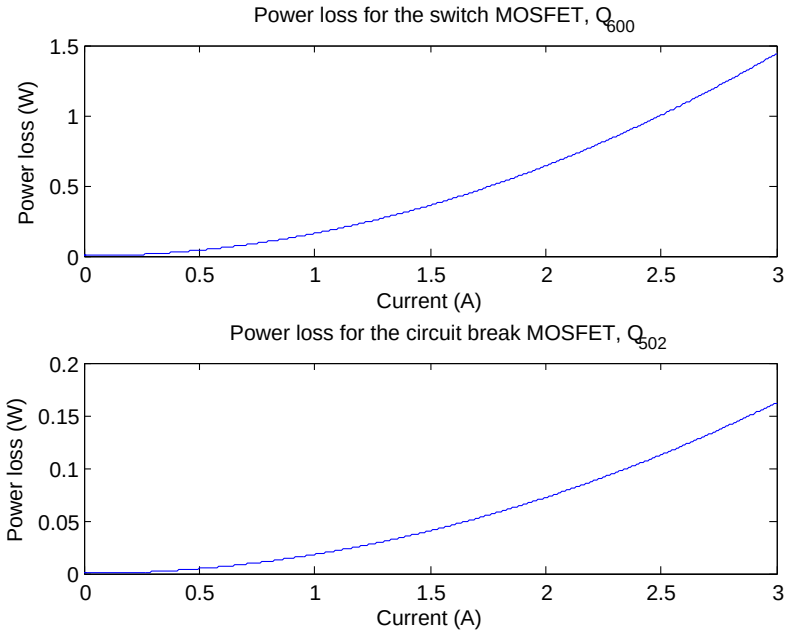


Figure B.6: The power losses in the MOSFETs related to DC effects in the MOSFETs where the MOSFETs is modelled as a resistor.

The frequency dependant losses can be divided into two categories, turn-on losses or drain-source charge up losses and cross-over loss. The turn-on losses is generated when the MOSFET is conducting and the drain-source capacitance is charged:

$$P_{Q_{600}} = \frac{(C_{OSS} + C_P) \cdot V^2 \cdot f}{2} \tag{B.13}$$

$$\begin{aligned} C_{OSS} &= 52\ pF,\ from\ data\ sheet\ for\ Q_{600}\ -\ ZXMP7A17K. \\ C_P &= 20\ pF,\ parasitic\ winding\ capacitance. \\ V &= 48\ V,\ drain\ voltage\ level. \\ f &= [400, 600, 800]\ kHz,\ switching\ frequency. \end{aligned}$$

Change in output current is not related to change in power loss, but the power loss is proportional to the switching frequency. The power loss for the different output voltage

levels, which are proportional to the switching frequency, is:

$$P_{Q_{600}-12\ V} = 33.2\ mW \tag{B.14}$$

$$P_{Q_{600}-15\ V} = 49.8mW \tag{B.15}$$

$$P_{Q_{600}-24\ V} = 66.4\ mW \tag{B.16}$$

The cross-over power dissipation can be calculated from:

$$P_S = f\left[ts_1 \int_0^{ts_1} V_{DS} \cdot I_D \mathrm{d}t + ts_2 \int_0^{ts_2} V_{DS} \cdot I_D \mathrm{d}t\right] \tag{B.17}$$

For a purely resistive load the power loss can be simplified to:

$$P_{RCL} = \frac{V_{DS} \cdot I_{DS}(ts_1 + ts_2) \cdot f}{6} \tag{B.18}$$

Where P_{RCL} is the resistive crossover power dissipation

$$\begin{aligned} V_{DS} &= 48\ V,\ the\ input\ to\ the\ buck\ converter\ voltage. \\ I_{DS} &= \ The\ current\ through\ the\ MOSFET,\ calculated\ below. \\ ts_1 &= 3.4\ ns,\ The\ rise\ time\ of\ the\ MOSFET. \\ ts_2 &= 8\ ns,\ The\ fall\ time\ of\ the\ MOSFET. \\ f &= [400, 600, 800]\ kHz,\ the\ frequency\ of\ the\ switching. \end{aligned}$$

The I_{DS} current is the current through the MOSFET during on-time and it is higher than the rms current:

$$I_{rms} = I_{DS} \cdot D \iff \tag{B.19}$$

$$I_{DS} = \frac{I_{rms}}{D} \tag{B.20}$$

D is the duty cycle for the switching signal

The duty cycle is different for different switching frequencies since the on-time is constant, the power loss for the MOSFET generated when the MOSFET is changed from turned on to off or vice versa, the loss can be seen in figure Figure B.7.

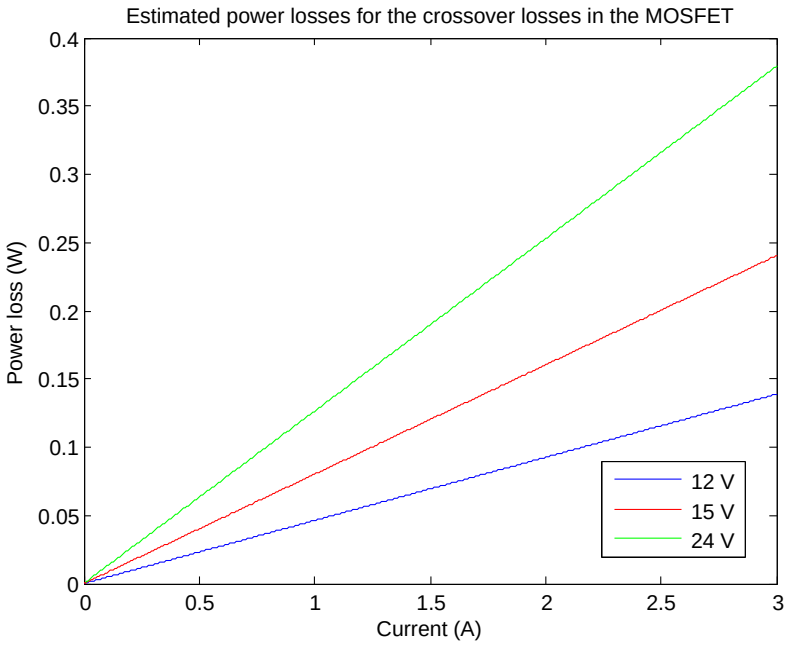


Figure B.7: The power loss for the MOSFET created by the crossover charge up which happens during the rise and fall time for the MOSFET.

An estimate of the total power loss can be seen in figure Figure B.8 and the maximum power loss for the buck converter and short circuit protection according to figure Figure B.8 is ca $2.7\ W$ since the rated current is max 2.7 A.

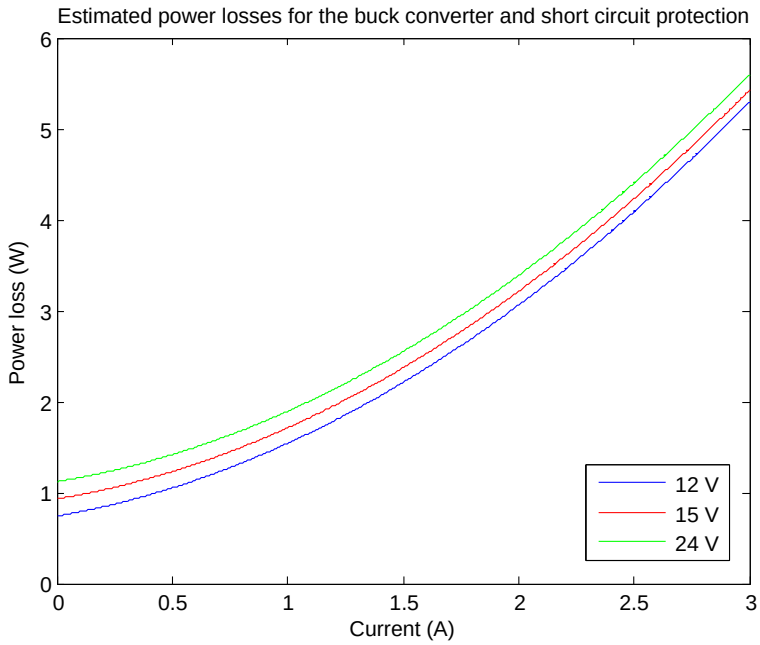


Figure B.8: This is an estimation of the total power loss of the buck converter and short circuit protection. The addends are the non neglectable components concerning power loss when a load is connected on the SIU.

The efficiency of the circuit can therefore be estimated since the output current and voltage is known along with the power losses, this can be seen in figure Figure B.9. The estimated efficiency should be relatively close to the real efficiency since the power losses not already included are very small compared to the output power.

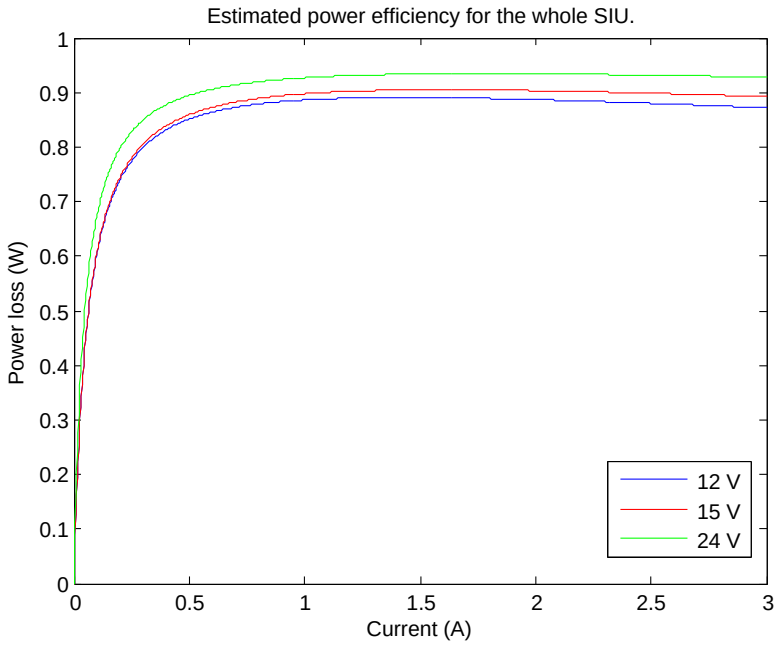


Figure B.9: The efficiency of the SIU calculated by estimating all major power losses in the power circuit

Appendix C

SIU 3.0 test procedure

C.1 Level conversion

Isolated test on level conversion and JTAG pass-through with no software involvement. Disconnect the SIU 3.0 extension board from the Yeager platform. Then connect the SIU IO pins to a MBD simulation circuit as seen in Figure 2.5 and Figure 2.6. Connect *pin 1* on connector X103 to a 3.3V voltage source. Connect *pin 1* of X102 to a 12-24 V supply and *pin 2* to ground. Make sure that the 3.3V and 12V supply share return path. Connect a wire to a $3.3\ k\Omega$ resistor and then to test point 107, (IO pull-up enabled), and connect to a ground.

Test 1 Apply a 50 Hz, 0 - 3.3 V , square wave with a duty cycle of $1 - 10\%$ to test point 109 through 113 and study response on MBD input simulation circuit test point A with an oscilloscope. Redo test for 100 Hz and 500 Hz.

Test 2 Connect the wire added to test-point 107 to a 3.3 V supply (through the added resistor). Apply a 50 Hz , 0 - 3.3 V, square wave with a duty cycle of $1 - 10\%$ to the MBD output simulation circuit and measure response with an oscilloscope on test points 100 through 105. Redo test for 100 Hz and 500 Hz.

C.2 JTAG pass-through

Isolated test of JTAG pass-through. with Disconnect the SIU 3.0 extension from the Yeager platform. Connect *pin 1* on connector X103 to a 3.3 V voltage source. Connect

pin 2 of connector X102 to ground. Tie test point 115 to 3.3 V in order to set the JTAG-pass through to programming state.

Test 3 Apply a symmetric 100 kHz , 0 - 3.3V, square wave to *pin 4* of connector X102. Measure response on *pin 15* of X103 with an oscilloscope. Redo test for 500 kHz and 1000 kHz.

Test 4 Apply a symmetric 100 Hz , 0 - 3.3 V, square wave to *pin 4* of connector X102. Measure *pin 15* of X103 and *pin 4* of connector X102 with an oscilloscope and increase the top voltage of the square wave until the signal is cut and note the voltage.

Test 5 Apply a symmetric 1 Hz , 0 - 12 V, square wave to *pin 4* of connector X102. Measure *pin 15* of X103 and *pin 4* of connector X102 with an oscilloscope and decrease duty cycle until signal is visible on X103. Note the time ratio of the duty cycle.

Test 6 Apply 3.3 V to X102 *pin 3* and measure test point 108.

C.3 Power converter

Testing the buck controller with minimal software involved. Disconnect the SIU 3.0 board from the Yeager platform then connect the SIU IO pins to a MBD simulation circuit as seen in Figure 2.4. Connect *pin 1* on connector X103 to a 3.3V voltage source. Apply a 48 VDC to X100 *pin 2* and ground to *pin 2*. Connect *pin 2 and 1* of header J600 with a jumper. Configure the IO expander U300 to set MOS12IN high and all other IO pins low.

Test 7 Connect a 10Ω load between *pin 2* and *pin 1* of the X102 connector. Measure the voltage at *pin 2*. Measure voltage between test point 506 and *pin 2* of X102. Measure voltage between test point 601 and 506 by means of an oscilloscope and studdy voltage ripple. Measure current through shunt resistor R508 by measuring the voltage between test point 505 and test point 506 note current ripple.

Test 8 Repeat test 6 but pull MOS12IN low and MOS15IN high.

Test 9 Repeat test 6 but pull MOS15IN low and MOS24IN high.

C.4 Short circuit protection

Testing the short circuit protection with no software involved. Disconnect the SIU 3.0 board from the Yeager platform then connect *pin 1* on connector X103 to a 3.3 V voltage source. Connect a current limited12V source to test point 505, ***limit current to 1 A on the 24 V source!*** Connect a 30 W power resistor of $7.5\ \Omega$ between *pin 1 & 2* of X102.

Test 10 Gradually increase current while measuring voltage at test point 503. When the measure voltage drops below 12 V note at what current this occurs. Repeat test after waiting 5 minutes three times.

Test 11 Measure trip time by comparing the R508 shunt resistor current to test point 507 voltage. When the shunt resistor voltage measured between test point 505 and 506 reaches 0.135 V measure the time until voltage at test point 507 is zero.

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