

# Numerical Modeling of Nanowire Transistors

Rasmus Wulff

Email: [tn07rw9@student.lth.se](mailto:tn07rw9@student.lth.se), or [rwulff88@gmail.com](mailto:rwulff88@gmail.com)

Department of Electrical and Information Technology

Faculty of Engineering

Lund University

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# Abstract

Numerical modeling and simulations of wrap-gate InAs nanowire transistors are performed using Atlas from Silvaco. The Drift-Diffusion Transport Model, the Drift-Diffusion Mode-Space Method and the Non-Equilibrium Green's Function (NEGF) Mode-Space Approach are used. The latter two simulation models take account of quantum mechanical effects, whereas the first one is a purely classical model. The NEGF mode-space model simulates ballistic transistors, where carriers are unaffected by scattering. The simulations are performed to investigate the effects of varying device parameters such as the NW radius, gate length and n-type doping. Transistors are assessed and compared using figures of merit like maximum transconductance, inverse subthreshold slope, DIBL and on-resistance. Some comparisons are made between the different models used.

It is found that low channel-doping is preferable, and that the low-doped region should be aligned with, or within, the gate edges. The simulations show that it is possible to scale the gate length to  $\leq 50\text{nm}$  for nanowire (NW) radiuses of  $\leq 10\text{nm}$ , and still get reasonably good inverse SS. For these transistors it is less important that the doping in the channel is lower than in the rest of the NW.

# **Acknowledgments**

I would like to thank my supervisor Erik Lind for his help with the direction of this project, and for providing valuable input during the course of the work.

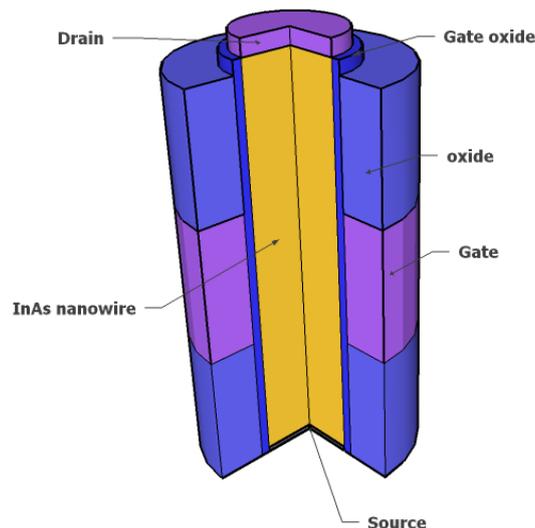
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# 1 Introduction

Since the first transistor devices were fabricated, transistors have been scaled to allow for higher device density. This development is described by the well-known Moore's law, named after Gordon E. Moore, who wrote about the trend in 1965 [1]. Unfortunately there are limits to how small the common planar transistor technologies can be scaled without encountering complications, like for instance increased leakage currents. One possible way of mitigating scaling problems is to use non-planar geometries like the finFET or the wrap-gate nanowire (NW) transistor. These transistors offer improved electrostatic control compared to planar transistors. The improved electrostatic control in NW transistors permits the gate length to be scaled further without causing unwanted short channel effects [2]. Another benefit of wrap-gate transistors is that if small NW diameters are used, the devices might operate in the quantum-capacitance regime, which would reduce the power consumption [3]. The possibility of making ballistic transistors using nanowires is also appealing. The term ballistic transport means that carriers are conducted through the channel without experiencing scattering events. Ballistic transistors therefore have minimal resistive voltage drop in the channel, which would be favorable [4]. The most commonly used semiconductor material in electronics is silicon; however III-V semiconductors such as InAs have enhanced material properties, primarily higher electron mobilities. InAs and other III-Vs are also known to have low contact resistance [2].

**Figure 1.1: Schematic image of a cylindrical NW transistor.** A piece of the device has been removed to display its interior.



This project uses the TCAD tool Atlas to execute the numerical modeling of NW transistors. Figure 1.1 displays a schematic image of such a transistor. Atlas is designed to be able to simulate a variety of different semiconductor devices, and includes models which can approximate quantum physics. The results of the simulations in this work are intended to help and complement the

experimental research on InAs nanowire transistors. Knowing how parameters like doping and gate-length affect NW transistor characteristics is useful when fabricating the transistors. The results should indicate what device design specifications to aim for when producing InAs NW transistors with the desired characteristics, and what specifications to avoid. Some of the transistor specifications investigated are: NW radius, doping, gate length  $L_g$ , distance between source and drain (i.e. the length of the NW), and the oxide thickness,  $t_{ox}$ . The radius affects the level of quantum confinement the carriers experience when this effect is simulated. The effects of adjusting material properties such as mobility and saturation velocity are also investigated. The results are presented as current-voltage curves and tables of the various figures of merit evaluated. The figures of merit are maximum transconductance, inverse subthreshold slope, DIBL, on/off ratio, on-resistance and  $I_{max}$ . These values describe specific aspects of the performance of a transistor.

## 2 Method

The software used to perform the NW transistor simulations is called Atlas, which is a physically-based device simulator. This means that the models in Atlas are based on scientific theory rather than experimental data. Specifically, Atlas uses differential equations derived using Maxwell's equations for electrostatics along with transport equations and the continuity equation to simulate the movement of carriers through the nodes in a specified grid-structure. The mathematical models used by Atlas can supposedly simulate any semiconductor device [5]. The program DeckBuild is used to write and input code to Atlas, and TonyPlot is used to plot the output data. The data can also be exported to a file format that can be imported in MatLab.

### 2.1 Electron transport physics and Atlas models

#### 2.1.1 The Drift-Diffusion Transport Model

$$\text{div}(\varepsilon \nabla \psi) = -\rho \quad (2.1)$$

Poisson's equation, the continuity equations, and the transport equations are fundamental to the numerical modeling done in Atlas. The electrostatic potential relates to the space charge density as stated in Poisson's equation, which can be written as equation 2.1.  $\psi$  is the electrostatic potential,  $\varepsilon$  is the local permittivity and  $\rho$  is the local space charge density, and  $\text{div}$  is the divergence operator. Equation 2.2 describes how the electric field  $\mathbf{E}$  is equal to the negative gradient of the potential. Note that the variables in bold are vectors.

$$\mathbf{E} = -\nabla \psi \quad (2.2)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \text{div} \mathbf{J}_n + G_n - R_n \quad (2.3)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \text{div} \mathbf{J}_p + G_p - R_p \quad (2.4)$$

The continuity equations used by Atlas are 2.3 and 2.4, where  $n$  and  $p$  are the electron and hole concentration,  $\mathbf{J}_n$  is the electron current density,  $\mathbf{J}_p$  is the hole current density,  $G_n$  and  $G_p$  are the generation rates for electrons and holes,  $R_n$  and  $R_p$  are the recombination rates for electrons and holes, and  $q$  is the elementary charge. The equations for  $\mathbf{J}_n$ ,  $\mathbf{J}_p$ ,  $G_n$ ,  $G_p$ ,  $R_n$  and  $R_p$  are different depending on what transport model is used. The simplest carrier transport model in Atlas is the Drift-Diffusion Transport Model. This model is convenient because it doesn't need any independent variables in addition to  $\psi$  and the carrier concentrations. The disadvantage of using the drift-diffusion model is that it becomes less accurate for smaller feature dimensions. Equations 2.5 and 2.6 are the drift-diffusion equations, where  $\mu_n$  and  $\mu_p$  are the carrier mobilities.  $D_n$  and  $D_p$  are the diffusion coefficients for electrons and holes.

$$\mathbf{J}_n = qn\mu_n\mathbf{E}_n + qD_n\nabla n \quad (2.5)$$

$$\mathbf{J}_p = qp\mu_p\mathbf{E}_p - qD_p\nabla p \quad (2.6)$$

These equations (2.5 and 2.6) have been derived assuming that the Einstein relationship is true. For Boltzmann-statistics this means that the diffusion coefficient relates to the mobility as expressed in equation 2.7, where  $k$  is Boltzmann's constant and  $T_L$  is the lattice temperature. The derivation of the drift-diffusion model is described in more detail in [5].

$$D = \frac{kT_L}{q}\mu \quad (2.7)$$

In this work the drift-diffusion model is used with Fermi-Dirac statistics. Compared to Boltzmann-statistics, Fermi-statistics are more suitable when regions with high doping are simulated. When Fermi-Dirac statistics are applied for electrons equation 2.7 becomes the more complicated equation 2.8.  $F_\alpha$  is the Fermi-Dirac integral of order  $\alpha$ ,  $\varepsilon_C$  is the conduction band energy, and  $\varepsilon_{Fn}$  is the quasi-Fermi level given by equation 2.9, where  $\phi_n$  is the quasi-Fermi potential and  $n_{ie}$  is the effective intrinsic carrier concentration. Similar expressions are used for holes. Additional information about carrier statistics can be found in [5].

$$D_n = \frac{\left(\frac{kT_L}{q}\mu_n\right)F_{1/2}\left\{\frac{1}{kT_L}[\varepsilon_{Fn} - \varepsilon_C]\right\}}{F_{-1/2}\left\{\frac{1}{kT_L}[\varepsilon_{Fn} - \varepsilon_C]\right\}} \quad (2.8)$$

$$\varepsilon_{Fn} = -q\phi_n = \psi - \frac{kT_L}{q}\ln\left(\frac{n}{n_{ie}}\right) \quad (2.9)$$

### 2.1.2 NEGF\_MS and DD\_MS

For the purposes of this work the main disadvantage of using the basic drift-diffusion model is that it does not take quantum effects, like the wave nature of electrons, into account. In a nanowire transistor, carriers are confined in one direction. This affects the radial carrier density, as well as the density of states, causing the occurrence of sub-bands. The effects of quantum confinement are simulated using the Self-Consistent Coupled Schrodinger Poisson Model; however this model can't solve transport problems by itself. It is therefore used in combination with either the Drift-Diffusion Mode-Space Method (DD\_MS), or the Mode Space Non-Equilibrium Green's Function Approach (NEGF\_MS). The Self-Consistent Coupled Schrodinger Poisson Model is used to solve Schrödinger's equation to give a quantized description of the density of states in the presence of quantum mechanical confinement. Atlas can solve the Schrödinger equation for various kinds of geometries and confinement. For simulating cylindrical nanowire devices the relevant equation for electrons is 2.10. This is the Schrödinger equation for cylindrical coordinates used by Atlas. The equation is solved in radial direction for different orbital quantum numbers and for all slices perpendicular to the axis.

$$-\frac{\hbar^2}{2}\left[\frac{1}{r}\frac{\partial}{\partial r}\left(\frac{1}{m_r^v(r,z)}r\frac{\partial R_{imv}}{\partial r}\right) - \frac{1}{m_r^v(r,z)}\frac{m^2}{r^2}\right] + E_C(r,z)R_{imv} = E_{imv}R_{imv} \quad (2.10)$$

$E_{imv}$  is an energy eigen state energy,  $R_{imv}(r)$  is the radial part of the wavefunction,  $m$  stands for the orbital quantum number,  $h$  is Planck's constant,  $m_r^v(r, z)$  is a spatially dependent effective mass for the  $v$ -th electron valley and  $E_C(r, z)$  is a conduction band edge. Equation 2.11 is used to calculate the electron concentration using Fermi-Dirac statistics in the cylindrical case, where  $\Psi_{iv}(x, y)$  is the wavefunction.

$$n(x, y) = 2 \frac{\sqrt{2kT}}{h} \sum_v \sqrt{m_z^v(x, y)} \sum_{l=0}^{\infty} |\Psi_{iv}(x, y)|^2 F_{-1/2} \left( -\frac{E_{iv} - E_F}{kT} \right) \quad (2.11)$$

$$H_0 = -\frac{\hbar^2}{2} \left[ \frac{1}{r} \frac{\partial}{\partial r} \left( \frac{1}{m_r^v(r, z)} r \frac{\partial}{\partial r} \right) - \frac{1}{m_r^v(r, z)} \frac{m^2}{r^2} + \frac{\partial}{\partial z} \left( \frac{1}{m_z^v(r, z)} \frac{\partial}{\partial z} \right) \right] \quad (2.12)$$

NEGF\_MS is capable of modeling effects such as source-to-drain tunneling, ballistic transport and quantum confinement. The model is useful for predicting subthreshold currents and threshold voltages. The transport in this model is ballistic, meaning that no scattering is simulated. Equation 2.12 describes the effective-mass Hamiltonian  $H_0$  in cylindrical coordinates. The NEGF\_MS model uses a mode-space approach, which should be faster than solving a problem in two or three dimensions. The Schrödinger equation is first solved in each slice of the device to find eigen energies and functions. With this information, an electron transport equation is solved for the sub-bands. Typically only a few low-energy sub-bands are occupied, so the upper sub-bands can be safely ignored. In the devices where the cross-section doesn't change (e.g. a NW transistor), the sub-bands are not quantum-mechanically coupled to each other and the transport equations become principally one-dimensional for each sub-band. Atlas will automatically decide on the minimum number of sub-bands necessary and whether to use coupled or uncoupled mode space approaches, though it's also possible to specify this in the models statement if required. Equation 2.13 shows how the real space Hamiltonian is transformed to mode space by taking a matrix element between  $m$ -th and  $n$ -th wave functions and  $k$ -th and  $l$ -th slices. Note that for cylindrical geometry, different orbital quantum numbers will result in zero matrix elements and are as a result uncoupled. Equation 2.14 and 2.15 are the transport equations in mode space.

$$H^{MS}_{mnkl} = \langle \Psi_m^k(y) | H_0 | \Psi_n^l(y) \rangle \quad (2.13)$$

$$(E - H^{MS}_{mnkl} - \Sigma_S^R - \Sigma_D^R) G^R = 1 \quad (2.14)$$

$$(E - H^{MS}_{mnkl} - \Sigma_S^R - \Sigma_D^R) G^< = (\Sigma_S^< + \Sigma_D^<) G^A \quad (2.15)$$

$E$  is the carrier energy,  $\Sigma^R$  is (depending on the lower index) the source or drain retarded self-energy, containing information about the density of states of the semi-infinite contacts.  $\Sigma^<$  is the source or drain less-than self-energy, holding information about the Fermi distribution function in the contact. A Green's function is a type of function used to solve an inhomogeneous differential equation bound by an initial or boundary condition. In this work the source and drain contacts had von Neumann boundary conditions during quantum simulations.  $G^R(E)$  is a retarded Green's function, and  $G^<(E)$  is a less-than Green's function. The diagonal elements in  $G^R$  are linked to the local density of states as a function of energy, and the diagonal elements in  $G^<$  are related to the carrier density as a function of

energy.  $G^A(E) = (G^R(E))^\dagger$  is an advanced Green's function. After solving 2.14 and 2.15 at each energy, Atlas is able to calculate the carrier and current density for the device.

Besides NEGF\_MS, the Drift-Diffusion Mode-Space Method is also used to execute simulations where quantum mechanical effects are modeled. DD\_MS is a semi-classical approach to transport in devices with strong transverse confinement, and is simpler than NEGF\_MS. The solution is decoupled into the Schrödinger equation in transverse direction and one-dimensional transport equations for each sub-band. The main difference between NEGF\_MS and DD\_MS is that the DD\_MS model solves a classical drift-diffusion equation instead of a quantum transport equation. DD\_MS incorporates quantum effects, and the usual Atlas models for mobility, recombination, impact ionization, and band-to-band tunneling. Unlike NEGF\_MS, DD\_MS completely neglects any quantum mechanical coupling between electron sub-bands, so the model can only simulate devices with uniform cross-section. 1D drift-diffusion transport in each sub-band is calculated using equations 2.16 and 2.17, where  $\nu$  is the sub-band index and  $b$  is the effective mass index.

$$\frac{1}{q} \frac{\partial J_{\nu b}}{\partial x} = R_{\nu b} - G_{\nu b} \quad (2.16)$$

$$J_{\nu b} = q\mu_{\nu b}n_{\nu b} \frac{\partial E_{\nu b}}{\partial x} - qD_{\nu b} \frac{\partial n_{\nu b}}{\partial x} \quad (2.17)$$

$J_{\nu b}(x)$  is the sub-band current,  $n_{\nu b}(x)$  is the sub-band carrier density to be obtained, and  $E_{\nu b}(x)$  is the eigen energy of the sub-band computed by the Schrodinger solver. The mobility  $\mu_{\nu b}(x)$  is determined by one of Atlas' mobility models. Equation 2.18 is used to calculate the diffusion coefficient,  $D_{\nu b}(x)$ . Fermi-Dirac statistics is assumed, making equation 2.19 the relation between sub-band carrier densities (in  $\text{cm}^{-3}$ ), quasi-Fermi levels and eigen energies for 1D confinement in the y direction. In this work, DD\_MS is used without generation-recombination mechanisms.  $A$  in equation 2.19 is a normalizing area.  $m_x$  and  $m_z$  are the isotropic effective masses in the x-direction and z-direction respectively.

$$D_{\nu b} = \mu_{\nu b} \left( \frac{\partial n_{\nu b}}{\partial E_{\nu b}} \right)^{-1} \quad (2.18)$$

$$n_{\nu b} = 2 \frac{kT}{A\pi\hbar^2} \sum_{\nu} \sqrt{m_x^{\nu b} m_z^{\nu b}} \ln \left[ 1 + \exp \left( -\frac{E_{\nu b} - E_{F,\nu b}}{kT} \right) \right] \quad (2.19)$$

After the transport equations are solved in each sub-band, and quasi-Fermi levels are computed, bulk carrier densities and currents are calculated by summing over all sub-bands, and weighting with the corresponding wave-function squared, as done in equation 2.11. Poisson's equation is solved self-consistently using a predictor-corrector scheme. Instead of the default Dirichlet boundary conditions for potential in contacts, in this thesis the DD\_MS simulations are made using von Neumann boundary conditions at source and drain contacts.

## 2.2 Simulation specifications

This section describes the simulation code. For a full source code example, see the appendix. Atlas is launched by the statement `go atlas`. Atlas allows user-defined variables, and it is a good idea to state these in the beginning of the code. A variable is defined using a `set`-statement, and used by typing `$` followed by the name of the variable. Comments in the code are made using the `#` symbol, as lines that start with `#` are ignored by Atlas. The nanowire transistor structure is simulated in Atlas2D using a quasi-3D model, by specifying cylindrical symmetry in the `mesh`-statement. Atlas will then simulate the structure as if its `x`-direction is the radial direction of a cylinder, with the `y`-axis at the center of the cylinder. Note that `y`-coordinates increase in the downward direction, with 0 at the top of the structure.

The mesh is a grid that covers the physical simulation domain, and acts as the basis for the device structure. To avoid creation of obtuse triangles, node smoothing and triangle smoothing are enabled in the `mesh` statement by specifying `smooth=1` and `diag.flip`. The mesh is created by specifying the spacing in `x`-direction between the line of nodes (grid-points) at a given `y` value and their neighboring lines, and vice versa. The area between lines specified with different spacings will have a gradual transition between node spacings. Note that Atlas uses the length unit  $\mu\text{m}$  for coordinates and spacing. The minimum required is to set the spacing for the nodes on the edges of the structure. It is generally best to use smaller spacing in areas of interest, where the carrier concentrations, electric field and other parameters may vary greatly. For the purposes of this work that would be the transistor channel. On the other hand, the meshes that seem to work best with the NEGF\_MS model have smaller spacings at source and drain. If there aren't any nodes located exactly on the border between regions, the border will become jagged or slightly moved from the intended location. Similarly there needs to be nodes at the edges of the electrodes, or else they will be shrunken. The number of nodes used will in general increase the accuracy of the simulation, but also the simulation time. The default maximum number of nodes in Atlas2D is 100,000.

Regions are defined with a number, a material type, and minimum and/or maximum coordinates in `x`- and `y`-direction. Every grid-point needs to be associated with a region or an electrode. Electrodes are defined in essentially the same way as regions, but for convenience the electrodes are given names, in this case source, gate and drain. In all simulations presented in this work, the source electrode is situated at the bottom of the InAs nanowire, and the drain is at the top. The gate is placed at the center of the length of the nanowire. An image of the NW transistor structure as generated by TonyPlot can be seen in figure 3.2. As previously stated, von Neumann boundary conditions are enabled in the quantum simulations. This is set by specifying `reflect` in the `contact` statement for source and drain respectively. For the regions with doping that is specified using `doping`-statements, where the doping concentration is given in units of  $\text{cm}^{-3}$ .

The `models` statement is where various models are activated, or deactivated using the `^` symbol. These models describe physical characteristics such as tunneling, carrier statistics, mobility, impact ionization and recombination. In the `models` statement, `print` is included to get the details of material parameters, constants and mobility models at the start of the run-time output. All simulations are made with Fermi-Dirac carrier statistics enabled through the `fermi` parameter. The field-dependent mobility model `fldmob` is used with the parameter setting `evsatmod=2`. This applies a simple electric field based velocity limiting model without any temperature dependency. Equation 2.20 describes how the carrier velocity  $v$  depends on the electric field and the mobility, and equation 2.21 describes how the model approximates velocity saturation for electrons. Naturally there is a corresponding equation for holes, with the index  $p$  in place of  $n$ .  $E$  is the parallel electric field,  $BETAN$  is 1 for the simulations in this work, and the low-field mobilities  $\mu_{n0}$  and  $\mu_{p0}$  are set by the parameters `mun` and `mup` in the `mobility` statement. Mobility is set in units of  $\text{cm}^2/\text{Vs}$ . The saturation velocity for electrons,  $VSATN$ , is also set in the `mobility` statement.

$$v = \mu E \quad (2.20)$$

$$\mu_n(E) = \mu_{n0} \left[ \frac{1}{1 + \left( \frac{\mu_{n0} E}{VSATN} \right)^{BETAN}} \right]^{\frac{1}{BETAN}} \quad (2.21)$$

Electron-hole pair generation and recombination are caused by impact ionization, transitions in the bandgap and tunneling events. The Shockley-Read-Hall model, enabled via writing `srh` in the `models` statement, is used to simulate band-gap transitions. The `schro` models parameter is needed for the quantum simulations, as this enables the Self-Consistent Coupled Schrodinger Poisson Model for electrons. To enable this model for holes, specify the `p.schro` parameter. The default Schrodinger solver geometry for cylindrical mesh in Atlas2D is `1DX`. Since this is the appropriate geometry for the quantum simulations in this work, there is no reason to specify the parameter `sp.geom` in the `models` statement. The parameter specified to use the Mode Space Non-Equilibrium Green's Function Approach is `negf_ms`, and for the Drift-Diffusion Mode-Space Method it's `dd_ms`. Note that for the classical drift-diffusion transport model no particular `models` parameter needs to be stated. The desired permittivity for a region can be specified by the `region` and `permittivity` parameters in a `material` statement. The relative permittivity of the gate dielectric is set to 20 during all the simulations in this project.

Atlas has different numerical methods that solve differential equations in different ways. The Gummel method is a decoupled solution technique. It considers all except one of the variables constant, and then solves each unknown consecutively. The solution process is repeated until a stable result is obtained. The Newton method is completely coupled, in other words tries to solve for all unknowns at the same time. Atlas' solution methods can be applied in combination. When the parameters `gummel` and `newton` are enabled together, the Gummel solution method is applied first

and the Newton method second, in cycles until convergence is reached. The method parameter `itlim` decides the maximum number of outer loops allowed for the Newton solution method. An automated Newton-Richardson procedure is implemented by stating `autonr` in the method statement. This method tries to reduce the number of lower-upper decompositions per bias point to speed up the `newton` solution process. The `trap` method parameter specifies that if a solution process starts to deviate, the electrode bias steps are reduced by the multiplication factor `atrap`. This is an easy and effective way of improving convergence. The default value of `atrap` is 0.5, but like most parameters in Atlas it can be modified. The `carriers` (alias `carr`) parameter in the method statement controls the number of carrier continuity equations that will be solved. If `carriers=2` is set, the continuity equations for both carriers are solved. In the case of quantum models, the Self-Consistent Coupled Schrodinger Poisson Model is only compatible with `carriers=0`. The purpose of the `output` statement is to specify the information that will be included in standard structure format files. The parameters `con.band` and `val.band` specifies that the conduction band edge and the valence band edge will be included.

Atlas is capable of calculating DC, AC small signal and transient solutions. The simulations made for this work consist of DC voltage sweeps. The first solution is specified by the statement `solve init` and uses the doping profile to make an initial guess for potential and carrier concentrations. This solution must be performed for zero bias. Having an initial solution is important because Atlas uses previous solutions to make the first guess from which to start solving from. This also makes it advisable not to make too large steps in bias between solutions. DC characteristics are simulated by first solving for a particular gate or drain bias voltage, and then the voltage of the drain or gate electrode is swept in an appropriate voltage interval with a suitable step size. The solutions for the simulated bias points are logged and then plotted in TonyPlot, where the results can also be exported. As the source voltage is left at zero,  $V_G$  is equal to  $V_{GS}$ , and  $V_D$  is equal to  $V_{DS}$ . The graph function `dydx (drain current, gate voltage)` is used in TonyPlot to get  $g_m$  curves [5].

## 2.3 Figures of merit

Figures of merit are used to measure and compare the characteristics of the simulated transistors. The on-resistance,  $R_{on}$ , is obtained by taking the inverse of the slope of the drain current ( $I_D$ ) as a function of the drain voltage ( $V_D$ ) at zero drain voltage, while the gate voltage ( $V_G$ ) is constant and the source voltage is zero. In this work  $R_{on}$  is measured at a  $V_G$  of 0.5V.  $R_{on}$  is normalized by multiplying with the circumference, and the normalized resistance is given in  $\Omega\mu\text{m}$ . From the  $I_D$ - $V_D$  data another figure is determined,  $I_{max}$ , which for the purposes of this work is the drain current at  $V_G = 0.5\text{V}$  and  $V_D = 0.8\text{V}$ . To normalize the current, it is divided by the circumference and presented in the unit  $\text{mA}/\mu\text{m}$ . Note that  $\text{mA}/\mu\text{m}$  is equivalent to  $\text{A}/\text{mm}$ . Both  $R_{on}$  and  $I_{max}$  should be affected by changes in the threshold

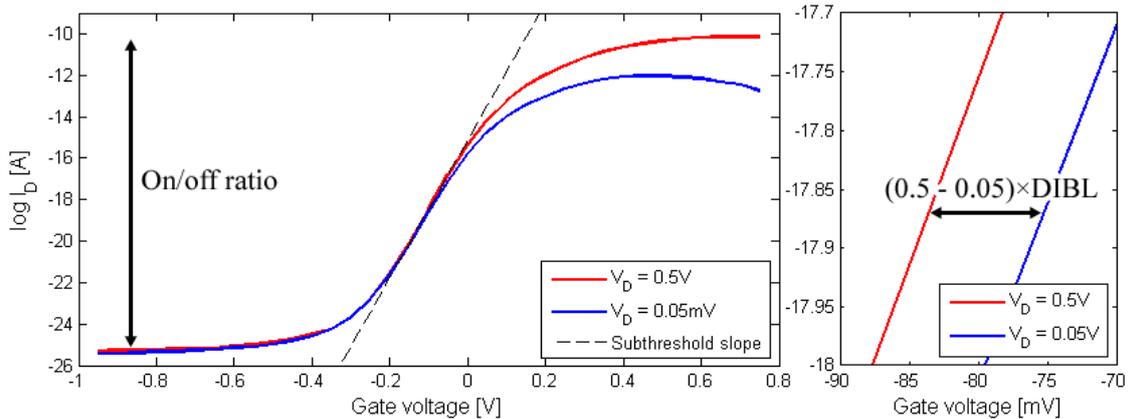
voltage. The threshold voltage is the gate-source voltage at which the transistor enters triode mode, also called the linear region.  $R_{on}$  will increase and  $I_{max}$  will decrease as the threshold voltage increases.

Equation 2.22 expresses the transconductance,  $g_m$ , which is the derivative of  $I_D$  as a function of  $V_G$  while  $V_D$  is constant and the source voltage is zero. Transconductance is acquired at  $V_D = 0.5V$  throughout this thesis. Transconductance is normally measured in siemens, the inverse of  $\Omega$ , however the convention for nanowire devices is to normalize the transconductance with the circumference. The normalized  $g_m$  is given in the unit mS/ $\mu m$ . This way of normalizing assumes that most of the current flows along the surface of the NW. Note that this unit is equivalent to S/mm. The maximum transconductance,  $g_{m,max}$  is used as a figure of merit.

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D} \quad (2.22)$$

The inverse subthreshold slope (SS) describes the transition between the on and off states of the transistor. The inverse SS is particularly significant for applications where the transistor is used as a switch, for example in digital logic [6]. It is determined by plotting  $I_D$  on a logarithmic scale as a function of  $V_G$  for  $V_D = 0.5V$ . This is done in TonyPlot, and the ruler tool is then used to determine the inverse SS. The inverse SS is presented in the unit mV/dec, where dec (short for decade) corresponds to  $I_D$  increasing 10 times. The inverse SS should ideally be close to the theoretical lower limit of 60mV/dec at room temperature. Drain induced barrier lowering, DIBL, is a measure of how much the threshold voltage is affected by a change in the drain voltage. DIBL is attained by comparing two  $I_D$ - $V_G$  sweeps, for  $V_D = 0.5V$  and  $V_D = 0.05V$  respectively. The logarithmic drain currents are then plotted, and DIBL is calculated by taking the difference in gate voltage between the two subthreshold slopes, and then dividing it by the difference in drain voltage. DIBL is usually preferred to be low, and the conventional unit for it is mV/V. The on/off ratio indicates how much the drain current changes between on and off states at a  $V_D$  of 0.5V. For simplicity the on/off ratio in this work is calculated by dividing the maximum  $I_D$  with the minimum  $I_D$  of the  $I_D$ - $V_G$  simulation result. The on/off ratio is unitless. Figure 2.1 is meant to illustrate how some of the figures of merit are obtained.

**Figure 2.1: Illustration of the subthreshold slope, on/off ratio and DIBL.**



### 3 Results and discussion

Section 3.1 concerns simulations made with the drift-diffusion transport model. Table 3.1 collects results from simulations with differently doped NWs of varied radius. Table 3.2 contains the figures of merit from simulations of transistor with different NW radius, where the transistor channel is low-doped and the rest of the NW is heavy-doped. Figure 3.1 is intended to illustrate this case, and figure 3.2 and 3.3 display the current-voltage characteristics from which the figures of merit in table 3.2 was determined. The NW length is varied for transistors with low-doped channels to reduce the lengths of the heavy-doped regions and thus reduce the resistance they cause. The figures of merit from these simulations are in table 3.3. Some possibilities of the low-doped region in the NW not matching the gate edges are explored, and the results are compiled in table 3.4. Table 3.5 contains the figures of merit for transistors with varied electron saturation velocity and electron mobility in the low-doped region. Different cases where  $\mu_n$  and  $v_{sat,n}$  are reduced in a NW surface layer are also investigated, see table 3.6. Table 3.7 compiles the figures of merit for InAs NW transistors simulated with different gate lengths and NW radiuses. The gate self-capacitances for three transistors with different NW radius are determined and plotted as functions of gate-voltage in figure 3.5. Figure 3.6 shows  $g_m/C_{gg}$ , which is a measure of how much the drain current changes as a function of the charge at the gate.

Section 3.2 contains the results acquired from the quantum models. Table 3.8 contains the figures of merit for transistor with different uniform NW doping and varying NW radius simulated with the drift-diffusion mode-space model. Employing the DD\_MS model, a transistor with n-doping concentrations as high as  $10^{19}\text{cm}^{-3}$  in parts of the NW could only be simulated with the NW radius 2.5nm. Figure 3.7 shows the simulated  $I_D-V_G$  characteristics of this device. Further quantum simulations are made utilizing the NEGF\_MS model. Figures 3.8 and 3.9 illustrate the  $I_D-V_G$  characteristics for transistors where part of the channel is low-doped and the doping in rest of the NW is high. The figures of merit obtained from these results are collected in table 3.9. The maximum transconductance for transistors with different  $t_{ox}$  is investigated, and figure 3.10 displays  $g_{m,max}$  as a function of  $t_{ox}$  for the NW radiuses 2.5nm and 5nm. Table 3.10 contains the figures of merit for transistors with the gate length 10nm and different length NWs with the radius 5nm. The gate self-capacitance,  $C_{gg}$ , is determined for three transistors with different radiuses using the NEGF\_MS model.  $C_{gg}$  is plotted in figure 3.11, and  $g_m/C_{gg}$  is plotted in figure 3.12. Table 3.11 collects the figures of merit for transistors simulated with different gate-lengths. NW transistors are simulated with different radiuses and doping levels in the lower  $\frac{3}{4}$  of the channel while  $L_g = 50\text{nm}$ . The figures of merit obtained are listed in table 3.12. Table 3.13, 3.14 and 3.15 contains the figures of merit for transistors with varied NW radius and channel-doping. For table 3.13 the gate length is 20nm, for table 3.14 the gate length is 10nm, and for table 3.15 the gate length is 5nm.

To compare the models, the radial current density for two cases are simulated with the drift-diffusion model and presented in figure 3.13. Equivalent graphs for the NEGF\_MS model are shown in figure 3.14. Figure 3.15 show the  $I_D$ - $V_G$  characteristics for identical InAs NW transistors simulated with the three different models used in this work.

### 3.1 Classical drift-diffusion transport simulations

The first sets of simulations are done with the classical drift-diffusion transport model. Note that unless otherwise stated, the lengths of the InAs NWs are 600nm, and the gate-lengths are 200nm, as these dimensions are used for most of the simulations. Initially the electron mobility parameter  $\mu_{n}$  is set to  $3000 \text{ cm}^2/\text{Vs}$  for the entire wire, and  $v_{satn}$  is set to  $2.0 \times 10^7 \text{ cm/s}$ . The relative dielectric constant,  $\epsilon_r$ , of the gate oxide is 20. First the effects of varying the radius of NWs with different n-doping concentrations are investigated. Table 3.1 presents the figures of merit from these simulations.

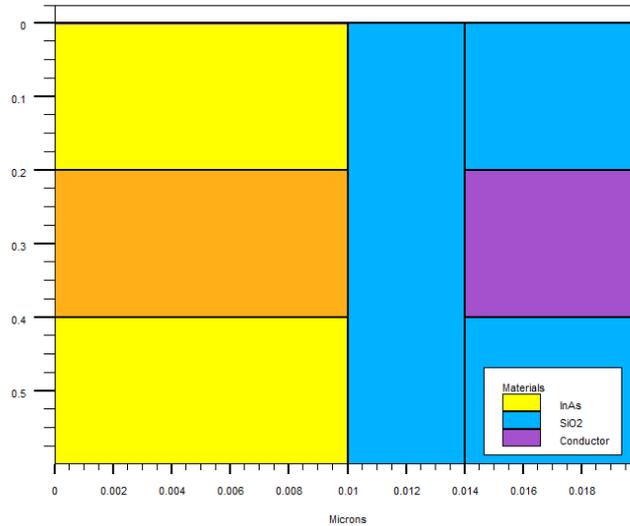
**Table 3.1: Figures of merit for transistors simulated with different radiuses and NW doping.** Inverse SS,  $g_{m,max}$  and on/off ratio are measured at  $V_D = 0.5\text{V}$ .  $R_{on}$  is extracted at  $V_G = 0.5\text{V}$  and  $I_{max}$  determined at  $V_G = 0.5\text{V}$  and  $V_D = 0.8\text{V}$ . DIBL is determined by using  $I_D$ - $V_G$  characteristics obtained at  $V_D = 0.5\text{V}$  and  $V_D = 0.05\text{V}$ .

n-doping [ $\text{cm}^{-3}$ ]	NW radius [nm]	$g_{m,max}$ [ $\text{mS}/\mu\text{m}$ ]	Inverse SS [ $\text{mV}/\text{dec}$ ]	DIBL [ $\text{mV}/\text{V}$ ]	On/off ratio	$R_{on}$ [ $\Omega\mu\text{m}$ ]	$I_{max}$ [ $\text{mA}/\mu\text{m}$ ]
$1.0 \times 10^{17}$	10	0.08	61	10	$2.6 \times 10^5$	10620	0.016
	15	0.12	61	11	$2.0 \times 10^5$	8710	0.024
	20	0.16	62	12	$1.3 \times 10^5$	7290	0.032
	30	0.21	63	14	$8.5 \times 10^4$	5390	0.048
$1.7 \times 10^{18}$	10	0.67	61	10	$1.6 \times 10^7$	1450	0.21
	15	0.92	62	11	$2.7 \times 10^6$	970	0.33
	20	1.11	69	15	$4.8 \times 10^5$	720	0.45
	30	1.35	250	220	200	470	0.71
$3.4 \times 10^{18}$	10	1.03	62	10	$1.7 \times 10^7$	720	0.33
	15	1.35	70	15	$8.5 \times 10^5$	480	0.54
	20	1.57	167	92	3130	360	0.77
	30	1.85	830	780	13	240	1.27
$5.0 \times 10^{18}$	10	1.30	62	11	$1.6 \times 10^7$	600	0.39
	15	1.68	107	33	$1.1 \times 10^5$	370	0.69
	20	1.99	360	510	160	270	1.03
	30	2.33	1380	>4000	7	170	1.77
$1.0 \times 10^{19}$	10	2.07	82	27	$1.3 \times 10^6$	580	0.55
	15	2.65	530	1560	100	290	1.11
	20	3.11	1230	2580	5	180	1.79
	30	3.71	3000	>4000	2	100	3.28

Based on the results in table 3.1, higher doping gives better transconductance, higher  $I_{max}$  and lower on-resistance, but worse inverse SS, DIBL and on/off ratio. Increasing the radius of the InAs NW has similar effects on the figures of merit as increasing the doping concentration.

In the previous case the entire InAs NW is n-doped with the same concentration. It's suspected to be more beneficial to have low n-doping, in this case  $10^{17} \text{ cm}^{-3}$ , in the channel, and high n-doping ( $10^{19} \text{ cm}^{-3}$ ) in the rest of the NW. Figure 3.1 illustrates this case, and table 3.2 compiles the figures of merit collected from simulations with this NW doping for different radiuses. Figure 3.2 and 3.3 displays the  $I$ - $V$  characteristics recorded from these simulations. It is clear from the figures of merit that this doping scheme is better than having uniform doping in the entire NW. The inverse SS and DIBL are low, the on/off ratio is high and  $g_{m,max}$  is greater than  $1 \text{ mS}/\mu\text{m}$  for all devices in table 3.2.

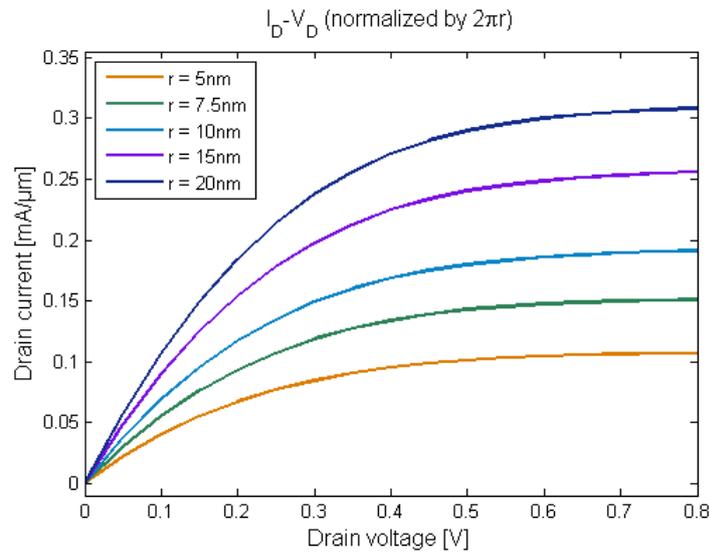
**Figure 3.1: InAs NW transistor structure, seen in radial cross-section of the simulated cylindrical devices.** The yellow regions are the parts of the InAs NWs that are doped with the donor concentration  $10^{19} \text{ cm}^{-3}$ . The orange region of the InAs NW has the donor concentration of  $10^{17} \text{ cm}^{-3}$ . Blue regions are oxides, and the purple region is the gate electrode. The source and drain electrodes are too thin to be seen in the image. See figure 1.1 for a three-dimensional view of a similar device.



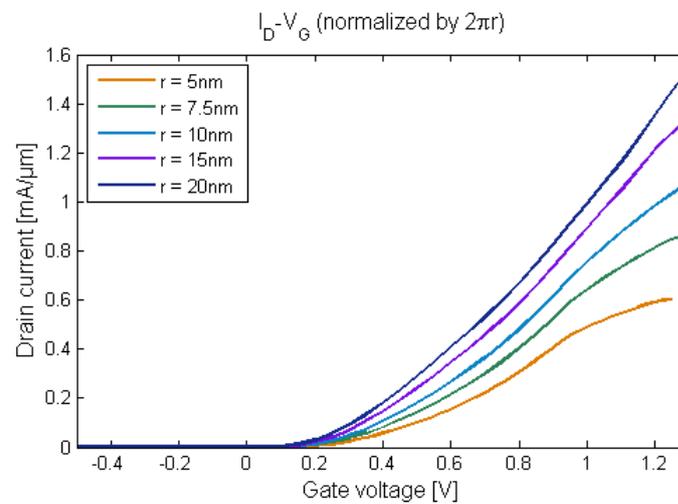
**Table 3.2: Figures of merit for transistors with different NW radiuses, simulated with the NW doping in figure 3.1.** Maximum transconductance, inverse SS and on/off ratio are extracted at  $V_D = 0.5 \text{ V}$ .  $R_{on}$  is determined at a  $V_G$  of  $0.5 \text{ V}$  and  $I_{max}$  is measured at the bias voltages  $V_G = 0.5 \text{ V}$  and  $V_D = 0.8 \text{ V}$ . DIBL is determined from  $I_D$ - $V_G$  characteristics simulated at  $V_D = 0.5 \text{ V}$  and  $V_D = 0.05 \text{ V}$ .

NW radius [nm]	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio	$R_{on}$ [ $\Omega\mu\text{m}$ ]	$I_{max}$ [mA/ $\mu\text{m}$ ]
5	1.035	60	9	$1.8 \times 10^8$	2270	0.107
7.5	1.280	60	10	$6.1 \times 10^7$	1640	0.151
10	1.488	60	10	$2.1 \times 10^7$	1340	0.191
15	1.684	61	11	$8.9 \times 10^6$	1040	0.256
20	1.981	62	12	$3.5 \times 10^6$	880	0.308

**Figure 3.2: The normalized  $I_D$ - $V_D$  characteristics for transistors with different NW radiuses, simulated with the NW doping profile in figure 3.1. The drain current is normalized by the NW circumference. The gate voltage is 0.5V.**



**Figure 3.3: The normalized  $I_D$ - $V_G$  characteristics for transistors with different NW radiuses,  $r$ , simulated with the NW doping in figure 3.1. The drain current is normalized by the NW circumference. The drain voltage is 0.5V.**



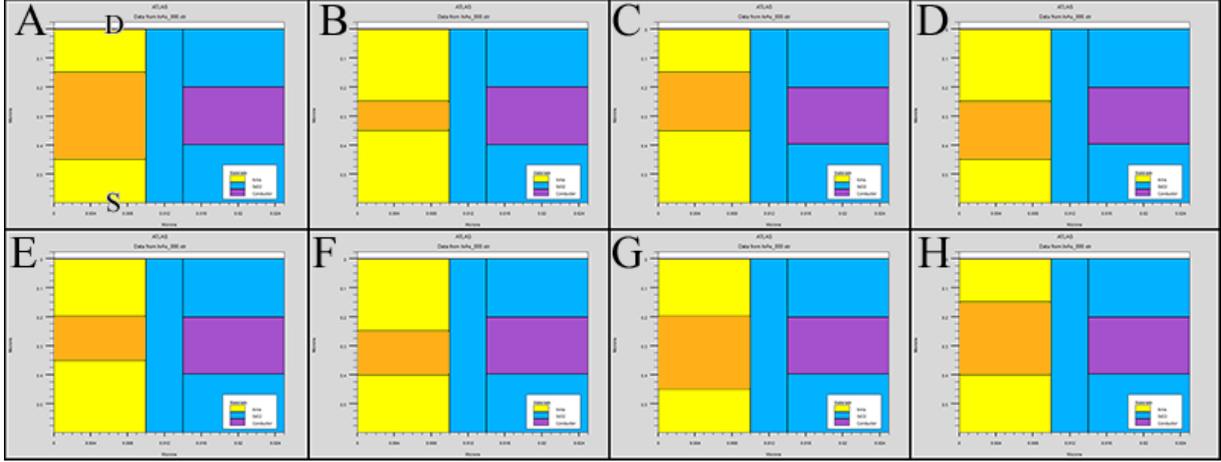
**Table 3.3: Figures of merit for transistors with different length InAs NWs.** The channel is n-doped with the concentration  $10^{17}\text{cm}^{-3}$  and the n-doping concentration in the rest of the NW is  $10^{19}\text{cm}^{-3}$ . Maximum transconductance, inverse SS and on/off ratio are measured at  $V_D = 0.5\text{V}$ .  $R_{on}$  is extracted at  $V_G = 0.5\text{V}$  and  $I_{max}$  is measured at  $V_G = 0.5\text{V}$  and  $V_D = 0.8\text{V}$ .

NW radius [nm]	NW length [nm]	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio	$R_{on}$ [ $\Omega\mu\text{m}$ ]	$I_{max}$ [mA/ $\mu\text{m}$ ]
5	600	1.035	60	9	$1.8 \times 10^8$	2270	0.107
	500	1.104	60	9	$5.5 \times 10^8$	2090	0.110
	400	1.185	60	9	$8.0 \times 10^8$	2010	0.113
	350	1.258	60	9	$9.8 \times 10^8$	1980	0.114
	300	1.230	60	9	$1.2 \times 10^9$	1980	0.114
10	600	1.488	60	10	$2.1 \times 10^7$	1340	0.191
	500	1.586	60	10	$2.5 \times 10^7$	1250	0.194
	400	1.688	60	10	$3.4 \times 10^7$	1210	0.199
	350	1.900	60	10	$4.6 \times 10^7$	1190	0.200
	300	1.906	60	10	$1.0 \times 10^9$	1180	0.201

Table 3.3 describes how the figures of merit are affected by the length of the NW being reduced from 600nm. The idea was that this would lower the on-resistance; however as the results show the decrease in resistance is less than 15% between the NW lengths of 600nm and 300nm for the selected radiuses. It seems like the low doped region is responsible for much of the on-resistance. One possible explanation is that the mobility model might be interpreting the band bending in the device as an electric field in the low doped region, when it's actually caused by the difference in doping.

When fabricating a device, it may be difficult to always get everything to line up. It is therefore informative to simulate NW transistors where the low doped region doesn't exactly match the gate. In these cases the low doped region does not cover the entire channel, and/or extends outside of the gate. Figure 3.3 illustrates the eight transistors, labeled A-H, simulated for this reason. The offset between the region limits and the gate edges is selected to be  $\pm 50\text{nm}$ . The possibility that one of the limits of the low doped region line up with the gate is also considered.

**Figure 3.4: The eight types of misalignment designated A-H, seen in radial cross-sections of the simulated cylindrical devices.** The yellow regions are the parts of the InAs NWs that are n-doped with the concentration  $10^{19} \text{ cm}^{-3}$ . The orange regions of the InAs NWs have an n-doping concentration of  $10^{17} \text{ cm}^{-3}$ . Blue regions are oxide, and the purple region is the gate electrode. Note that the drain is located at the top of the NWs, and the source at the bottom, however these electrodes are too thin to be seen in the figure. The length of the NWs are 600nm, the radiuses are 10nm, the gate lengths are 200nm and  $t_{ox} = 4\text{nm}$ .



**Table 3.4: The figures of merit corresponding to transistors simulated with misaligned low-doped regions shown in figure 3.4.** The simulated NWs all have the radius of 10nm. Inverse SS,  $g_{m,max}$  and on/off ratio are observed at  $V_D = 0.5\text{V}$ .  $R_{on}$  is determined at  $V_G = 0.5\text{V}$  and  $I_{max}$  at  $V_G = 0.5\text{V}$  and  $V_D = 0.8\text{V}$ .

transistor	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio	$R_{on}$ [ $\Omega\mu\text{m}$ ]	$I_{max}$ [mA/ $\mu\text{m}$ ]
A	0.394	60	10	$4.9 \times 10^6$	2830	0.124
B	1.225	62	10	$1.3 \times 10^7$	1180	0.224
C	0.656	61	11	$6.3 \times 10^6$	2010	0.198
D	0.426	61	10	$5.9 \times 10^6$	2010	0.136
E	1.163	60	10	$2.4 \times 10^7$	1270	0.205
F	1.537	61	10	$2.4 \times 10^7$	1270	0.205
G	0.401	61	10	$9.2 \times 10^6$	2100	0.128
H	0.630	61	11	$8.2 \times 10^6$	2090	0.183

Based on the figures in table 3.4, having the low-doped region outside of the gate edges gives low  $g_{m,max}$  and high  $R_{on}$ . It's better to keep the low-doped region within the channel, like in the case of transistors B, E and F. The results indicate that it is more important for the transconductance that the low-doped region is aligned with the gate edge on the source side than on the drain side. The F transistor in table 3.4 is noted to have a higher  $g_{m,max}$  than a transistor with the same NW radius and the low-doped region aligned with the gate. Because of this, simulations are continued using the F misalignment.

To get a sense of what happens when the mobility and saturation velocity are increased, these properties are varied in the low doped region. Table 3.5 charts the figures of merit recorded from these simulations. DIBL was determined to 10mV/V for six of the cases, and presumably the other three would also give this figure, particularly since the inverse SS didn't vary either. The maximum transconductance increases with both  $\mu_n$  and  $v_{sat,n}$ , as does  $I_{max}$ . The on-resistance decreases as  $\mu_n$  and/or  $v_{sat,n}$  is increased.

**Table 3.5: Figures of merit at different  $v_{sat,n}$  and  $\mu_n$  in the low-doped region of the transistor.** The NW radius is 10nm. Other device dimensions and the doping are also the same as for transistor F in figure 3.4 and table 3.4. Inverse SS,  $g_{m,max}$  and on/off ratio are determined at  $V_D = 0.5V$ .  $R_{on}$  is measured at  $V_G = 0.5V$  and  $I_{max}$  at  $V_G = 0.5V$  and  $V_D = 0.8V$ .

$v_{sat,n}$ [cm/s]	$\mu_n$ [cm <sup>2</sup> /Vs]	$g_{m,max}$ [mS/ $\mu$ m]	Inverse SS [mV/dec]	On/off ratio	$R_{on}$ [ $\Omega\mu$ m]	$I_{max}$ [mA/ $\mu$ m]
$2 \times 10^7$	3000	1.54	61	$2.4 \times 10^7$	1270	0.205
	6000	1.66	61	$2.5 \times 10^7$	1170	0.227
	9000	1.78	61	$1.9 \times 10^7$	1140	0.235
$5 \times 10^7$	3000	1.84	61	$3.6 \times 10^7$	1020	0.271
	6000	2.07	61	$2.2 \times 10^7$	930	0.309
	9000	2.14	61	$2.0 \times 10^7$	900	0.323
$1 \times 10^8$	3000	1.99	61	$1.4 \times 10^7$	960	0.297
	6000	2.16	61	$1.2 \times 10^7$	850	0.345
	9000	2.25	61	$8.9 \times 10^6$	790	0.363

In real devices, defects at the surface of the nanowire may reduce mobility and saturation velocity. This is simulated by having a surface layer where  $\mu_n$  and  $v_{sat,n}$  are reduced to a specified percentage of the normal values. The layer thickness,  $t_{surf}$ , is also varied, while the total InAs NW radius is constant at 10nm. Like in the previous case the transistor dimensions, doping concentrations and misalignment from transistor F in figure 3.4 are used. The unreduced  $v_{sat,n}$  is set to  $2 \times 10^7$  cm/s, and the unreduced  $\mu_n$  in the low-doped region is  $8000 \text{ cm}^2/\text{Vs}$ . The electron mobility is  $3000 \text{ cm}^2/\text{Vs}$  in the higher doped regions. The figures of merit from these simulations are summarized in table 3.6. DIBL is assumed to be 10mV/V for all instances in table 3.6, though due to time constraints this is only verified for a few of the cases. Like in table 3.5 the inverse SS is unaffected by the changes in mobility and saturation velocity. The simulated surface layers severely reduce the transconductance and raise  $R_{on}$ . This kind of phenomena is therefore very undesirable.

**Table 3.6: Figures of merit for NW transistors with a surface layer where  $\mu_n$  and  $v_{sat,n}$  are reduced.** The device dimensions and doping are the same as for transistor F in figure 3.4 and table 3.4. The NW radiuses for the simulated devices are 10nm. The unreduced  $v_{sat,n}$  is  $2 \times 10^7$  cm/s. The unreduced electron mobility is  $8000 \text{ cm}^2/\text{Vs}$  in the low-doped region, and  $3000 \text{ cm}^2/\text{Vs}$  in the high doped regions. Inverse SS,  $g_{m,max}$  and on/off ratio are measured at  $V_D = 0.5\text{V}$ .  $R_{on}$  extracted at  $V_G = 0.5\text{V}$  and  $I_{max}$  determined at  $V_G = 0.5\text{V}$  and  $V_D = 0.8\text{V}$ .

$t_{surf}$	percentage	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	On/off ratio	$R_{on}$ [ $\Omega\mu\text{m}$ ]	$I_{max}$ [mA/ $\mu\text{m}$ ]
0 nm	-	1.77	61	$2.7 \times 10^7$	1110	0.232
1 nm	50%	1.41	61	$1.3 \times 10^7$	1320	0.196
	20%	1.17	61	$1.4 \times 10^7$	1550	0.174
	10%	1.09	61	$1.3 \times 10^7$	1620	0.166
2 nm	50%	1.24	61	$1.7 \times 10^7$	1460	0.177
	20%	0.93	61	$1.2 \times 10^7$	1880	0.143
	10%	0.83	61	$1.8 \times 10^7$	2050	0.132
3 nm	50%	1.14	61	$1.4 \times 10^7$	1600	0.161
	20%	0.76	61	$1.0 \times 10^7$	2280	0.118
	10%	0.63	61	$8.9 \times 10^6$	2620	0.103

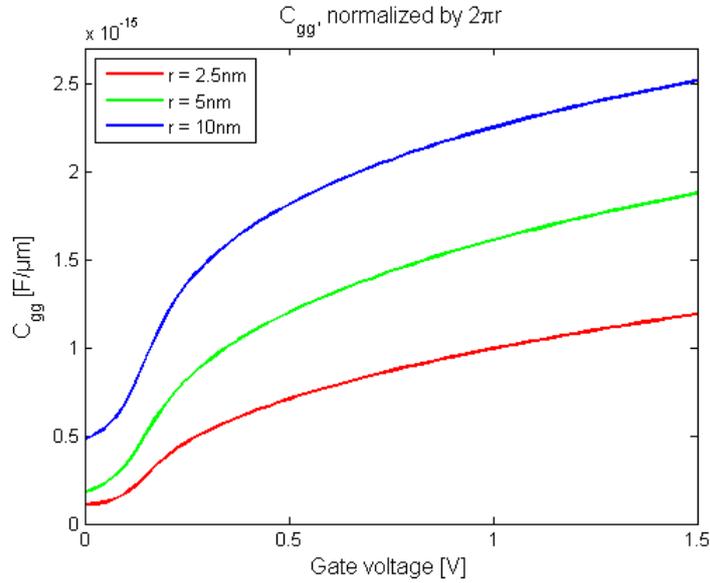
Table 3.7 displays the figures of merit when the gate length is scaled for transistors with different NW radiuses. The lightly doped region is scaled as well, so that it covers the lower  $\frac{3}{4}$  of the channel, like for transistor F in figure 3.4. Decreasing the gate-length doesn't have much effect on  $g_{m,max}$  or  $R_{on}$ . According to the results in table 3.7, the inverse SS and DIBL become worse as  $L_g$  is decreased if the NW radius is too large. For example if the gate-length is close to 50nm, the NW radius should be around 10nm or less to get good figures for the inverse SS and DIBL.

**Table 3.7: Figures of merit for simulated InAs NW transistors with different gate lengths and NW radiuses.** The NW length is 600nm,  $t_{ox}$  is 4nm, and  $\epsilon_r$  for the gate oxide is 20. Like in previous cases the high doping concentration is  $10^{19} \text{ cm}^{-3}$ , and the low  $10^{17} \text{ cm}^{-3}$ , both n-type. The low doped region is scaled to cover the lower  $\frac{3}{4}$  of the channel. The electron mobility is  $8000 \text{ cm}^2/\text{Vs}$  in the lightly doped region, and  $3000 \text{ cm}^2/\text{Vs}$  in the highly doped regions. Inverse SS,  $g_{m,max}$  and on/off ratio are assessed at  $V_D = 0.5\text{V}$ .  $R_{on}$  is extracted at  $V_G = 0.5\text{V}$  and  $I_{max}$  is evaluated while  $V_G = 0.5\text{V}$  and  $V_D = 0.8\text{V}$ . DIBL is extrapolated using  $I_D-V_G$  characteristics simulated at  $V_D = 0.5\text{V}$  and  $V_D = 0.05\text{V}$ .

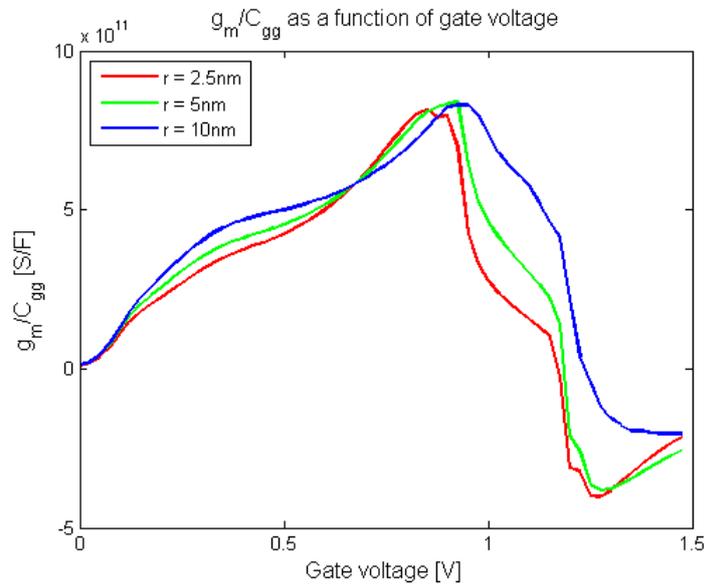
$L_g$ [nm]	NW radius [nm]	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio	$R_{on}$ [ $\Omega\mu\text{m}$ ]	$I_{max}$ [mA/ $\mu\text{m}$ ]
200	5	1.25	60	9	$2.8 \times 10^8$	1890	0.129
	10	1.74	61	10	$2.7 \times 10^7$	1110	0.232
	20	2.06	62	11	$1.4 \times 10^6$	700	0.377
100	5	1.24	61	10	$2.3 \times 10^8$	1840	0.135
	10	1.71	61	10	$3.1 \times 10^7$	1090	0.239
	20	1.99	64	17	$4.1 \times 10^6$	690	0.395
50	5	1.25	61	10	$1.4 \times 10^8$	1880	0.134
	10	1.72	62	12	$1.9 \times 10^7$	1100	0.245
	20	1.96	87	92	$4.4 \times 10^5$	660	0.462
20	5	1.24	62	16	$2.7 \times 10^8$	1840	0.144
	10	1.71	73	56	$1.2 \times 10^7$	960	0.325
	20	2.09	700	1280	140	480	0.836

The quasi-static gate self-capacitance,  $C_{gg}$ , is determined for three NW radiuses; 2.5nm, 5nm and 10nm. Other transistor dimensions are the same as for transistor F in figure 3.4.  $C_{gg}$  is measured as a function of the gate voltage, with no bias at source or drain. Figure 3.5 displays the results of these simulations.  $C_{gg}$  is normalized by the circumference of the corresponding NW. Using these values,  $g_m/C_{gg}$  can be calculated, and is plotted in figure 3.5.  $g_m/C_{gg}$  is a measure of how much the drain current changes depending on the charge at the gate. As the transconductance and the capacitance are normalized the same way, the normalization factors take each other out for  $g_m/C_{gg}$ . At least up to about  $V_G = 1\text{V}$  the curves are close together. This means that  $g_m/C_{gg}$  is independent of the radius of the NW. This suggests that normalizing the transconductance by the gate capacitance might be better than normalizing using the nanowire circumference, since the normalization is done to make it easier to compare transistors that have different NW radiuses.

**Figure 3.5: Gate self-capacitance as a function of  $V_G$ .** The capacitance is normalized by the circumference  $2\pi r$ , where  $r$  is the NW radius. The relative permittivity,  $\epsilon_r$ , for the gate oxide is 20. Except for NW radius, the transistor dimensions and doping distribution are that of transistor F in figure 3.4. The high n-doping concentration is  $10^{19} \text{ cm}^{-3}$ , and the low concentration is  $10^{17} \text{ cm}^{-3}$ . The electron mobility is  $8000 \text{ cm}^2/\text{Vs}$  in the lightly doped region, and  $3000 \text{ cm}^2/\text{Vs}$  in the heavily doped regions. The drain voltage is 0V, as is the source voltage.



**Figure 3.6: Transconductance divided by gate self-capacitance as a function of gate voltage.** The transconductance is measured at  $V_D = 0.5 \text{ V}$ . The transistor specifications are the same as for the previous figure.



## 3.2 Quantum simulations

The NW transistors modeled in the previous should in reality be influenced by quantum mechanical effects. The drift-diffusion mode-space model and the NEGF mode-space model are used to make simulations that cover effects like quantum confinement. For the quantum models, only  $I_D$ - $V_G$  characteristics are simulated. This means that the quantum models are not used to determine  $R_{on}$  and  $I_{max}$ .

### 3.2.1 Drift-diffusion mode-space simulations

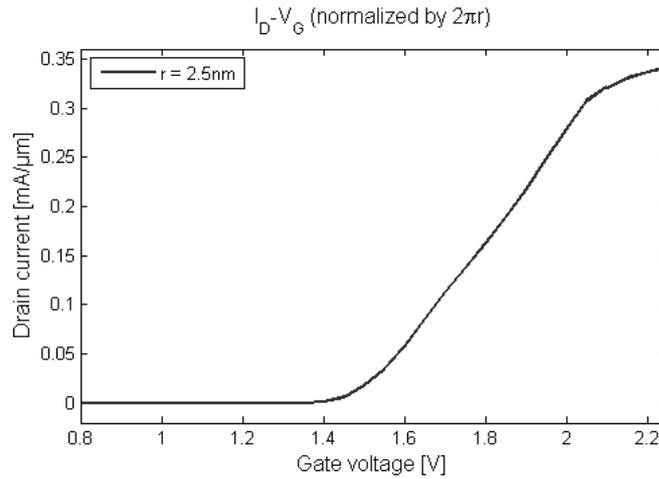
DD\_MS is similar to the drift-diffusion transport model, but with added quantum mechanical ability. It's referred to as "semiclassical" in the Atlas User's manual [5]. Unfortunately simulations of NW transistors with donor concentrations as high as  $10^{19}\text{cm}^{-3}$  in parts of the NW at radiuses of 5nm and larger gave unreasonable results, if any. These current-voltage curves were irregular and did not look anything like the other results. This may be because of problems with convergence. Transistors with InAs NWs of different radius are simulated with different n-doping concentrations in the entire wire. Table 3.8 shows the results of these simulations. The  $g_{m,max}$  and inverse SS figures are slightly lower than for InAs NW transistors simulated with the classical drift-diffusion transport model.

**Table 3.8: Figures of merit of InAs NW transistors simulated with different NW radiuses and n-doping.** On/off ratio, inverse SS and maximum transconductance are measured for  $V_D = 0.5\text{V}$ . The NW length is 600nm, the gate length is 200nm,  $t_{ox}$  is 4nm, and  $\epsilon_r$  for the gate oxide is 20 for the simulations.

n-doping [ $\text{cm}^{-3}$ ]	NW radius [nm]	$g_{m,max}$ [ $\text{mS}/\mu\text{m}$ ]	Inverse SS [ $\text{mV}/\text{dec}$ ]	On/off ratio
$10^{17}$	5	0.05	60.0	$8.1 \times 10^{11}$
	7.5	0.07	60.0	$4.9 \times 10^8$
	10	0.08	60.0	$4.5 \times 10^7$
	15	0.12	60.6	$3.9 \times 10^6$
	20	0.16	60.5	$1.2 \times 10^6$
$10^{18}$	5	0.31	60.0	$1.6 \times 10^{11}$
	7.5	0.33	60.0	$6.3 \times 10^9$
	10	0.47	60.7	$2.9 \times 10^8$
	15	0.64	62.4	$1.9 \times 10^7$
	20	0.78	62.0	$3.4 \times 10^6$

The transistor NW radius 2.5nm is technically too small to be in the scope of interest for this work. Unfortunately this is the only simulation attempt with the doping settings of transistor F (from figure 3.4) that worked properly with DD\_MS. The normalized maximum transconductance at  $V_D = 0.5V$  is determined to 0.61mS/ $\mu\text{m}$  for this device. The inverse SS is 60mV/dec and the on/off ratio is  $3.4 \times 10^{11}$ . The  $I_D-V_G$  characteristics can be seen in figure 3.7.

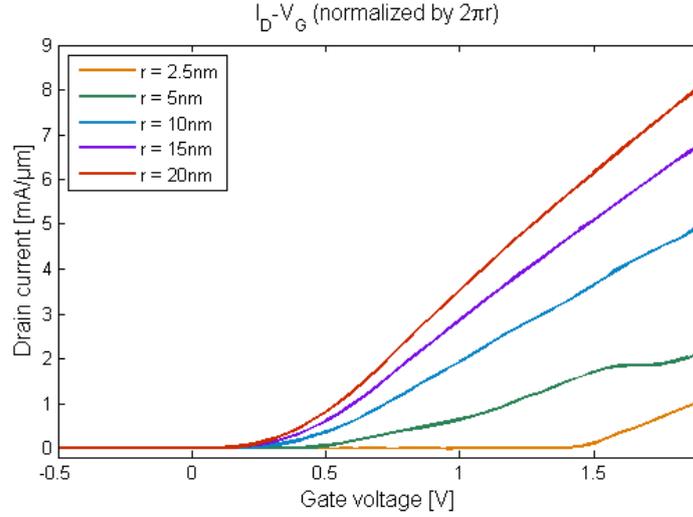
**Figure 3.7:  $I_D-V_G$  characteristics for an InAs NW transistor.** The NW length is 600nm, the gate length is 200nm,  $t_{ox}$  is 4nm and  $\epsilon_r$  for the gate oxide is 20. The lower  $\frac{3}{4}$  of the channel is n-doped with the concentration  $10^{17} \text{ cm}^{-3}$ , and the rest of the NW with the concentration  $10^{19} \text{ cm}^{-3}$ . The electron mobility is  $8000 \text{ cm}^2/\text{Vs}$  in the lightly doped region, and  $3000 \text{ cm}^2/\text{Vs}$  in the highly doped regions. The drain voltage is 0.5V.



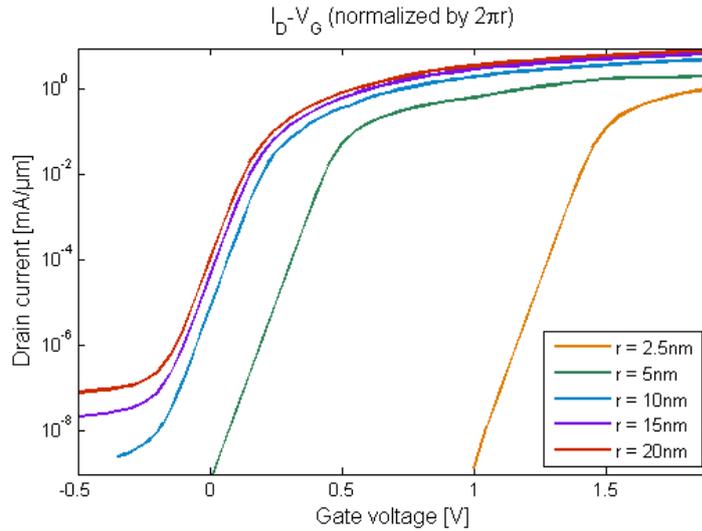
### 3.2.2 Non-equilibrium Green's function mode-space simulations

The NEGF\_MS model takes quantum mechanics into account and it simulates ballistic transport, meaning that the model ignores scattering events. These simulations should give the maximum theoretically possible drain current and transconductance for a given NW transistor at specified bias. The first simulations are for devices using the dimensions of the transistor labeled F in figure 3.4, but the NW radius is varied. The  $I_D-V_G$  characteristics are plotted in linear scale in figure 3.8, and in logarithmic scale in figure 3.9. The figures of merit are listed in table 3.9. Like expected the drain currents in this case are much larger than for the non-ballistic transport models. This can be observed by comparing figure 3.8 to figure 3.3. The smallest transistor simulated has a NW radius of 2.5nm, which is so small that there is only one subband. The un-normalized transconductance of this device is approximately  $37 \mu\text{S}$ . This is curious because in theory the ballistic transconductance for a single subband should be around  $77 \mu\text{S}$ , or specifically  $2q^2/h$  [7], but the NEGF\_MS model seems to only give about half of that. This may be because of an error in the model.

**Figure 3.8:  $I_D$ - $V_G$  characteristics for transistors with different NW radiuses.** Except for the radiuses, the device dimensions and doping are that of transistor F in figure 3.4. The drain voltage is 0.5V.



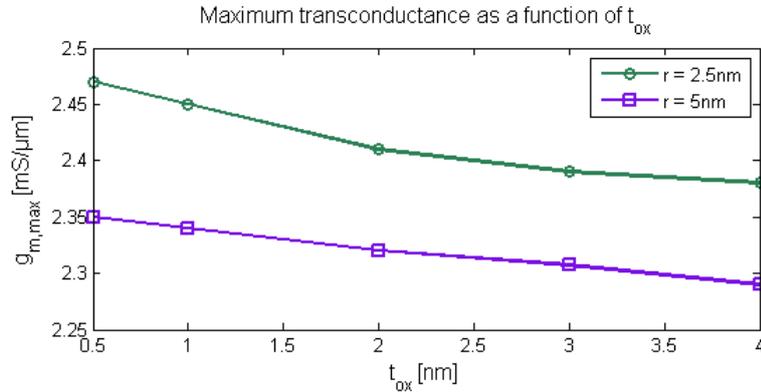
**Figure 3.9: The currents in figure 3.8 plotted in logarithmic scale to show the subthreshold slopes.** The conditions are the same as for figure 3.8, as this figure displays the same data. The drain voltage is 0.5V.



**Table 3.9: Figures of merit for simulated InAs NW transistors with different NW radiuses.** The NW length is 600nm, the gate length is 200nm,  $t_{ox}$  is 4nm, and  $\epsilon_r$  for the gate oxide is 20. The high doping concentration is  $10^{19} \text{ cm}^{-3}$ , and the low  $10^{17} \text{ cm}^{-3}$ , both n-type. The low doped region covers the lower  $\frac{3}{4}$  of the channel, like in the case of transistor F in figure 3.4. Inverse SS,  $g_{m,max}$ , on/off ratio are evaluated at  $V_D = 0.5\text{V}$  and DIBL is measured using simulations at  $V_D = 0.5\text{V}$  and  $V_D = 0.05\text{V}$ .

NW radius [nm]	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio
2.5	2.38	60	8	$3.6 \times 10^{14}$
5	2.29	60	9	$1.1 \times 10^{14}$
10	3.90	60	9	$2.3 \times 10^9$
15	4.91	60	9	$2.1 \times 10^8$
20	5.95	60	9	$3.9 \times 10^7$

**Figure 3.10: Maximum transconductance as a function of oxide thickness for two different NW radii.** The transconductance is normalized by the circumference of the NW. The relative permittivity of the gate oxide is 20. The transconductance is obtained at  $V_D = 0.5V$ .



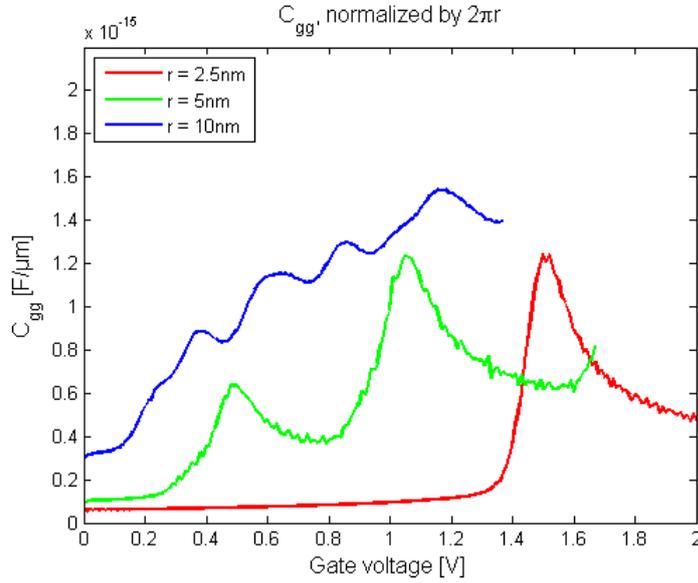
To see if  $t_{ox}$  is a large influence on the transconductance, and thus the cause of the unexpectedly low transconductance, simulations with different  $t_{ox}$  are made. For these simulations only  $g_{m,max}$  is noted, and the plotted as a function of  $t_{ox}$ , see figure 3.10. The maximum transconductance doesn't change much in these two cases. This means that the devices are close to the quantum capacitance limit. The oxide thickness does not seem to be the cause of the low transconductance.

The length of the NW is varied to decrease the distance between the gate and drain,  $L_{GD}$ , as well as the gate and source,  $L_{GS}$ . During these simulations the gate length is 10nm, and always situated at the center of the length of the NW. In other words  $L_{GD}$  and  $L_{GS}$  are equal. The NW radius used is 5nm, and the figures of merit are compiled in table 3.10. Decreasing the length of the NW doesn't improve  $g_{m,max}$  much. This makes it more likely that there is an error or bug in Atlas which causes the transconductance to be about half of the expected ballistic transconductance. It is also noted that the inverse SS and DIBL start to decrease somewhere between  $L_{GD} = 50$ nm and  $L_{GD} = 25$ nm.

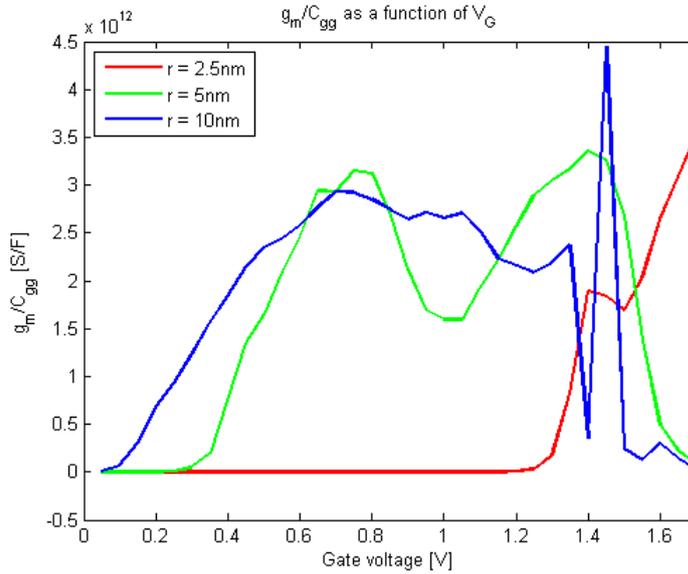
**Table 3.10: Figures of merit for transistors simulated with different length NWs.** The NW radius is 5nm and the gate length is 10nm. The lower  $\frac{3}{4}$  of the channel is n-doped to the concentration  $10^{17} \text{ cm}^{-3}$ , like in the case of transistor F in figure 3.4. The rest of the NW has a donor concentration of  $10^{19} \text{ cm}^{-3}$ . Inverse SS,  $g_{m,max}$  and on/off ratio are measured for  $V_D = 0.5V$ . DIBL is determined using  $I_D-V_G$  characteristics simulated at drain voltages of 0.5V and 0.05V.

$L_{GD} (= L_{GS})$ [nm]	Total NW length [nm]	$g_{m,max}$ [mS/ $\mu$ m]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio
200	410	2.15	70	52	$3.8 \times 10^{13}$
100	210	2.15	70	55	$4.3 \times 10^{13}$
50	110	2.15	70	55	$4.2 \times 10^{13}$
25	60	2.18	62	29	$9.1 \times 10^{13}$
10	30	2.25	60	10	$1.3 \times 10^{14}$

**Figure 3.11: The gate self-capacitance,  $C_{gg}$ , as a function of the gate voltage.**  $C_{gg}$  is normalized by the circumference of the NW, and  $r$  in the figure is the NW radius. The relative permittivity,  $\epsilon_r$ , for the gate oxide is 20. The transistor dimensions and doping distribution are the same as for transistor F in figure 3.4, except for the NW radius. The high donor concentration is  $10^{19} \text{ cm}^{-3}$ , and the low donor concentration is  $10^{17} \text{ cm}^{-3}$ . The drain voltage and the source voltage are not biased.



**Figure 3.12: Transconductance divided by gate self-capacitance as a function of gate voltage.** The transconductance is measured at  $V_D = 0.5 \text{ V}$ . The transistor dimensions and properties are as specified in the description of figure 3.10.



The quasi-static gate self-capacitance,  $C_{gg}$ , is determined for three NW radiuses; 2.5nm, 5nm and 10nm. The other transistor dimensions and material properties are the same as for the previous simulation, so the relative permittivity of the gate oxide is still 20.  $C_{gg}$  is measured for varying  $V_G$  and without any source or drain bias. Figure 3.11 displays the results of these simulations. The peaks in capacitance-curve for the radiuses 2.5nm and 5nm are due to the electron subbands. For the transistor

with a NW radius of 10nm, the subbands are too many and too close to give peaks that are noticeable. Using the  $C_{gg}$  data,  $g_m/C_{gg}$  can be calculated, and is plotted in figure 3.12. Table 3.11 summarizes the figures of merit found for transistors with different gate lengths and the NW radius 5nm. Like in the case of the drift-diffusion transport model, the low doped region is scaled along with the gate. The figures of merit barely change when  $L_g$  is scaled from 200nm to 25nm. At  $L_g = 10$ nm short channel effects appear, as indicated by the increased inverse SS and DIBL.

**Table 3.11: Figures of merit for simulated InAs NW transistors with different gate lengths,  $L_g$ .** The lower  $\frac{3}{4}$  of the channel has the donor concentration  $10^{17} \text{ cm}^{-3}$ , like in the case of transistor F in figure 3.4. This region is scaled along with the gate length. The rest of the NW has the higher donor concentration of  $10^{19} \text{ cm}^{-3}$ . The NW radius is 5nm and the NW length is 600nm. Inverse SS,  $g_{m,max}$  and on/off ratio are determined for  $V_D = 0.5\text{V}$ .

$L_g$ [nm]	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	DIBL [mV/V]	On/off ratio
200	2.29	60	9	$1.1 \times 10^{14}$
100	2.29	60	9	$4.1 \times 10^{13}$
50	2.28	60	13	$9.3 \times 10^{13}$
25	2.26	60	14	$8.2 \times 10^{13}$
10	2.15	70	62	$4.2 \times 10^{13}$

**Table 3.12: Figures of merit for NW transistors simulated with different radiuses and doping levels in the lower  $\frac{3}{4}$  of the channel.** The n-doping concentration in the rest of the wire is  $10^{19} \text{ cm}^{-3}$ . The NW length is 600nm,  $L_g$  is 50nm and  $t_{ox}$  is 4nm. Inverse SS, on/off ratio and  $g_{m,max}$  are measured at  $V_D = 0.5\text{V}$ .

NW radius [nm]	Low n-doping	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	On/off ratio
5	$1 \times 10^{17}$	2.28	60	$9.3 \times 10^{13}$
	$1 \times 10^{18}$	2.29	60	$1.8 \times 10^{14}$
	$1 \times 10^{19}$	2.29	60	$1.8 \times 10^{14}$
10	$1 \times 10^{17}$	3.77	60	$3.7 \times 10^9$
	$1 \times 10^{18}$	3.76	60	$2.2 \times 10^9$
	$1 \times 10^{19}$	3.55	63	$2.8 \times 10^7$
15	$1 \times 10^{17}$	4.65	64	$2.5 \times 10^8$
	$1 \times 10^{18}$	4.59	65	$1.2 \times 10^8$
	$2.5 \times 10^{18}$	4.56	67	$2.0 \times 10^8$
	$5 \times 10^{18}$	4.47	94	$3.4 \times 10^5$
	$1 \times 10^{19}$	4.38	385	164

During fabrication, the low doped region of the NW may end up with doping higher than desired. This could cause the inverse SS to increase. Simulations are therefore performed to find out how varying the doping in the low doped region impacts the figures of merit for transistors with different NW radiuses. The gate length of the transistors is 50nm. The results are collected in table 3.12. When the NW radius is 5nm the transistor can be highly doped in the whole NW without this causing any negative effects on  $g_{m,max}$ , inverse SS or the on/off ratio. When the NW radius is 10nm the transistor is slightly affected by higher doping in the channel. In the case of transistors with the NW radius 15nm, these are significantly affected by the increase in doping. Ideally the doping concentration in the low-doped region should be lower than  $2.5 \times 10^{18} \text{cm}^{-3}$  for transistors with the NW radius of 15nm and gate length of 50nm.

Scaling is always an objective when it comes to transistors, which is why NW transistors with gate lengths of 20nm, 10nm, and 5nm are simulated. As these lengths are so small, the n-doping in the entire channel is varied between the concentrations  $10^{18} \text{cm}^{-3}$  and  $10^{19} \text{cm}^{-3}$ , and the length of the NW is set to 400nm. The thickness of the gate oxide is set to 3nm. The main goal of these simulations is to find out which NW radiuses will give low inverse SS under these circumstances. The figures of merit gathered from these simulations are displayed in tables 3.13, 3.14 and 3.15. The results show that the transistors simulated for tables 3.13, 3.14 and 3.15 are generally unaffected if the channel doping is increased from  $10^{18} \text{cm}^{-3}$  to  $10^{19} \text{cm}^{-3}$ . NW transistors with 20nm gate length and high channel doping should have a NW radius of less than 10nm to achieve a good inverse SS value. For transistors with an  $L_g$  that is 10nm, the NW radius should be around 3.5nm or less to get a low inverse SS while the channel doping is high. When the gate length is 5nm the NW radius should ideally be even smaller, at the most 2.5nm, to get a somewhat low inverse SS.

**Table 3.13: Figures of merit for different NW radiuses and doping of the entire channel.**  $L_g$  is 20nm, the NW length is 400nm,  $t_{ox}$  is 3nm and the relative permittivity of the gate oxide is 20. Maximum transconductance, inverse SS, and on/off ratio are measured at  $V_D = 0.5V$ .

NW radius [nm]	Channel n-doping [ $\text{cm}^{-3}$ ]	$g_{m,max}$ [mS/ $\mu\text{m}$ ]	Inverse SS [mV/dec]	On/off ratio
10	$1 \times 10^{18}$	3.67	71	$1.2 \times 10^9$
7.5	$1 \times 10^{19}$	3.04	64	$1.5 \times 10^{10}$
7.5	$1 \times 10^{18}$	3.04	64	$9.0 \times 10^{10}$
7	$1 \times 10^{19}$	2.87	63	$6.0 \times 10^{10}$
7	$5 \times 10^{18}$	2.90	63	$1.4 \times 10^{11}$
7	$1 \times 10^{18}$	2.90	63	$3.3 \times 10^{11}$
6.5	$1 \times 10^{19}$	2.56	62	$2.6 \times 10^{11}$
6.5	$1 \times 10^{18}$	2.64	62	$1.2 \times 10^{12}$
6	$1 \times 10^{19}$	2.69	61	$1.5 \times 10^{12}$

**Table 3.14: Figures of merit for different NW radiuses and doping of the entire channel.**  $L_g$  is 10nm and  $t_{ox}$  is 3nm. The length of the NW is 400nm. Maximum transconductance, inverse SS, and on/off ratio are measured at  $V_D = 0.5V$ .

NW radius [nm]	Channel n-doping [ $cm^{-3}$ ]	$g_{m,max}$ [mS/ $\mu m$ ]	Inverse SS [mV/dec]	On/off ratio
4.5	$1 \times 10^{18}$	2.47	68.4	$1.3 \times 10^{14}$
3.5	$1 \times 10^{19}$	2.88	65.5	$1.2 \times 10^{14}$
3.5	$1 \times 10^{18}$	2.16	65.5	$8.8 \times 10^{14}$
3	$1 \times 10^{19}$	1.97	65.1	$6.4 \times 10^{14}$
3	$1 \times 10^{18}$	1.95	64.0	$5.2 \times 10^{14}$
2.5	$1 \times 10^{19}$	2.37	62.3	$4.1 \times 10^{15}$
2.5	$5 \times 10^{18}$	2.37	62.3	$6.1 \times 10^{14}$
2.5	$1 \times 10^{18}$	2.36	62.5	$2.0 \times 10^{15}$
2	$1 \times 10^{19}$	2.97	61.5	$4.6 \times 10^{15}$

**Table 3.15: Figures of merit for different NW radiuses and doping of the entire channel.**  $L_g$  is 5nm,  $t_{ox}$  is 3nm and the NW length is 400nm. Maximum transconductance, inverse SS, and on/off ratio are obtained at the drain voltage 0.5V.

NW radius [nm]	Channel n-doping [ $cm^{-3}$ ]	$g_{m,max}$ [mS/ $\mu m$ ]	Inverse SS [mV/dec]	On/off ratio
4	$1 \times 10^{19}$	2.63	80.0	$3.5 \times 10^{14}$
4	$1 \times 10^{18}$	2.65	80.3	$6.3 \times 10^{13}$
2.5	$1 \times 10^{18}$	2.27	68.5	$1.4 \times 10^{15}$
2	$1 \times 10^{19}$	3.83	66.5	$3.2 \times 10^{15}$
2	$1 \times 10^{18}$	3.19	67.4	$3.1 \times 10^{15}$

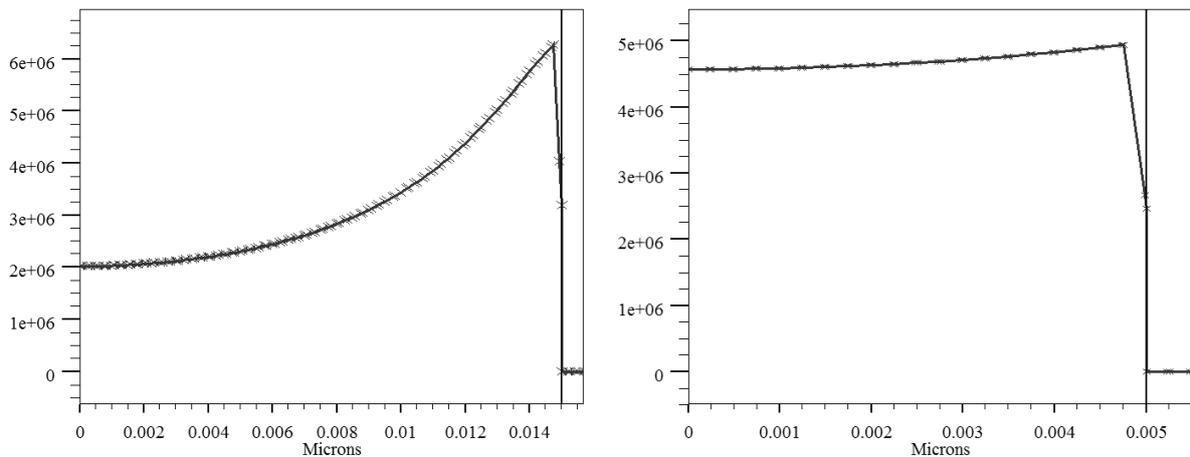
### 3.3 Comparison of models

One of the differences between simulating with or without quantum mechanical effects is the current density perpendicular to the transport direction, see figures 3.13 and 3.14. The differences arise because the quantum models consider the wave nature of the carriers. For the classical drift-diffusion transport model it is also found that the difference between the electron current density close to the surface of the NW and the current density at the center of the NW decreases along with the radius. At small radiuses, the electron current density is practically constant in the radial direction of the NW when the classical model is used. As stated in section 2.3, using the circumference to normalize transconductance, resistance and current assumes that the large majority of the current flows along the surface of the NW. The results show that this is a bad assumption which is why the normalized figures

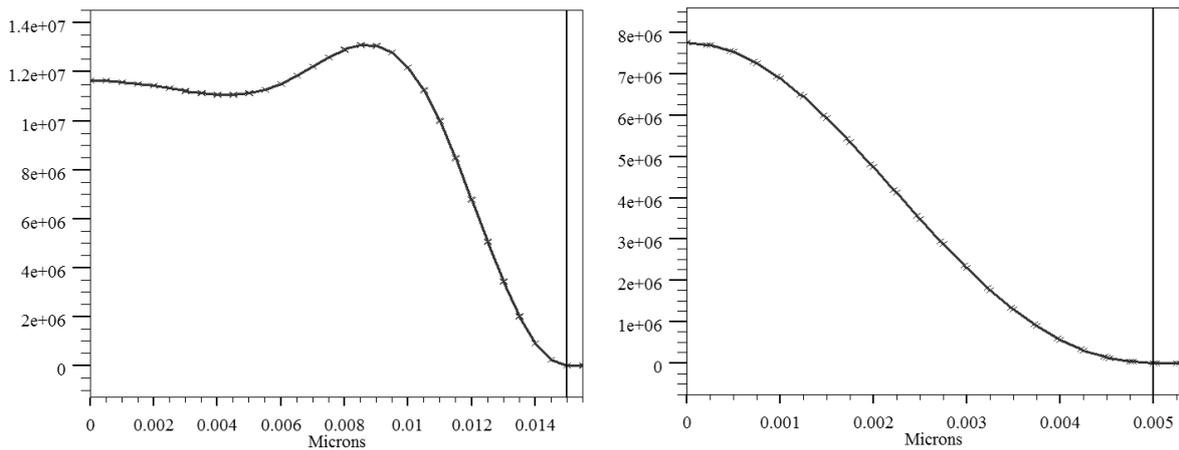
of merit presented in this work are still noticeably affected by the NW radius. Perhaps normalizing with the area ( $\pi r^2$ ) would be more suitable.

The differences in  $I_D$ - $V_G$  characteristics between transistors simulated with the different models are illustrated in figure 3.15.

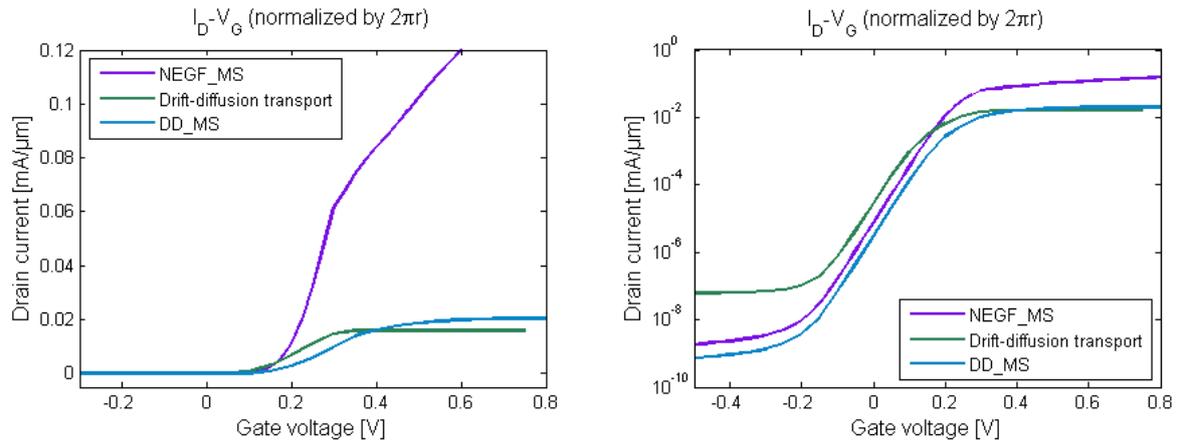
**Figure 3.13: Radial current density for two transistor NWs with the radiuses 15nm (left) and 5nm (right) simulated with the classical drift-diffusion transport model.** The current density (y-axis) is measured in  $A/cm^2$ . Gate and drain voltages are 0.5V. The vertical line marks where the InAs NW and the gate oxide interface.



**Figure 3.14: Radial current density for two transistors with the NW radius 15nm (left) and 5nm (right) simulated with the NEGF\_MS model.** The current density (y-axis) is measured in  $A/cm^2$ . Gate and drain voltages are 0.5V. The vertical line marks the interface between the InAs NW and the gate oxide.



**Figure 3.15:**  $I_D$ - $V_G$  characteristics for identical InAs NW transistors simulated with different models. The NW radius is 10nm and the NW n-doping is  $10^{17}\text{cm}^{-3}$ . The current is plotted in linear scale and logarithmic scale.



## 4 Conclusions and future work

The preferred doping is to have a low donor concentration in the channel, or part of it, and high donor concentration in the rest of the wire. This gives relatively high transconductance, and at the same time low inverse SS and DIBL. The results show that it's important that the low doped region is aligned with or within the gate edges. It's more important that the low doped region edge matches the gate edge at the source side than the drain side. On the drain side it seems like some gate overlap is beneficial, as shown by the figures of merit for transistor F in table 3.4. Note however that the inverse SS and DIBL are only slightly affected by the misalignment. It also seems that in most, if not all, cases low inverse SS and low DIBL go together.

Table 3.7 shows that the gate length can be scaled more for transistors with thinner NWs. Based on these figures  $L_g$  should be kept at least 4-5 times larger than the NW radius to get a low inverse SS. Gate scaling is investigated further using NEGF\_MS, see tables 3.11, 3.13, 3.14 and 3.15. These results show that it's possible to get somewhat low inverse SS even with gate lengths below three times the radius. According to the results in table 3.10, it would even be possible to achieve good figures of merit with a gate length that is twice the NW radius, if the length of the NW is very short. However such devices may be difficult to realize. The results of the NEGF\_MS simulations also indicate that the inverse SS of NWs with smaller radiuses is less affected by increases in the channel doping.

Tough no specific analysis of threshold voltages were made, it is clear from figures 3.8 and 3.9 that the threshold voltage increases when the NW radius decreases. The change in threshold voltage is particularly noticeable for smaller radiuses, as the threshold voltage is linked to the level of quantum confinement experienced by the carriers. High threshold voltages may become a concern when scaling the NW radius below 10nm.

Future work could include investigating if the on-resistance changes noticeably when quantum mechanical effects are modeled. As previously implied, the threshold voltage may be a parameter worth examining further. Atlas has a variety of different models that were not tried in this work. It is also possible to make more than just DC simulations. AC and transient modes of operation can also be modeled. It would therefore be possible to use Atlas to determine the performance and suitability of NW transistors with respect to RF and other analog applications.

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## Appendix – Source code example

```
#
# InAs NW
#
# Drift-diffusion transport model
#

go atlas

# STRUCTURE SPECIFICATION

set rwire=0.010
set high_k=0.004
set highk_r="$rwire"+"$high_k"

mesh cylindrical smooth=1 diag.flip

x.m l=0.000 spac=0.0005
x.m l="$highk_r" spac=0.0005
x.m l=0.020 spac=0.003

y.m l=0.00 spac=0.002
y.m l=0.20 spac=0.0005
y.m l=0.40 spac=0.0005
y.m l=0.60 spac=0.002

# top
region num=1 material=InAs x.min=0 y.min=0.0 y.max=0.25

#channel
region num=2 material=InAs x.min=0 y.min=0.25 y.max=0.4

#bottom
region num=3 material=InAs x.min=0 y.min=0.4 y.max=0.6

# SiO2
region num=4 material=SiO2 x.min="$rwire"

# Gate oxide
region num=5 material=SiO2 x.min="$rwire" x.max="$highk_r" \
y.min=0 y.max=0.6

electrode name=gate num=1 x.min="$highk_r" y.min=0.2 y.max=0.4
electrode name=drain num=2 x.min=0.000 x.max="$rwire" y.max=0.00
electrode name=source num=3 x.min=0.000 x.max="$rwire" y.min=0.60

doping uniform region=1 n.type conc=1e19
doping uniform region=2 n.type conc=1e17
doping uniform region=3 n.type conc=1e19

# MATERIAL MODELS SPECIFICATION

models material=InAs srh fldmob print fermi evsatmod=2 temperature=300

material region=5 permittivity=20.0

mobility region=1 vsatn=2e7 mun=3000 mup=100
mobility region=2 vsatn=2e7 mun=8000 mup=100
```

```

mobility region=3 vsatn=2e7 mun=3000 mup=100

# NUMERICAL METHOD SELECTION

method newton gummel autonr trap itlim=10 carriers=2
output con.band val.band e.temp e.velocity

# SOLUTION SPECIFICATION

solve init
save outf=InAs_000.str
tonyplot InAs_000.str

# Id-Vd

solve vdrain=0
log outf=Id_Vd_r$"rwire"_0.5V.log
solve vgate=0.5
solve vstep=0.025 vfinal=0.8 name=drain

log off

tonyplot Id_Vd_r$"rwire"_0.5V.log

# Id-Vg

solve vdrain=0.5
log outf=Id_Vgs_r$"rwire"_0.5V.log
solve vgate=-0.7
solve vstep=0.025 vfinal=1.25 name=gate

log off

tonyplot Id_Vgs_r$"rwire"_0.5V.log
tonyplot Id_Vgs_r$"rwire"_0.5V.log -set gm.set

solve vdrain=0.05
log outf=Id_Vgs_r$"rwire"_0.05V.log
solve vgate=-0.7
solve vstep=0.025 vfinal=1.25 name=gate

log off

tonyplot Id_Vgs_r$"rwire"_0.5V.log -overlay Id_Vgs_r$"rwire"_0.05V.log

quit

```