



Master's Thesis

A Feasibility Study of PreAmplifier Design for Hearing Aid

By

Usman Farooq
(aso10ufa)

Department of Electrical and Information Technology
Faculty of Engineering, LTH, Lund University
SE-221 00 Lund, Sweden

Abstract

The trend of scaling down the mixed signal integrated circuit (IC) technologies is on one hand facilitating the digital circuits to fully embrace the smaller feature sizes but on the other hand it severely limits the performance of analog circuits. This poses a tough demand for analog circuits to give comparable and acceptable performance in a CMOS technology with higher threshold voltage compared to available supply voltages.

This work describes the design, implementation and simulations of low-voltage and low power PreAmplifier in 65nm CMOS technology. The PreAmplifier is used in the front-end of a hearing aid and its gain is digitally controlled based on input signal power level. The gain is programmable in steps of 6 dB ranging from 0 to 24 dB i.e. 0, 6, 12, 18 and 24 dB with less 1% gain variation from the specified values.

The designed PreAmplifier primarily consists of a two Stage Miller compensated operational amplifier. It uses switched capacitor technique to implement the feedback resistor around the operational amplifier. The lower cutoff (-3dB frequency) of the specified bandwidth for the PreAmplifier is simulated to be 100Hz for all gain configurations. The power supply rejection ratio (PSSR) is -45dB, the total input referred voltage noise is -107 dBV, and the total harmonic distortion (THD) is -87dB. The total current consumption of the PreAmplifier with 1V power supply is 32 μ A. All the simulations of PreAmplifier are performed using Analog Design Environment tool of the CADENCE at 27° C and the load capacitance of 1pF. The approximate chip area of the designed PreAmplifier is 250 μ m x 250 μ m.

Acknowledgement

I would like to thank Waqas from Electrical and information technology, Lund University and Lars from GN ReSound for finding this opportunity for me. Thanks to my supervisor Peter Siegumfeldt for his patience and supporting me right from the beginning till the end of project, without him this project was not possible. I would also like to thank my examiner Henrik Sjöland for his timely support and useful feedbacks.

Deep thanks and gratitude to the people of Sweden for supporting my education on their tax money and same to people of my country Pakistan whose tax money supported my boarding and loading expenses.

Thanks to all my friends especially Ali, Ateeq, Omar, Kamal, Asheesh for their time and support and encouragement.

Thanks to my family for supporting me throughout my life.

Table of Contents

Abstract.....	2
Acknowledgments	3
Table of Contents.....	4
1 Introduction	6
1.1 Introduction	6
1.1.1 What is Hearing Aid?.....	6
1.1.2 PreAmplifier in a Hearing Aid instrument.....	6
1.2 Project Specifications.....	7
1.3 Thesis Motivation	7
1.4 Thesis Organization.....	8
2 Feasibility Study	10
2.1 Feedback network for High Gain Amplification with enhanced bandwidth and gain control [1]	10
2.2 Variable Gain Amplifier for gain scaling in an analog-to-digital converter [2].....	12
2.3 Variable Gain and Low Noise Amplifier for received signals in Imaging Apparata [3].....	13
2.4 Proposed method of PreAmplifier Design.....	15
2.5 Summary.....	16
3 System Model Design of the PreAmplifier.....	17
3.1 PreAmplifier System Model Design Considerations	17
3.2 PreAmplifier System Model Development	19
3.3 PreAmplifier System Model Test-bench.....	19
3.4 Simulation Results	20
3.5 Summary and Conclusion	22
4 Design of a High Value Resistor	23
4.1 Introduction	23
4.2 Realizing high value resistance in a CMOS process.....	23
4.2.1 Ultra High Value floating tunable resistor [6].....	24
4.2.2 Diode connected PMOS transistor as resistor [7].....	26
4.2.3 Switched Capacitor resistor [8]	27
4.3 Comparison of techniques to realize HVR in CMOS.....	28
4.4 Designing R_f as a SC resistor.....	28
4.5 Summary.....	30
5 Operational Amplifier Specifications and Design Considerations.....	31
5.1 Opamp specifications.....	31
5.1.1 Gain.....	32

5.1.2	Input common mode range.....	32
5.1.3	Output voltage swing.....	33
5.1.4	Unity Gain Bandwidth and Phase Margin	33
5.1.5	Power Supply Rejection Ratio (PSRR)	34
5.1.6	Equivalent Input Noise	34
5.1.7	Total Harmonics distortion plus Noise (THD+N)	34
5.2	Choice of opamp topologies.....	35
5.3	Summary.....	38
6	Technology characterization using gm/Id method	39
6.1	Introduction	39
6.1.1	Performance metric of interests.....	40
6.1.2	Technology characterization.....	41
6.2	Generation of gm/Id versus $Id/(W/L)$ characteristic curves	41
6.3	Important features of gm/id method	44
7	Design of a Two Stage operational amplifier using gm/id based method.....	46
7.1	Review of a Two Stage Opamp architecture	46
7.1.1	Input stage	47
7.1.2	Output stage.....	48
7.1.3	Biassing stage	48
7.1.4	Compensation Stage.....	49
7.2	Two Stage opamp Specifications.....	49
7.3	Design of a two stage opamp	50
7.4	Simulation Results	54
7.4.1	AC Analysis	55
7.4.2	Noise Analysis	55
7.4.3	XF Analysis.....	57
7.5	Summary.....	58
8	System Integration and Simulation Results	59
8.1	System integration	59
8.2	Simulation Results	60
8.2.1	Closed Loop AC gain.....	60
8.2.2	Noise.....	61
8.2.3	PSRR.....	62
8.2.4	Transient response.....	63
8.2.5	THD.....	64
8.3	Summary.....	66
9	Conclusion and Future Recommendations.....	67
	References	68
	Appendixes.....	70

CHAPTER 1

1.1 Introduction

1.1.1 What is Hearing Aid?

In simple words, a hearing aid is a highly sophisticated communication device which enables people with hearing loss to hear well. As the hearing loss varies from person to person therefore there are many different types of hearing aid accordingly available. The main principle of a hearing aid device is to amplify the sounds to enhance particular hearing range issues. So a hearing aid works in a way that it picks sound signal from a microphone, the sound signal is amplified based on different parameters and then the amplified signal is analyzed by digital processing. The digitally processed signal is sent to the loud speaker by which the sound is transmitted into inner part of ear where they are transformed into electrical impulses. These electrical impulses are picked by brain and hence the person is able to hear the sound. So a typical hearing aid involves analog and digital signal processing. In analog signal processing the device receives the sound signal, amplifies it and filters out the information signal. While in digital signal processing, different mathematical functions are performed in order to make the sound compatible with the listener's level of hearing loss.

1.1.2 PreAmplifier in a Hearing Aid instrument

A PreAmplifier is one of the important components in the analog signal processing of a hearing aid. The main function of a PreAmplifier is to amplify the sound signal, received by the microphone, to a certain level so that it can be processed by the digital sound processing circuitry. The PreAmplifier is typically a variable gain amplifier which amplifies or attenuates the microphone signal according to its power level. In other words, the gain of PreAmplifier is a function of signal power level of the microphone. Whereas the Digital signal processing circuitry notifies the PreAmplifier with gain control information. The preamplifier amplifies or attenuates the sound signal only in the specified information bandwidth i.e. from 100 Hz to 10 KHz in case of this project.

1.2 Project Specifications

The main objective of this work is to design a low-voltage low-power variable gain PreAmplifier in standard 65nm CMOS process. The specifications of the PreAmplifier are provided by the hearing aid manufacture which is summarized in Table 1.1. These specifications are set by the manufacturer according to their requirements and to explore design facets of modern CMOS technologies. The closed loop gain of PreAmplifier is specified to be programmable from 0 to 24dB in steps of 6dB i.e. 0, 6, 12, 18 and 24. The information bandwidth should be between 100 Hz and 10 kHz. The PSRR requirements are set to be 50dB in a band from 0 to 10 KHz. The input referred integrated noise should be -110 dB between the information bandwidth. The Total Harmonic Distortion (THD) is specified to be -60 dB. The supply voltage (VDD) is specified as 1V and the total available current as 28uAmps. The area available for complete design of PreAmplifier is specified to be 0.1mm². This report describes the first two phases of design in a typical analog IC design flow i.e. system level modeling in Verilog-A and transistor level schematic design using CADENCE. The layout aspects of the design will be also described in order for the design to estimate maximum required area.

TABLE 1.1: SUMMARY OF PREAMPLIFIER'S SPECIFICATIONS PROVIDED BY HEARING AID MANUFACTURER

Parameter/ Specification	Value
Closed Loop Gain	0-24 dB (programmable in 6dB steps)
Closed Loop Bandwidth	100 Hz to 10 KHz
Input referred Noise (between 100Hz to 10 KHz)	-110 dB
THD+N	-60 dB
PSRR	50dB (0 to 10 KHz)
Supply Voltage (VDD)	1V
Power Constraint	28 uA
Area Constraint	0.1 mm ²
Temp	-10 to 60 °C
Process	65nm Standard CMOS Process

1.3 Thesis Motivation

A hearing aid device like many other battery operated products i.e. pacemaker, mobile phone etc. has always been requiring extended battery

life to prolong its operating period. The extended battery life of such devices can only be achieved their integrated circuits (ICs) implementation becomes less power hungry. With the advent of latest nanometer CMOS processes, it has now become a common trend in the microelectronics industry to achieve the greater on chip functionality at lower power consumption. Each new sub- micron process offers smaller devices and provides lower levels of supply voltages. It is also common to integrate analog and digital functions on the same chip to get maximum benefit out of the digital CMOS processes. The smaller devices and lower supply voltages are very suitable to integrate the digital circuits but it makes integration of analog circuit more challenging. Also the threshold voltage (V_{th}) of a MOS transistor is not reducing at same rate as that of supply voltage in the modern CMOS processes. The higher threshold voltage compared to the available supply voltage thus makes the analog design procedure less flexible in which several design variables i.e. Gain, Noise, input/ Output voltage swing and DC offset needs to taken into account. In short, when the technology shrinks, short channels effects become more evident and capturing transistor behavior requires more accurate modeling. Also the conventional analog design techniques i.e. to operate transistors in saturation/ strong inversion region need to be replaced by non conventional methods.

So the low voltage low power analog designs require non-conventional design methods and more accurate transistor models to reach at a good compromise between afore mentioned analog design variables. This report focuses on characterizing the available CMOS process technology and devising low voltage low power design methodologies to meet the Preamplifiers' specifications. The report will also present in great details the factors affecting the Preamplifier's performance parameters such as Gain, Noise, PSRR and THD.

1.4 Thesis Organization

This work is divided into nine chapters. Chapter 2 discusses some state of art techniques for Variable gain amplifier along with the proposed method of implementation. In chapter 3, a system model for the proposed method of PreAmplifier design is developed for proof of concept purpose and some of the layout aspects for the purpose of area estimation are also disclosed. Chapter 4 discusses the design of a high value resistor and different trade-offs related to its design. Chapter 5 describes operational amplifier (opamp)

specifications and provides motivation to choose opamp topology from the common opamp topologies. Chapter 6 discusses the g_m/I_d methodology and the steps to get the characteristic curves which greatly assist a designer to find out a transistor dimensions. Chapter 7 describes the steps taken in order to design a 2 Stage operational amplifier and also presents some standard results to characterize the designed opamp. In chapter 8, the PreAmplifier is developed at schematic level and is characterized by various simulation results. Finally in chapter 9 conclusion are drawn with recommendations to the future work.

CHAPTER 2

2 Feasibility Study

Variable gain amplifier (VGA), which is termed as PreAmplifier for this work, is used in many different applications i.e. fiber optic receivers, mobile phones, hearing aids and also in variety of ways in biomedical instruments. In each set of these applications, design of PreAmplifier is mainly characterized by factors including bandwidth, gain and power consumption. Although the main emphasis of this work is to investigate PreAmplifier with capacitive coupled input and capacitive feedback but for sake of relevance some state of art techniques are presented in this chapter. Most of the literature related to this work is found form patents which are available online at different national and international patent offices. The first technique utilizes a nonconventional feedback network, consisting of a Tee resistor, to develop a variable gain and wide bandwidth amplifier. In the 2nd technique, multiple input and feedback paths lead to the amplifier inverting input and by selecting these paths in different ways enable the amplifier to have variable gain. The amplifier in the 3rd technique contains capacitive divider in its feedback network wherein the variations in capacitive ratio results in gain control. The last technique describes the proposed method of VGA implementation in which an opamp has a capacitive coupled input and negative feedback formed by parallel combination of a capacitor and a resistor. The ratio between the input and feedback capacitance determines the gain of proposed amplifier. These techniques are discussed one by one in the respective order as follows;

2.1 Feedback network for High Gain Amplification with enhanced bandwidth and gain control [1]

Fig 2.1 shows a transimpedance amplifier with a Tee resistive feedback network and its inverting input tied to a reverse biased photo detector diode. The amplifier utilizes Tee resistive feedback network to realize enhanced bandwidth and gain control. The Tee resistive network has been used to replace the otherwise conventional feedback formed by resistor of very high value. The pole formed by the Tee resistor and the amplifier's input parasitic capacitance is moved up in the frequency domain due to reduced

value of the Tee resistor. The gain of the amplifier depends on how the values of R_{200} , R_{201} and R_{202} of a Tee resistor are selected. It is required that value of R_{200} may not be set randomly small to make overall gain of amplifier unrealizable. The values of R_{200} and R_{202} are usually set to be equal where as the value of R_{201} , which is shunt resistor in the Tee resistor, is set to be as small as possible. Higher gain is achieved for lower values of R_{201} so value of R_{201} is selected practically to be as small as possible i.e. 10-ohms.

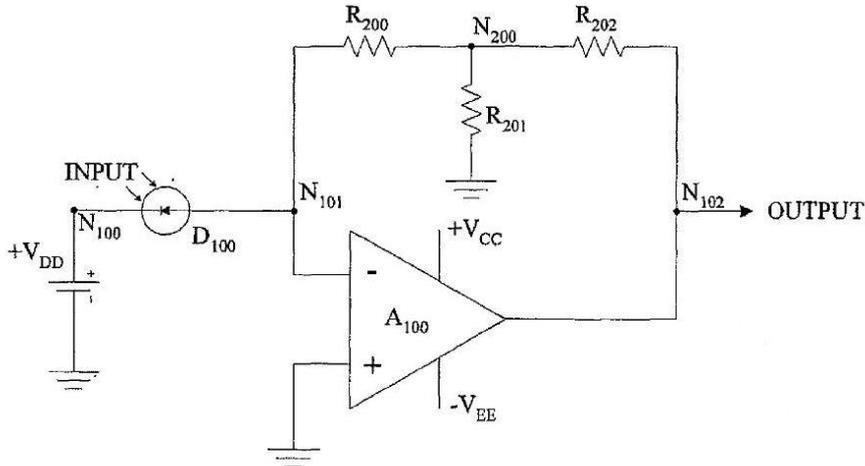


Fig 2.1: Transimpedance Amplifier with Tee-resistor feedback network [1]

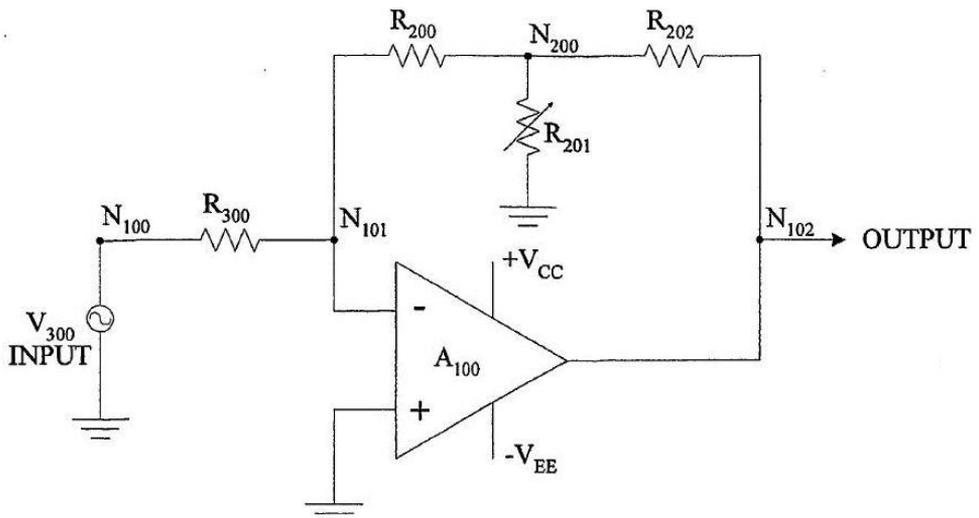


Fig 2.2: Variable gain amplifier with Tee- resistor feedback network [1]

The configuration of the amplifier in the fig 2.1 is changed to a voltage amplifier as shown in fig 2.2. The resistor R201 is marked to be variable which reflects that R201 is responsible for gain control.

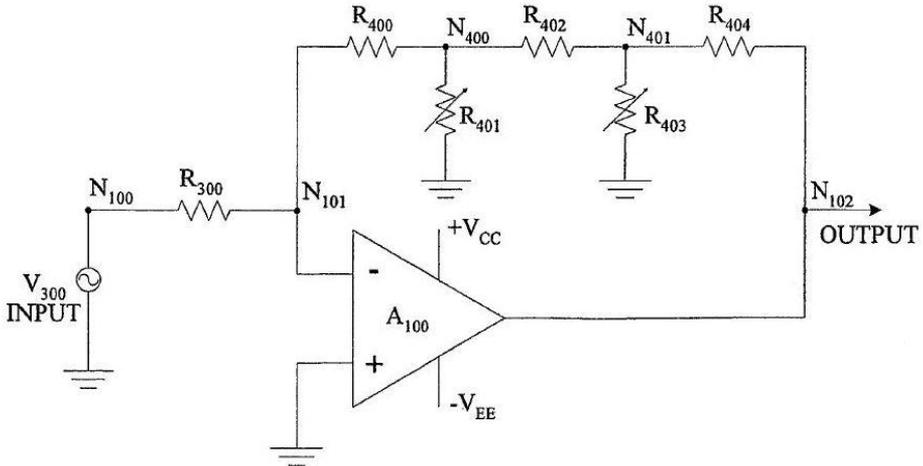


Fig 2.3: Variable gain amplifier with multiple Tee- resistor feedback networks [1]

Fig 2.3 shows a voltage amplifier in which feedback network consists of multiple Tee resistive networks. The multiple Tee resistor network are used to enhance the overall gain of the amplifier.

2.2 Variable Gain Amplifier for gain scaling in an analog-to-digital converter [2]

The VGA shown in the fig 2.4 is configured as an integrator and is used in an analog-to-digital converter to function both as VGA and integrator to make the system power efficient. It has multiple paths between the input “Vin” and the inverting terminal “Vopi” of the opamp. Each of these paths contains a resistor and a first switch and hence forms a set of resistors and a first set of switches. The resistors and on resistance of switches in branches following the first branch are scaled with an integer or non-integer factor of the first branch. The feedback is connected to the intermediate node between resistor sand first set of switches via a second set of switches. The on resistance of 2nd set of switches is also scaled according to the scaling factor used in the first set of switches and resistors. The gain of the amplifier is varied by setting the first and second set of switches accordingly. These switches can also be set in the form of pairs to achieve more linear gain control. But the main motivation for using this technique is

to reduce the nonlinearity caused by the input switches if the 2nd set of switches were not used. As in this VGA no current ideally flow through the first set of switches and voltage at the inverting terminal of opamp will be same as the voltage at the intermediate node between resistors and first set of switches. Therefore ideally the first set of switches will not cause any nonlinearity to the overall system performance. Furthermore the nonlinearity caused by the 2nd set of switches, due to any variations in their on resistances, will have some additive effect on the output of opamp which is comparably less than that in the prior art.

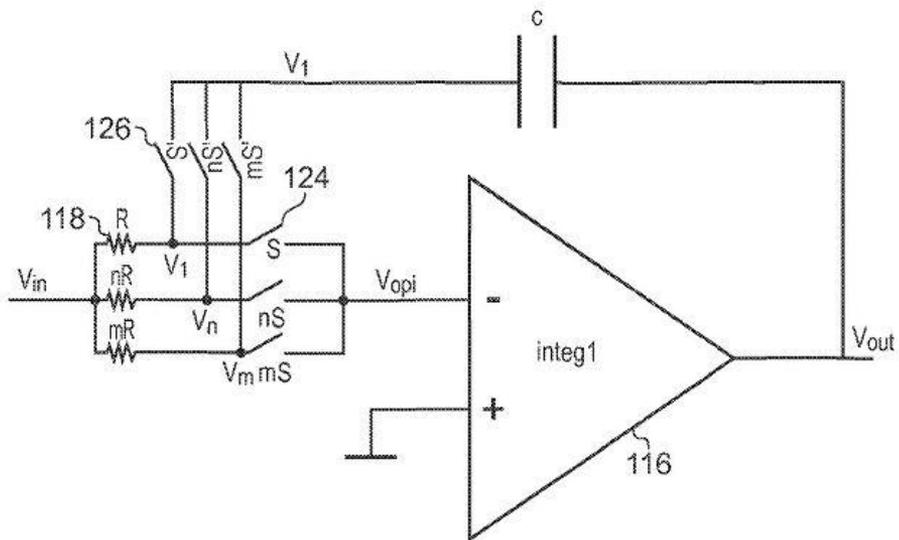


Fig 2.4: VGA having multiple input paths from input to the opamp input and feedback [2]

2.3 Variable Gain and Low Noise Amplifier for received signals in Imaging Apparata [3]

The system in fig 2.5 shows a variable gain amplifier which is designed for received signals in ultrasound or nuclear magnetic resonance imaging apparata. It is basically the exploitation of most common feedback provided by the resistive divider as shown in fig 2.6 in which the ratio of resistances (R_2/R_1) determines the gain. Although the feedback provided solely by resistors allows the amplifier to easily adjust the gain but it makes the amplifier more prone to thermal noise caused by the resistors. Therefore the feedback in the amplifier shown in the fig 2.5 consisting of combination of capacitive and resistive divider achieves comparably same amplification factor but low noise. The upper branch of the feedback is connected

between the output of amplifier and the feedback input and its lower branch is connected between the feedback input and common ground. The value of capacitor in the lower branch of the feedback is varied to change the amplification factor of the amplifier. This capacitor can be implemented as a varicap or varactor diode and the rest of the work presented in [3] is related to implement the same. The provision of having components in the feedback network, whose parameter can be changed, enables the amplifier designed in [3] to vary its parameters mainly gain and the information bandwidth.

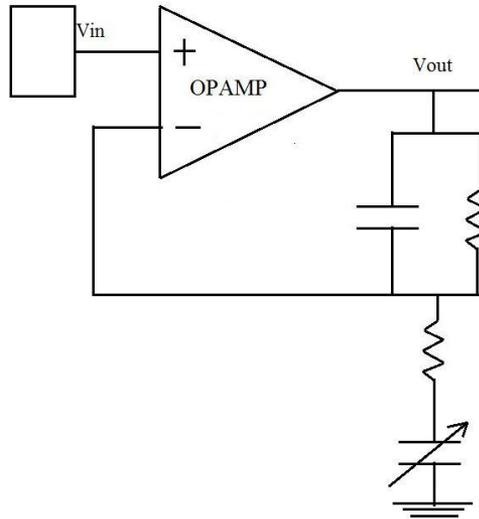


Fig 2.5: Variable gain amplifier with capacitive divider feedback [3]

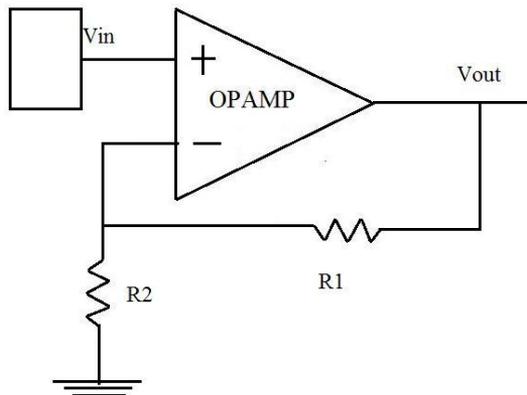


Fig 2.6: Amplifier with common resistive feedback network [3]

2.4 Proposed method of PreAmplifier Design

The previous sections have briefly described some of the techniques to realize a VGA depending on its end application. In case of a hearing aid, due to very low cutoff frequency (100Hz) of the information bandwidth, the PreAmplifier (VGA) needs to have a filter with either very high resistance or very high capacitance. The VGA developed by the Tee resistor network as discussed in section 2.2 seems not to be a relevant solution as it doesn't involve gain control by capacitive variation which is the focus of this work. The 2nd method is not suitable for the PreAmplifier to be designed as using too many switches in the input path increases nonlinearity [2]. In the third method, the amplifier has feedback consisting of combination of capacitors and resistors and capacitive variations determine the amplification factor. So the third technique forms the basis for the PreAmplifier to be designed considering the requirement provided by the hearing aid manufacturer.

In this work a new method of PreAmplifier (VGA) design has been devised and investigated and is shown in fig 2.7. The PreAmplifier consists of an inverting opamp with AC coupled input i.e. V_{mic} connected through the capacitor C_{in} . The feedback is formed by a high pass filter consisting of resistor R_f and a capacitor C_f . The ratio C_{in}/C_f determines the amplification factor of the PreAmplifier and it can be varied by varying either one of these capacitances. The pole formed by R_f and C_f determines the lower cutoff frequency of the bandwidth. This indicates that it is not desirable to change the value of C_f as it will then change the bandwidth. So instead of C_f the value of C_{in} is varied which changes the ratio C_{in}/C_f to control the gain of PreAmplifier. Detailed analysis of the proposed method concerning the mathematical expression for gain and choice of components values which are based on different parameters is presented in next chapter.

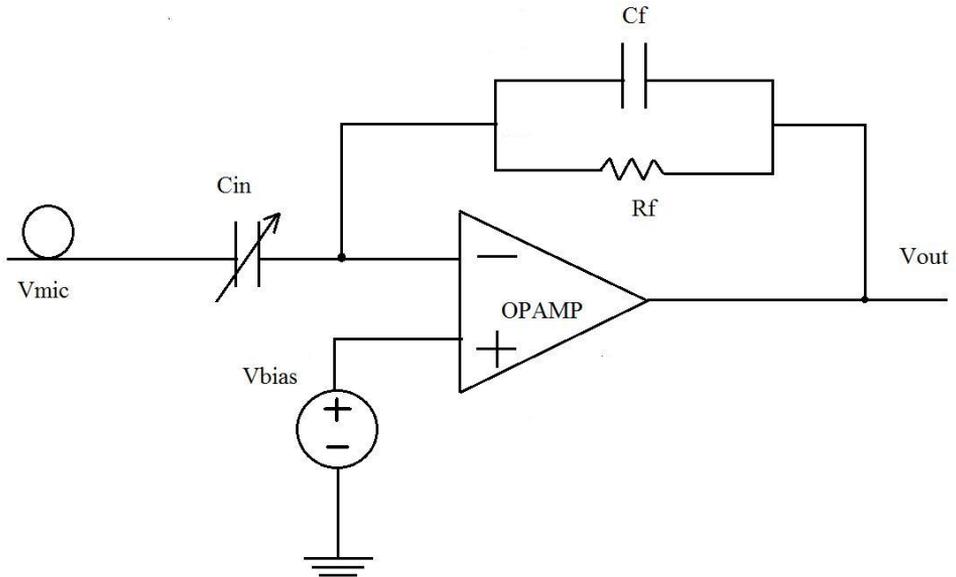


Fig 2.7: Proposed method of Variable Gain amplifier with AC coupled input and Capacitive Feedback

2.5 Summary

Different state of art methods have been discussed to realize a VGA suitable for different set of applications. As the VGAs designed in these methods target specific applications so they are not completely utilized to design the PreAmplifier specified for this project. But these methods have given very useful thoughts which are incorporated in the proposed method of PreAmplifier design. The proposed method is the results of consultations with project supervisor at the hearing aid manufacturer and the following chapters investigate the design and usefulness of this method.

CHAPTER 3

3 System Model Design of the PreAmplifier

A system model is usually developed for the proof of concept purpose and it is the first design step in the process of Analog IC design flow. It enables the designer to know whether or not the proposed topology is workable, and also how to modify it or even replace it with a new one in order to continue the design processes. During the system model development, complicated components in analog design i.e. amplifier, PLL and ADC/DAC can be very effectively described using Verilog-A- an IEEE standard to describe the behavior of Analog systems [4]. The passive components i.e. capacitance, resistance and inductance are also calculated according to the specifications. These components are then used to form a complete system which is passed through a Test bench to perform some analysis and simulations in order to characterize the system. These analyses usually include AC Analysis which is used to illustrate the Gain response and Transient Analysis which illustrate the input/output time response. This chapter describes all the steps to a make a complete system model for PreAmplifier, make a test-bench to perform simulations and illustrates some important simulations results to validate the proposed method of PreAmplifier.

3.1 PreAmplifier System Model Design Considerations

The proposed topology of PreAmplifier design is shown in shown fig 2.7. The amplifier is configured as an inverting amplifier wherein an input signal V_{mic} is applied to its inverting terminal through AC coupling. The positive terminal of the amplifier is tied to a common mode dc voltage V_{bias} which in this case is the half way between positive supply voltage VDD and negative supply voltage VSS. According to the specifications provided by the hearing aid manufacturer, summarized in table 1.1, VDD and VSS are defined to be 1 V and 0 V respectively, so V_{bias} turns out to be 500 mV. The negative feedback around the amplifier consists of parallel combination

of capacitance C_f and resistance R_f – which provides DC feedback and reduces DC offset. The feedback forms a filter wherein the values of C_f and R_f defines the lower cutoff $f_{lower\ cutoff}$ (100Hz) of required bandwidth.

The closed loop transfer function or the Amplification factor " A_v " of the amplifier can be simplified as the ratio of C_{in} to C_f ; if the resistance of R_f is neglected being very high as compared to reactance of C_f and can be expressed as;

$$A_v = \frac{V_{out}}{V_{mic}} = -\frac{C_{in}}{C_f} \quad (1)$$

Equation number 1 reveals that the values of C_{in} and C_f need to be specified in such a way that the ratio C_{in}/C_f becomes equal to the specified gain i.e. 0 dB to 24 dB. So to get A_v equal to 0, 6, 12, 18 and 24dB, the ratio C_{in}/C_f needs to be equal to 1, 2, 4, 8 and 16 respectively which can be achieved by fixing C_f to some value and then varying the value of C_{in} accordingly. These values needs to be selected by considering the layout aspect of system in order to comply with the area constraints as specified in table 1.1. The layout aspects in this regards are reviewed in the summary conclusions section of this chapter.

The expression for the pole frequency $f_{lower\ cutoff}$ made by the parallel combination of C_f and R_f can be expressed as;

$$f_{lower\ cutoff} = \frac{1}{2\pi.R_f .C_f} \quad (2)$$

The value of $f_{lower\ cutoff}$ is 100 Hz for the specified PreAmplifier and solving equation no. 2 with the given value $f_{lower\ cutoff}$ can lead to the approximate the values of C_f and R_f . The value of C_f is taken to be 1pF by analyzing the best case area utilization, the values of R_f then turns out to be 1.59 G-ohms. The feedback capacitance C_f is fixed instead of input capacitance C_{in} as if C_f is varied the $f_{lower\ cutoff}$ will also vary which is not desirable. So in this case, the value of C_{ins} is varied from 1 pF to 16 pF in order for the closed loop gain A_v to vary from 0 dB to 24 dB.

3.2 PreAmplifier System Model Development

Developing a system model for the PreAmplifier requires models and values of individual components i.e. amplifier/opamp, resistance, capacitance. It also requires a mechanism to vary the capacitance C_{in} in order to vary A_v . In this regard the amplifier designed as an ideal voltage amplifier and is described in Verilog-A. The gain of amplifier can be set from 0 to +ve infinity through its input parameter “Gain”. The source code for the amplifier is provided in appendix-A. The input capacitance C_{in} is replaced by a variable capacitor $C_{varicap}$ which is implemented using parallel capacitors and switches as shown in fig 3.1. In this arrangement one or more parallel capacitors can be selected by setting the switches (S0, S1, S2, S3, and S4) of the respective branch. For example to get the value of $C_{varicap}$ to be 16 pF all the switches are asserted. The values of R_f and C_f are already calculated to be 1pF and 1.59GOhms. So these components take their respective places in the PreAmplifier shown in the fig 2.7 and hence form a complete system.

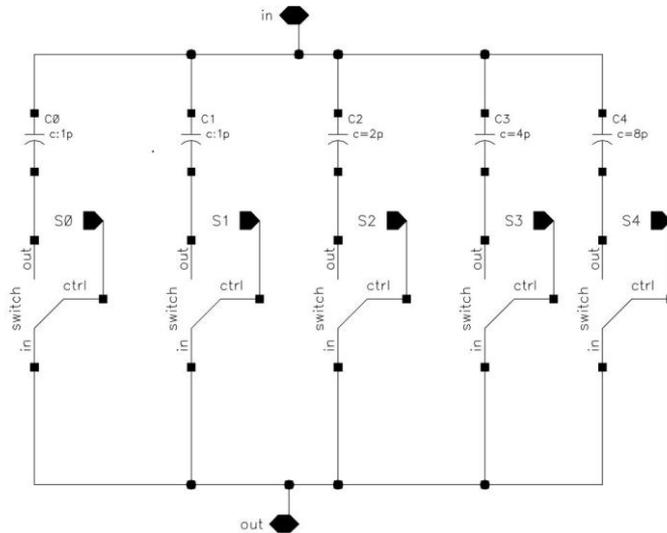


Fig 3.1: Implementation of Variable capacitor $C_{varicap}$ using parallel capacitors and switches.

3.3 PreAmplifier System Model Test-bench

Fig 3.2 shows a test-bench schematic of the PreAmplifier developed in Virtuoso Schematic Editor. It contains a VerilogA model of a Gain Control Unit (GCU), appendix-B, which generates control signals (S0, S1, S2, S3

and S4) for $C_{varicap}$ depending on the required A_v . The input to GCU is an integer in steps of 6 from 0 to 24 to set the value of control signals which accordingly set the value input capacitance ($C_{varicap}$). The supply terminals VDD, VSS and V_{bias} are connected to 1V, 0V and 0.5V respectively. The AC source V_{mic} has DC voltage level as 500 mV, its amplitude is 10 mV and the frequency is set to 10 KHz. The gain of amplifier is set to 70dB for a first approximation. The positive terminal of amplifier is connected to biasing source of 500mV and the negative terminal is connected to a sinusoidal AC source V_{mic} through $C_{varicap}$. The outputs of GCUs are connected to the respective inputs of $C_{varicap}$. The amplifier's output V_{out} is connected to an output capacitance C_{out} (1pF) which is the assumed load to the PreAmplifier.

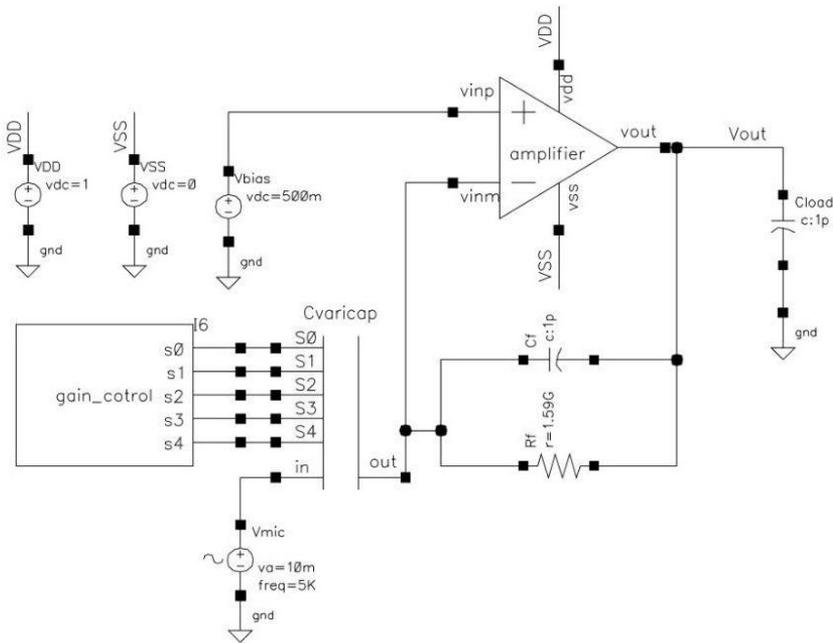


Fig 3.2: Test-bench schematic of PreAmplifier's System Model

3.4 Simulation Results

Fig 3.3 depicts the AC analysis results which show the variations in the amplification factor $A_v = V_{out}/V_{iv}$ of the PreAmplifier as a result of variations in the capacitance ratio C_{in}/C_f . The results depict increase in Gain A_v from 0 dB to 24, with less than 1% variation from the specified

value, as the capacitance ratio C_{in}/C_f increase from 1 to 16. The $f_{lower\ cutoff}$ can be depicted to be 100Hz as -3 dB frequency for any Gain trace shown in fig 3.3. Figure 3.4 shows the transient response of the PreAmplifier for various gain configurations which shows in time domain how V_{out} is amplified, around the same bias voltage as of input. Markers in both fig 3.3 and fig 3.4 are set to motivate the reader to observe the gain variations as a result of variations in the ratio C_{in}/C_f .

It can be concluded after seeing the simulation results that the suggested method can be regarded as a potential method to design the specified PreAmplifier in which the gain variations is achieved by varying capacitive ratio C_{in}/C_f . Furthermore, as the system model contains ideal components models so other specifications i.e. Noise and PSSR cannot be simulated. These specifications can be modeled using Verilog-A but that is out of the scope of this project.

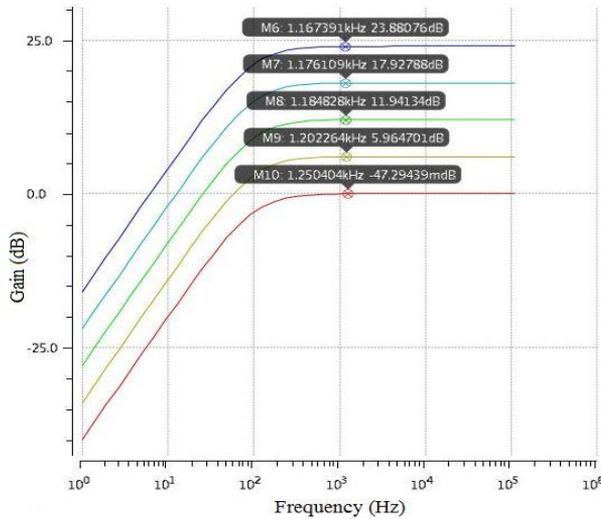


Fig 3.3: Closed Loop Gain Versus Frequency plot of PreAmplifier

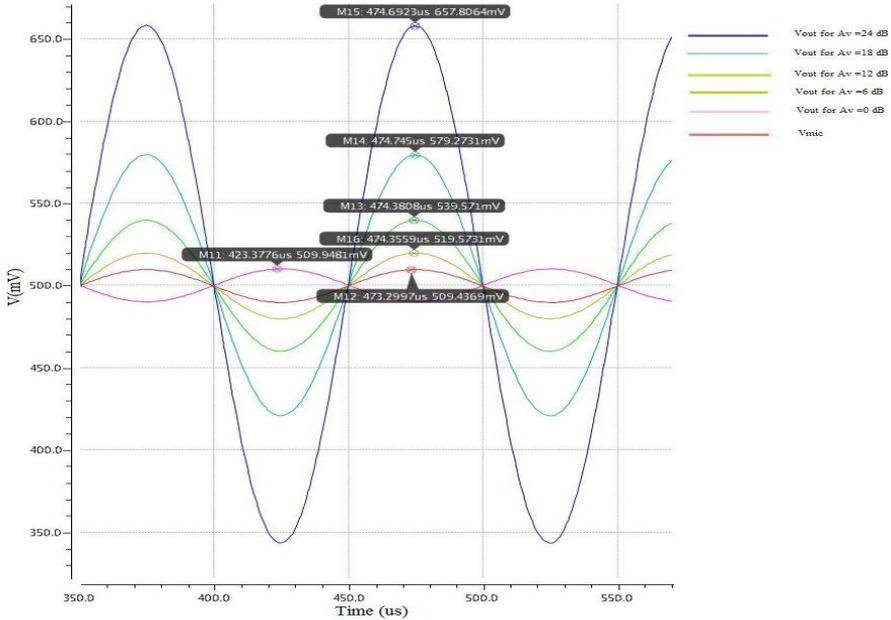


Fig 3.4: Transient simulations showing V_{out} signal for various gain configurations and V_{mic} signal with respect to time

3.5 Summary and Conclusion

In this chapter a system model and its test-bench setup have been very briefly described. The main goal of this chapter was to present a proof of concept for the proposed method of PreAmplifier design and to determine approximated values and parameters of its different components. The simulation results presented in this chapter validates that the proposed technique can be used to design a PreAmplifier for hearing aid devices. A quick review of layout of the passive components used in the amplifier reveals that the layout of capacitors takes most of the available area. While $R_f = 1.59$ G-ohms is not realizable in the specified area or it is useless to integrate such a high value resistor with conventionally.

These aspects of layout and the simulation results were discussed with the supervisor at hearing aid manufacturer. As a result it was suggested to keep the values of capacitances to see the maximum area limitations and to implement R_f with an area efficient way i.e. MOS resistor or switched capacitor resistor. The following chapters discuss the designing of building blocks of PreAmplifier i.e. switched capacitor resistor and the operational amplifier in details.

CHAPTER 4

4 Design of a High Value Resistor

The feedback filter, consisting of R_f and C_f , has been discussed very briefly in the last chapter in context of their values for a given value of $f_{lower\ cutoff}$ (i.e. 100 Hz). This chapter discusses some well known approaches to realize a high value resistance in the order of G-ohms in standard CMOS process to realize such a filter. It also discusses the chosen technique (Switched capacitor technique) to design the required 1.59Gohms feedback resistance.

4.1 Introduction

The bandwidth specification of PreAmplifier is from 100 Hz to 10 KHz. The closed loop AC Analysis results of PreAmplifier, as shown in fig 3.3 indicate that the lower cutoff frequency $f_{lower\ cutoff}$ (100 Hz) is achieved using of R_f as 1.59GOhmas and C_f as 1pF. The main challenge here is to accommodate resulting large values primarily of R_f and of C_f . In this regards efforts have been made to figure out the best case area utilization to achieve 100 Hz cutoff using R_f and C_f . Considering the densities of both capacitor and resistor in the available CMOS process the values of R_f and over all capacitance cannot be realized in the allocated area of 0.1 mm^2 . This leads to a conclusion that the capacitance C_f should be considered as small as possible i.e. 1pF and some technique should be utilized accordingly to design the resulting resistance of i.e. 1.59G-ohms.

4.2 Realizing high value resistance in a CMOS process

In this section some well known techniques has been discussed to design a resistance in the order of G-ohms in a standard CMOS process. The techniques are listed as follows;

- Ultra High Value floating tunable resistor
- Diode connected PMOS transistor as resistor

- Switches Capacitor resistor

These methods have been discussed one by one in the following subsections;

4.2.1 Ultra High Value floating tunable resistor [6]

This technique presents a tunable high value resistor (HVR) using PMOS transistors operating in sub-threshold region [6]. The technique is very useful for low power applications and to design filters with very low cutoff frequency i.e. 100 Hz are realizable. Another usability of this method is that the resistance is tunable in a wide range. Fig 4.1 (inset) shows a PMOS transistor operating in sub-threshold region and its drain and bulk are connected together. The IV characteristics of this PMOS transistor characterize it as a resistor. The drain and bulk of the PMOS transistor are shorted which modifies the threshold voltage in such a way that it increases the drain current. The output conductance G_{SD} of this transistor due to the dependence of drain current on drain voltage can be expressed as;

$$G_{SD} = \left(I_{SD} / nU_T \right) \cdot n / \left(1 - \exp \left(-V_{SD} / U_T \right) - 1 \right) \quad (2)$$

where n is the sub-threshold slope factor of the PMOS transistor being used in this technique $U_T = kT/q$ is thermal voltage. The finite conductance (output resistance) G_{SD0} for $V_{SD} = 0$ can be expressed as;

$$G_{SD0} = \lim_{V_{SD} \rightarrow 0} (G_{SD}) \cdot \left(I_0 / U_T \right) \cdot \exp \left(V_{SG} / nU_T \right) \quad (3)$$

Equation 3 shows that the value of conductance can be adjusted by changing the value of V_{SG} . Equation 2 and 3 are valid for $V_{SD} \geq 0$ as for $V_{SD} < 0$ the PMOS transistor switches operates in moderate inversion region and the drain current increases rapidly. To overcome this issue two PMOS transistors, with drain and bulk of each transistor connected together, are used as shown in Fig 4.2. The V_{SG} of both transistor is controllable by controlling the flow of current through transistor M3. Figure 16 shows the IV characteristics of a resistor designed by two PMOS transistors.

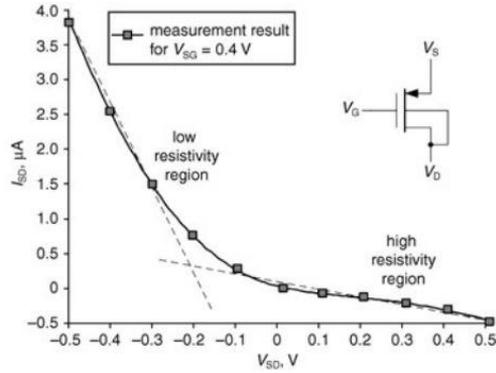


Fig 4.1: HVR with Bulk-Drain connected PMOS transistor with its IV characteristics [6]

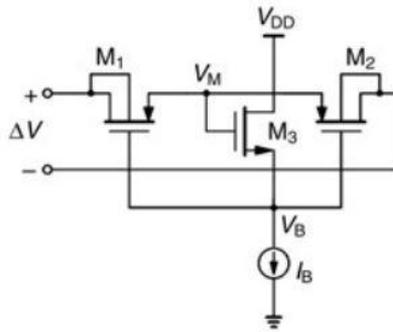


Fig 4.2: HVR with Two bulk-drain connected PMOS transistor with V_{SG} controllable by M3 [6]

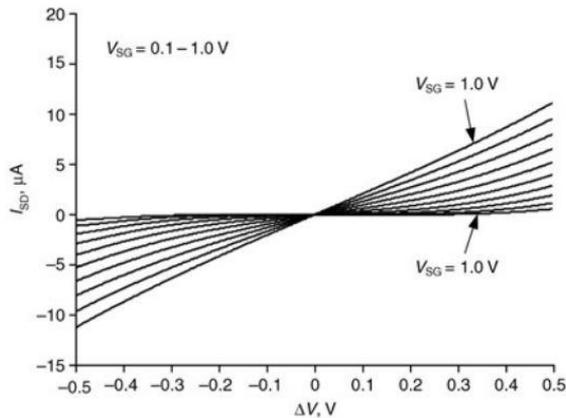


Fig 4.3: IV characteristic of HVR depicted in figure 15 [6]

4.2.2 Diode connected PMOS transistor as resistor [7]

The method in [7] describes another way of achieving an HVR using PMOS transistors as shown in the figure 4.4. The MOS resistor consists of a cascaded of two diode bulk PMOS transistors and its characteristics depends on voltage difference between its IN-OUT terminals. When $V_{in} > V_{out}$ then transistor T1 operates in triode region acting as a resistor and T2 behaves like a BJT with considerably small forward current. The situation is reversed when $V_{out} > V_{in}$ where T1 acts like resistor and T2 as BJT with very small forward current. The IV characteristics of the resistor proposed in [7] are shown in figure 4.5.

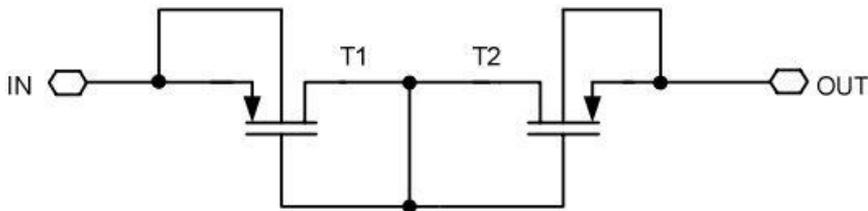


Fig 4.4: High value resistor using cascade of Diode bulk PMOS transistors [7]

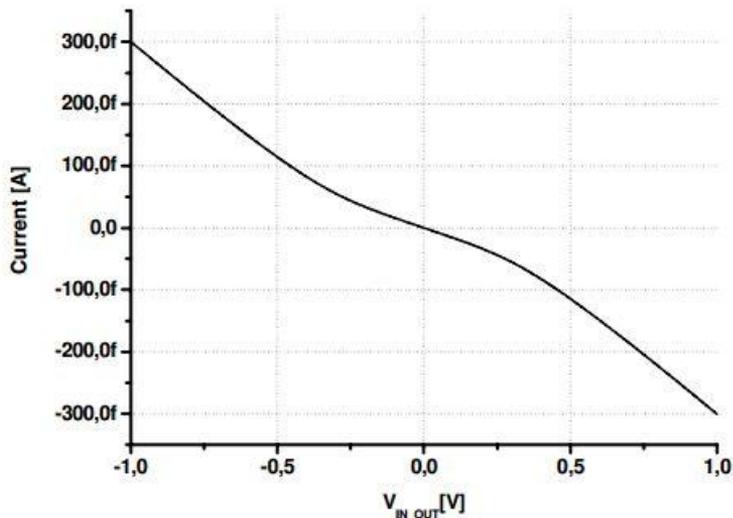


Fig 4.5: IV characteristics of High value resistor using cascade of Diode bulk PMOS Transistors [7]

4.2.3 Switched Capacitor resistor [8]

In the previous techniques HVRs are realized with MOS transistors but in this method [8] a combination of switches $sw1$ and $sw2$ with a parallel capacitor “C” emulates the behavior of an HVR as shown in Figure 4.6. The clock phases (ϕ_1 and ϕ_2) of switches $sw1$ and $sw2$ are non-overlapping and their duty cycle should be less than 50%, as shown in figure 4.7. The switching frequency of these clock phase should be much higher than that of signals $V_{in}(t)$ and $V_{out}(t)$. The resistance of such a resistor can be very accurately controlled by the changing the switching frequency.

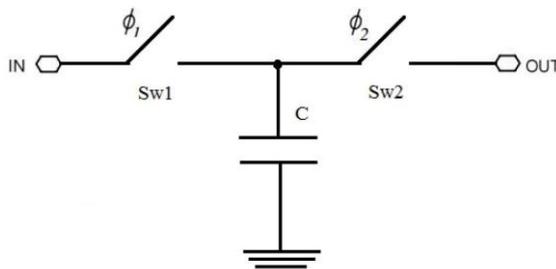


Fig 4.6: Schematic of a switched capacitor resistor

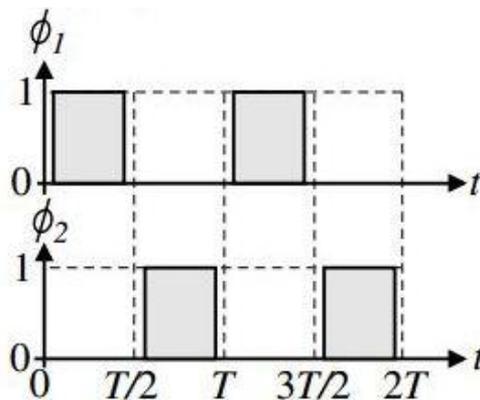


Fig 4.7: Non overlapping Phase clocks for the switched capacitor resistor [8]

The detailed derivation in [8] leads to expression of resistance of a switched capacitor resistor as a function of parallel capacitance C and the time period of clock phases T as;

$$R = T/C \quad (4)$$

Equation 4 can be illustrated by a simple example; To emulate 1 M-ohms resistance for the switching frequency of 100 KHz (T =10 μ sec) the parallel capacitance C is expressed to be 10 pF as follows;

$$C = T/R = \frac{10 \mu}{1 M} = 10pF$$

4.3 Comparison of techniques to realize HVR in CMOS

The first two techniques seem very attractive because of the small in number and sizes of PMOS devices and also they don't require overhead compared to switched capacitor resistor. But replacing feedback resistor R_f with any one of PMOS transistor based HVRs can substantially increase the noise floor of the PreAmplifier. They also introduce small DC offset in the output voltage (as they require bias voltage to operate) which may not be suitable for the low voltage PreAmplifier to be designed. Switched capacitor resistor on the other hand offer high linearity and low distortion and offer less noise compared to PMOS transistor resistors. The only overhead is the non-overlapping clock phases which can be easily designed in CMOS. So it can be concluded that switched capacitor resistor can be a good choice to implement the feedback resistance R_f . A discussion is provided in the following sections to analyze and design the required resistor (1.59GOhms) using switched capacitor technique.

4.4 Designing R_f as a SC resistor

Equation 4 reveals that for a larger value of resistor R the capacitance C needs to be as small as possible. The minimum value of realizable capacitance in layout in the available process is 10 fF. Considering the values of $R_f = 1.59M\text{-Ohms}$, $C_f = 1\text{Pf}$ (for $f_{lower\ cutoff} = 100\text{ Hz}$) and C = 10 fF, the switching frequency $f_{switching}$ of the SC resistor becomes equal to 62.5 KHz. In this regard C_f can be decreased to relax the area constraints and the R_f can be increased accordingly to get the same $f_{lower\ cutoff}$. But increasing R_f requires either lower value of C, which is not possible as it is already 10fF, or lower value of switching frequency which is not

considered as a good choice as it may corrupt the output voltage spectrum of the PreAmplifier. So by considering all these factors in mind it is finally decided to design the filter with $R_f = 1.59\text{G-ohms}$ and $C_f = 1\text{pF}$.

Using equation 4, an SC resistor for $R_f = 1.59\text{ G-ohms}$ and $C = 10\text{ fF}$ requires $f_{swinging}$ of the non overlapping clock phases to be 62.5 KHz . The duty cycle of the clock phases should be less than 50%. Other parameters i.e. delay time and pulse-width are computed and adjusted using computer simulations to achieve non overlapping clock phases in order to emulate R_f as 1.59 G-ohms . The values of different parameters for the non overlapping clock phases are summarized in Table 4.1 and the clock phases are also shown in fig 4.8.

TABLE 4.1: PARAMETER VALUES FOR NON OVERLAPPING CLOCK PHASES Ø1AND Ø1

Parameter	Clock Phases Ø1	Clock Phases Ø2
Time Period	16 µsec	16 µsec
Delay time	3.18 µsec	12.7 µsec
Pulse Width (µsec)	3.18 µsec	3.18 µsec

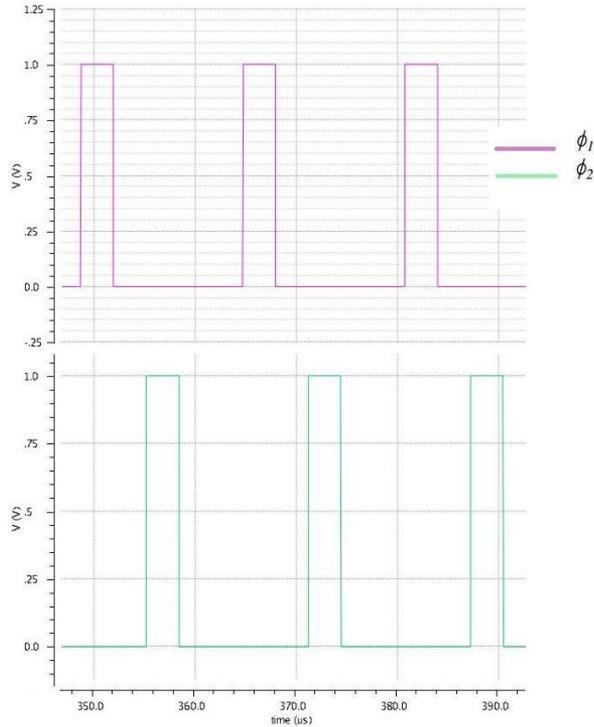


Fig 4.8: Waveforms showing the non-overlapping clock phases

4.5 Summary

Various methods to realize a high value resistor (HVR) in a standard CMOS process have been discussed in details with their respective merits and demerits. The SC technique has been finally chosen to implement the resistance R_f . The parameters values required to design R_f with SC resistor has been calculated and signal waveforms are shown accordingly. The filter thus consist $C_f = 1\text{pF}$ and the $R_f = 1.59\text{ G-ohm}$ which is implemented as an SC resistor. Once the feedback filter is designed the next task is to design the amplifier and the following chapters discuss this in great details.

CHAPTER 5

5 Operational Amplifier Specifications and Design Considerations

The design of an operational amplifier (opamp) requires setting its specifications depending on the type of its application. Based on these specifications the designer chooses suitable opamp architecture in order to meet those specifications. In this chapter, section 5.1 discusses some of the operational amplifiers specifications which are crucial to the design of PreAmplifier. Section 5.2 describes different CMOS architectural implementations of an opamp. The chapter ends with a summary and provides some recommendations to go forward with design of two stage opamp.

5.1 Opamp specifications

The specifications of an opamp are determined to characterize its performance and to take into account the non ideal effects which limit the performance of an ideal opamp. Although an opamp can be characterized with lot of specifications as described in [9] and [10] but most often only some of these specifications are needed for the design of an opamp.

The opamp to be designed for the PreAmplifier is responsible for setting many of its specifications i.e. gain, Noise, PSR and THD, etc. So the specifications of opamp related to the design of PreAmplifier can be listed as follows;

- Gain
- Input common mode range
- Output swing
- Unity Gain Bandwidth and Phase Margin
- PSRR
- Equivalent Input Noise

- Total Harmonics distortion plus Noise (THD+N)

These specifications enable the designer to decide about which kind of opamp architecture is suitable and are discussed briefly in the following subsections;

5.1.1 Gain

In any CMOS topology the gain is defined as the product of transconductance (g_m) of input stage and the resistance (R_{out}) of its output stage and can be expressed as;

$$A_v = Gain = g_m * R_{out} \quad (5)$$

The gain of opamp is a function of input signal frequency and it rolls off rapidly at the higher frequencies due to the poles which are formed by the parasitic capacitances. When an opamp is used along with negative feedback, the closed loop gain of the amplifier becomes insensitive to the gain of the opamp. The feedback, which is normally realized from passive components, then defines the closed loop gain of the amplifier.

5.1.2 Input common mode range

The input common mode range or ICMR specifies the range of input voltage (common to both input terminals of an opamp) over which the amplifier responds to small input differential signals properly. The ICMR depends upon the type of input stage i.e. an N-channel differential pair and a P-channel differential input pair [15]. ICMR of an input stage with P-channel differential input transistors, as shown in the fig 5.1 can be expresses as;

$$V_{SS} < V_{common} < V_{DD} - V_{DSAT} - V_{SGP} \quad (6)$$

where V_{common} is the common-mode input voltage, V_{DSAT} is the voltage across the current mirror, V_{SGP} is the source-gate voltage of an input transistor and V_{SS} and V_{DD} are the negative and positive supplies respectively.

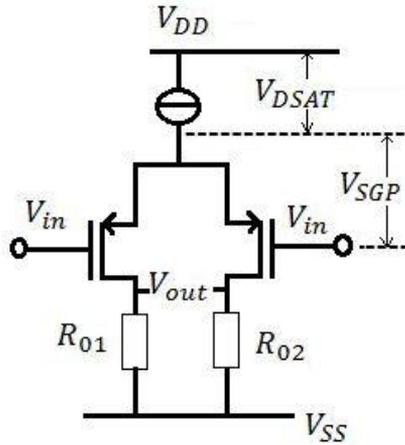


Fig 5.1: P-channel differential input stage [10]

5.1.3 Output voltage swing

The type of output stage in an amplifier specifies the output voltage swing. The more stacked transistor in the output stage results in reduced output swing. In general the output swing of an opamp is the summation of V_{DSAT} of stacked transistors subtracted from V_{DD} and can be expressed as follows;

$$V_{DD} - \sum V_{DSAT} \quad (7)$$

5.1.4 Unity Gain Bandwidth and Phase Margin

These two parameters are related to the frequency response of an opamp. The Unity Gain Bandwidth, f_u , also known as Gain Bandwidth Product specifies the frequency at which the open loop gain of an opamp is unity or 0dB. The phase margin specifies the stability of an opamp and is the difference between the amount of phase shift experienced by a signal through the opamp at unity gain and 180° . The phase margin can be expressed as;

$$\phi_m = 180^\circ - \text{phase @ } f_u \quad (8)$$

5.1.5 Power Supply Rejection Ratio (PSRR)

Power supply rejection ratio, PSRR, is defined as the ratio of changes in power supply voltage to the changes in the output voltage. It can be expressed as;

$$PSRR = \frac{\Delta V_{supply}}{\Delta V_{out}} \quad (9)$$

5.1.6 Equivalent Input Noise

Noise can be present in an opamp noise due to various sources. Noise is usually referred to input through dividing the output noise by the gain of amplifier and hence called the equivalent input noise. Noise in an opamp is generally specified as integrated noise between a bandwidth say from 100 Hz to 10 KHz and is measured as nV/\sqrt{Hz} or pA/\sqrt{Hz} .

5.1.7 Total Harmonics distortion plus Noise (THD+N)

THD+N is an important parameters which compares the frequency contents of output signal to the frequency contents of input signal. It is the ratio of harmonics of fundamental frequency to the fundamental frequency and the output, and is generally specified as percentage;

$$THD + N = \frac{\sum (\text{Harmonic Voltage} + \text{Noise Voltages})}{\text{Total output voltage}} * 100\% \quad (10)$$

In the light of above discussion, important opamp specifications i.e. open loop DC gain A_{DC} , input and output voltage ranges, load capacitance, supply voltage (VDD) and current consumption (I_{DC}) are listed in Table 5.1. The A_{ol} specification is set after observing the closed loop gain A_v of the PreAmplifier in the system model AC simulation by changing the “gain” parameter of system model opamp. The supply voltage VDD and current consumption I_{DC} are already specified for the PreAmplifier. The input and output voltage requirements are specified after consulting the team at hearing aid manufacturer. These specifications entail to develop a true schematic approximation of the opamp and then to improve the opamp design by analyzing the specified results of PreAmplifier in closed loop simulations.

TABLE 5.1 SUMMARY OF OPAMP SPECIFICATIONS

Parameter	Specification
Open loop DC Gain (A_{DC})	> 50 dB
Supply Voltage (VDD, VSS)	1 V , 0V
Current consumption	28 μ Amp
Input Voltage range	100mV – 900 mV
Output Voltage range	100mV – 900 mV
Load Capacitance (C_L)	500 fF – 1pF

5.2 Choice of opamp topologies

The supply voltage (1V) and current consumption (28 μ Amp) requirements of the PreAmplifier brings the design of opamp into the low voltage and low power category in the available CMOS process. Also the hearing aid (the target application of the PreAmplifier) like many other battery operated devices requires low power for its reliable and long lasting operation. The latest CMOS technologies have favored the density and reliability of integrated circuits and offer less power consumption due to decreased power supply voltage. These factors have enabled the compact and more reliable designs of battery operated devices mostly used in biomedical applications such as ambulatory heart rate detectors and hearing aids. But this is also followed by some potential problem i.e. the threshold voltage of a MOS transistor is not scaling down at the same rate as the power supply voltage is being scaled down. This concern analog circuits a lot as the dynamic range of analog circuits is severely limited which makes the design of analog/ mixed signal circuits more challenging.

In this regard many innovative techniques of designing an operational with acceptable and comparable performance have been reported. These techniques include floating gate technique [11], current driven bulk (CDB) [12], bulk driven technique [13] [14] [15] and analog circuit design in weak inversion [10].

Among these techniques, the weak inversion technique has been considered to be a better choice of designing a low voltage and low power opamp. The weak inversion technique gives the provision to design an opamp using many different opamp topologies which include telescopic opamp, folded cascode opamp and a two stage opamp. The choice of right opamp topology mainly depends upon the opamp specifications as shown in table 5.1. Some

of the merits and demerits of these topologies which lead to decide the suitable opamp topology are described briefly as follows;

Telescopic opamp Topology

In this type of opamp architecture, as shown in fig 5.2, stacked transistors (M5-M8) which are placed on top of the input differential pair severely limits the amplifier’s input common mode range ICMR [16]. It has internal compensation and offers high PSRR.

Folded cascode opamp topology

In this type of opamp architecture, as shown in the fig 5.3 the stacked transistors (M3-M6 and M7-M10) in the folded cascode stage limits the output voltage swing. The amplifier also needs more biasing circuits and consumes more power [16]. It has internal compensation and offer high PSRR.

The Two Stage Topology

The two stage opamp architecture, as shown in fig 5.4, is very compact and offers moderate gain, has large input and output swings compared and offer less power consumption. But it has no internal compensation and offers poor PSRR.

As the primary concerns for the opamp to be designed are low supply voltage and high dynamic range of input and output signals so the 2 stage opamp topology seems to be the natural design choice.

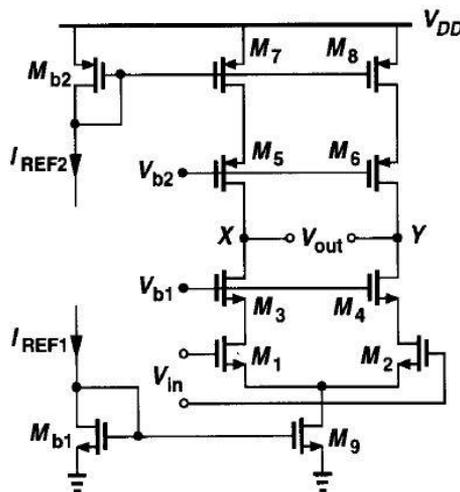


Fig 5.2 [16]: Fully differential Telescopic operational amplifier

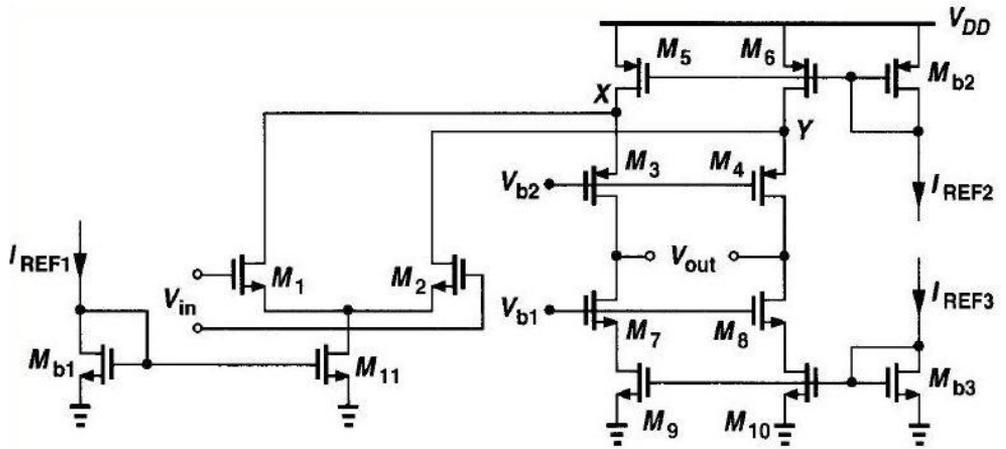


Fig 5.3 [16]: Fully differential Folded Cascode operational amplifier

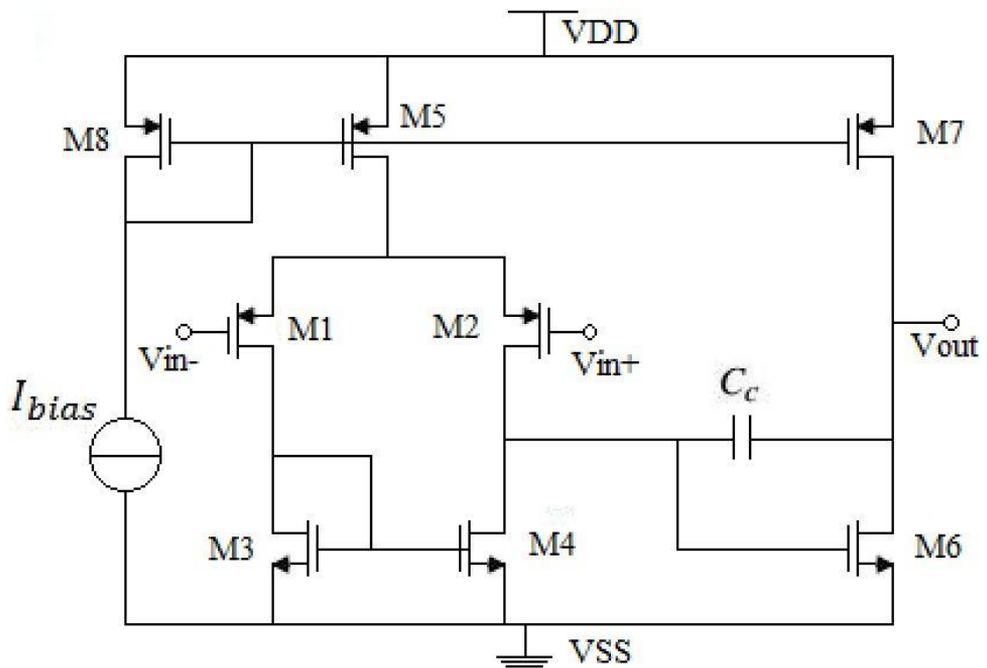


Fig 5.4: Single ended 2 stage operational amplifier

5.3 Summary

In this chapter the specifications which are important in the design of an opamp are briefly described. The summary of the specifications for the opamp to be designed for the PreAmplifier is also provided in the tabular form. A brief review of different opamp topologies used to design an opamp is presented in order to design the specified opamp. The two stage opamp topology is selected to implement the specified opamp due to its moderate gain and better input and output dynamic ranges. The next step in the design of such an opamp is developing a method to find transistor dimensions which includes overdrive voltage (V_{ov}) method and relatively new method which is g_m/I_d method. In the next chapter efforts have been made to address g_m/I_d method which in comparison to V_{ov} method is very efficient and reliable method.

CHAPTER 6

6 Technology characterization using g_m/I_d method

The evolution of ultra scaled VLSI technologies is marked by increasing demand for more signal processing integrated on a single chip [17]. The minimum feature sizes have been exponentially reduced following this evolution. This trend has benefited the digital circuits because of higher densities but has critically affected the performance of analog circuits mainly due to reduced power supply rails, lower gain and lower dynamic range. As a result, the conventional paper and pencil methods for analog design, employing long channel equations are not producing desired results. Moreover the reduced supply voltage headroom entails a transistor to work in all regions of operations in order to get acceptable performance. This situation called for a precise and an intuitive design procedure which involves a through technology characterization. A method known as “ g_m/I_d method” is developed wherein current I_d is fixed to find out transistor dimensions in order to comply with the specifications such as gain-bandwidth, power consumption, area, etc. This method involves family of curves to characterize the PMOS and NMOS transistors of a particular technology and it is independent of transistor dimensions. The following section describes the g_m/I_d method in more details.

6.1 Introduction

The conventional analog design method is based on a set of long channel equations and involves V_{ov} (over drive voltage) as a key design parameter. The V_{ov} defines the operating regions of MOS transistor. It has been found that to make a compromise between bandwidth and power consumption of a common source amplifier, V_{ov} needs to be reduced which in turn results in increased size of a transistor [18]. The following equation expresses the relationship between the size of transistor and V_{ov} .

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox} V_{ov}} \quad (11)$$

The above equation suggests that for fixed values of g_m and L , smaller V_{ov} results into a bigger (wider) device and hence a larger C_{gs} . So it can be concluded from this scenario that V_{ov} is not a very good design parameter.

During the design phase the performance of an analog circuit mainly takes into account the large signal and small signal characteristics. The large signal characteristics involve drain current I_d and drain–source voltage V_{DS} . The power consumption P (determined by product I_d and V_{DS}) thus determines the available signal swing i.e. ICMR and output swing. The small signal characteristics involve the transconductance g_m , intrinsic capacitances C_{gg} (C_{GS} , C_{GD} , C_{DB}) and output impedance r_o . The voltage gain is determined by g_m , the speed by intrinsic capacitances and r_o signifies the voltage gain. These characteristics are expressed as follow;

DC voltage gain

$$A_{DC} = g_m \cdot r_o$$

Bandwidth

$$f_{transit} = \frac{1}{2\pi R_{in} C_{gg}}$$

Power dissipation

$$P = V_{DD} \cdot I_d$$

Based on above discussion it can be concluded that a transistor is required to have large gm without having high current consumption and large C_{gg} .

6.1.1 Performance metric of interests

For technology characterization of a transistor and to quantify its performance following performance measures are expressed;

Transit Frequency

$$\omega_T = \frac{g_m}{C_{gs}}$$

Trans-conductance Efficiency

$$\frac{g_m}{I_d} = \frac{3}{2} \cdot \frac{\mu V_{ov}}{L^2}$$

Intrinsic Gain

$$\frac{g_m}{g_{ds}} = \frac{2}{\lambda \cdot V_{ov}}$$

6.1.2 Technology characterization

In g_m/I_d methodology, for each of the above mentioned performance parameters respective characteristic curves are obtained. These curves can accordingly be classified as follows;

Intrinsic gain $\rightarrow g_m/I_d$ versus $I_d/(W/L)$

Transconductance efficiency $\rightarrow f_T$ versus $\frac{g_m}{I_d}$

Transit Frequency $\rightarrow g_m/g_{ds}$ versus g_m/I_d

These characteristic curves give the provisions to find out the dimensions of a transistor in a variety of ways by considering the performance parameters. The relationship between g_m/I_d versus $I_d/(W/L)$ represents a unique characteristic for all transistors of same type (i.e. PMOS or NMOS) in a specific technology. This unique characteristic of g_m/I_d versus $I_d/(W/L)$ method can be exploited during the design phase to determine the transistor sizes. Once the g_m/I_d ratio is specified based on the operating region of a transistor or from the specifications, the W/L ratio can be determined by specifying the drain current from current consumption requirements.

In the design of 2 stage opamp normally g_m/I_d ratio can be specified from the gain bandwidth specifications whereas the drain current of a transistor can be determined from current consumption requirements. So this work will only focus on g_m/I_d versus $I_d/(W/L)$ characteristic curves. The following section describes the steps involved in generating the g_m/I_d versus $I_d/(W/L)$ characteristic curves.

6.2 Generation of g_m/I_d versus $I_d/(W/L)$ characteristic curves

Figure 6.1 shows a typical g_m/I_d versus $I_d/(W/L)$ curve wherein the three regions of operation i.e. weak inversion, moderate inversion and strong inversion can be identified.

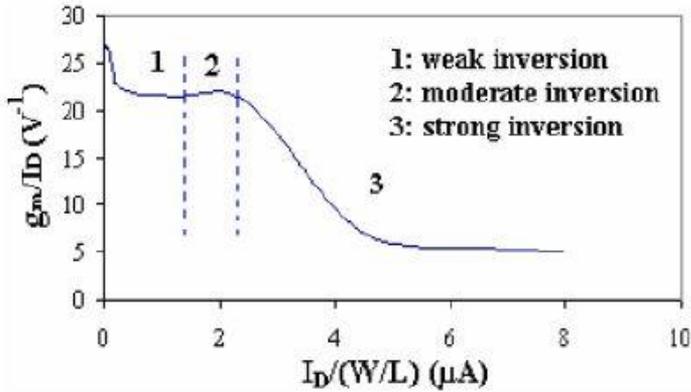


Fig 6.1: g_m/I_D versus $I_D/(W/L)$ curve [17]

But for the better choice of operating regions, $\frac{g_m}{I_D}$ versus V_{GS} and $I_D/(W/L)$ versus V_{GS} curves can also be plotted. The values of V_{GS} determine the region of operation and for a chosen value of V_{GS} values of both $\frac{g_m}{I_D}$ and $I_D/(W/L)$ can be determined which can then be used in the process of determining the transistor dimensions. To generate such curves for a NMOS and a PMOS transistor of the technology in hand, two different schematics has been setup wherein a variable voltage source is connected between gate and source of the diode connected transistor. Fig 6.2 a shows the schematic setup for NMOS transistor whereas fig 6.2 b PMOS transistor respectively.

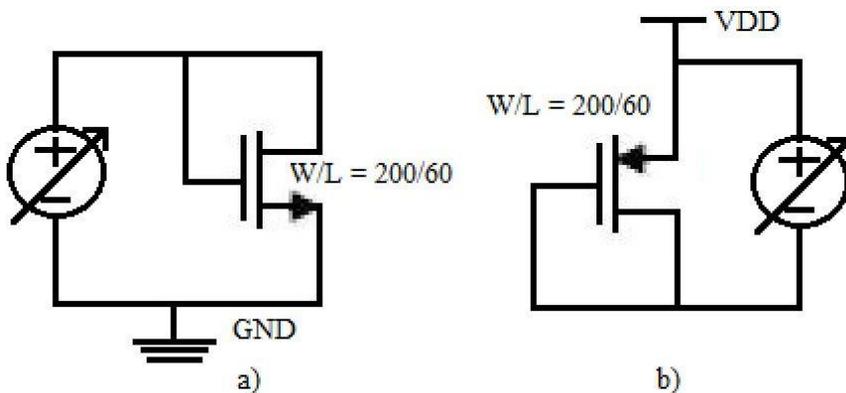


Figure 6.2: a) schematic setup for NMOS transistor b) schematic setup for PMOS transistor

Setting up the schematics is followed by DC analysis in which value of voltage V_{GS} is swept from 0 to 1V (which is the available power supply headroom) for both transistors. After the DC analysis, calculator function “op” brings up a list of transistors op (operating points) parameters by selecting the respective transistor from the schematic. These parameters include intrinsic capacitances, transconductance, DC currents and voltages, etc. Selecting op parameters import their values over the entire DC sweep into the work space of calculator where they can be used to form expressions and these expressions can also be plotted afterwards. The results of these DC simulations and their manipulation in the form of required characteristic curves are shown in the following figures;

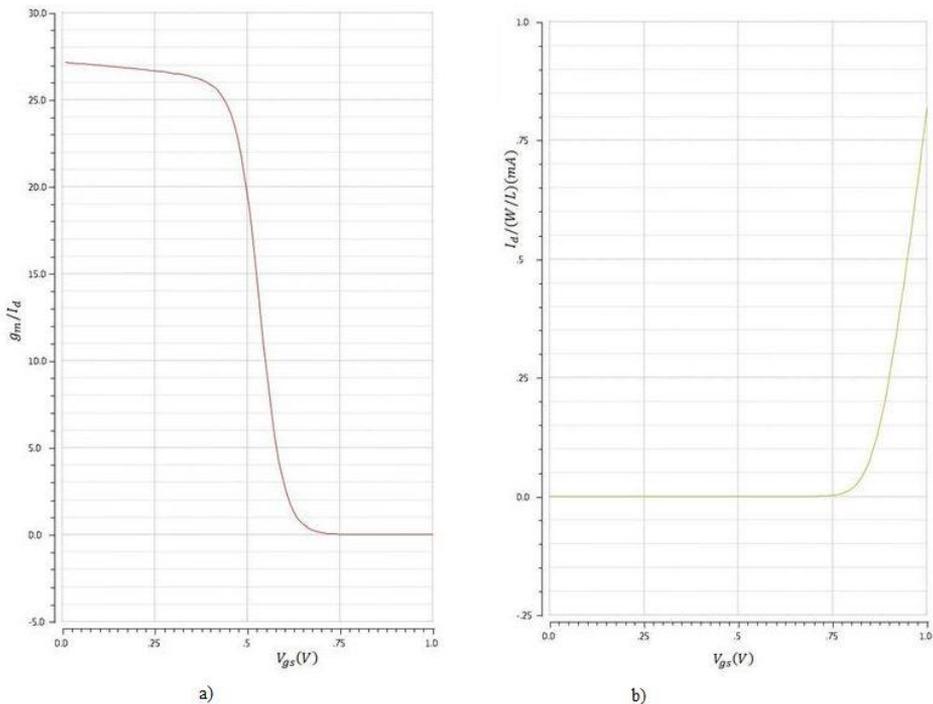


Figure 6.3: g_m/I_d curves for PMOS transistor a) g_m/I_d versus V_{GS} b) $I_d/(W/L)$ versus V_{GS}

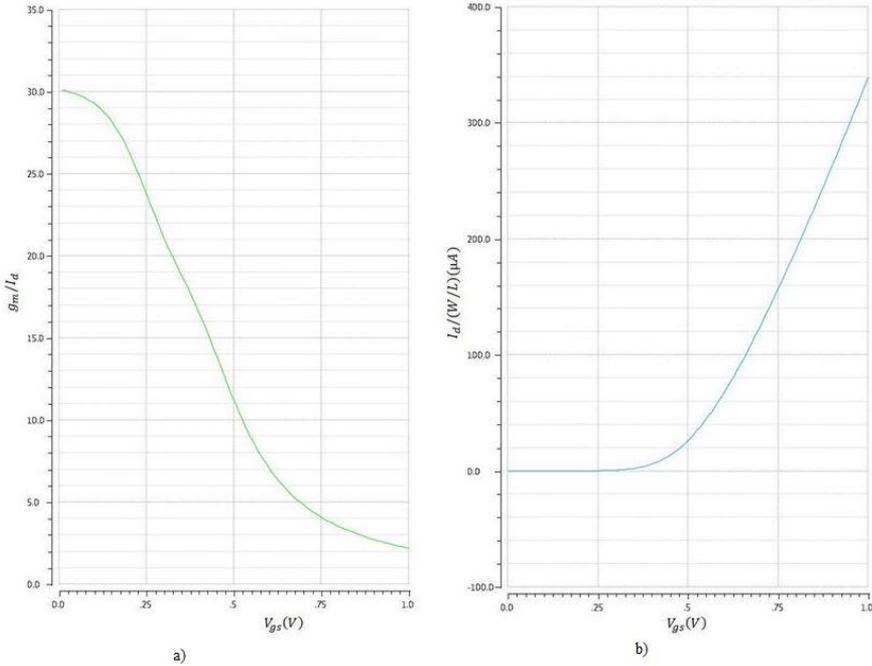


Figure 6.4: g_m/I_d curves for NMOS transistor a) g_m/I_d versus V_{GS} b) $I_d/(W/L)$ versus V_{GS}

6.3 Important features of gm/id method

Following are some of the important features of gm/id method which are extracted from [19] [20].

- It gives the designer full provision to choose any region of operation as the curves are continuous and there is no transition between different regions. Moreover this method is reliable as the curves are unique for a particular technology and are independent of the size of a transistor.
- The level of transistor inversion level can be chosen by this method which allows the designer to make important design tradeoffs i.e. between bandwidth, gain and power consumptions, etc.
- The family of pre-generated characteristic curves for a particular technology enables a complete analog circuit like a two stage opamp to be divided into smaller parts. The transistor sizes of these

smaller parts can then be easily found based on large signal and small signal specifications.

- Once technology is comprehensively characterized, the iterative design process as required in a complex analog circuit can be considerably reduced.

CHAPTER 7

7 Design of a Two Stage operational amplifier using gm/id based method

This chapter deals with the design and simulation results of a two stage opamp. It begins with a review of the two stage opamp architecture and discusses its different stages. Section 7.2 highlights some of the specifications which are important to understand a two stage opamp before proceeding with the design. Section 7.3 describes the design procedure of two stage opamp using gm/ id methodology. Section 7.4 characterizes the designed opamp with its various simulation results. The chapter ends with a summary and compares the simulated values of opamp design parameters with the specified values.

7.1 Review of a Two Stage Opamp architecture

In chapter 5, it has been motivated that a two stage opamp is suitable for low voltage applications and for larger input and output voltage swings. A two stage opamp isolates the input stage from the output stage contrary to telescopic and folded cascode opamps [16]. So in the two stage opamp the input stage provides high gain and the output stage provides high swing. Figure 7.1 shows a schematic diagram of a typical two stage miller compensated CMOS opamp.

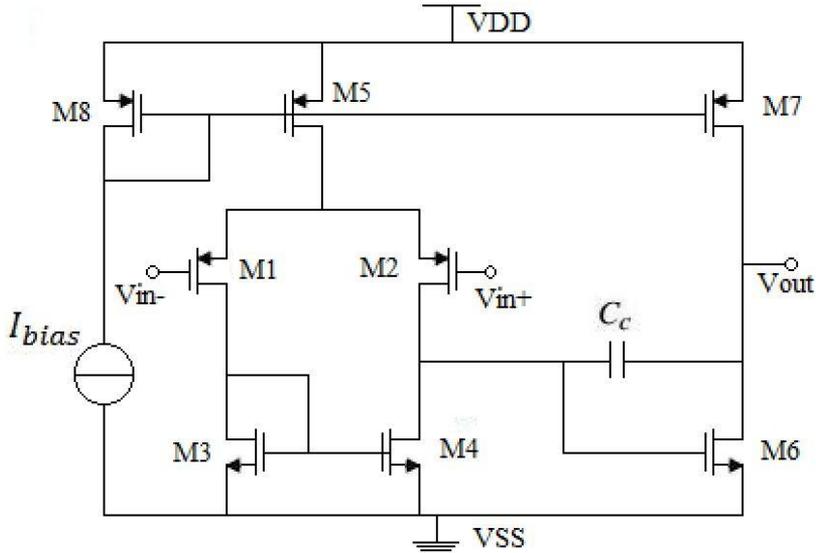


Fig 7.1: Schematic diagram of a typical two stage CMOS operational amplifier

The two stage opamp schematic as shown above can be divided into 4 distinct stages, depending upon their operation which makes it a bit easier to understand the principle of a two stage opamp. These stages can be listed as follows; [8] [21]

- Input stage consisting of M1, M2, M3, M4
- Biasing Stage consisting of M8, M5
- Compensation stage consisting of C_c
- Output Stage consisting M6, M7

The following sub-sections briefly describe each of these stages.

7.1.1 Input stage

The input stage, which is responsible for high gain and high ICMR, comprises of differential input transistors M1 and M2 with their active loads transistor M3 and M4. The input pair can either be N-channel devices or P-channel devices depending upon the requirements i.e. noise, gain and ICMR. The P-channel transistors are less prone to noise whereas N-channel transistors offer more gain. The gain A_{v1} and the output resistance R_{o1} of the input stage can be expressed as.

$$A_{v1} = g_{m1,2} \cdot R_{o1} \quad (12)$$

$$R_{o1} = \frac{1}{g_{ds1} + g_{ds2}} \quad (13)$$

7.1.2 Output stage

Output stage consists of a common source amplifier (M6 and M7) which allow maximum output dynamic range. The output stage also increases opamp open loop gain. The output voltage swing of common source output stage can be expressed as;

$$V_{DSAT7} < V_{out} < V_{DD} - V_{DSAT} \quad (14)$$

Also the gain of the output stage A_{v2} and the output resistance R_{o2} of the output stage can be expressed as;

$$A_{v2} = g_{m6} \cdot R_{o1} \quad (15)$$

$$R_{o1} = \frac{1}{g_{ds6} + g_{ds7}} \quad (16)$$

7.1.3 Biasing stage

The current mirror transistors M8 and M5 forms the biasing circuit. The tail transistor, M5, provides the biasing current I_5 to the input differential pair where I_5 is a multiplied version of I_{bias} , drain current of M8. For I_5 to be a good multiplied replica of I_{bias} , transistor M5 also need to be a multiplied version of transistor M8. Also the tail transistor determines the PSRR of the opamp and thus special considerations are required to design while designing the current mirror bias stage expressed as follows;

$$PSRR = \frac{A_{DC}}{g_{m5} \cdot R_{o2}} \quad (17)$$

where A_{DC} is the open-loop gain of the opamp. The PSRR of opamp can be improved by using cascaded current mirror transistor.

7.1.4 Compensation Stage

Opamps require compensation to make it more stable or in other words to increase the phase margin. The two stage opamp uses Miller compensation technique wherein the miller capacitance C_c moves the two poles in the output nodes of input and output stage in opposite directions. One pole becomes the dominant pole while the other pole is pushed towards higher frequencies. Although there are different methods of compensation which can be found in literature [16] [21] [22] but the designed opamp uses miller compensation technique.

7.2 Two Stage opamp Specifications

The specifications which play important role in the design of a 2 stage opamp specifications are expressed as follows; [21]

Current consumption

$$I_{DC} = I_{D5} + I_{D7} + I_{bias}$$

DC Gain “ A_{DC} ”

$$A_{DC} = A_{v1} + A_{v2}$$

$$A_{DC} = g_{m1,2} \cdot g_{m6} \cdot R_{o1} \cdot R_{o2}$$

Unity gain frequency “ ω_u ” and Phase Margin “PM”

$$\omega_u = \frac{g_{m1}}{C_c}$$

$$PM = 180^\circ - \arctan\left(\frac{\omega}{f_{p1}}\right) - \arctan\left(\frac{\omega}{f_{p2}}\right) - \arctan\left(\frac{\omega}{f_{z1}}\right)$$

where f_{p1} , f_{p2} are the frequencies of poles and f_{z1} is the zero in the transfer function of a two stage opamp.

7.3 Design of a two stage opamp

The summary of the two stage opamp specifications is shown in Table 7.1. These specifications are basically derived from PreAmplifier system model simulation results and are the result of discussion with the team at hearing aid manufacturer.

TABLE 7.1: TABLE OF OPAMP SPECIFICATIONS

Parameter	Specification
A_{DC} (dB)	> 50
PM ($^{\circ}$)	60
GBW or ω_u (MHz)	25
I_{DC}	28 μ Amp
VDD (V)	1
VSS (V)	0
C_L (pF)	1

The opamp uses g_m/I_d method which has been extensively discussed in the previous chapter. Before describing the actual design procedure of a two stage opamp it is necessary to understand how g_m/I_d method can be used to determine a transistor dimension. The procedure of finding the dimension of a transistor of a two stage opamp using gm/id method for can be described as following steps[18];

1. Determine the drain current I_d from the power consumption requirement
2. Specify the transconductance g_m based on given specification i.e. GBW and determine g_m/I_d
3. Determine the value of $(I_d/(W/L))$ based on the values of g_m/I_d using characteristic curves
4. Determine the aspect ratio W/L from $(I_d/(W/L))$
5. Specify the Length of transistor, L, and determine its width.

Having established an understanding of g_m/I_d method to determine a transistor dimension, design of a two stage opamp based on gm/id method has been described in the form of following steps; [19][20]

Step 1: Current Budget

The total current budget for the opamp, as shown in Table 7.1, is 28 μ Amp. To burn less current in the current mirror of the biasing stage, I_{D8} is specified to be 500nAmp. The current in the output stage is normally higher than the input stage so the input stage current I_{D5} and the output stage current I_{D7} are specified as 12 μ Amp and 15 μ Amp respectively.

Step 2: Compensation capacitance C_c

The values of compensation capacitance C_c can be found by considering the phase margin specification as follows [9];

$$C_c = 0.22 * C_L$$

So for the $C_L = 1$ pF the value of C_c turns out to be 220fF which can be modified as 500fF during the simulations to in order for the opamp improve its phase margin.

Step 3: Specify $(g_m/I_d)_{1,2}$

The input pair transistors are chosen to be PMOS channel devices for better noise response. The g_m of input pair transistors can be found out from gain-bandwidth specifications of the opamp and can be expressed as follows;

$$GBW = g_{m1,2}/C_c$$

Following the above equation, for the values of GBW as 25 M Hz and C_c as 500fF, $g_{m1,2}$ is calculated to be 12. 5 μ S. As the current flowing through the input pair is 6 μ Amp $(g_m/I_d)_{1,2}$ turns out to be 2. This value is approximated to be 15 for the transistor to be in sub-threshold and represented as.

$$\left(\frac{g_m}{I_d}\right)_{1,2} = 15$$

The value of $I_d/(W/L)$ for the value of $(g_m/I_d)_{1,2}$ is specified as 30nA from the g_m/I_d curves shown in the previous. Putting the value of I_d as 6 μ A the W/L is determined to be;

$$\left(\frac{W}{L}\right)_{1,2} = 200$$

Step 4: Specify $\left(\frac{g_m}{I_d}\right)_{3,4}$

For the transistors M3 and M4 to work in weak inversion the value of $(g_m/I_d)_{3,4}$ is specified as;

$$\left(\frac{g_m}{I_d}\right)_{3,4} = 20$$

As the current flowing through M3 and M4 is the same in M1 and M2 so following the description in step 1 $\left(\frac{W}{L}\right)_{3,4}$ is specified as;

$$\left(\frac{W}{L}\right)_{3,4} = 415$$

Step 5: Specify $(g_m/I_d)_6$

To set the output voltage midway between the supplies, $\left(\frac{g_m}{I_d}\right)$ of the transistor M6 should be equal to $\left(\frac{g_m}{I_d}\right)$ of transistor M3 and M4 [18] [24].

So considering the current in the output stage ($I_{D7} = 15\mu\text{Amp}$), the aspect ratio of the transistor M6 is specified as follows;

$$\left(\frac{g_m}{I_d}\right)_{3,4} = \left(\frac{g_m}{I_d}\right)_6 = 15$$

$$\left(\frac{W}{L}\right)_6 = 900$$

Step 6: Specify $(g_m/I_d)_7$

The transconductance g_{m7} of output stage transistor is normally an integer multiple of the transconductance of input pair transistors M1 and M2. In this case $\left(\frac{g_m}{I_d}\right)$ of transistor M7 is specified to be two times $\left(\frac{g_m}{I_d}\right)_{1,2}$;

$$\left(\frac{g_m}{I_d}\right)_7 = 2 * \left(\frac{g_m}{I_d}\right)_{1,2} = 30$$

So for current $I_{D7} = 15\mu\text{Amp}$, the aspect ratio of the transistor M6 is determined to be;

$$\left(\frac{W}{L}\right)_7 = 960$$

Step 7 Biasing stage M5, M8

Considering the PSRR specifications of PreAmplifier, the current mirror in the bias circuit is implemented as cascaded stages as shown in the fig 7.2. All the transistors in the bias circuit are operating in weak inversion region so their respective $\left(\frac{g_m}{I_d}\right)$ is specified as 28. Considering the drain currents in the respective transistors, $\left(\frac{W}{L}\right)_{8_{1,2}}$ and $\left(\frac{W}{L}\right)_{5_{1,2}}$ are determined as follows;

$$\left(\frac{W}{L}\right)_{8_{1,2}} = 35$$

$$\left(\frac{W}{L}\right)_{5_{1,2}} = 900$$

Table 7.2 summarizes the transistors dimension of 2 stage opamp designed using g_m/I_d methodology. The length of input pair transistors has been chosen to be $1\mu\text{m}$ as bigger devices are suitable for better matching. The length of other transistors has been chosen to be 400nm to minimize the short channel effects found in the latest technologies and also for better matching. As the gate lengths of all transistors are larger so their gates are divided into fingers accordingly to minimize the gate resistance. All transistors are in sub-threshold regime.

TABLE 7.2: TABLE OF TRANSISTOR SIZES OPAMP

Transistor/ Component	Aspect Ratio $\left(\frac{W}{L}\right)$	Length (L) μm	Width (W) μm	Region of operation
M 1,2	200	1	200	Sub-Threshold
M 3,4	415	0.4	166	Sub-Threshold
M 5_1,2	900	0.4	360	Sub-Threshold
M6	900	0.4	360	Sub-Threshold
M7	960	0.4	385	Sub-Threshold
M8_1,2	35	0.4	14	Sub-Threshold
$C_c = 220 \text{ fF}$ for $C_L = 1 \text{ pF}$				

7.4.1 AC Analysis

The AC analysis are easy to setup and the procedure to set it up has been already been described in the system model simulation results in chapter 3. The important AC analysis results for an opamp are the gain and phase response. The gain response shows open-loop DC gain and unity gain frequency of opamp whereas the phase response characterizes the stability of an opamp. Fig 7.3 shows the gain and the phase response of designed opamp wherein the open-loop DC gain is measured to be 55 dB, unity gain bandwidth is 24 MHz and the phase margin 48°.

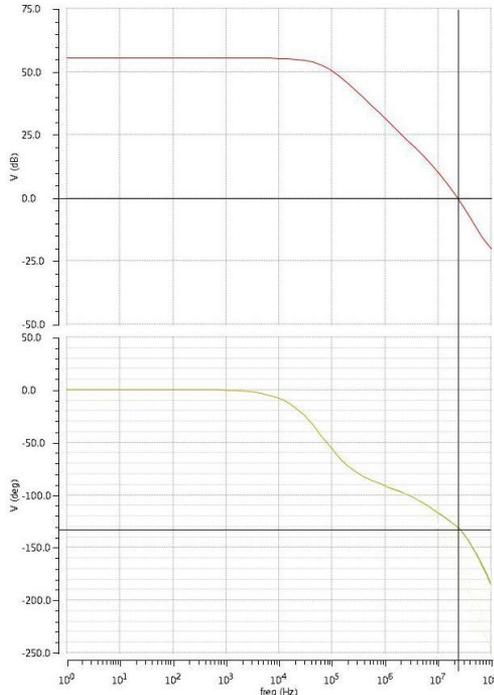


Fig 7.3: Gain and phase response of designed two stage opamp

7.4.2 Noise Analysis

The noise of an opamp is computed using the Noise analysis in ADE. Fig 7.5 shows the input referred noise voltage versus frequency plot of the designed opamp. The noise plot shows that the noise spectrum is dominated by flicker or $1/f$ noise.

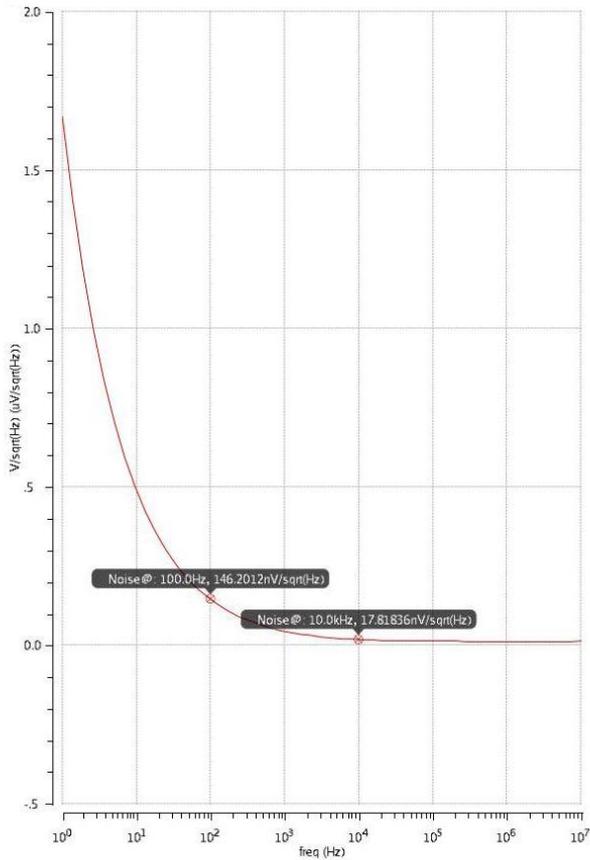


Figure 7.5 Noise spectrum of two stage opamp

Device	Param	Noise Contribution	% Of Total
/I0/PM2	fn	0.000781034	22.36
/I0/PM1	fn	0.000781003	22.36
/I0/NM4	fn	0.000766863	21.56
/I0/NM3	fn	0.000732583	19.67
/I0/PM2	id	0.000317008	3.68
/I0/PM1	id	0.000316996	3.68
/I0/NM4	id	0.000304743	3.40
/I0/NM3	id	0.000291121	3.11
/I0/PM5	fn	4.27241e-05	0.07
/I0/PM7	fn	4.1831e-05	0.06

Integrated Noise Summary (in V) Sorted By Noise Contributors
 Total Summarized Noise = 0.00165164
 Total Input Referred Noise = 3.22229e-06
 The above noise summary info is for noise data

Figure 7.6 Noise Summary of the two stage opamp

Fig 7.6 shows PreAmplifier's noise summary in which the flicker noise (fn) of input pair devices (PM1, PM2) and active load devices (NM3, NM4) are the major source of noise. Thermal noise (id) of the same transistors is also apparent with considerably less proportion. The total input referred noise which is integrated between 100 Hz to 10 KHz can be computed as follows;

$$\text{Total noise} = 20 * \log(3.2229 * 10^{-6}) = -109 \text{ dB}$$

The total input referred noise (-109 dB) is reached by iteratively reducing the flicker noise of input pair devices (PM1, PM2) and the active load devices (NM3 and NM4). The opamp is main source of noise in the PreAmplifier design.

7.4.3 XF Analysis

The PSRR of the opamp is computed by performing XF analysis (transfer function analysis) in ADE. The XF analysis is a very handy analysis which enables the designer to compute the transfer function of a system from the output to any input in the system. The PSRR is actually the inverse of the transfer function from the output node of opamp to the power supply voltage VDD. The measured value of PSRR of the designed two stage opamp is 45 dB in the frequency range from 1 to 10 KHz.

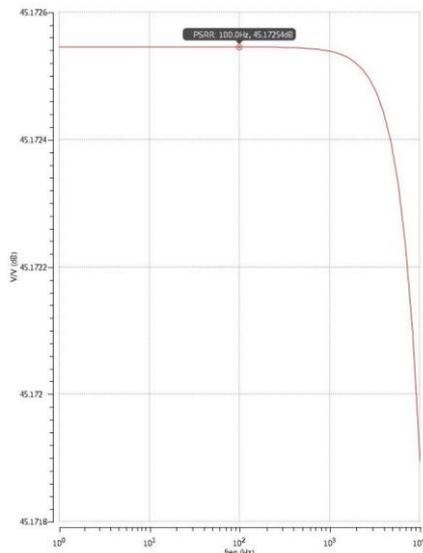


Figure 7.8 PSRR plot for the two stage opamp

7.5 Summary

A two stage opamp has been specified, designed using g_m/I_d methodology and is characterized by performing different simulations. Table 7.3 summarizes the specified and a simulated value of the designed opamp which tells that the designed opamp meet the specifications with a need to improve its phase margin. The simulated values of noise and PSRR are the result of iterative modifications of the transistor dimensions and other parameters. It can be deduced in the light of this discussion that the designed two stage opamp can be used in the PreAmplifier. In the next chapter all the ideal components in the PreAmplifier design will be replaced by their real counterparts and simulation are performed to characterize the PreAmplifier.

TABLE 7.3: TWO STAGE OPAMP RESULTS AND SPECIFICATIONS

Parameter	Specified Value	Simulated Value
Gain (dB)	> 50	54
Phase Margin (°)	60	48
Unity Gain Bandwidth (MHz)	25	23
Current Consumption (μ A)	28	27.5
Input referred integrated Noise (100 Hz to 10 KHz)	--	-109 dB
PSRR	--	45 dB
$C_L = 1\text{pF}, C_c = 500\text{fF}$		

CHAPTER 8

8 System Integration and Simulation Results

8.1 System integration

The test-bench for PreAmplifier schematic model is shown in fig 8.1. It is similar to the test-bench used for system model simulation as shown in fig 3.2. The difference here is that the ideal components are replaced by their real counterparts. The feedback resistor R_f has been replaced by its switched capacitor implementation and ideal feedback capacitor C_f is replaced by equivalent MIM capacitor. In $C_{varicap}$ all the ideal capacitors are also replaced by their equivalent MIM capacitors and the ideal switches are replaced by NMOS transistors. Two new input voltages source (vpulse) i.e. V_{phase1} and V_{phase2} are added to provide phase signals to the switched capacitor resistor. The amplifier is replaced by the 2 stage opamp designed in the previous chapter.

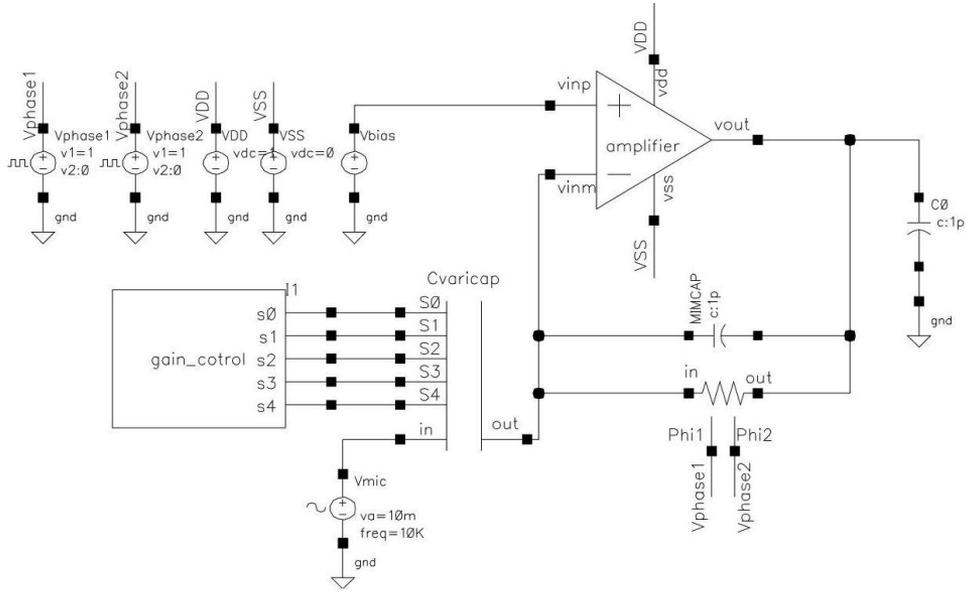


Fig 8.1 Test-bench schematic of PreAmplifier's schematic Model

8.2 Simulation Results

This section shows different simulation results i.e. closed loop gain, noise, PSRR and THD to characterize the PreAmplifier. Table 8.1 summarizes and compares PreAmplifier simulated results with the specified value in table 1.1. A very brief procedure to set up each of these simulations in Analog Design Environment (ADE) IC6.1.5, and the discussion about their results are described in the following sub-sections;

8.2.1 Closed Loop AC gain

Normal AC analysis, as used in PreAmplifier’s system model simulations, cannot be used to evaluate the gain response of PreAmplifier’s schematic model which includes a switched capacitor circuit. For this purpose PSS (periodic steady state) analysis is performed which, as the name suggests, can compute the steady state of a switched capacitor circuit based on a periodic stimulus. Once the steady state is computed other analysis like PAC (periodic ac analysis) is performed to compute gain and many other parameters which characterize an amplifier. Fig 8.2 shows the results of PAC analysis which are performed once the PSS has converged to steady state.

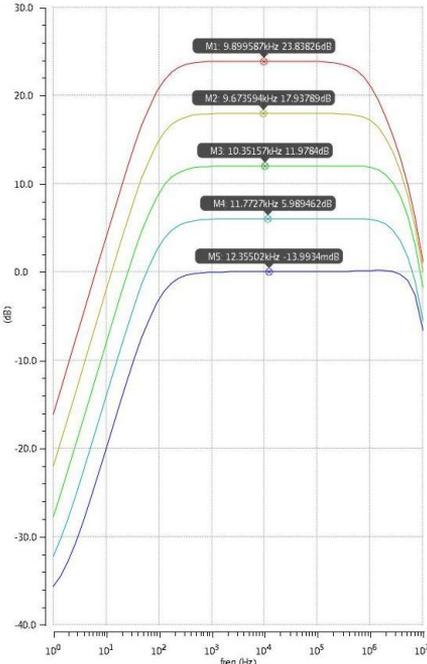


Fig 8.2 PreAmplifier’s Closed loop gain versus frequency

The simulation results in fig 8.2 shows that PreAmplifier is capable to vary the closed loop gain A_v with less than 1% variation from the specified value. The gain variation is specifications needed for the PreAmplifier which can be fulfilled by this suggested approach.

8.2.2 Noise

Noise of PreAmplifier is computed using PSS analysis followed by PNOISE analysis in ADE. Fig 8.3 shows PreAmplifier's input referred noise versus frequency plot wherein it can be inferred that the noise spectrum is dominated by flicker or $1/f$ noise.

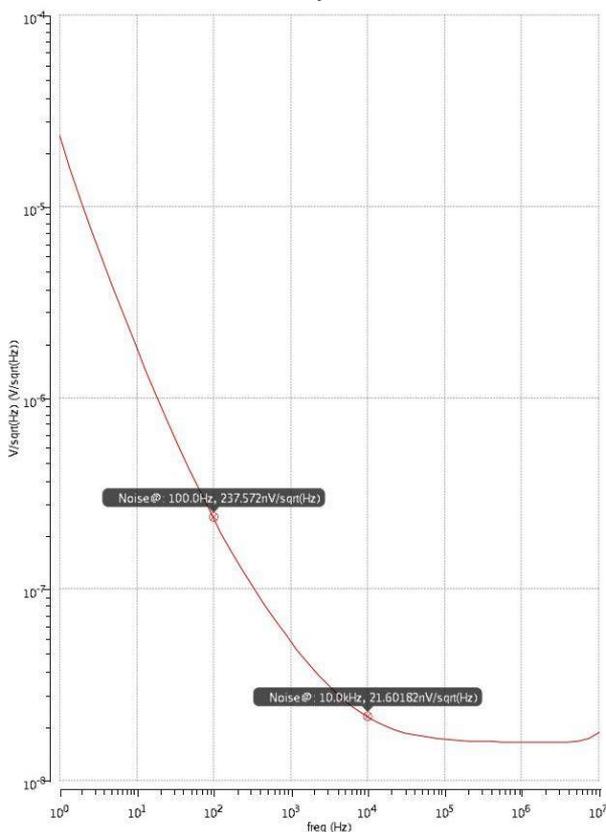


Fig 8.3 PreAmplifier's Noise Spectrum

Fig 8.4 shows PreAmplifier's noise summary in which the flicker noise (fn) of input pair devices (PM1, PM2) and active load devices (NM3, NM4) is the major source of noise. Other noise sources include gate induced noise

(igs and igd) and thermal noise (id) which are apparent due to presence of high feedback resistance. The input referred noise which is integrated between 100 Hz to 10 KHz can be computed as follows;

$$\text{Total noise} = 20 * \log(4.0037 * 10^{-6}) = -107 \text{ dB}$$

Device	Param	Noise Contribution	% Of Total
/I29/PM1	fn	2.46628e-05	17.36
/I29/NM4	fn	2.43907e-05	16.98
/I29/NM3	fn	2.33404e-05	15.55
/I29/PM2	fn	2.33397e-05	15.55
/I29/PM1	igs	1.88794e-05	10.17
/I29/PM1	igd	1.17828e-05	3.96
/I29/PM1	id	1.08846e-05	3.38
/I27/I3/M0	id	1.08355e-05	3.35
/I29/PM2	id	1.0297e-05	3.03
/I29/NM4	id	1.02245e-05	2.98

Integrated Noise Summary (in V) Sorted By Noise Contributors
 Total Summarized Noise = 5.91899e-05
 Total Input Referred Noise = 4.00037e-06
 The above noise summary info is for pnoise data

Fig 8.4 PreAmplifier's Noise Summary

8.2.3 PSRR

Power supply rejection ration (PSRR) of PreAmplifier is computed using PSS analysis followed by PXF analysis in ADE. Fig 8.5 shows the PreAmplifier's PSRR versus frequency plot. The plot shows that PreAmplifier is unable to meet the PSRR specifications in the entire specified bandwidth i.e. 100 Hz to 10 KHz. The PSRR of an amplifier is topology dependent and a two stage operational amplifier is not famous to give good PSRR. So the PreAmplifier in the suggested implementation needs to make a trade between PSRR and the input/output dynamic range available in the power supply voltage of 1V.

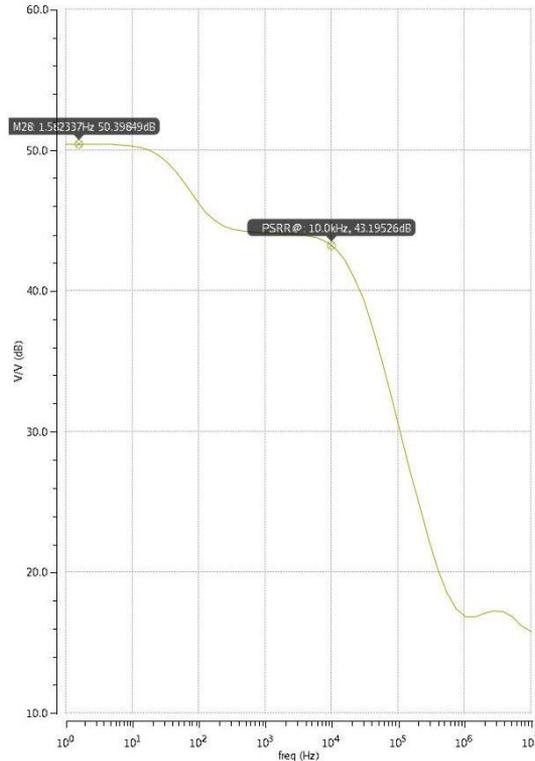


Fig 8.5 PreAmplifier's PSRR simulation results

8.2.4 Transient response

The transient analysis in ADE for the PreAmplifier's schematic model is set in the same way as in system model simulations. The time duration for transient simulation is set to be 50msec in order for the PreAmplifier to reach steady state. Fig 8.6 shows transient response of the PreAmplifier wherein the input signal V_{mic} and the output signal V_{out} are plotted against time axis. The gain of the PreAmplifier is configured to be 24dB. The result of this analysis is used to compute the THD of PreAmplifier which is discussed in the next sub-section.

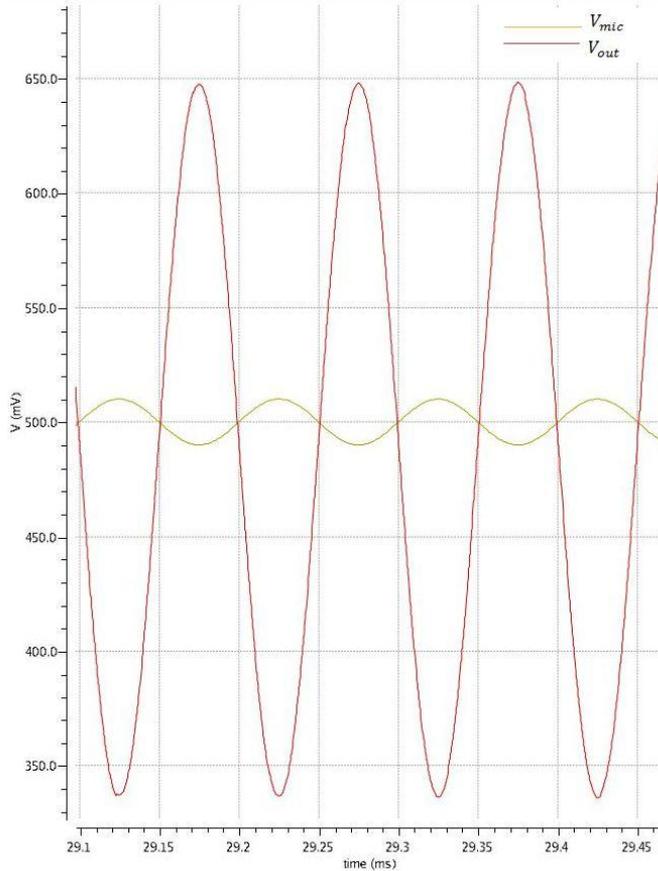


Fig 8.6 PreAmplifier's transient simulation results

8.2.5 THD

The THD of the designed PreAmplifier is computed using THD function of calculator. The function mainly needs integer number of periods (taken as between 40msec to 41msec) of the output signal and number of samples (i.e. 1024) to calculate THD. The THD function give output in percentage and for the designed PreAmplifier it gives 4.05m %. THD in dBs can be computed as follows;

$$\text{THD} = 20 * \log(4.05m / 100) = -87dB$$

So THD of the designed PreAmplifier is actually better than the specified value of -60dB. But it is important here to see the output voltage spectrum of the PreAmplifier. In this regard PSS analysis is performed specifying 50 harmonics of the beat frequency which is the average of all tones in the

test-bench. Figure 8.7 shows the output voltage spectrum of the designed PreAmplifier.

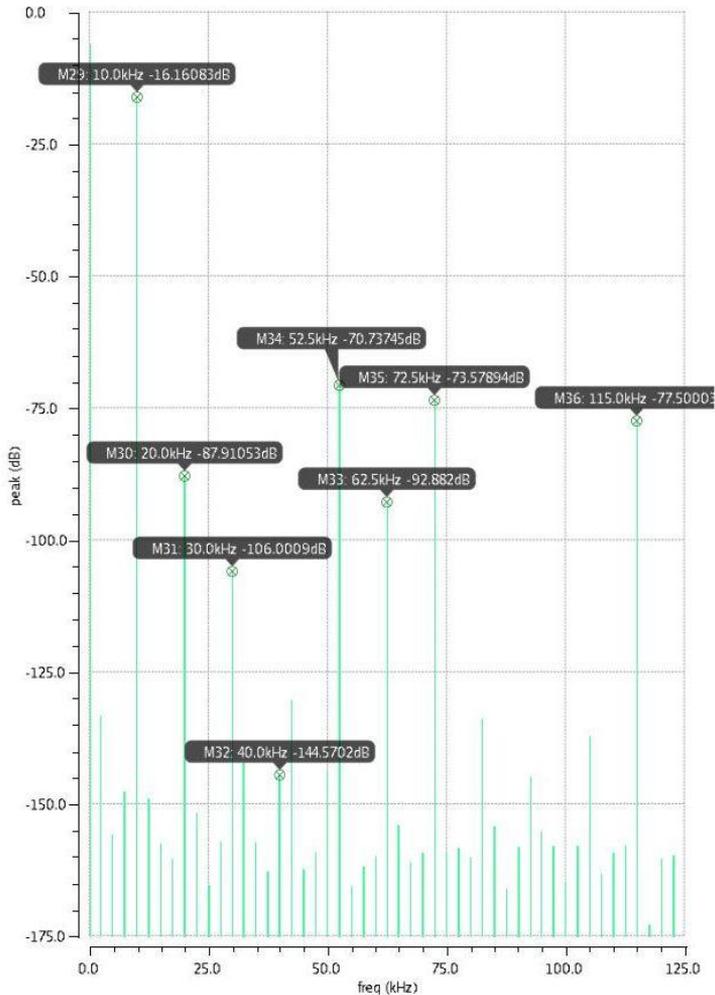


Fig 8.7 Output voltage spectrum of PreAmplifier

The voltage spectrum in the above figure shows many undesired tones i.e. the tones the switched capacitor resistor (62.5KHz) as well as their intermeditation with the input signal tone (10KHz). This situation is unavoidable as the frequencies of phase signals cannot be increased because in that case the capacitor (C) in the SC resistor needs to be reduced which is not possible. So this is actually a trade-off between linearity, noise and DC offset of the PreAmplifier.

8.3 Summary

In this chapter simulation results which characterizes the PreAmplifier has been presented. Table 8.1 summarizes the simulated results and compares them with the specified values. The closed loop gain of the PreAmplifier meets the specification with less than 1% variations. The noise of the PreAmplifier is almost 3dB higher than the specified value and can be improved by making the width of transistors PM1, PM2 and NM1 and NM2 as wide as possible. The PreAmplifier is not able to match up the PSRR specification in the entire specified bandwidth. The THD of PreAmplifier is actually higher than the specified value but the output voltage spectrum of is affected by the tones of SC resistor. The constraint area cannot be fulfilled with capacitive approach as the approximated area required is around $250\mu\text{m} \times 250 \mu\text{m}$. Based on the results summarized in the table below, the suggested implementation of PreAmplifier design doesn't fulfill all of the requirements.

TABLE 8.1: SUMMARY OF SIMULATION RESULTS FOR THE PREAMPLIFIER

Parameter	Specified value	Simulated value	Unit	Status (Fulfilled/ Not Fulfilled)
Gain	0-24	Less than 1% variation	dB	Fulfilled
Noise	-110	-107	dB	Almost fulfilled
PSRR (0 to 10 KHZ)	-50	-45	dB	Not fulfilled
THD	-60dB	-87	dB	Fulfilled
Current consumption	28	32	μA	Almost Fulfilled
Area	0.1	250x250	μm^2 mm^2	Fulfilled
CL = 1pF, T= 27 VDD= 1V				

9 Conclusion and Future Recommendations

Conclusions

A variable gain PreAmplifier with gain variations from 0 – 24 dB, in steps of 6 dBs, has been designed in 65nm CMOS technology. It has total input referred noise of -107dB, PSRR of 45dB (between 1Hz to 10 KHz), and THD of -87dB. The PreAmplifier can take up to 250 μ m x250 μ m of die area and has power consumption of 32 μ W. The PreAmplifier is unable to meet PSRR specifications. But the idea of gain variation of PreAmplifier by varying the capacitive ratio between the input capacitance and feedback capacitance has been successfully validated.

Future Recommendations

The noise of the PreAmplifier can be improved by making the input transistor (PM1, PM2) and the active load transistor (NM3, NM4) bigger on the cost of more power consumption. The PSRR of the PreAmplifier is dependent upon the topology to implement the opamp. It can be improved by implementing the opamp using folded cascode or telescopic topology on the cost of reduced input/ out voltage swing.

The output voltage spectrum of the PreAmplifier can be improved by making the switched capacitor feedback resistor smaller and feedback capacitor bigger. The smaller switched capacitor resistor will have clock phases with higher frequencies and their tones will not appear in the output voltage spectrum. But this will definitely increase the total area required for the PreAmplifier.

References

- [1] W. Robert, M. Robert “Feedback network for High Gain Amplifier with Enhanced Bandwidth and Gain Control”, WO2007019509
- [2] H. Z. Hoseini, “Variable gain amplifier for suitable for gain scaling in an analogue-to-digital converter”, GA2464770-A
- [3] F. Pomata, A. Questa, “Variable gain and Low Noise Amplifier for Received Signal in Imaging Apparata”, US20020175752A1
- [4] “Verilog-A Language Reference Manual”, Open Verilog International, August 1996
- [5] Kenneth S. Kundert, “The Designer’s guide to spectre & spice”, Kulwer Academic Publisher, 1995
- [6] A. Tajalli, Y. Leblebici and E.J. Brauer, “Implementing ultra-high-value floating tunable CMOS resistors”, Electronic Letters Volume 44 No.5, February 2008
- [7] P. Kmon, A.U. Cracow, “Low-Power Low-Noise Versatile Amplifier for Neural Signal Recording”, International Conference on Signals and Electronic Systems, ICSES 2008
- [8] Phillip E. Allen “CMOS Analog Circuit Design, 3rd Edition”, Oxford University Press, August 2011
- [9] J. Karki, “Understanding Operational Amplifier Specifications”, Texas Instruments, Digital Signal Processing Solutions, April 1998
- [10] R. Hogervost, J. H. Huijsing, “Design of Low-Voltage Low Power Operational Amplifier Cells” Huijsing, Kulwer Academic Publisher, 1996
- [11] E. Räisänen-Ruotsalainen, K. Lasanen, J. Kostmovaara “A 1.2V Micropower CMOS Opamp with Floating-Gat input Transistors” IEEE Midwest Symposium on Circuit and Systems, 2000
- [12] S. Ardalan, K. Raahemifar, F. Yuhan, “Low Voltage Low Power Operational Amplifier”, IEEE Circuit and Systems, 2005
- [13] B. Balock, P. Allen, “Designing 1V Op Amps using Standard Digital CMOS technology”, IEEE Transaction on Circuit and Systems, 1998
- [14] K. Lasanen, E. Räisänen-Ruotsalainen, J. Kostmovaara, “A 1-V 5 μ W CMOS-Opamp with Bulk-Driven Input transistors ”, IEEE Midwest Symposium on Circuit and Systems, 2000
- [15] S. Chatterjee, Y. Tsvividis, P. Kinget, “A 0.5-V Bulk-Input Fully Differential Operational Transconductance Amplifier” ESSCIC 2004
- [16] B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill,
- [17] H. Daoud Dammak, S. Bensalem, S. Zouari, M. Loulou “Design of Folded Cascode OTA in Different Regions of Operation through gm/ID

Methodology”, International Journal of Electrical and Computer Engineering, 2008

[18] A. Tiwari, “Design of MOS Amplifier Using gm/id Methodology”, http://discovery.bits-pilani.ac.in/discipline/eee/agupta/microelectronic-circuits/spice-online/online-2/Gm_BY_ID_Methodology.pdf.

[19] F. P. Cortes, S. Bampi “MILLER OTA DESIGN USING A DESIGN METHODOLOGY BASED ON THE GM/ID AND EARLY-VOLTAGE CHARACTERISTICS: DESIGN CONSIDERATIONS AND EXPERIMENTAL RESULTS”

[20] F.P. Cortes, E. Fabris, S. Bampi, “Analysis and design of amplifiers and comparators in CMOS 0.35um technology” Microelectronics Reliability 44, 2004.

[21] D. **Stefanovic**, M. **Kayal**, “Structured Analog CMOS Design”, Analog Circuits and Signal Processing, 2009

[22] P. Gray, P. Hurst, S. Lewis, R. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley, February 2001

Appendix 1

A.1 Verilog-A scripts for an amplifier

```
// VerilogA for amp, opamp, veriloga
`include "constants.vams"
`include "disciplines.vams"
`define dB2dec(x) pow(10,x/20)
module opamp( vinp, vinm, vdd, vss, vout );
inout vinp,vinm,vdd,vss,vout;
electrical vinp,vinm,vdd,vss,vout;
real vouta;
parameter gain = 70 from (0:inf);
analog begin
vouta = `dB2dec(gain)*V(vinp,vinm);
if (vouta > V(vdd))
vouta = V(vdd);
else if (vouta < V(vss))
vouta = V(vss);
V(vout) <+ vouta;
end
endmodule
```

A.2 Verilog-A scripts for Gain Control Unit

```
// VerilogA for auxiliary, gainctrl, veriloga
`include "constants.vams"
`include "disciplines.vams"
module gainctrl(s0,s1,s2,s3,s4);
output s0,s1,s2,s3,s4;
electrical s0,s1,s2,s3,s4;

parameter gain = 24 from [0:24];
real vs0,vs1,vs2,vs3,vs4;
analog begin
if(gain == 0 )begin
vs0 = 1;
vs1 = 0;
vs2 = 0;
vs3 = 0;
vs4 = 0;
```

```
end
if(gain==6) begin
vs0 = 0;
vs1 = 1;
vs2 = 0;
vs3 = 0;
vs4 = 0;
end
else if (gain==12)
begin
vs0 = 0;
vs1 = 1;
vs2 = 1;
vs3 = 0;
vs4 = 0;
end
else if (gain==18)
begin
vs0 = 0;
vs1 = 1;
vs2 = 1;
vs3 = 1;
vs4 = 0;
end
else if (gain==24)
begin
vs0 = 0;
vs1 = 1;
vs2 = 1;
vs3 = 1;
vs4 = 1;
end
else
begin
vs0 = 1;
vs1 = 0;
vs2 = 0;
vs3 = 0;
vs4 = 0;
end
```

```
V(s0)<+ vs0;  
V(s1)<+ vs1;  
V(s2)<+ vs2;  
V(s3)<+ vs3;  
V(s4)<+ vs4;  
end  
endmodule
```