Master's Thesis

Multiple Supply Voltages in Digital Baseband

by

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Abstract

This thesis deals with low power research using low voltages. The special interest is to implement multiple supply voltages using a single supply voltage. The power consumption is reduced by reducing the operating voltage. A diode connected NMOS transistor is used for voltage scaling. The robustness and feasibility of the diode connected NMOS devices as a voltage converter is tested and analyzed.

As the operating frequency decreases the supply voltage required is decreased, making this scenario ideal for the requirement of multiple supply voltages. A typical case of digital baseband filtering with decimation stages is used for testing. Multiple diode connected NMOS transistors are implemented for generating multiple supply voltages to be used in baseband filtering stages. An approximate power saving of 75% is achieved from one stage to next stage and area of 70 μm^2 by using this novel technique. The ultimate aim is to implement a low cost circuit to provide multiple voltages for saving the power, whose power consumption itself is minimal.

Acknowledgments

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CHAPTER 1

1 Introduction

Saving energy and reducing power is a need in today's integrated circuits. With the increasing complexity of the digital designs, power and energy requirements are intended to increase. The VLSI designs are continuously shrinking in size, which requires the power consumption to be reduced. Using multiple supply voltages is an effective way to reduce the power consumption, since decrease in operating voltage drastically decreases power consumption. This causes the low power designs to translate into low voltage designs, where the lower supply voltages are becoming more significant.

To reduce the power consumption, the operating voltage needs to be brought down. This can be achieved by using multiple supply voltages based on single supply voltage. Scaling of supply voltage is usually done using conventional DC- DC converters, which are complex in design and in turn consumes power. Here is the need for a simple circuit for voltage scaling in place of DC-DC converter which reduces power consumed by voltage scaling. A diode connected NMOS devices causes the voltage to step down by an amount equal to its threshold voltage and this concept is used to implement the simple circuit for voltage scaling.

A typical case where multiple supply voltages can be implemented is digital baseband filtering along with decimation stages in between. Since its throughput and operating frequency is reduced at each stage, the supply voltage can be reduced for each stage.

1.1 Thesis outline

The outline of the remaining chapters is described below

Chapter 2 deals with the design overview giving a brief introduction to the topic.

Chapter 3 explains in detail the test setup implemented in the design to test the feasibility of diode connected NMOS devices as a voltage converter.

Chapter 4, the different circuits tested, final results and their analysis are discussed here.

Chapter 5 deals with a comparison of the thesis work with the similar prior works.

Chapter 6 deals with the conclusion, future work, and extension of the thesis.

CHAPTER 2

2 Design Overview

The purpose of the project is to do low power research by using the concept of multiple supply voltages. In a typical case of digital baseband filter with decimation stages in between, the throughput is reduced after each stage. With the reduced throughput and frequency the supply voltage required is further reduced. Here the digital baseband filtering is implemented using a wave-digital half-band filter, which is a third-order low-pass filter. A block diagram of a baseband filtering along with the decimation and clock divider required for down sampling is shown in Fig. 1.

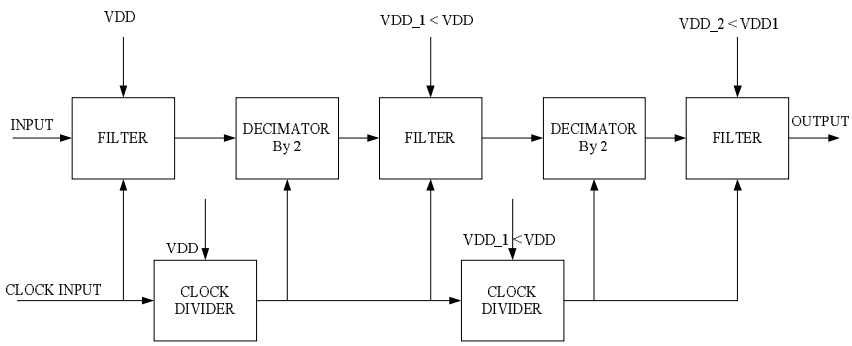

Figure 1. Multiple supply voltage in digital baseband filtering

As can be seen in Fig. 1, the supply voltage required for baseband filter decreases after each stage. The circuit requires the multiple supply voltages for its power efficient operation. The multiple supply voltages can be achieved with the single supply voltage and voltage scaling are done after each stage. This voltage scaling is intended to be achieved with the diode connected NMOS transistor.

2.1 Architecture

The detailed architecture of digital baseband filtering using multiple supply voltages is shown in Fig. 2. The circuit in Fig. 2 uses diode connected NMOS devices for voltage scaling.

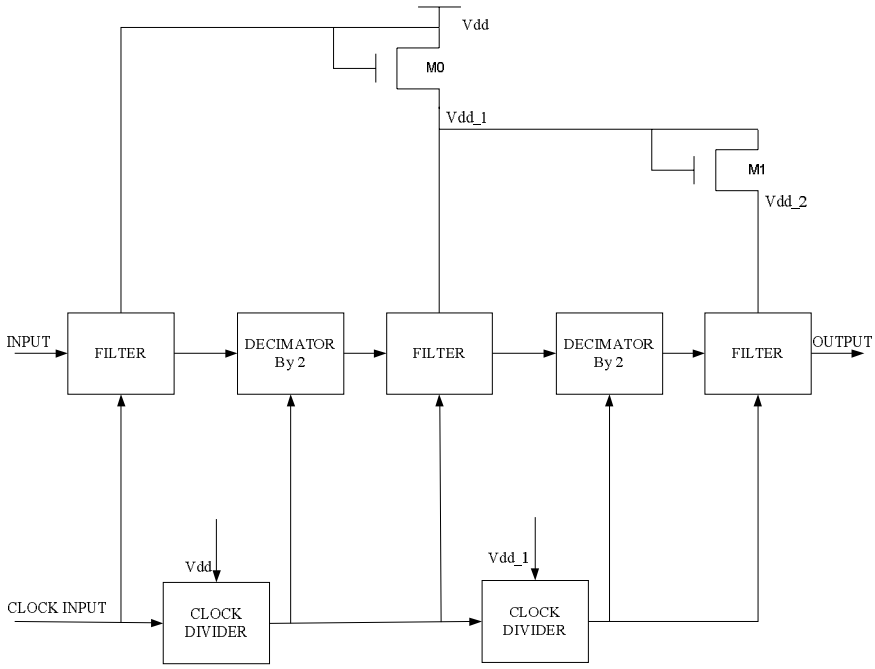

Figure 2. Diode connected NMOS devices for multiple supply voltage

The circuit consists of digital baseband filters which are third order wave-digital half-band filter, down sampler, clock divider, and diode connected NMOS.

2.1.1 Diode connected NMOS devices

A diode connected NMOS devices is used for voltage down conversion. The diode connected NMOS devices has the gate and drain terminals shorted to supply and bulk connected to ground. The circuit diagram of diode connected NMOS devices is shown in Fig. 3.

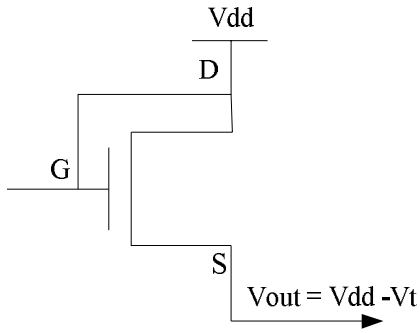

Figure 3. Diode connected NMOS devices

As can be seen in Fig. 3, the gate is shorted to the drain which is connected to supply voltage (V_{dd}) i.e. $V_G = V_D = 1.2$ V and the output voltage (V_{out}) is derived from the source terminal. The condition to keep the transistor ON is that V_{GS} should be greater than the threshold voltage (V_T). The condition is shown in (1).

$$V_{GS} > V_T \tag{1}$$

Since the gate and drain terminals are connected to supply which satisfies the condition for saturation as shown in (2), making the transistor to operate in the saturated region.

$$V_{DS} > V_{GS} - V_T \tag{2}$$

This makes the drain current (I_d) independent of V_{dd}. As the drain current starts flowing, the output voltage increases. The diode connected transistor qualitatively acts like as a diode, making the source voltage (V_{out}) lesser than drain voltage (V_{dd}) by an amount equal to threshold voltage (V_T). The output voltage (V_{out}) relation is shown in (3).

$$V_{out} = V_{DD} - V_T \tag{3}$$

This causes the supply voltage to step down by an amount equal to threshold voltage (V_T). In a typical case with supply voltage of 1.2 V, where threshold voltage is 0.3 V the output voltage (V_{out}) is equal to 0.9 V, which is 0.3 V lesser than V_{dd}. This behavior of diode connected NMOS devices which makes the supply voltage to step down by an amount equal to the

threshold voltage is used to scale down the voltage and create multiple supply voltages using single supply voltage.

2.1.2 Low pass filter

A third order wave-digital half-band filter performing a low-pass operation is used as the test load for different stages of multiple voltage supplies. A wave-digital filter (WDF) provides an approximately similar characteristic as that of their analog counterparts. However, WDF has the higher stability, compared to the analog filter and also provides a higher degree of parallelism that makes them suitable for hardware implementation [1]. The structure of the filter implemented is shown in Fig. 4.

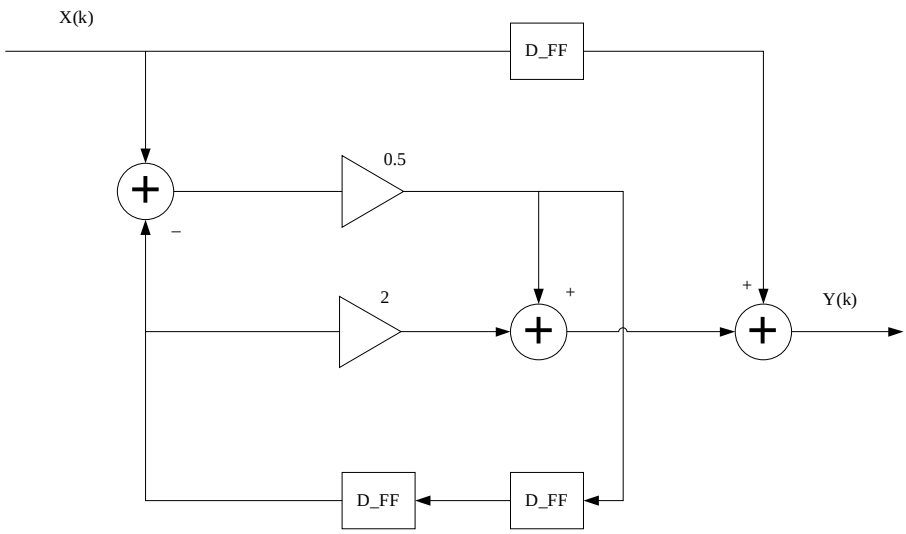

Figure 4. Half-band wave-digital filter

Another advantage of WDF in terms of implementation is that it can be implemented with simple shift and addition operations. The transfer function of the filter implemented in the Matlab is shown in Fig. 5 and the transfer function after adding the floor function to emulate the hardware counterpart is shown in Fig. 6. The floor function is added to represent hardware filter transfer function. As a filter designed in Matlab is ideal and has higher accuracy to represent filter co-efficient, whereas in hardware the co-efficient are represented in limited binary digits which reduces the accuracy. The impulse response of the implemented hardware filter is

evaluated and its transfer function is plotted in Fig. 7. It can be seen that Fig. 6 and Fig. 7 are equal and resembles the low pass filtering of WDF.

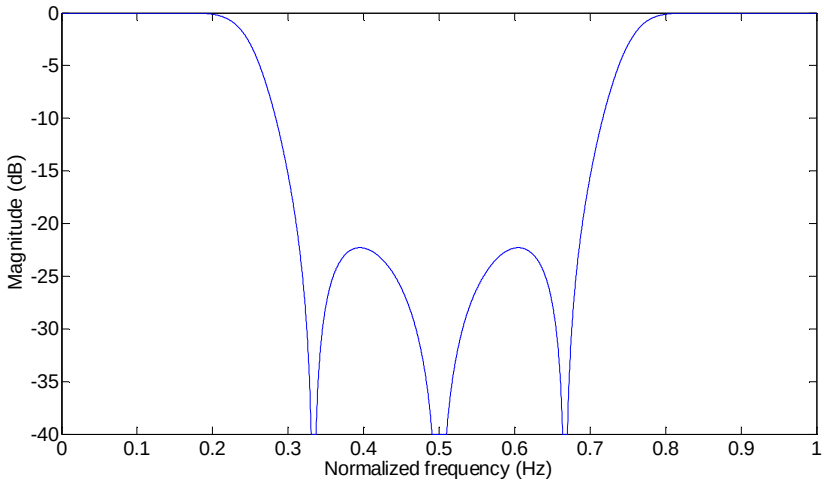

Figure 5. The transfer function of the WDF

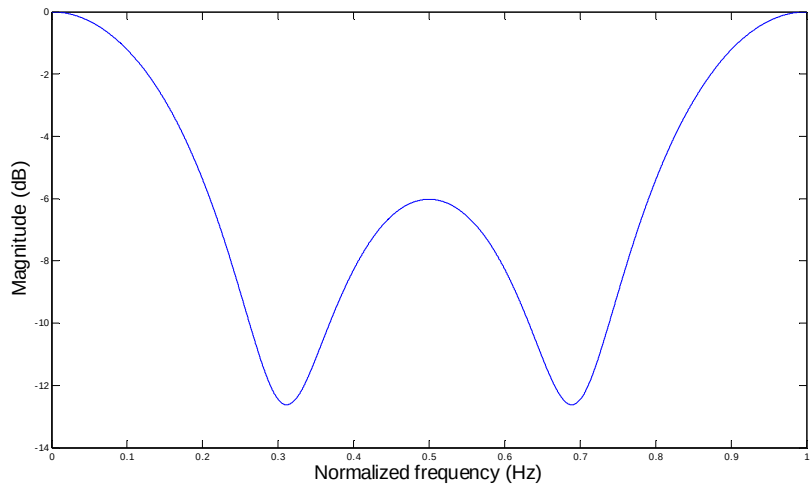

Figure 6. The transfer function of the WDF with floor function

The filter lowers the rate of sampling at each stage and thereby reducing the supply voltage required in the subsequent stages of the digital baseband filtering.

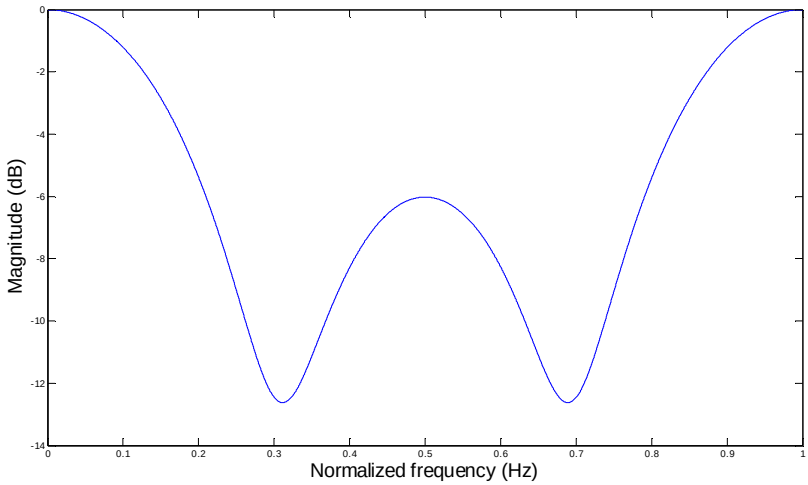

Figure 7. Hardware filter transfer function

2.1.3 Decimator

The decimation reduces the original sampling rate of the input digital signal. Decimation by a factor of 2 picks up every second sample of the digital input signal, causing the sampling rate to be reduced by 2. A conventional D flip-flop (D_FF) is used to implement the down sampler. The flip flop used as a decimator is shown in Fig. 8.

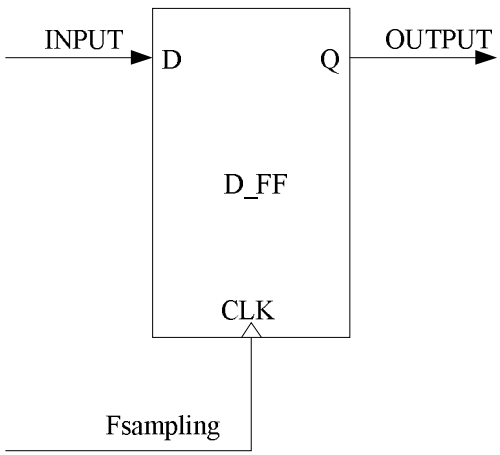

Figure 8. Decimator

As seen in the Fig. 8 a D flip-flop is used as a down sampler where, an input digital signal is fed as the input to the D flip-flop and down sampled signal is taken from output Q of the D flip-flop. The rate of the clock signal fed to the clock input is equal to the output sampling rate. For example, if the input rate is 32 MHz, which is intended to be down sampled by 2, i.e. the output rate will be equal to 16 MHz; the rate of clock signal fed is equal to 16 MHz.

2.1.4 Clock divider

A clock divider is used to down sample the clock signal by a factor of 2, as the clock frequency required for digital baseband filtering shown in Fig. 2 decreases by a factor of 2 for each stage. The clock divider is implemented using the D flip-flop and an inverter as shown in the circuit diagram in Fig. 9.

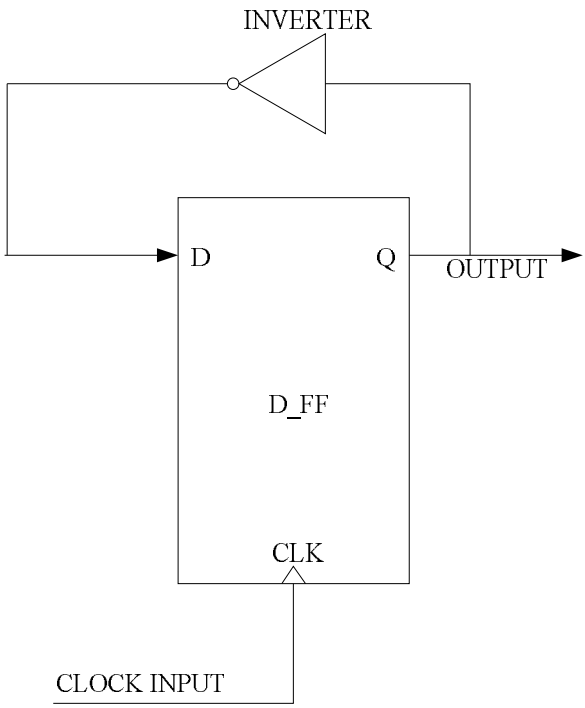

Figure 9. Clock divider

The clock signal to be divided is fed to clock input of the D flip-flop. The output of D flip-flop is fed back to the input through an inverter. The output

of the flip flop is also the output of the clock divider. This circuit makes the output clock frequency equal to half of the input clock frequency.

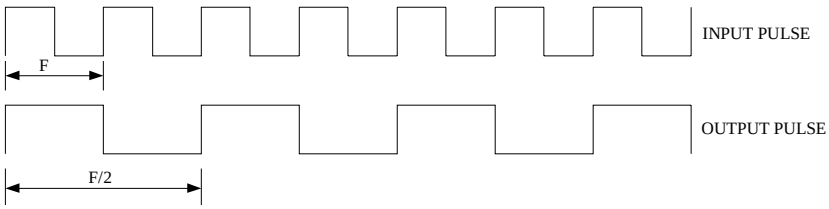

Figure 10. Waveform of clock divider

As can be seen from the waveforms shown in Fig. 10 that by connecting the output Q to input D through the inverter, the output pulses at Q has the frequency half that of input clock frequency. In other words the circuit acts as a clock divider that divides the input clock frequency by a factor of 2.

CHAPTER 3

3 Design implementation

The design is implemented using STM 65nm CMOS technology. Virtuoso schematic editor of Cadence is used for design entry and the simulation is done using virtuoso Analog design environment (Spectre). Wave-digital half-band filters in digital baseband filtering, used for testing multiple supply voltage scenarios are first implemented in Matlab to generate a golden reference output. The transfer function of the filter designed in the schematic is cross checked with the golden output. Voltage, current, power, and performance for the different tests performed are evaluated using virtuoso analog design environment.

3.1 Test setup

The ultimate aim is to test the feasibility of diode connected NMOS devices for voltage scaling used in a typical scenario which requires multiple voltages, such as digital baseband filtering as shown in Fig. 2. To begin with the tests, a smaller load when compared to low pass filter is used. Initially a cascaded chain of 2 inverters is used as a load to evaluate the different readings such as voltage, current and power. Different possible combinations of diode connected NMOS transistor, load capacitance, and inverter are tested for the best possible results. Different types of transistors are used as diode connected NMOS devices, such as HVTLP, SVTLP, and LVTLP. HVTLP NMOS transistor has high threshold voltage and low power, SVTLP NMOS transistor has standard threshold voltage and low power, and LVTLP NMOS transistor has low threshold voltage and low power. Results are also obtained for various widths of diode connected NMOS transistors. A load capacitance C_L is connected to the source of the diode connected NMOS devices, to charge to the output voltage level. The load capacitance and input frequency are also varied to obtain the different sets of results.

3.1.1 Inverter as a load

Initially, an inverter is used as a load for the diode connected NMOS transistor. Fig. 11 shows the circuit of a diode connected NMOS devices with the cascaded chain of inverters. Inverters are used as a load beginning from the cascaded chain of 2 inverters to the cascaded chain of 64 inverters.

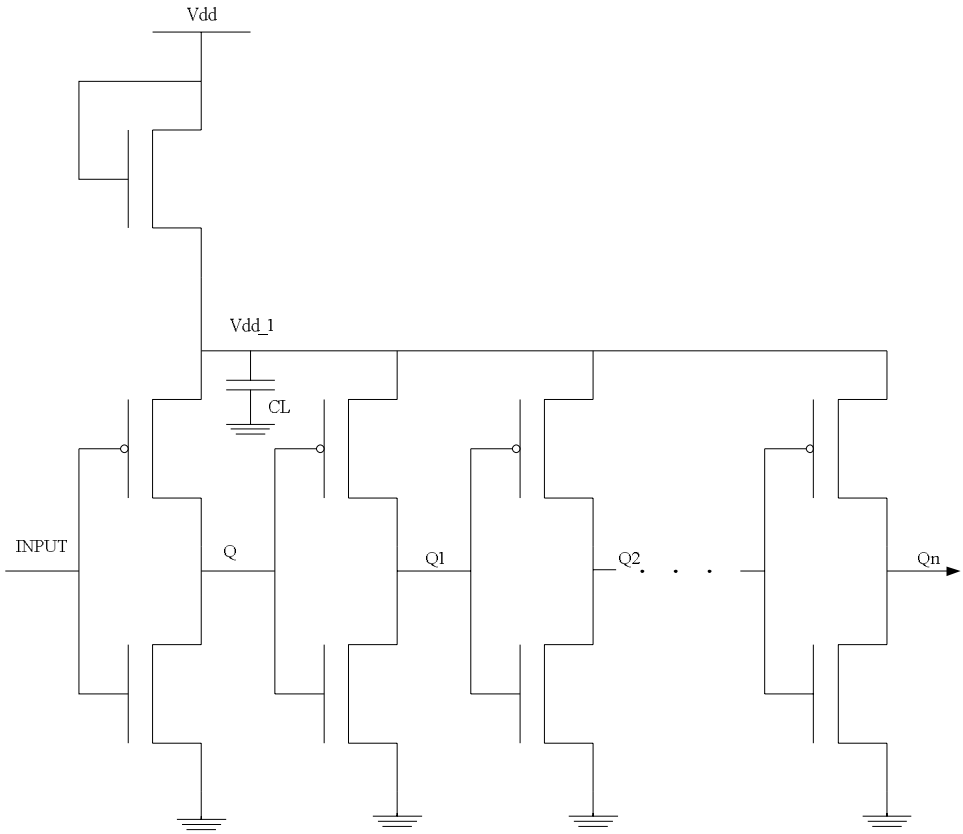

Figure 11. Diode connected NMOS devices with inverter as a load

3.1.2 Inverter

The circuit diagram of a static CMOS inverter is shown in Fig. 12. Its operation can be interpreted as that of a switch with infinite off resistance and finite on resistance. When the input voltage is high and equal to V_{dd}, the NMOS and PMOS transistors are on and off respectively. This creates a direct path from the output to ground, making the output voltage equal to 0 V. When the input voltage is low and equal to 0 V, the NMOS devices and PMOS transistors are off and on respectively. This creates a direct path

from the output to V_{dd}, making the output voltage equal to V_{dd}. For the low and high input, output is high and low respectively, thus the circuit in Fig. 12 perfectly functions as an inverter.

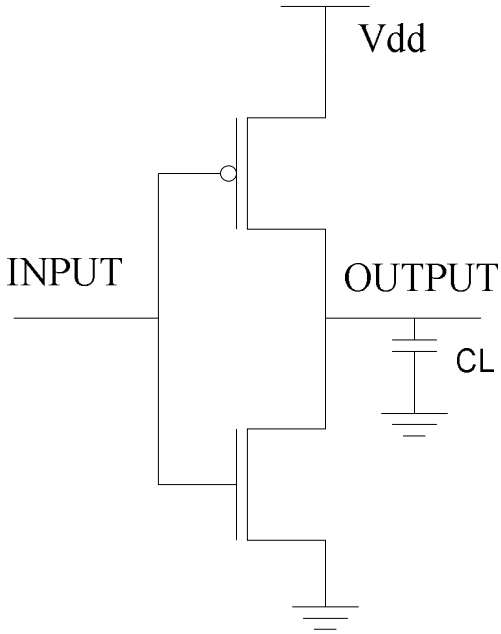

Figure 12. Inverter

Waveforms of the input and output, when a pulse is applied as an input are shown in Fig. 13.

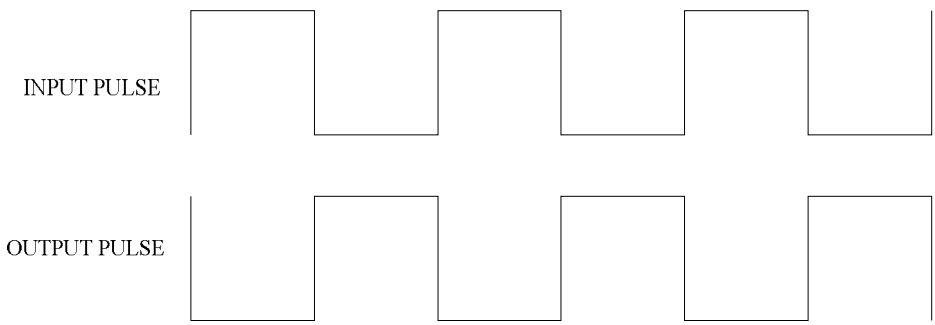

Figure 13. Inverter waveform

The high and low levels of the inverter are equal to the supply rails i.e. V_{dd} and *GND*. Since the input of the inverter is connected to the gates of the transistors, the input resistance of the inverter is extremely high. An

inverter has a high fan out and this fact is used in the testing of diode connected NMOS devices having chain of inverters as a load. [2].

3.2 Effect of parameters on step down voltage

Type of transistor, width of the transistor, chain of inverters used as a load, and input frequency are the various parameters that are varied. The response of the circuit in Fig. 11 for the variations in different parameters is tabulated and plotted for the analysis.

3.2.1 Type of transistor

LVTLP, HVTLP, and SVTLP are the various types of transistors used as a diode connected NMOS devices in Fig. 11, to find the amount of voltage scaled by the transistor. In this test a supply voltage (V_{dd}) of 1.2 V is used with the cascaded chain of inverters. Input applied to the chain of inverters is a pulse of 8 MHz and a load capacitance of 25 fF is connected. The output voltage V_{dd_1} is observed for each case of transistor and tabulated. The results are shown in table 1 and plotted in Fig. 14.

TABLE 1. STEP DOW VOLTAGE WITH TRANSISTOR TYPE

Transistor type	V_{dd} (V)	Voltage scaling (mV)	V_{dd_1} (mV)
LVTLP	1.2	250	950
SVTLP	1.2	320	880
HVTLP	1.2	450	750

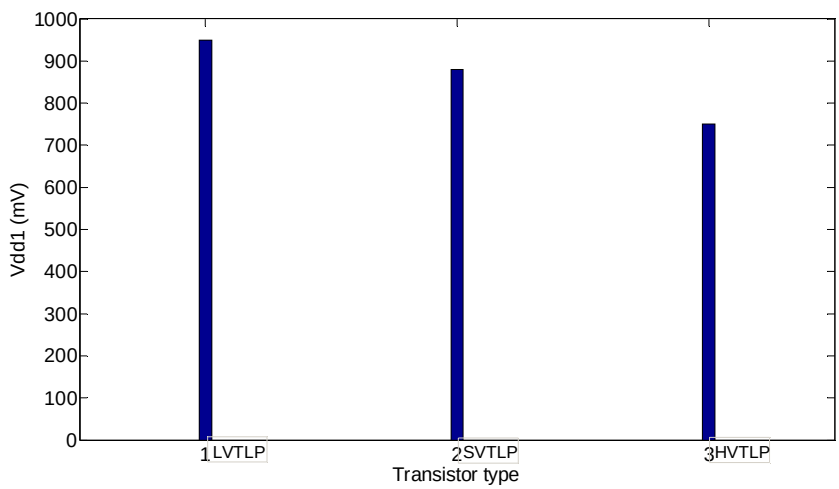

Figure 14. Variations with the transistor type

As shown in table 1 and in Fig. 14, HVTLP transistor provides the highest voltage drop of 0.45 V and LVTLP transistor provides the lowest voltage drop of 0.25 V, while SVTLP provides the voltage drop of 0.32 V. Depending on the voltage scaling requirement and the step down voltage required different transistor can be used.

3.2.2 Width of transistor

The circuit in Fig. 11 is used for testing diode connected NMOS devices with the chain of inverters as a load. The transistor type, input frequency, and chain of inverters are kept constant and width is varied by a factor of 10 from 0.135 µm to 135 µm and V_{dd_1} is evaluated for each case. The transistor type used is HVTLP, input frequency is set to 16 MHz, a load capacitance of 50 fF is connected, and chain of 2 inverters is used. The results are shown in table 2 and plotted in Fig. 15.

TABLE 2. STEP DOWN VOLGTAGE WITH TRANSISTOR WIDTH

Width (µm)	V_{dd} (V)	Voltage scaling (mV)	V_{dd_1} (mV)
0.135	1.2	455	745
1.35	1.2	430	770
13.5	1.2	370	830
135	1.2	300	900

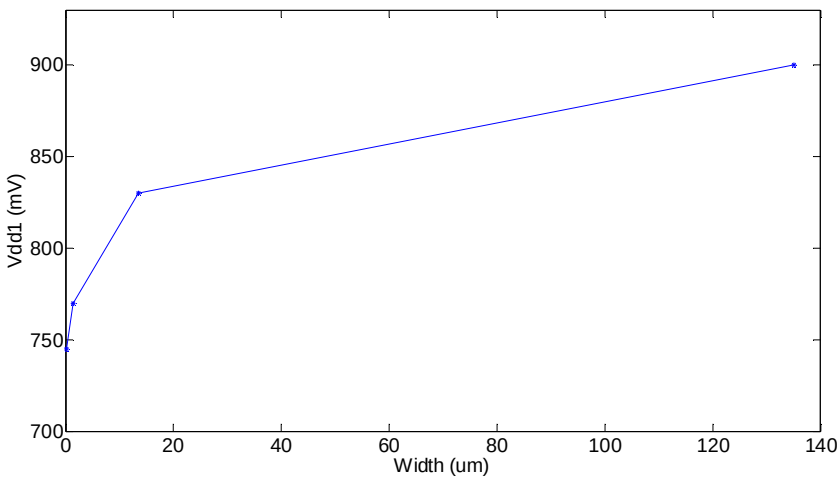

Figure 15. Variations with the transistor width

As can be seen from table 2 and Fig. 15, the step down voltage V_{dd_1} gradually increases with the width of the diode connected NMOS transistor.

This is due to the fact that the effective resistance of the transistor decreases with the increased width thereby causes the V_{dd_1} to increase. The choice of transistor type and transistor widths will thus give several degrees of freedom in the choice of the multiple supply voltages.

3.2.3 Input frequency

The input pulse of different frequencies is applied as the input to the inverter. In this test case the input frequency is varied from 1 MHz to 32 MHz in steps of multiples of 2, while keeping the other parameters constant. A HVTLP transistor is used as a diode connected NMOS transistor with the width of 13.5 µm, load capacitance of 50 fF, and chain of 2 inverters is used. The results obtained are shown in table 3 and plotted in Fig. 16.

The step down voltage V_{dd_1} decreases with the increase in the input frequency. With the increase in the input frequency, the ripple value in the step down voltage decreases causing the average or root mean square (RMS) value of the step down voltage to decrease. The reason for decrease in the ripple value is that with the increased frequency, the rate of capacitor charging and discharging increases causing the capacitor not to charge to the maximum value.

TABLE 3. STEP DOWN VOLTAGE WITH INPUT FREQUENCY

Input frequency (MHz)	V_{dd} (V)	Voltage scaling (mV)	V_{dd_1} (mV)
1	1.2	290	910
2	1.2	310	890
4	1.2	330	870
8	1.2	350	850
16	1.2	370	830
32	1.2	385	815

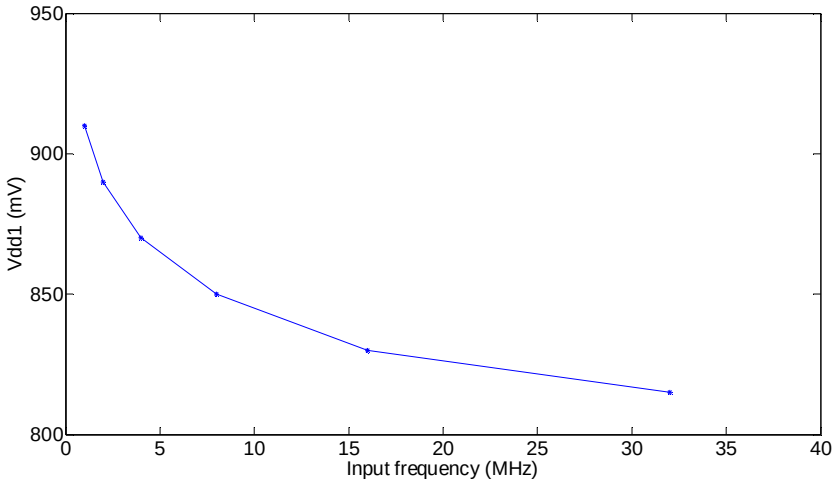

Figure 16. Variations with the input frequency

3.2.4 Chain of inverters

In this case the chain of inverters used as a load are varied from 2 to 64 in steps of power of 2 and the corresponding step down voltage is evaluated. The other parameters are kept constant. A HVTLP transistor is used as a diode connected NMOS devices with the width of 13.5 µm, an input frequency of 16 MHz is applied, and a load capacitance of 50 fF is connected. The results obtained with this setup are tabulated in table 4 and plotted in Fig. 17.

As depicted in the Fig. 17, the value of step down voltage decreases with the increase in chain of inverters connected as the load.

TABLE 4. STEP DOWN VOLTAGE WITH CHAIN OF INVERTERS

Chain of inverters	V_{dd} (V)	Voltage scaling (mV)	V_{dd_1} (mV)
2	1.2	370	830
4	1.2	385	815
16	1.2	405	795
32	1.2	430	770
64	1.2	430	750

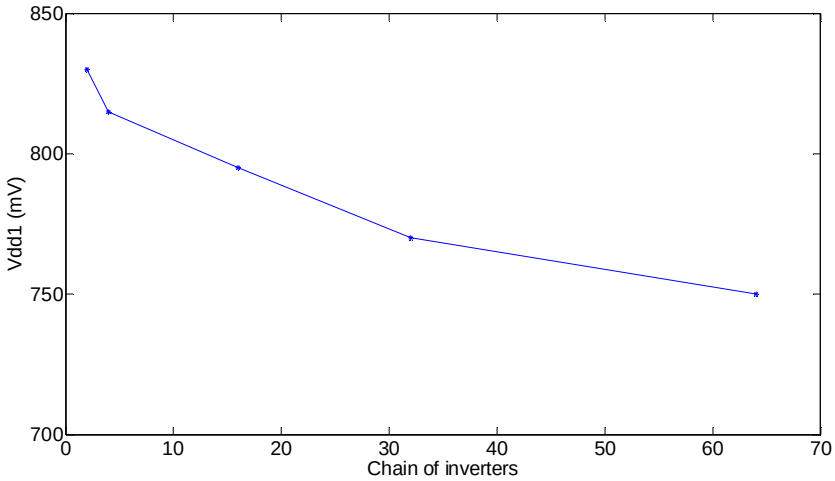

Figure 17. Variations with the chain of inverters

The reason behind the decrease in the step down voltage is that with the increase in the chain of inverters connected, the effective load resistance decreases, because the chain of inverters are connected in parallel as seen from the diode connected NMOS transistor. This causes the voltage at load to decrease.

3.3 Current, power, and efficiency

The same setup used for evaluating the effect of a chain of inverters on step down voltage is used to evaluate the current, power, and efficiency variations with the chain of inverters.

3.3.1 Current and power variations with the chain of inverters

The current drawn by the load and its variations for the change in the chain of inverters is evaluated. The results obtained are tabulated in table 5 and plotted in Fig. 18.

TABLE 5. LOAD CURRENT WITH CHAIN OF INVERTERS

Chain of inverters	Current drawn by the load (nA)
2	92
4	124
16	350
32	698
64	1140

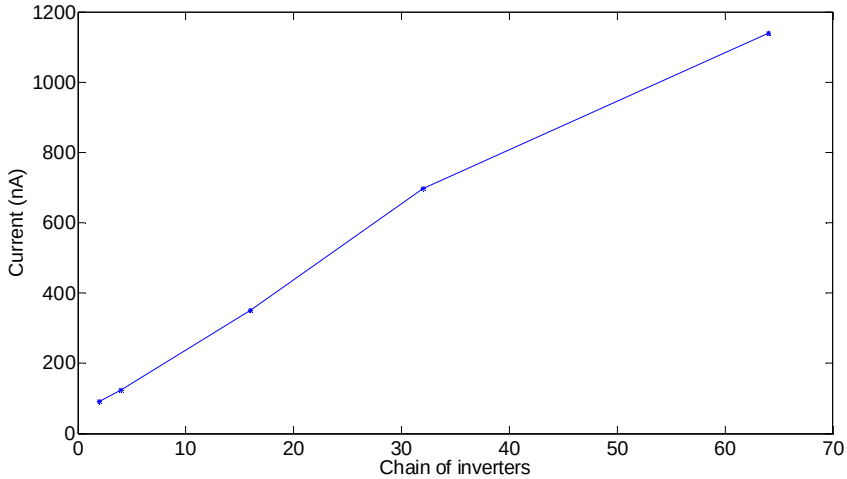

Figure 18. Variations in current with the chain of inverters

It is clear from the Fig. 18 that the current drawn by the load increases with the increase in the chain of inverters i.e. as the load increases the current drawn increases.

The power dissipated in the load (chain of inverters) and its variations with the increase in the chain of inverters is shown in table 6 and plotted in Fig. 19. As it can be observed in Fig. 19, the curve of power dissipated in the load is similar to that of the current drawn by the load. The power dissipated in the load is increasing with increase in the chain of inverters and it is obvious as the current drawn also increases with the chain of inverters.

TABLE 6. LOAD POWER WITH CHAIN OF INVERTERS

Chain of inverters	Power dissipated in the load (nW)
2	76
4	101
16	278
32	537
64	855

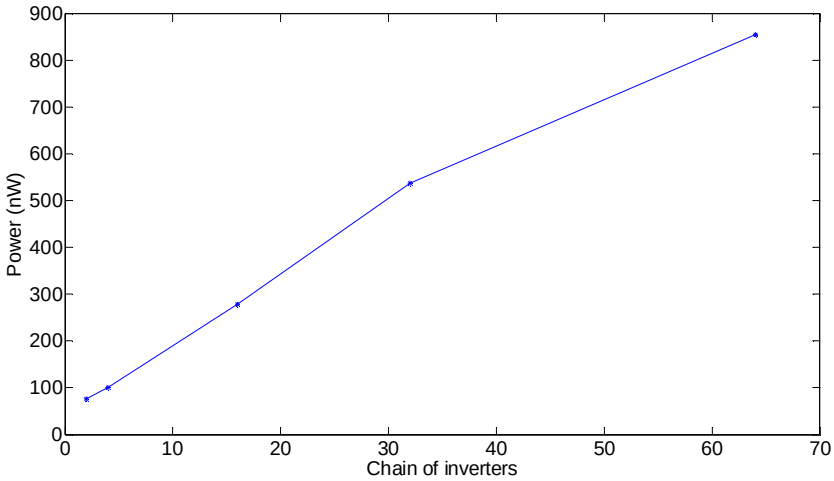

Figure 19. Variations in power dissipated in load with the chain of inverters

The power dissipated in the diode connected NMOS transistor, which can be seen as the power consumed by the voltage converter during the conversion is also evaluated. The variations in the power dissipated in the diode connected NMOS transistor with the chain of inverters is tabulated in table 7 and plotted in Fig. 20.

As it can be seen from the table 7 and Fig. 20, the power dissipated in the diode connected NMOS transistor increases with the chain of inverters. The shape of the curve in Fig. 20 is similar to that of Fig. 19 and Fig. 18 i.e. the curve of power dissipated in the diode connected NMOS transistor is the same as that of the current drawn by the load and the power consumed by the load. The power dissipated in the diode connected NMOS transistor is approximately 30 % to 40 % of the power consumed by the load.

TABLE 7. DIODE CONNECTED NMOS DEVICES POWER DISSIPATION WITH CHAIN OF INVERTERS

Chain of inverters	Power dissipated in the diode connected NMOS transistor (nW)
2	34
4	47
16	141
32	300
64	513

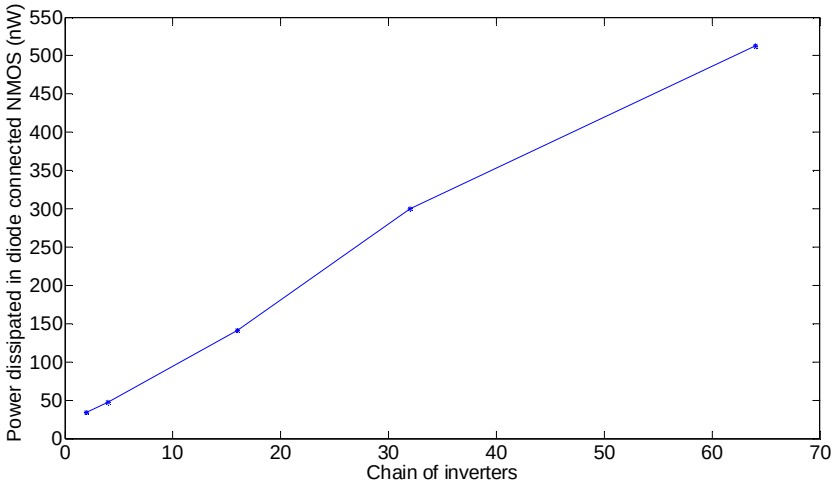

Figure 20. Power dissipated in diode connected NMOS transistor with the chain of inverters

3.3.2 Efficiency and its variations with the chain of inverters

The efficiency of a diode connected NMOS transistor used as a voltage converter is calculated. The efficiency calculation for a voltage converter is shown in (4).

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{4}$$

Where,
P_{OUT} = Power consumed by the load
P_{IN} = Power consumed by the load + Power dissipated in the diode connected NMOS transistor

The results obtained for the efficiency and its variations with the chain of inverters are tabulated in table 8 and plotted in Fig. 21.

TABLE 8. EFFICIENCY WITH CHAIN OF INVERTERS

Chain of inverters	Efficiency (%)
2	70
4	68
16	66
32	64
64	62

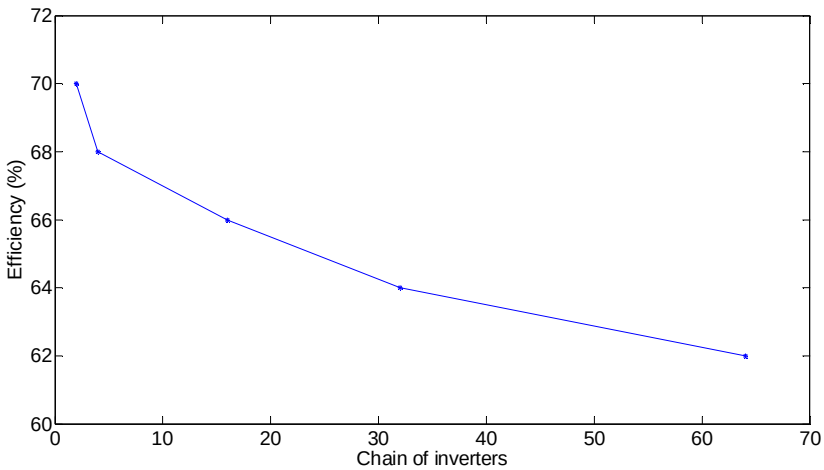

Figure 21. Efficiency and its variations with the chain of inverters

The efficiency of around 70 % is achieved for the case of chain of 2 inverters. It can be seen from the Fig. 21, the efficiency is gradually decreasing with the increase in the chain of inverters. As the load increases more current is drawn by the load which causes the amount of power dissipated in the diode connected NMOS transistor to increase, which has the effect of decreasing the efficiency.

CHAPTER 4

4 Results and analysis

Initially, diode connected NMOS devices were used for single step down of the supply voltage and this voltage was used for the case of chain of inverters. The effect of different parameters such as transistor type, transistor width, chain of inverters, and input frequency on the step down voltage was tested, whose results are tabulated and plotted in chapter 3.

Now the diode connected NMOS devices is used for stepping down the supply voltage for multiple steps. To begin with, the inverter is used as a load with the same input frequency for all stages. Then the output of each stage is decimated and applied as input to the next stage causing the operating frequency to decrease. Going forward, the inverter is replaced with the low pass filter, with the output of each filter stage decimated before connecting to the input of next stage. Then this circuitry is compared with the circuit having the ideal voltage supplies connected instead of step down voltage. In each case voltage, current, and power are evaluated and compared with the others.

4.1 Inverters as a load with same input frequency

The first test with the multiple voltage supplies is with the inverter as a load and same input frequency of 32 MHz, as beyond this frequency output gets distorted. The SVTLP transistor type is used as a diode connected NMOS devices. The reason for choosing the SVTLP transistor type is that, the HVTLP transistor type has higher voltage drop compared to SVTLP transistor type causing the step down voltage to be lesser than the required for higher loads. Load capacitance of 50 fF is connected. Width of the diode connected NMOS transistors is varied and its effect on the step down voltage, current, power, and efficiency is evaluated. The circuit diagram for the test is shown in Fig. 22.

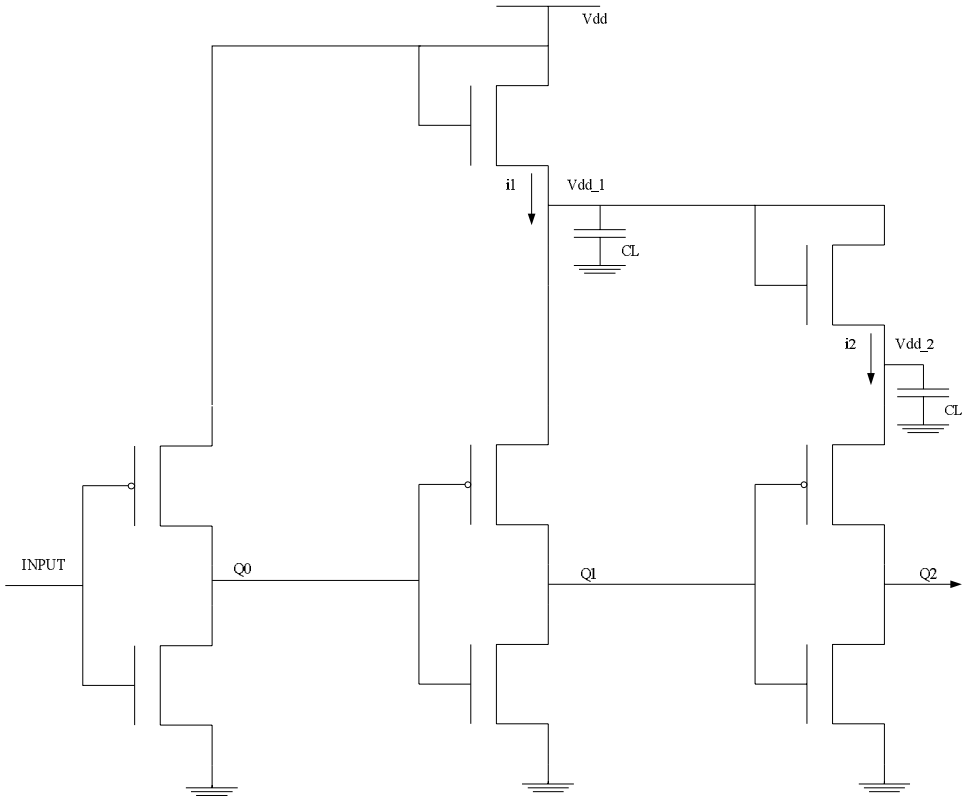

Figure 22. Inverter as a load with same frequency

The width is varied from 0.135 µm to 135 µm in steps of factor of 10. The first step down voltage (V_{dd_1}), second step down voltage (V_{dd_2}), current drawn by each inverter stage i_0, i_1, i_2, power consumed by each inverter stage p_0, p_1, p_2 and power dissipated in the diode connected NMOS transistors p_{t1}, p_{t2} are evaluated in each case.

4.1.1 Step down voltages

The step down voltages V_{dd_1} and V_{dd_2} and their variations with the width of the diode connected NMOS transistors are shown in table 9 and plotted in Fig. 23.

As can be seen from the table 9 and Fig. 23, the step down voltages V_{dd_1} and V_{dd_2} gradually increases with the width of the diode connected NMOS transistor. This is due to the fact that the effective resistance of the transistor decreases with the increased width thereby causes the step down voltages to increase.

TABLE 9. STEP DOWN VOLTAGES WITH THE WIDTH OF THE DIODE CONNECTED NMOS TRANSISTOR

Width (µm)	V_{dd} (mV)	V_{dd_1} (mV)	V_{dd_2} (mV)
0.135	1.2	756	408
1.35	1.2	773	431
13.5	1.2	834	554
135	1.2	905	662

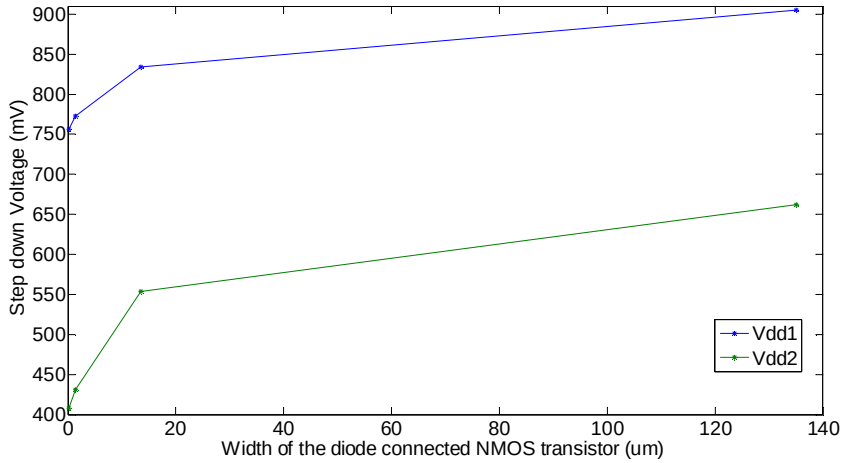

Figure 23. Step down voltages with the width of the diode connected NMOS transistors

4.1.2 Current drawn by the inverter stages

The current drawn by the first and second inverter stages having the step down voltages as the supply is evaluated, and its variations with the width of the diode connected NMOS transistor is tabulated in table 10 and plotted in Fig. 24.

TABLE 10. INVERTER CURRENTS WITH THE WIDTH OF THE DIODE CONNECTED NMOS TRANSISTOR

Width (µm)	i_1 (nA)	i_2 (nA)
0.135	32	6.5
1.35	38	11
13.5	85	55
135	270	240

In table 10, i_1 is the current drawn by the inverter stage using V_{dd_1} as the supply voltage, and i_2 is the current drawn by the inverter stage using V_{dd_2} as the supply voltage.

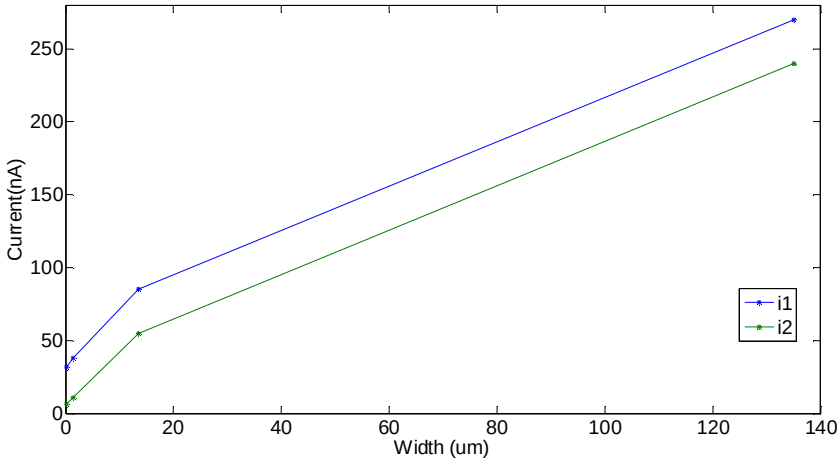

Figure 24. Inverter currents with the width of the diode connected NMOS transistors

As observed in the Fig. 24 the current drawn by the first and second inverter stage increases with the increase in the width of the diode connected NMOS transistor. This is obvious as the width of the diode connected NMOS transistor increases its effective resistance decreases causing the more current to flow.

4.1.3 Power consumed by the inverter stages

The power consumed by the first and second inverter stages having V_{dd_1} and V_{dd_2} as the supply voltage is evaluated and its variations with the width of the diode connected NMOS transistor are tabulated in table 11 and plotted in Fig. 25.

TABLE 11. INVERTER POWER CONSUMPTION WITH THE WIDTH OF THE DIODE CONNECTED NMOS TRANSISTOR

Width (µm)	p_1 (nW)	p_2 (nW)
0.135	24	2.5
1.35	29	5
13.5	71	32
135	242	161

In the table 11 p_1 is the power consumed by the first inverter stage i.e. the one having V_{dd_1} as the supply voltage, and p_2 is the power consumed by the second inverter stage having V_{dd_2} as the supply voltage.

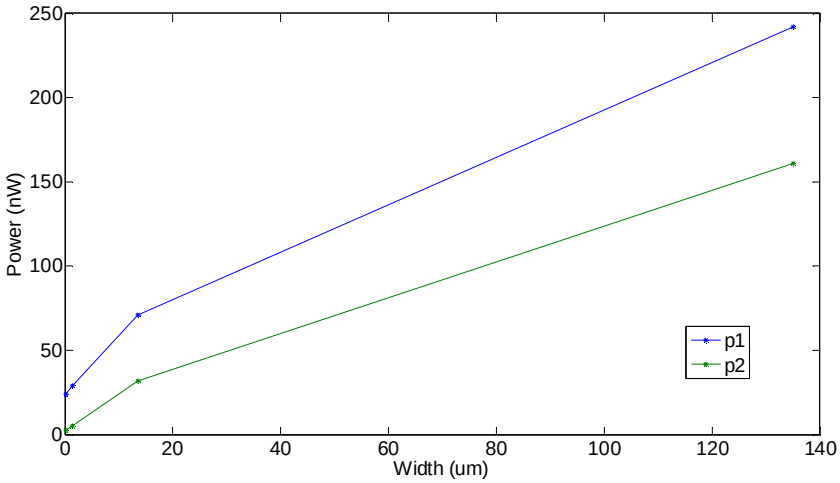

Figure 25. Power consumed by inverter stages with the width of the diode connected NMOS transistors

It is clear from the Fig. 25 that the power consumed by the load i.e. inverter increases with the width of the diode connected NMOS transistor. The power curve in Fig. 25 is similar to the current curve in Fig. 24. The increase in the power consumption with the increase in the width of the transistor is obvious, as both step down voltage and current drawn increases with increase in the width of the transistor.

4.1.4 Power dissipated in diode connected NMOS transistor

The power dissipated in the diode connected NMOS transistor, which its power consumed during the voltage conversion, is evaluated. The results obtained for the power dissipated in both the diode connected NMOS transistor and its variations with the width of the diode connected NMOS transistors are tabulated in table 12 and plotted in Fig. 26.

As it can be seen from the Fig. 26, the power dissipated in the diode connected NMOS transistor increases with the increase in the width of the transistor. The curve in Fig. 26, for the power dissipation in the diode connected NMOS transistor is similar to the curve in Fig. 25, for the power consumed by the load. The power dissipated in the diode connected NMOS transistor is around 30 % to 40 % of the power consumed by the load. Hence it can be said that a higher amount of power is delivered to the load and lesser power is wasted in the voltage conversion.

TABLE 12. POWER DISSIPATED IN THE DIODE CONNECTED NMOS TRANSISTORS

Width (µm)	p_{tr1} (nW)	p_{tr2} (nW)
0.135	14	2.2
1.35	16	3.7
13.5	31	15.4
135	79	58.3

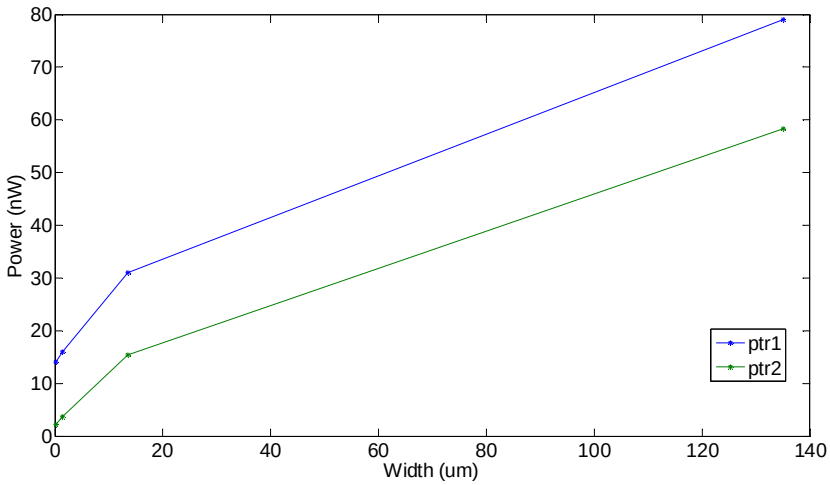

Figure 26. Power dissipated in diode connected NMOS transistor with the width of the transistor

4.1.5 Efficiency

It is desired that the all or the larger part of the input power is delivered to the load, and the lesser part of the input power is dissipated during the voltage conversion. This is effectively measured with the efficiency parameter. The efficiency calculation for a voltage converter is shown in (4). For the voltage converter implemented using a diode connected NMOS transistor to have higher efficiency, lesser amount of input power should be dissipated in the diode connected NMOS transistor and larger part of input power should be delivered to the load.

For the circuit in Fig. 22, where 2 diode connected NMOS transistors are used for stepping down the supply voltage in two steps, having inverter as a load with the same input frequency, efficiency of each diode connected NMOS transistor is evaluated as each is acting as a voltage converter. The results obtained and its variations with the width of the diode connected NMOS transistor are tabulated in table 13 and Fig. 27.

TABLE 13. EFFICIENCY OF EACH STAGE AND ITS VARIATIONS WITH THE WIDTH OF THE DIODE CONNECTED NMOS TRANSISTOR

Width (µm)	η_1 (%)	η_2 (%)
0.135	63	53
1.35	64	57
13.5	69	68
135	75	73

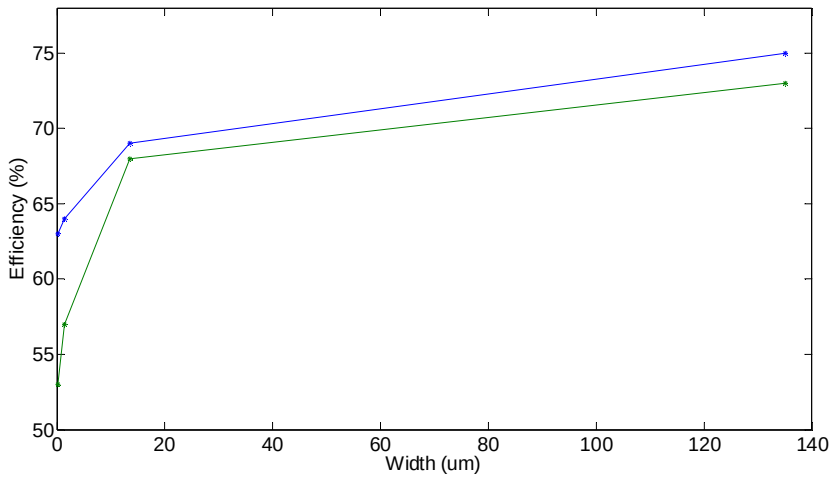

Figure 27. Efficiency and its variations with the width of the diode connected NMOS transistors

In table 13, η_1 is the efficiency of the first stage, and η_2 is the efficiency of the second stage. It can be seen from the table 13 and Fig. 27 that the efficiency is increasing with the increase in the width of the transistor. At higher widths of around 135 µm, around 75 % efficiency is achieved.

4.2 Inverters as a load with frequency scaling

In this case the inverter is used as a load with the output of each stage fed to the next stage after decimation. This causes the operating frequency to decrease by 2 after each stage. This frequency down conversion is done with the aid of a decimator and clock divider. The circuit diagram for the test circuit is shown in Fig. 28.

The SVTLP transistor is used as a diode connected NMOS transistor and the width chosen is 13.5 µm, based on the results obtained in chapter 3 and

chapter 4.1. The frequency of 32 MHz is applied as the input at the first stage, which is decimated by 2 at the output of each stage before going to the input of next stage. This makes the inverter at the input stage to operate at 32 MHz, first stage inverter to operate at 16 MHz, and the second stage inverter to operate at 8 MHz. As the operating frequency of each stage decreases the supply voltage required for its successful operation decreases, hence the reduced step down voltage is applied as supply at each stage. At each stage voltage, current, and power is evaluated and efficiency for each stage is calculated.

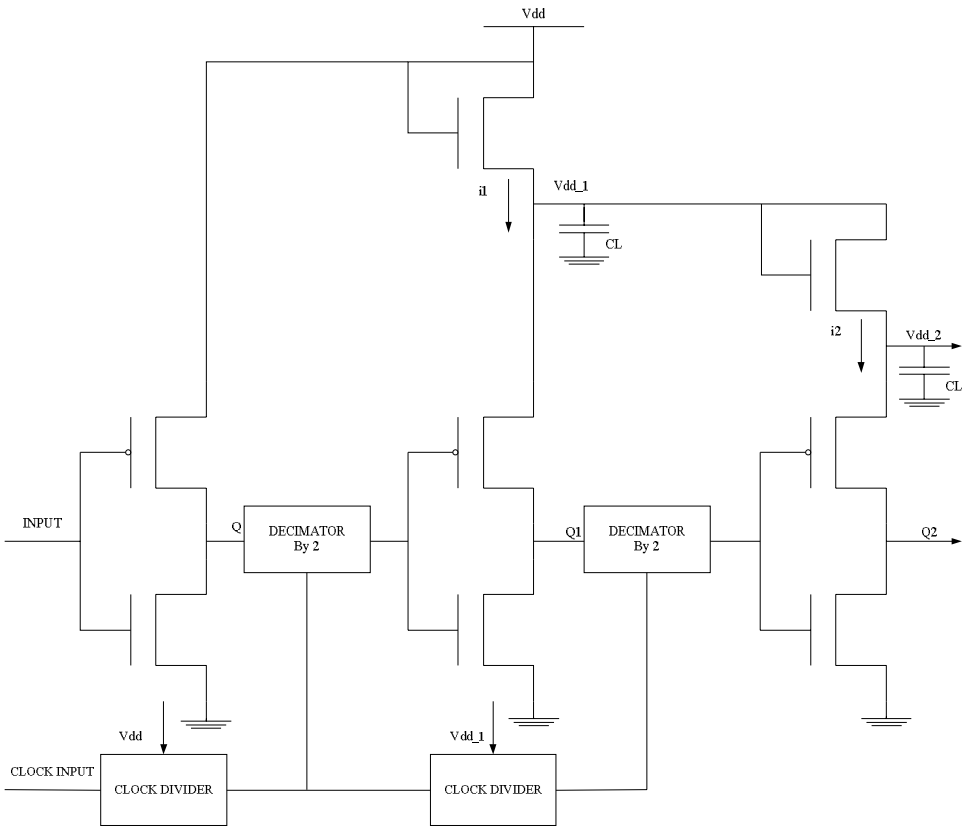

Figure 28. Inverter as a load with frequency scaling

4.2.1 Supply and step down voltages

The supply for each inverter stage along with its input frequency is tabulated in table 14 and plotted in Fig. 29. The input stage inverter has a

direct supply of 1.2 V, step down voltages V_{dd_1} and V_{dd_2} are connected as the supply to the first and second inverter stage respectively.

TABLE 14. SUPPLY VOLTAGE AND OPERATING FREQUENCY FOR INVERTER STAGES

Inverter stage	Input frequency (MHz)	Voltage (mV)
Input	32	1200
First	16	890
Second	8	630

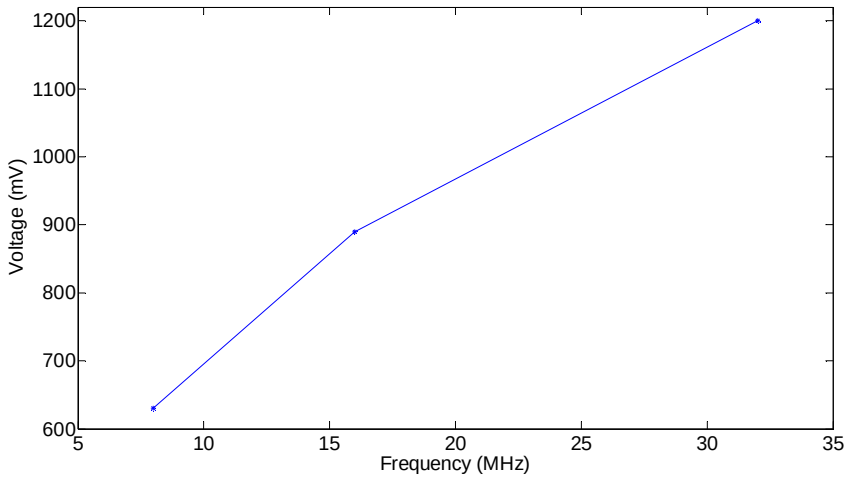

Figure 29. Supply voltage at each inverter stage with its input frequency

4.2.2 Current drawn by the load (inverter)

The current drawn by each inverter stage with respect to the input frequency of the stage are tabulated in table 15 and plotted in Fig. 30.

TABLE 15. CURRENT DRAWN BY THE LOAD

Inverter Stage	Input frequency (MHz)	Current (nA)
Input	32	1560
First	16	350
Second	8	150

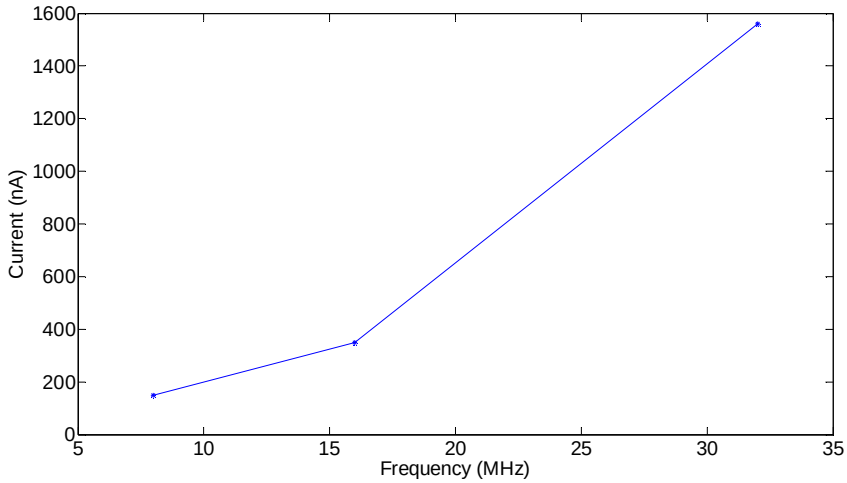

Figure 30. Current drawn by each inverter stage with its input frequency

The current drawn by the input inverter stage is higher when compared to the current drawn by the first and second inverter stage. This is shown in Fig. 30 as the function of the input frequency of the inverter stage. The current drawn by the each consecutive inverter stage is decreasing as the supply voltage for each stage is also reduced.

4.2.3 Power and energy consumed by the load (inverter)

The power and energy consumed by each inverter stage is tabulated in table 16 and table 17, and plotted in Fig. 31 and Fig. 32 respectively. Each inverter stage is represented by its input frequency.

TABLE 16.POWER CONSUMED BY THE LOAD (INVERTER)

Inverter Stage	Input frequency (MHz)	Power consumed by the load (nW)
Input	32	1870
First	16	312
Second	8	95

TABLE 17. ENERGY CONSUMED BY THE LOAD (INVERTER)

Inverter Stage	Input frequency (MHz)	Energy consumed by the load (fJ)
Input	32	58
First	16	19
Second	8	11

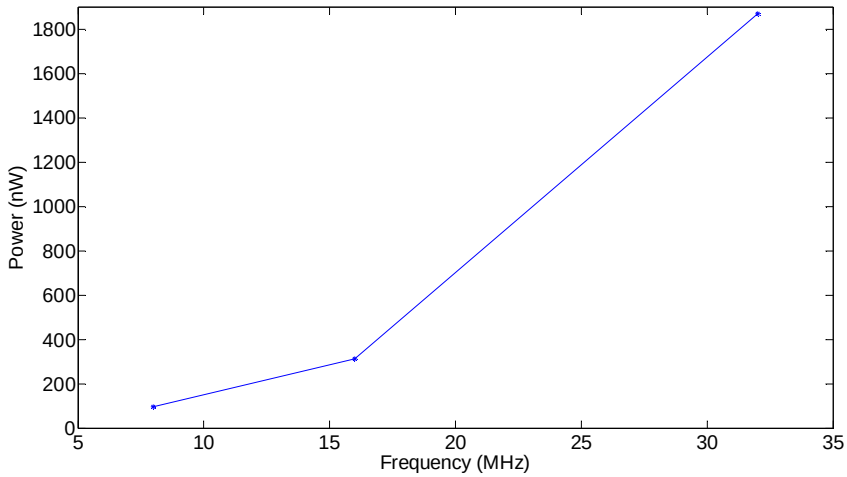

Figure 31. Power consumed by each inverter stage with its input frequency

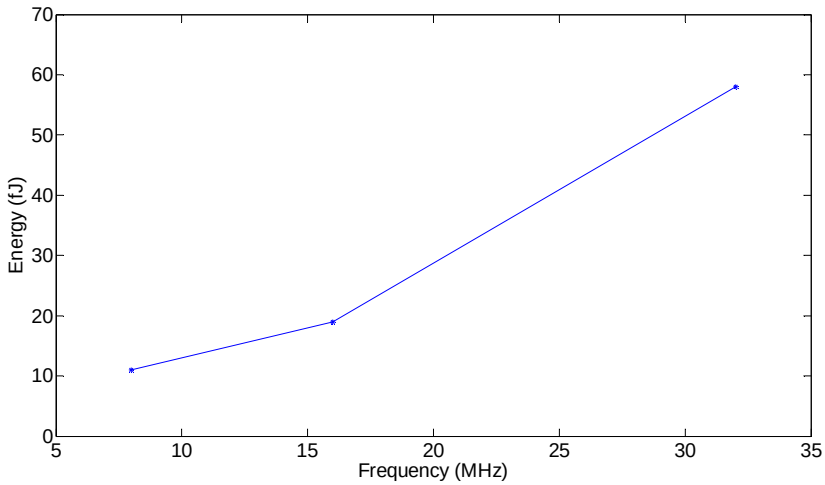

Figure 32. Energy consumed by each inverter stage with its input frequency

It can be observed from the Fig. 31 and Fig. 32 behavior of both power and energy curve is almost similar. The power and energy consumption is higher at input stage than the first stage followed by the second stage. This is obvious as the supply voltage and current for each consecutive stage decreases. Here it can be observed by using stepped down voltage for first stage and second stage inverters, the amount of power consumed and energy consumed for the respective stages considerably decreases when compared to the input stage having direct supply voltage.

4.2.4 Power dissipated in diode connected NMOS transistor and efficiency of each stage

Power dissipated in the diode connected NMOS transistors during the voltage conversion is shown in table 18 and the efficiency for each diode connected NMOS transistor as a voltage converter is shown in table 19.

TABLE 18. POWER DISSIPATED IN THE DIODE CONNECTED NMOS TRANSISTOR

Transistor	Power dissipated in diode connected NMOS transistor (nW)
1	155
2	39

TABLE 19. EFFICIENCY OF THE VOLTAGE CONVERTER

Stage	η (%)
1	67
2	70

The power dissipated in the first stage diode connected NMOS transistor is higher than the power dissipated in second stage diode connected NMOS transistor. This is obvious as the first stage has higher supply voltage and draws higher amount of current when compared to the second stage. Efficiency of the second stage is higher in this case when compared to the efficiency of the first stage. This can be attributed to the fact that second stage is operating at lower frequency.

4.3 Low pass filter as a load

In the section 4.2 the variations in step down voltage, current, and power are evaluated and plotted with inverters as a load. In this section inverters as a load are replaced with wave-digital-half band filters performing low pass filtering. The circuit diagram of using multiple supply voltages with digital baseband filtering is shown in Fig. 33.

As can be seen in Fig. 33, the input supply voltage is stepped down twice using diode connected NMOS transistors. An SVTLP transistor is used as the diode connected NMOS devices with the width of 270 µm and increased finger value, so that the step down voltage is sufficient to drive the filter stage and provide the supply to the second step down transistor.

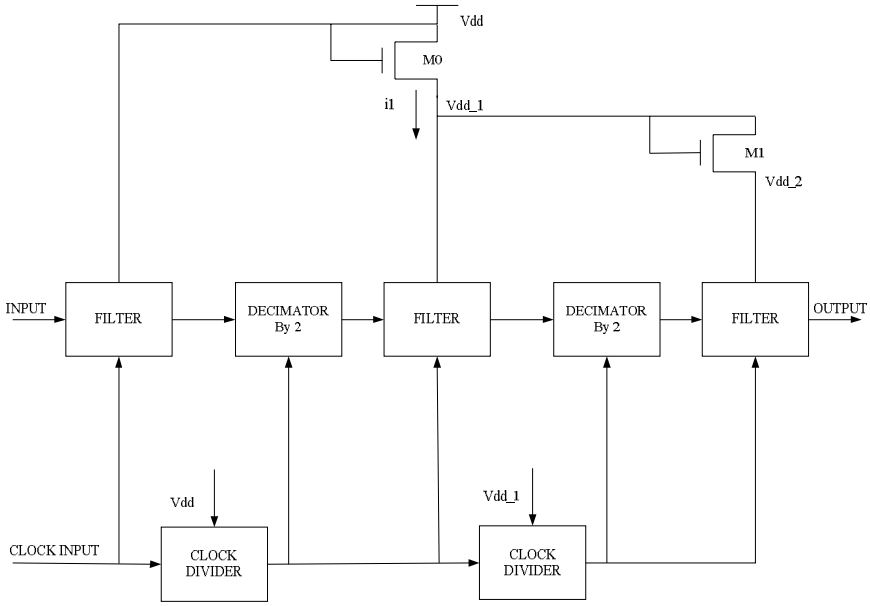

Figure 33. Low pass filter with voltage scaling

The circuit has three filter stages, with input stage receiving supply voltage from V_{dd}, first stage filter from first step down voltage V_{dd_1}, and second stage filter from second step down voltage V_{dd_2}. The output of each filter is decimated and connected to next filter stage, thereby reducing the signal frequency at each stage. An input signal of 32 MHz is fed to the input stage filter. Voltage, current, and power at each stage is evaluated.

4.3.1 Supply and step down voltages

The supply voltage for each filter stage along with its input frequency is tabulated in table 20 and plotted in Fig. 34. The input stage filter has a direct supply of 1.2 V, step down voltages V_{dd_1} and V_{dd_2} are connected as the supply to the first and second filter stage respectively.

In Fig. 34, the supply voltage for each stage is plotted with respect to the operating frequency of the respective stage.

TABLE 20. SUPPLY VOLTAGE FOR EACH FILTER STAGE

Filter Stage	Input frequency (MHz)	Voltage (mV)
Input	32	1200
First	16	880
Second	8	606

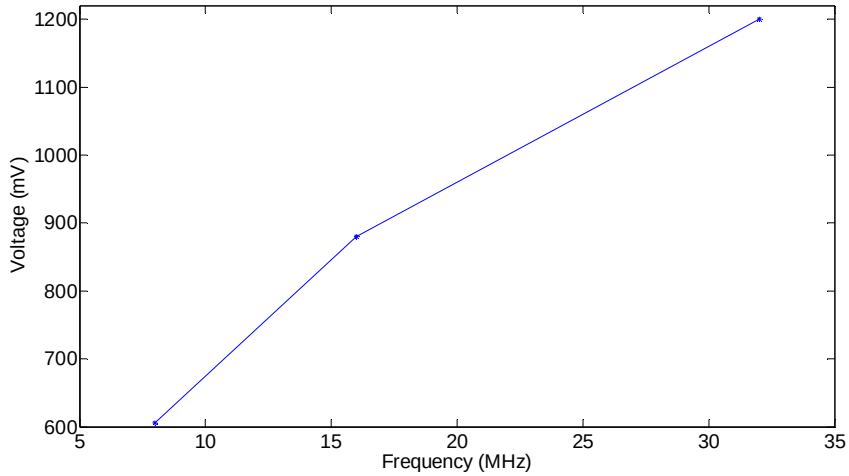

Figure 34. Supply voltage at each filter stage with its input frequency

The value of the required supply voltage decreases for each stage, i.e. with the decrease in the operating frequency. In this case the width of the diode connected NMOS device is increased to achieve the step down voltage approximately equal to 900 mV and 600 mV for the first and second stage respectively. As filter output gets distorted once the filter supply voltage is less than 550 mV i.e. the filter does not function properly.

4.3.2 Current drawn by the load (filter)

The current drawn by each filter stage with respect to the input frequency of the stage are tabulated in table 21 and plotted in Fig. 35.

TABLE 21. CURRENT DRAWN BY THE LOAD (FILTER)

Filter Stage	Input frequency (MHz)	Current (µA)
Input	32	61
First	16	24
Second	8	9.8

As can be seen in Fig. 35 the value of the current drawn by each filter stage decreases for each consecutive stage i.e. with the decrease in the operating frequency. The current drawn by the each stage is decreasing as the voltage supplied decreases with the stage.

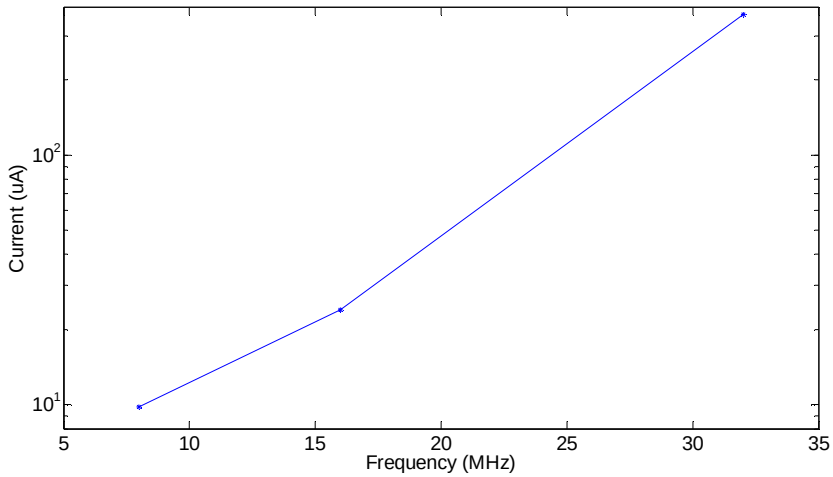

Figure 35. Current drawn by each filter stage with its input frequency

4.3.3 Power and energy consumed by the load (filter)

The power and energy consumed by each filter stage is tabulated in table 22 and table 23, and plotted in Fig. 36 and Fig. 37 respectively. Each filter stage is represented by its input frequency.

TABLE 22. POWER CONSUMED BY THE LOAD (FILTER)

Filter Stage	Input frequency (MHz)	Power consumed by the load (µW)
Input	32	73.2
First	16	21
Second	8	6

TABLE 23. ENERGY CONSUMED BY THE LOAD (FILTER)

Filter Stage	Input frequency (MHz)	Energy consumed by the load (pJ)
Input	32	2.2
First	16	1.3
Second	8	0.7

It can be observed from the Fig. 35 and Fig. 36 behavior of both power and energy curve is almost similar to the current curve in Fig. 34.

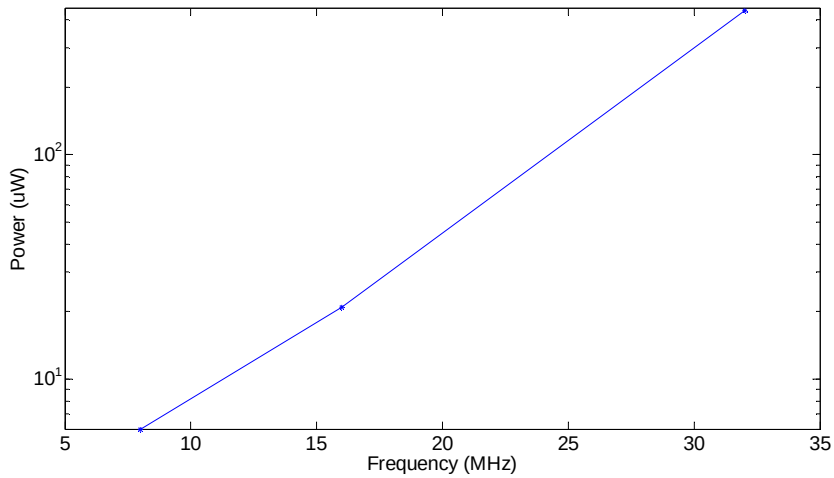

Figure 36. Power consumed by each filter stage with its input frequency

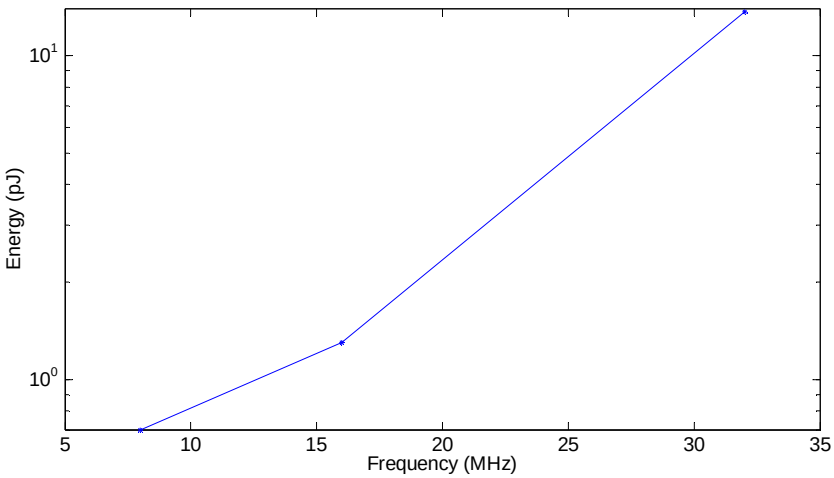

Figure 37. Energy consumed by each filter stage with its input frequency

The power and energy consumption is higher at input stage, which is followed by the first stage and by the second stage. This is obvious as the supply voltage and current for each consecutive stage decreases. Here it can be observed by using stepped down voltage for the first stage and second stage inverters, the amount of power consumed and energy consumed for the respective stages is considerably decreased when compared to the input stage having direct supply voltage. The power consumption in second stage

is 3.5 times lesser than the power consumption in first stage i.e. approximately 70 % of power saving is achieved in the second stage.

4.3.4 Power dissipated in diode connected NMOS transistor and efficiency of each stage

The power dissipated in the diode connected NMOS transistors during the voltage conversion is shown in table 24 and the efficiency for each diode connected NMOS transistor as a voltage converter is shown in table 25.

TABLE 24. POWER DIISSIPATED IN THE DIODE CONNECTED NMOS TRANSISTOR

Transistor	Power dissipated in diode connected NMOS transistor (µW)
1	10
2	2

TABLE 25. EFFICIENCY OF THE VOLTAGE CONVERTER

Stage	Ŋ (%)
1	68
2	75

The power dissipated in first stage diode connected NMOS transistor is higher than the power dissipated in second stage diode connected NMOS transistor. This is obvious as the first stage has a higher supply voltage and draws a higher amount of current when compared to the second stage. The efficiency of the second stage is higher in this case when compared to the efficiency of the first stage. This can be attributed to the fact that the second stage is operating at a lower frequency.

4.4 Low pass filter with different direct supply voltages

In this case, a direct supply voltage is connected instead of step down voltage i.e. no diode connected NMOS device is required for step down. The same 3-stage baseband filtering is used for test as in section 4.3. The supply voltage of 1.2 V, 900 mV, and 600 mV is applied to input stage, first stage, and second stage filters. The voltage, current, and power readings are evaluated at each stage and compared with the readings obtained in sections 4.3 and 4.5. The circuit diagram for the mentioned test is shown in Fig. 38.

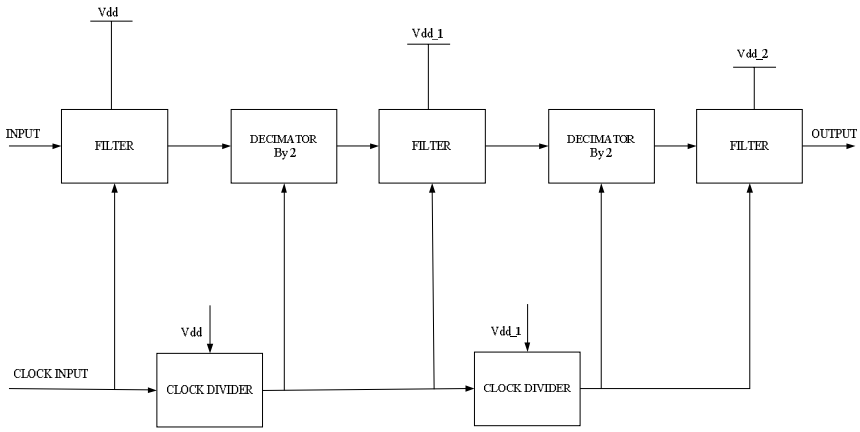

Figure 38. Low pass filter with direct voltage supply

An input signal of 32 MHz is applied to the input filter stage similar to the section 4.3. The output of each filter is connected to the input of next filter stage after the decimation. The results obtained for this test are tabulated in table 26. The power consumed by first and second stage in case of direct supply voltage is more when compared to the case of step down voltage. This is because in the case of direct supply voltage, the supply voltage is constant and stable whereas in the case of step down voltage, the supply voltage is not constant and has ripples.

TABLE 26. LOW PASS FILTER WITH DIRECT VOLTAGE SUPPLY

Frequency (MHz)	Voltage (mV)	Current (µA)	Power (µW)
32	1200	61	73.2
16	900	27	24
8	600	16	9.6

4.5 Low pass filter with same direct supply voltage

Even in this case, the direct supply voltage is connected instead of step down voltage i.e. no diode connected NMOS device is required for step down. The same 3-stage baseband filtering is used for test as in section 4.3. The same supply voltage of 1.2 V is applied to the input stage, first stage, and second stage filters. Voltage, current, and power readings are evaluated at each stage and compared with the readings obtained in sections 4.3 and 4.4.

An input signal of 32 MHz is applied to the input filter stage similar to the section 4.3. The output of each filter is connected to the input of next filter stage after the decimation. The results obtained for this test are tabulated in table 27. In this case of same direct supply voltages (1200 mV) more power is consumed in first and second stages when compared with the previous cases. This is because the higher supply voltage causes more current to flow which in turn increases the power consumption.

TABLE 27. LOW PASS FILTER WITH SAME DIRECT VOLTAGE SUPPLY

Frequency (MHz)	Voltage (mV)	Current (µA)	Power (µW)
32	1200	61	73.2
16	1200	36	43.2
8	1200	33	39.6

4.6 Comparison

The variations in the current with the frequency i.e. each stage for the step down voltage case (section 4.3) and for the two cases of direct supply voltage (section 4.4 and 4.5) are plotted and compared in Fig. 39.

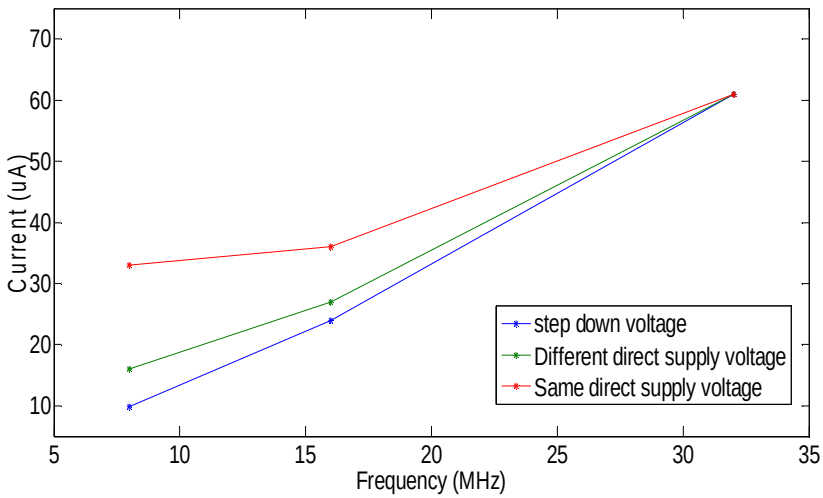

Figure 39. Comparison of current

As depicted in Fig. 39, the current decrease with the decrease in frequency i.e. it decreases for each stage. It is clear from Fig. 39 that the current for the step down voltage case is lesser than the current for the different direct supply voltage cases, which in turn is lesser than the current for the same direct supply voltage case. When the step down voltage case and the

different direct supply voltage case is compared, it is clear that the current drawn in the former case is lesser. This is due to the current limiting property and the internal resistance of the diode connected NMOS transistor. Where as in the direct supply case it is an ideal supply providing the higher amount of current as required by the load.

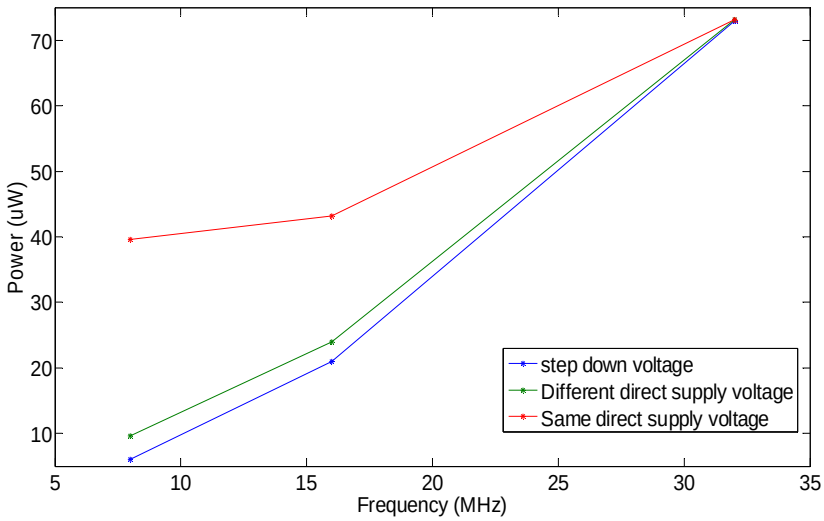

Figure 40. Comparison of power

The variations in the power consumption with respect to frequency i.e. for each stage and its comparisons with the power consumption in section 4.3 and section 4.4 are plotted in Fig. 40. The power consumption curves approximately follow the current curves. The power consumption decreases with each stage. When the power consumption in the step down voltage case and direct supply voltage case is compared, the former one is lesser as is the case with the current. It is clear from Fig. 40 that a considerable amount of power can be saved by using multiple supply voltages instead of same voltages for all the stages.

The total power consumed by the circuit in Fig. 33 for the step down voltage case is 100 µW and it's around 156 µW for the case of same direct supply voltage. The power saving of around 56 % is achieved by using multiple supply voltages.

CHAPTER 5

5 Comparison with prior work

The sources of power dissipation in digital circuit can be broadly classified into static and dynamic power dissipation. Dynamic power consumption can be further classified into charging and discharging capacitances and direct path current. Charging and discharging capacitance power dissipation is a function of the load capacitance, supply voltage, and operating frequency. Here the supply voltage and the operating frequency can be varied to control the power dissipation. The charging and discharging capacitances power dissipation shares a quadratic relation with supply voltage and a linear relation with operating frequency, hence it is prudent to scale down the supply voltage to achieve the low power dissipation.

There are numerous ways to scale down the supply voltage. A well-known and effective technique would be to use an on-chip DC-DC buck converter [3, 4, and 5], even though they occupy larger chip area and consume lot of power. In a practical circuit configuration as in Fig. 33, it is feasible to implement voltage scaling by using diode connected NMOS transistors.

TABLE 28. LOAD POWER AND EFFICIENCY OF THE CIRCUIT CONFIGURATION IN FIG. 29

Stages	Voltage (mV)	Current (µA)	Load Power (µW)	Power dissipated in the diode connected NMOS devices(µW)	Efficiency (%)
1	880	24	21	10	68
2	606	9.8	6	2	75

Table 28 shows the evaluation of load power and efficiency of the circuit configuration in Fig. 33. The circuit in Fig. 33 operates at frequency of 32 MHz with an input supply voltage of 1.2V. The RMS voltages and currents

were measured at each stage. The efficiency for each stage is evaluated by estimating the load power and power dissipated in the diode connected NMOS transistor. It is evident that efficiency increases drastically for increasing the number of stages and an average efficiency of 68% for the first stage is obtained.

TABLE 29. COMPARISON WITH PRIOR WORK

Technique	Technology (nm)	Chip area (mm^2)	Output Voltage (V)	Efficiency (%)
[5]	45	0.16	0.8 to 1	> 60
[4]	130	2.56	0.4 to 1.4	≤ 77
[3]	130	1.59	0.3 to 0.88	≤ 74.5
This work	65	$70x10^{-6}$	0.88	≤ 68

Table 29 shows comparing this technique with prior work. There are no prior work targeted only for digital circuits and it would not be fair to compare works in [3, 4, and 5] as they are targeted for analog circuits with on-chip inductors. Nevertheless they have the same operating voltage range with the first stage of the circuit in Fig. 33. Furthermore the test setup in Fig. 33 does not have a constant load, which varies as stages are added as opposed to the constant load in [3, 4, and 5].

It is clearly evident from the table 29 that this work achieves comparable efficiency with much lesser chip area for the same output voltage range. Also this work proposes a fully integrated on-chip solutions with very little chip area occupied and loss in efficiency. The disadvantage in this work is the limited and fixed output voltage range for a higher efficiency. The number of stages that can be implemented through this technique is limited by the lower operating supply voltage. The step down voltage itself is not constant and has ripple in it.

CHAPTER 6

6 Conclusions and Future work

This thesis presents a method of using multiple supply voltages based on single supply voltage thereby saving the power consumed. The feasibility of the diode connected NMOS transistor to be used for voltage conversion is tested here. Multiple voltages are generated using a multiple number of diode connected NMOS transistors, which is used in a typical case of digital baseband filtering.

It is observed that the step down voltage provided by the diode connected NMOS transistor depends on a number of parameters such as type and width of transistor, load capacitance value, and the type of load. The step down voltage increases with increase in width of the transistor and is higher for LVTLP type of transistor when compared to SVTLP and HVTLP transistor types.

In the case of digital baseband filtering used as a test, the power consumed in subsequent stages is approximately 4 to 5 times lesser when compared to previous stages. In final comparison of digital baseband filtering using scaled step down voltage and direct voltage supplies, the power consumed in the former case is much lesser as compared to the later one.

Possible future work in this design is to stabilize the output voltage. To stabilize the voltage, transistor stack can be used. Furthermore, to make this design for constant load and constant frequency to evaluate the load power for each stage.

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LVTLP	Low threshold voltage low power
SVTLP	Standards threshold voltage low power
HVTLP	High threshold voltage low power
WDF	Wave digital filter