



Master's Thesis

Signal Integrity Analysis of Package and PCB for High Speed Data link Application

By

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ABSTRACT

With ever shrinking geometry size, we have reached a point in time in which we cannot draw a direct correlation of the performance of the IC design with respect to the number of transistors on a single chip. As in limited silicon area available factors like tighter packaging space, circuit boards and increasing clock frequencies, packaging issues and system-level performance issues such as crosstalk and transmission lines are becoming increasingly significant. Multi-chip packages and increased IO counts are forcing package design to become more challenging like chip design [1]. This thesis targets a fundamental evaluation of variety of approaches in board design viz. varying the length, width, and design structure for a high speed electrical channel. The application of electrical interface is simulated with HSPICE® software. It also demonstrates the jitter variation effect by the use of microstrip versus stripline traces. The jitter results for various line parameters and line terminations are compared with results published in literature. The crosstalk between coupled microstrip lines in both “time” and “frequency” domain are presented and simulated in HSPICE®. In addition the thesis studies with simulation results, shows that ground conductors need to be placed in between the aggressor and victim to reduce crosstalk effectively. However the presence of the grounded conductors will increase the layout complexity and waveform distortion for the signal on the aggressor line. The crosstalk analysis in frequency domain for different packages had been analyzed and simulated. A crosstalk and jitter minimization technique is implemented in 2D field solver for both package and board. The rated frequency at which DDR3 sub-systems are targeted in Texas Instruments (TI) designs showed a 10% reduction in the expected frequency of operation, after accounting the various extraneous parameters obtained as part of the thesis findings. This is based on the assumption that they are linearly accounted in to the link layer timing calculation, but from a Gaussian distribution curve the effective impact is root-sum-square of the results obtained.

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CHAPTER 1

INTRODUCTION

The continuous scaling of integrated circuit technology, confirming Moore's prediction, over the recent years has resulted in high bandwidth and hence data processing capability which in turn has created the demand for high-speed communication across different components in a system [2]. Channel design will be a major bottle neck for high speed communication. The increase in data rates in Giga bits per second (Gbps) has prompted more careful signal integrity considerations in the design of the channel from one chip to the next. The channel band width is highly depended upon the channel length and channel design structure. It will indirectly depend upon the materials used, the physical structure, signal coupling due to compact routing and power integrity [2].

As system bandwidth is continuously increasing, memory technologies have been optimized for higher speed and performance. The next generation family of Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) is the DDR3-SDRAM. They have several advantages compared to DDR2. DDR3 is having lower power, higher frequency and offer higher performance. DDR3 devices provide around thirty percentage power reduction compared to DDR2, primarily due to smaller die size and the lower rail voltage. DDR3 devices present a host of challenges for the memory controller. DDR3 will be capable of reaching a data rate of 1.333-1.600Gbps. DDR2 uses T-branch topology but DDR3 adopts fly-by architecture which provides better signal integrity at higher speeds. The Read and Write leveling has introduced an additional level of complexity for the DDR3 memory controller architecture. The fly-by signals are the command, address, control and clock signals. These signals from the memory controller are connected in series to each Dynamic Random Access Memory (DRAM) device. This improves signal integrity by reducing the number of stubs and the stub lengths. However, this creates a skew issue. This can be compensated for by using the Read/Write Leveling techniques [15].

This thesis presents the Jitter and Crosstalk analysis of high speed DDR3 interface of different Package, Printed Circuit Board (PCB) and the entire system. Device level simulation is performed in HSPICE® (Simulation Program with Integrated Circuit Emphasis) and Sentinel™-SSO (Simultaneous Switching Output). Printed Circuit Board (PCB) and Package (PKG) were implemented in 2D Field Solver

(2DFS) and the time domain analysis is performed by varying channel length and design structure. The frequency domain analysis of Package is done using HSPICE® software.

Chapter 2 describes the different factors affecting the signal integrity of high-speed data links such as Track length/Width, Dielectric material properties of the PCB, type and length of track used (microstrip/strip line) , data pattern dependency of the signal quality. The different scenario is implemented in 2DFS and is simulated using HSPICE® software. It demonstrated how the signal quality can be affected by the use of microstrip versus stripline traces.

Chapter 3 describes the frequency-domain approach of a package to efficiently simulate the crosstalk. The time domain approach has been the most popular approach in digital systems. The main disadvantage of this method is that crosstalk may vary extremely with frequency. Crosstalk simulated can increase significantly with small changes in the transient waveform.

Chapter 4 describes the Jitter analysis of a device which uses two 32-bit DDR3 platforms for Cable Set-top Box Digital Video Recording (DVR) Hub, Video Transcoding, Hybrid Internet Protocol (IP) Set-top Box, High Definition (HD) Video Conferencing, and Multi-channel Security DVR applications. The DDR interface of this device comprises of 8-bit Data macro, which includes the DDR Physical Layer (DDR PHY), Delay Locked Loop (DLL) and the Input/Outputs (IOs).

Chapter 5 describes the Jitter and Crosstalk analysis of the same device using Sentinel™-SSO tool from APACHE® and compares the result obtained through HSPICE® simulation software.

CHAPTER 2

HIGH SPEED 4 LAYER PCB-JITTER ANALYSIS

The first considerations when designing PCB is how many routing layers and power planes are required for functionality. The number of layers is determined by noise immunity, component density, routing of buses and impedance control. The important rule while designing the layer stackup is that each and every routing layer must be adjacent to a solid plane (power or ground). There is only one way to perform a four-layer stackup.

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)
1		SURFACE	AIR			1	0			
2	TOP	CONDUCTOR	COPPER	1	595900	1	0	☐		4.0
3		DIELECTRIC	FR-4	3	0	4.5	0.035			
4	GROUND	PLANE	COPPER	1	595900	1	0	☐	☒	
5		DIELECTRIC	FR-4	52	0	4.5	0.035			
6	POWER	PLANE	COPPER	1	595900	1	0	☐	☒	
7		DIELECTRIC	FR-4	3	0	4.5	0.035			
8	BOTTOM	CONDUCTOR	COPPER	1	595900	1	0	☐		4.0
9		SURFACE	AIR			1	0			

Figure 2.1 PCB stackup of the device

Figure 2.1 shows the stackup details of the device.

- First layer, signals and clocks
- Second layer, ground plane
- Third layer, power plane
- Fourth layer, signals and clocks

Multilayer boards provide superior signal quality performance because by using stripline or microstrip signal impedance can be controlled. This chapter describes the main considerations in the design of a PCB for the transmission of high speed data.

2.1 Microstrip versus Stripline Implementation

Figure 2.2 shows the difference between microstrip and stripline topologies. Microstrip refers to outer traces on a PCB and is separated by a dielectric material and then a solid plane. This technique provides faster clock and logic signals are possible than with stripline. The faster signals are due to less capacitive coupling and lower unloaded propagation delay between traces routed on the outer layers and an adjacent plane [3]. The lower coupling capacitance between the solid planes, faster signal propagation can be achieved. By using microstrip, longer track length can be used and the impedance discontinuities will be minimal. The main drawback of microstrip is the outer layers of the PCB can radiate RF energy unless shielding of both top and bottom side of the traces.

Stripline refers to placement of a circuit plane between power and ground. It provides better noise immunity for Radio Frequency (RF) emissions but slower propagation speeds. Since the signal plane is located between power and ground, capacitive coupling will occur between these two planes, which reduces the propagation. If the rise time is faster than 1ns capacitive coupling will happen. The main advantage of using stripline is the complete shielding of RF energy and thus suppresses the RF radiation.

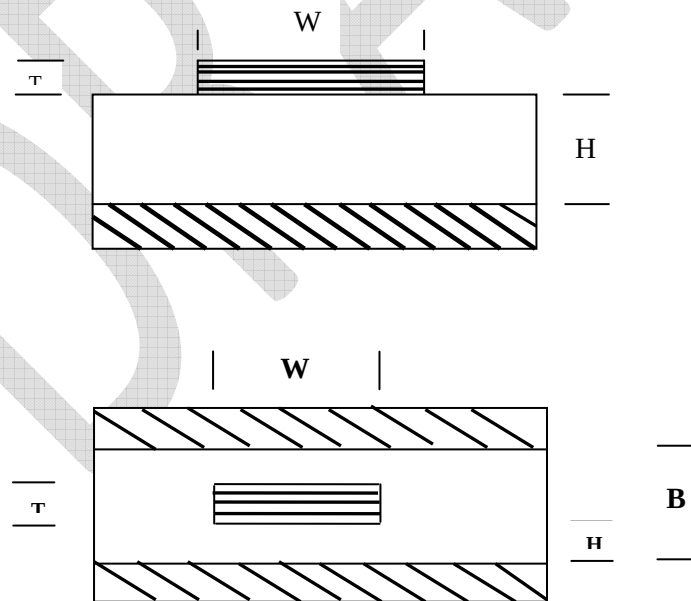


Figure 2.2 Microstrip and Stripline topologies. [3]

2.1.1 Impedance Control

Clock traces and signal traces should be impedance controlled. While designing the PCB determine the trace width and the distance between the traces. The characteristic impedance for the microstrip and stripline implementation is shown in the below functions.

For microstrip topology the characteristic impedance

$$Z_0 = \left(\frac{87}{\sqrt{E_r + 1.414}} \right) * \ln \left(\frac{5.98H}{0.8W + T} \right) \quad [3]$$

Where Z_0 = characteristic impedance (ohms)

W = width of the trace (inches)

T = thickness of the trace (inches)

H = distance between signal trace and reference plane (inches)

B = overall dielectric thickness

E_r = dielectric constant.

The characteristic impedance in terms of capacitance and inductance is given by

$$Z_0 = \sqrt{\frac{L}{C}}$$

The approximate formula for single stripline impedance is

$$Z_0 = \left(\frac{60}{\sqrt{E_r}} \right) * \ln \left(\frac{4H}{0.67 * \pi * W \left(0.8 + \frac{T}{W} \right)} \right) \quad [3]$$

Where A = dielectric thickness between trace and power/ground plane.

The modeling of the transmission line is implemented using W-element. The parameters of the transmission line were computed using *field solver*.

Note: A transmission line is a passive element that connects any two conductors. One conductor sends the input signal through the transmission line and the other conductor receives the output signal from the transmission line.

The W-element is a versatile transmission line model which can efficiently and accurately simulate the transmission line (both lossless and lossy-coupled). The output will be accurate as compared to U-element implementation.

Since the transmission line simulation is challenging and time consuming the microstrip and stripline topologies were implemented in 2-D electromagnetic field

solver, which calculates the electrical parameters of the transmission line based on its cross-section. Table 2.1 shows the Jitter value comparison for the microstrip and stripline topologies for a given simulation configuration. The eye diagram is also shown in the figure 2.3. The analysis show that, in terms of jitter stripline topology is better compared to microstrip topology.

SimulationConf::1:Er=4.5,loss tangent=0.035,thickness=1mil,Width=4mil and Length=0.5m				
Parameters	Microstrip		Stripline	
	Near End	Far End	Near End	Far End
Pk2pk Jitter	12.7ps	74.2ps	17ps	14.2ps
Hold Jitter	2.57ps	3.3ps	7.5ps	1.98ps
Setup Jitter	10.1ps	70.8ps	9.5ps	12.2ps
Max Overshoot voltage	1.23v	1.21v	1.22v	1.24v
Min Undershoot voltage	0.18v	0.20v	0.2v	0.17v
Min V_{IH} voltage	1.20v	1.19v	1.16v	1.19v
Max V_{IL} voltage	0.21v	0.22v	0.25v	0.22v

Table 2.1 Jitter value comparison

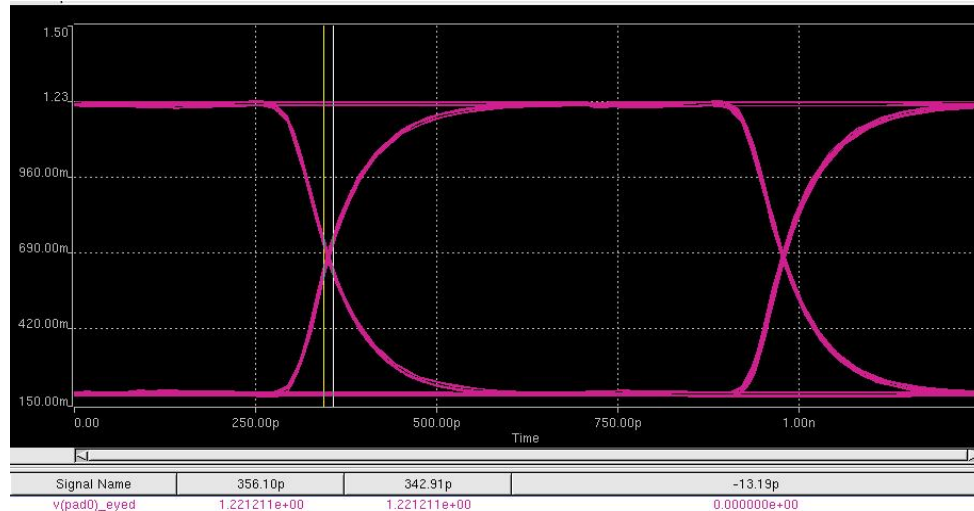


Figure 2.3(a) Microstrip-Near End Eye diagram

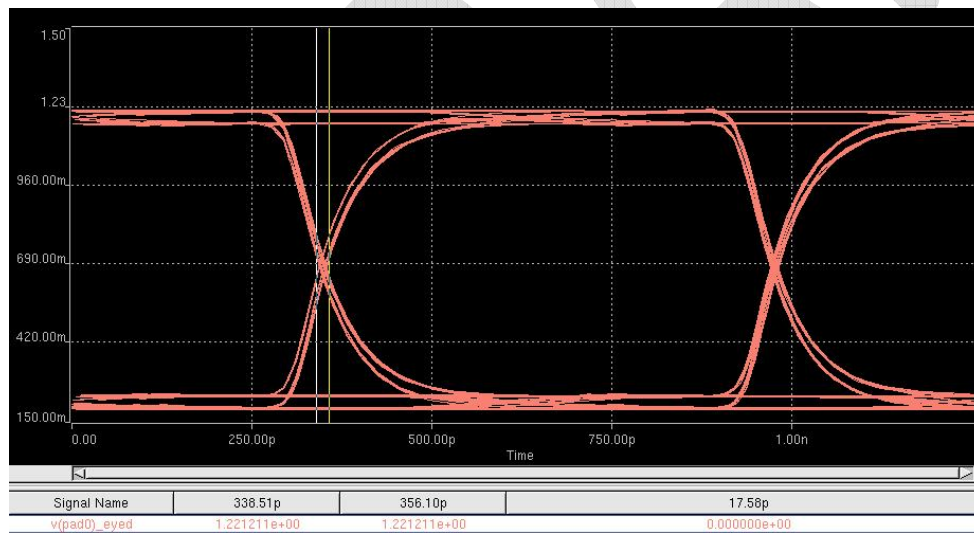


Figure 2.3(b) Stripline-Near End Eye diagram

2.2 Track Length/Width Analysis

Inductance in a trace may cause functional signal quality and potential RF emissions. When frequency increases the track dimensions together with PCB material properties become more prominent. When the trace length increases, RF currents will be produced and more spectral distribution of RF energy is created. The traces must be terminated to reduce ringing and reduction of RF currents. This is because unterminated traces generate signal reflections that can cause Electro Magnetic Interference (EMI) generation. The losses of transmission line are determined by the skin effect of the conductor and the dielectric. Increasing the surface area that is increasing the width of the transmission line can mitigate the skin effect. Skin effect losses will become dominating when the data rate of the system is very high. Table 2.2 shows the two different simulation configuration of microstrip (different width and thickness) by varying the track length. The details of the configuration together with the eye diagram analysis are listed in the table. It can be seen from the plot below in figure 2.4 that the deterministic jitter is evident due to the increase in track length. The increased jitter and the reduced eye opening as a function of the chosen microstrip geometry and the dielectric material are shown.

Simulation Conf::1:Er=4.5,loss tangent=0.035,thickness=1mil,4mil wide micro-strip				
Trace length	Inner Eye Width (ps)	Pk2Pk Jitter (ps)	Setup Jitter (ps)	Hold Jitter (ps)
0.1m track length	602.82	22.18	10.28	11.89
0.3m track length	600.19	24.81	9.28	15.53
0.4m track length	597.26	27.74	12.15	15.64
0.5m track length	588.1	36.9	20.53	16.36

Simulation Conf::1:Er=4.5,loss tangent=0.035,thickness=3mil,6mil wide micro-strip				
Trace length	Inner Eye Width (ps)	Pk2Pk Jitter (ps)	Setup Jitter (ps)	Hold Jitter (ps)
0.1m track length	602.35	22.65	10.64	12
0.3m track length	596.96	28.04	13.82	14.22
0.4m track length	594.39	30.61	17.32	13.28

Table 2.2: Jitter value by varying track length/width

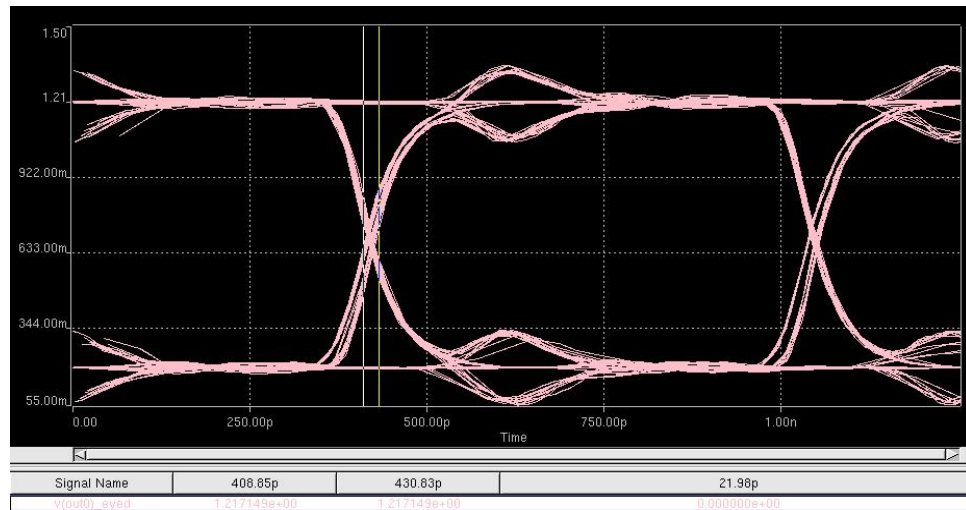


Figure 2.4(a) Eye-diagram of Microstrip-Track length (L) =0.1m

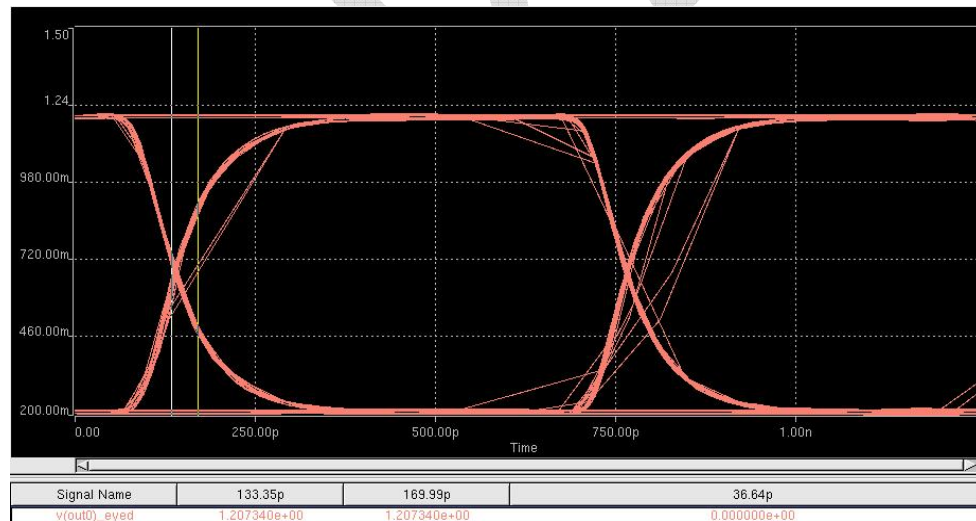


Figure 2.4(b) Eye-diagram of Microstrip-Track length (L) =0.5m

2.3 Multiple Conductor Analysis [Trace separation and Spacing]

Crosstalk may exist between traces on a PCB. Data, address, control and IO traces affected by crosstalk and coupling between the traces. When the separation between the traces increases the crosstalk will be less. The 3-W rule will allow the PCB designer to avoid guard traces. It will minimize the coupling between traces and signals and it provide a clean path along the board, such that the signal flux and the return flux will cancel each other. The 3-W rule states that “the separation between the traces must be three times the width of the traces measured from center to center”. Figure 2.5 shows the 3W spacing between the traces [3]. This technique minimizes RF fringing between traces.

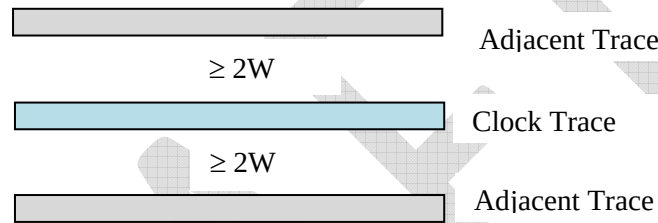


Figure 2.5 3W spacing without via between the traces

Even (symmetric) and odd (anti-symmetric) modes are the two main modes of propagation of the signal through a coupled transmission line. Coupled lines are usually designed to be differential pairs. In this case the signal propagation along the line shows a differential impedance behavior. This impedance will be lower than the impedance of the line by applying equal and opposite polarity of two propagating signals. In the case of odd mode (opposite signals applied to both victim and aggressor) the impedance will be half the value of the differential impedance. In the case of even mode (Identical signals applied to both aggressor and victim) the impedance measured testing one of a pair of lines is twice the common mode value. Figure 2.6 shows the difference between the even mode and odd mode configuration [4].

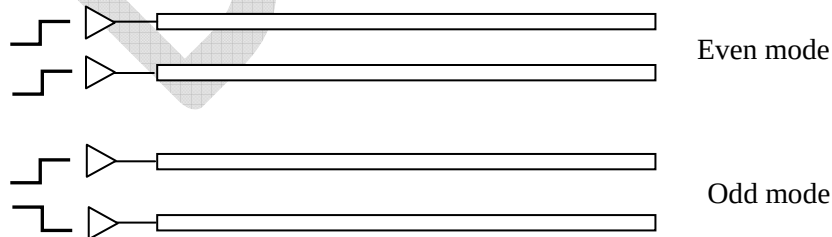


Figure 2.6 Even mode and Odd mode

In odd mode the characteristic impedance (Z_0) and propagation time delay (TD) will reduce. However in even mode the above two parameter will increase. The equation for finding Z_0 and TD are given below.

$$Z_{odd} = \sqrt{\frac{L_{odd}}{C_{odd}}} = \sqrt{\frac{L_{11}-L_{12}}{C_{11}+C_{12}}} \quad [4]$$

$$TD_{odd} = \sqrt{L_{odd} * C_{odd}} = \sqrt{(L_{11} - L_{12}) * (C_{11} + C_{12})}$$

$$Z_{even} = \sqrt{\frac{L_{even}}{C_{even}}} = \sqrt{\frac{L_{11}+L_{12}}{C_{11}-C_{12}}} \quad [4]$$

$$TD_{even} = \sqrt{L_{even} * C_{even}} = \sqrt{(L_{11} + L_{12}) * (C_{11} - C_{12})}$$

Where L_{11} and L_{22} are the self inductance, C_{11} and C_{22} are the self capacitance respectively. Similarly L_{12} and C_{12} are the mutual inductance and mutual capacitance.

In odd-mode the equivalent inductance is reduced by the mutual inductance and the equivalent capacitance for odd mode switching increases but in even-mode the equivalent inductance increases by the mutual inductance and the equivalent capacitance decreases. As the length of the conductor increases the coupling noise increases or the rise time of the driving signal decreases.

Table 2.3 below shows the different simulation configuration of a microstrip in different mode (ODD, EVEN and STANDBY) by varying the separation between the traces. The analysis shows that for the same termination, the even mode jitter will be higher compared to other modes. Also when the spacing between the traces increases the jitter will reduce.

Simulation Conf :: Er=4.5,loss tangent=0.035 ,thickness=1mil,Width=4mil Trace length=0.5m micro-strip, ODD mode Agressor-DQ0,DQ2 (same direction), Victim-DQ1 (opposite direction)				
Width, Spacing	Inner Eye Width (ps)	Pk2PkJitter (FE) (ps)	Setup Jitter (ps)	Hold Jitter (ps)
W,W	597.36	27.64	15.35	12.29
W,2W	611.92	13.08	1.38	11.7
W,3W	612.13	12.87	4.65	8.22
W,4W	612.17	12.83	2.93	9.89

Simulation Conf ::Er=4.5,loss tangent=0.035 ,thickness=1mil,Width=4mil ,Trace length=0.5m micro-strip, EVEN mode DQ0,DQ1 and DQ2 (same direction)				
Width, Spacing	Inner Eye Width (ps)	Pk2PkJitter (FE) (ps)	Setup Jitter (ps)	Hold Jitter (ps)
W,W	565.25	59.75	29.19	30.56
W,2W	574.4	50.6	52.34	-1.73
W,3W	576.9	48.1	45.32	2.78
W,4W	580.84	44.16	40.14	4.02

Simulation Conf ::Er=4.5,loss tangent=0.035 ,thickness=1mil,Width=4mil , Trace length =0.5m micro-strip, STANDBY mode Victim-DQ1 switching Agressor-DQ0,DQ2-Zero voltage				
Width, Spacing	Inner Eye Width (ps)	Pk2PkJitter (FE) (ps)	Setup Jitter (ps)	Hold Jitter (ps)
W,W	599.38	25.62	0.33	25.28
W,2W	602.94	22.06	19.52	2.53
W,3W	603.96	21.04	17.54	3.5
W,4W	606.1	18.9	15.49	3.4

Table 2.3: Jitter value in different mode (ODD, EVEN and STANDBY)

2.3.1 Influence of the Ground-Shield Line

In the design of high-speed application, the grounded conductors are placed between signal lines for reducing the crosstalk. This is called shielding. For reducing the crosstalk effectively, the grounded-shield conductor should be placed on both sides of the signal (G-S-G-S-G). The presence of the ground conductor will increase the routing congestion and severe waveform distortion for the signal on the active line. Table 2.4 shows the jitter value after shielding the victim line. This is implemented in 2DFS and the shielded conductor is connected to ground. The jitter value is reduced after shielding. Figure 2.7 shows the eye diagram in EVEN mode with and without shielding of the victim line.

Shielding given to the Victim line

Simulation Conf :: Er=4.5,loss tangent=0.035 ,thickness=1mil,Width=4mil Trace length=0.5m micro-strip, ODD mode Aggressor-DQ0,DQ2 (same direction), Victim-DQ1 (opposite direction)				
Width, Spacing	Inner Eye Width (ps)	Pk2PkJitter (FE) (ps)	Setup Jitter (ps)	Hold Jitter (ps)
W,W	599.21	25.79	25.49	0.29
W,2W	609.04	15.96	14.15	1.81
W,3W	612.28	12.72	14.03	-1.3
W,4W	612.86	12.14	13.1	-0.96

Simulation Conf ::Er=4.5,loss tangent=0.035 ,thickness=1mil,Width=4mil ,Trace length=0.5m micro-strip, EVEN mode DQ0,DQ1 and DQ2 (same direction)				
Width, Spacing	Inner Eye Width (ps)	Pk2PkJitter (FE) (ps)	Setup Jitter (ps)	Hold Jitter (ps)
W,W	577.27	47.73	56.55	-8.82
W,2W	610.29	14.71	19.4	-4.68
W,3W	613.26	11.74	15.85	-4.1
W,4W	614.28	10.72	14.09	-3.37

Simulation Conf :: Er=4.5, loss tangent=0.035 , thickness=1mil, Width=4mil , Trace length =0.5m micro-strip, STANDBY mode Victim-DQ1 switching Agressor-DQ0,DQ2-Zero voltage				
Width, Spacing	Inner Eye Width (ps)	Pk2PkJitter (FE) (ps)	Setup Jitter (ps)	Hold Jitter (ps)
W,W	599.38	25.62	0.33	25.28
W,2W	602.94	22.06	19.52	2.53
W,3W	603.96	21.04	17.54	3.5

Table 2.4: Jitter value in different mode with shielding (ODD, EVEN and STANDBY)

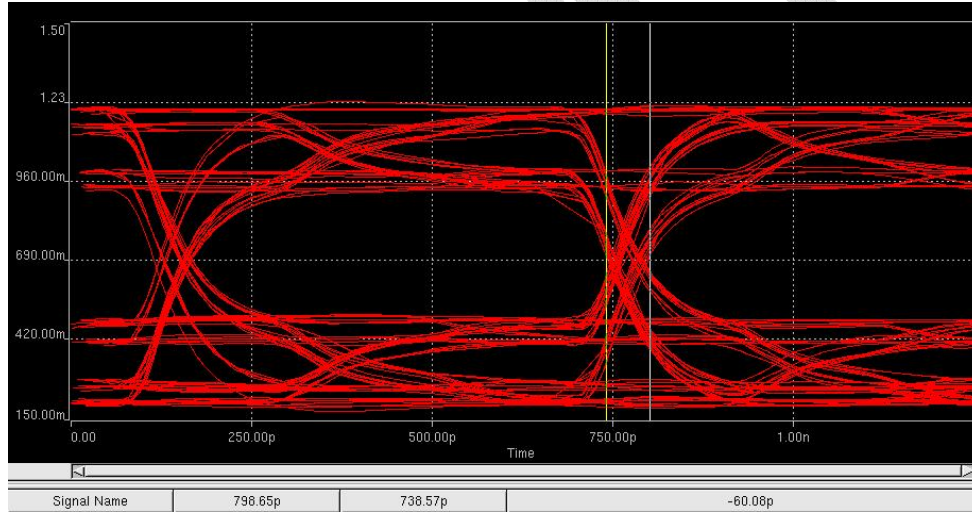


Figure 2.7(a) Eye-diagram-Jitter value in EVEN mode w/o shielding (Spacing=W)

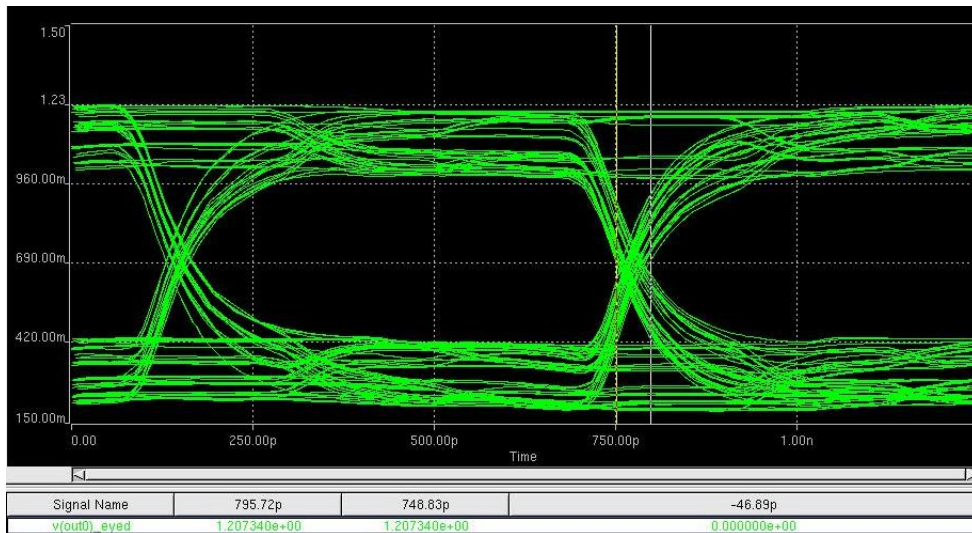


Figure 2.7(b) Eye-diagram-Jitter value in EVEN mode with shielding (Spacing=W)

2.4 Different types of Terminations [Trace Terminations]

Trace termination plays an important role in reduction of RF energy. To prevent the characteristic impedance corruption (Z_0) and for getting high quality signal transfer between circuits, termination is required. Impedance mismatches between the source, line and load will cause reflections, overshoot, and undershoot. When a driver is overloaded, the signal can degrade if the termination is not proper. There are five common termination methods are available. These methods are dependent on the power consumption, layout geometry, and the component density. Figure 2.8 shows the different termination schemes.

- Series termination resistor
- Parallel termination resistor
- Thevenin termination
- RC termination and
- Diode termination

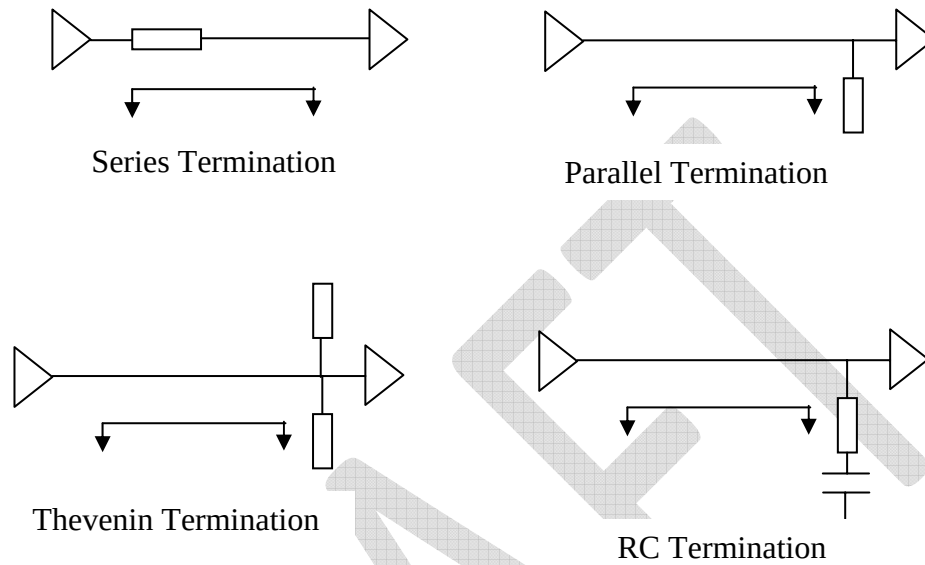


Figure 2.8 Termination Schemes [5]

2.4.1 Series termination

It is connecting in series to the line. It is used when lumped load is at the end of the trace, the driver output impedance is less than the characteristic impedance of the trace and when the fan out is low [3]. Series termination reduces power consumption and dissipate less energy than no termination. The resistor value can be computed as $R_s = Z_0 - R_d$, where R_s is the series resistor value, Z_0 is the characteristic impedance and R_d is the driver resistance.

2.4.2 Parallel termination

In parallel termination, a single resistor is used and the value of the resistor should be equal to the characteristic impedance (Z_0) of the trace. The other end is tied to ground. The advantage is that this method allows for incident wave switching. The main disadvantage of parallel termination is it consumes dc (static) power.

2.4.3 Thevenin termination

This termination method connects one resistor (pull-up) to power and the other resistor (pull-down) to ground. The swing between logic high and logic low will be proper. The static power consumption is a function of duty cycle and resistor values. If the resistors are matched, the static power consumption is not dependent

upon the duty cycle. For proper impedance matching, the equivalent Thevenin resistance should be the same as the line characteristic impedance (Z_0). This method is suitable for Transistor Transistor Logic (TTL) families but not recommended for low voltage Complementary Metal Oxide Semiconductor (CMOS) logic if power dissipation is a concern. The termination is placed at the end of the line as close to the receiver.

2.4.4 RC termination

This termination works well in both TTL and CMOS logic. The resistor value will be same as the impedance of the trace and the capacitor blocks the dc current. As a result ac current flows to ground during the switching state. The power dissipation will be less compared to parallel termination.

2.4.5 Diode termination

This termination is commonly used on differential networks. It will limit the overshoot and provide less power dissipation. Since diodes do not affect the trace impedance, the reflection will exist in the trace.

The termination will sometimes slow down the slew rate of the signal, if the parameters are not set properly.

Table 2.5 shows a comparison for series, parallel and Thevenin termination. From the table it shows that jitter will be more in parallel termination but less for series termination. In series termination the maximum overshoot will be more. A compromise between jitter value and maximum overshoot, Thevenin termination will be the best. All the analysis uses Thevenin termination. Figure 2.9 shows the output waveform for the different termination topology. Figure 2.10 shows the eye diagram and jitter value for different terminations.

2.5 Data pattern dependency

PRBS waveform is used as input for the simulation. Figure 2.11 shows the eye diagram of DQ signal with two different patterns. From the diagram it shows that the jitter value is dependent on the input pattern and worst case happens when the pattern is having low frequency content.

Simulation Conf :: 1:Er=4.5,loss tangent=0.035 ,thickness=1mil,4mil wide , L=0.5m micro-strip				
Terminations	Pk2Pk Jitter(ps)	Max overshoot(v)	Min undershoot(v)	Noise Margin(v)
Parallel	145.13	1.0	-0.02	0.95
Series	63.45	1.41	-0.01	0.98
Thevenin	84.64	1.21	0.20	0.96

Table 2.5 Comparison table for different terminations

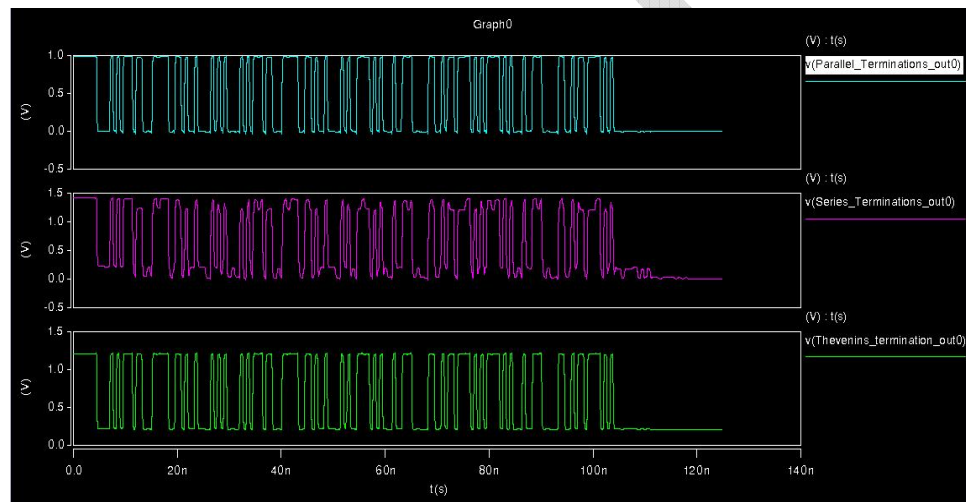


Figure 2.9 Output waveform of different termination

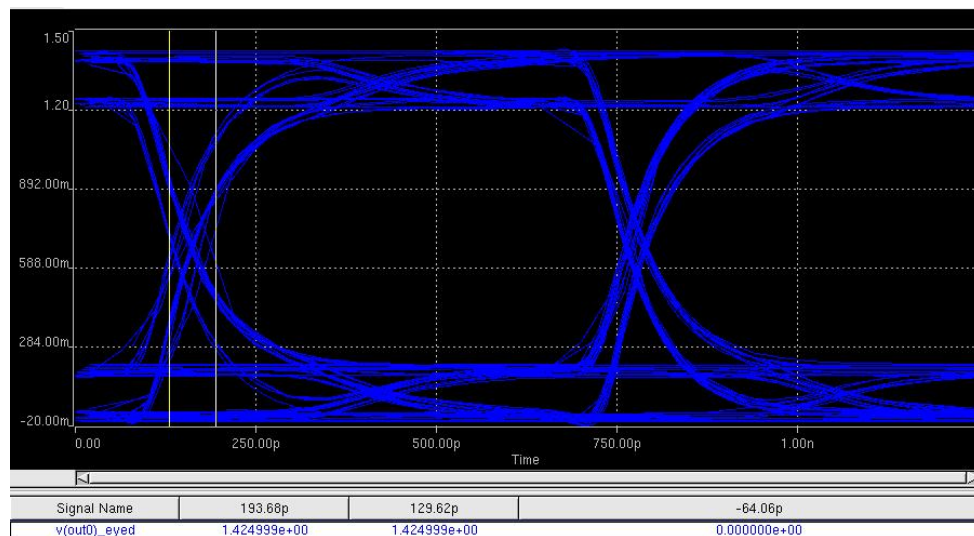


Figure 2.10(a) Eye diagram for series termination



Figure 2.10(b) Eye diagram for parallel termination

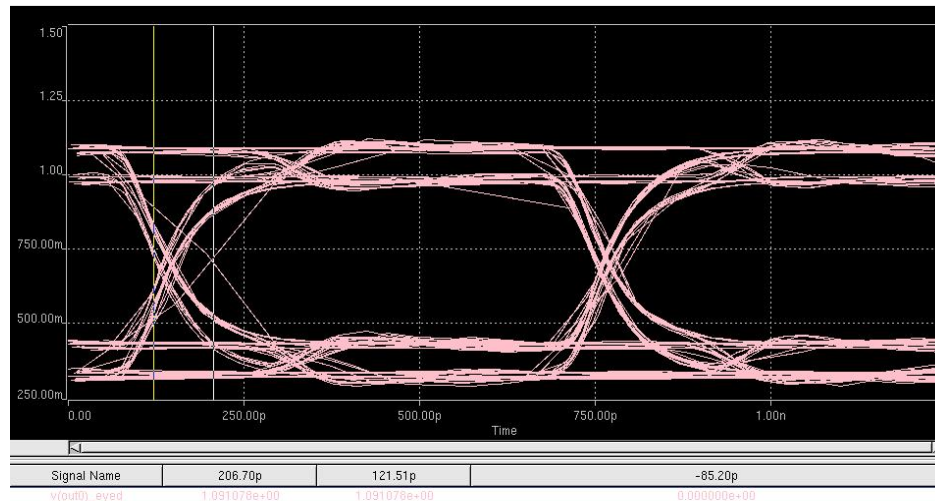


Figure 2.10(c) Eye diagram for Thevenin termination

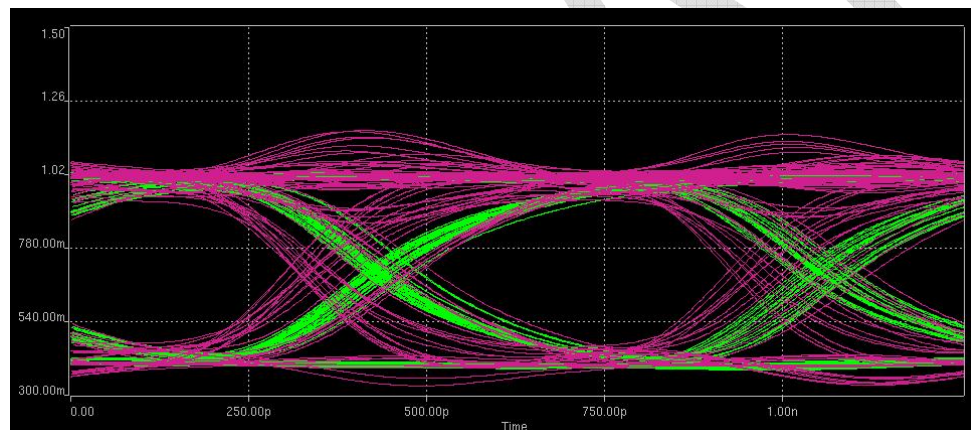


Figure 2.11 Eye diagram for different pattern

CHAPTER 3

HIGH SPEED 6 LAYER PACKAGE- CROSSTALK AND JITTER ANALYSIS

The dramatic increase in the switching speed and the density of integrated circuits poses a challenge the interconnection problems [6]. The performance will become more pronounced as the interconnection line width and spacing decrease and the interconnection line length and clock rate increase. Electromagnetic radiation, crosstalk, simultaneous switching noise (SSO), impedance mismatch and reflections are problems associated with high-performance interconnections. Even though crosstalk between signal lines is a major concern in high speed package designs. Accurate modeling and crosstalk analysis of coupled lines are important for the design and simulation of high speed integrated circuits (IC's). The frequency domain analysis of crosstalk between signal lines in package and time domain jitter analysis were described in this chapter. Scattering parameters provide a powerful analysis tool for crosstalk. Figure 3.1 shows a six layer Flip Chip Ball Grid Array (FCBGA) package. Generally the signal density is very high in package compared to PCB; package requires a balance between impedance target (line width) and crosstalk (line spacing).

		Type	Name	Pad Height	Thickness	Height
1	☒	CONDUCTOR	L01	0.00	14.50	1025.50
2	☒	DIELECTRIC	DP12	0.00	33.00	992.50
3	☒	CONDUCTOR	L02	0.00	14.50	978.00
4	☒	DIELECTRIC	DP23	0.00	33.00	945.00
5	☒	CONDUCTOR	L03	0.00	25.00	920.00
6	☒	DIELECTRIC	DP34	0.00	800.00	120.00
7	☒	CONDUCTOR	L04	0.00	25.00	95.00
8	☒	DIELECTRIC	DP45	0.00	33.00	62.00
9	☒	CONDUCTOR	L05	0.00	14.50	47.50
10	☒	DIELECTRIC	DP56	0.00	33.00	14.50
11	☒	CONDUCTOR	L06	0.00	14.50	0.00

Figure 3.1 shows a six layer package

The Package is the holder of the chip (die) and it provides mechanical, thermal and electrical connections between the chips to the rest of the system. The physical attributes of the package is divided into three: Die side (attachment of the die to the package), package connection and Ball side (attachment of the package to the PCB). The die side attachment can be wire bound or flip chip. The common method used for connecting package to the PCB is ball grid array (BGA). In the case of high speed application the routing of the signals in the package is done in an impedance controlled fashion.

3.1 Frequency Domain approach

Transient analysis (time-domain) has been the most popular method for simulating the crosstalk between the coupled transmission lines. The main disadvantage of this method is that the crosstalk may vary extremely with frequency, so a small change in the transient input waveform will have a significant change in the crosstalk. An alternative method for crosstalk analysis is in frequency-domain approach. This method can be used for both linear and non-linear termination of coupled transmission lines.

3.1.1 Crosstalk between interconnects

Crosstalk between two channels is defined as the ratio of the output of the first channel, with no input signal divided by the output of the second channel excited by an input signal. In dB the crosstalk from second channel to first channel is defined as

$$XT = 20 \log \frac{v_{o1}}{v_{o2}} \text{ dB}$$

where v_{o1} is the output of the channel 1 and v_{o2} is the output of the channel 2. Ideally, the crosstalk between channels that are electrically unconnected should be zero. However in the case of coupled transmission line, crosstalk depends on the operating frequency, physical dimensions, and the material used. It occurs due to the coupling effect caused by the mutual capacitance and mutual inductance of the aggressor and victim. Figure 3.2 represent a general two channel system. The end of the victim closest to the driver of the aggressor is called the near end and the end of the victim closest to the receiver of the aggressor is called far end. Channel 1 is excited by an input signal and far end is terminated to ground through a resistor. Similarly for the channel 2 both the ends are terminated to ground through a resistor.

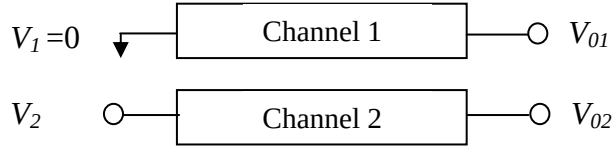


Figure 3.2 General two-channel systems [7]

Generally two types of crosstalk are formed in the victim line, near-end crosstalk (NEXT) and far-end crosstalk (FEXT). NEXT is defined as the crosstalk of the victim nearest to the driver and FEXT is defined as the crosstalk of the victim farthest away from the driver. The total crosstalk is the sum of the effects of the mutual capacitance and inductance in response to the input signal.

3.1.2 Frequency-domain analysis

Figure 3.3 shows a general two-port network characterized by its scattering parameters (S-parameters). The device package S-parameter is extracted by using HFSS or Sentinel™-PSI tool. An ac input voltage of 1.425V is applied at the corresponding input of DQ0 (aggressor) of the device package. A logarithmic frequency sweep from 10Hz to 8000MHz is applied at the input of the aggressor. (This is ten times as the fundamental frequency -800MHz). The far-end of the aggressor is terminated by 50/120 Ohm (Thevenin termination). Both ends of the victim line (DQM) is also terminated with the same resistor value. The spacing between the aggressor and victim is 15um, width of DQ0 and DQM is 15um (Data from device mcm file). By using the above equation FEXT and NEXT is calculated.

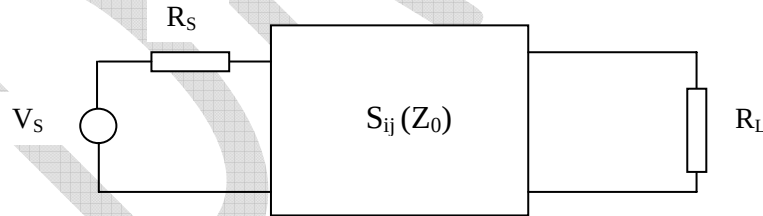


Figure 3.3 General two-port networks

3.1.3 Modeling the interconnects

The physical structure of a coupled microstrip transmission line can be modeled by full-wave electromagnetic analysis. The coupled lossless transmission line functions are [7]

$$-\frac{d}{dz}\begin{pmatrix} V \\ I \end{pmatrix} = \begin{pmatrix} 0 & Z \\ Y & 0 \end{pmatrix} \begin{pmatrix} V \\ I \end{pmatrix}$$

$$Z=j\omega\mathbf{L} = j\omega\begin{pmatrix} L_s & L_m \\ L_m & L_s \end{pmatrix} \text{ and}$$

$$Y=j\omega\mathbf{C} = j\omega\begin{pmatrix} C_s & -C_m \\ -C_m & C_s \end{pmatrix}$$

where L_s and L_m are the self and mutual inductance and C_s and C_m are the self and mutual capacitance respectively.

There are different methods for modeling the coupled microstrip transmission line.

- Walker's formulas
- HSPICE model
- Frequency-domain model

For modeling the coupled transmission line, we use 2D field solver implementation using W-element modeling. W-element modeling will be more efficient and accurate compared to other modeling of transmission line. The W-element statement for a two conductor is

W1 N=2 pad0 pad1 0 out0 out1 0 RLGCMODEL= example_rlc l=0.01

The corresponding circuit component value is dumped in the RLGCMODEL file. The L and C matrices values are obtained from Walker's formula and the length of the coupled microstrip can be used for obtaining the circuit components [7].

3.1.4 Shielding/Guard Trace

The crosstalk can be reduced by increasing the spacing between the aggressor and victim. However when the separation between the traces decreases will cause more mutual inductance and crosstalk for high-density and high speed PKG design. By adding a guard traces or shielding between the aggressor and victim will change the capacitive and inductive coupling to reduce crosstalk. Since a single guard trace will act as a noise source, therefore it has to be connected to ground, which will reduce the noise by eliminating the interference between the aggressor and victim. Figure 3.4 shows the topology of the guard trace, by terminating both ends to the ground. Figure 3.5 and 3.6 shows the simulation result of the guard trace with two terminated ends connected to ground and with different spacing between the aggressor and victim. This is implemented in 2D field solver. From the figure it is seen that the crosstalk will reduce with shielding and with increased spacing.

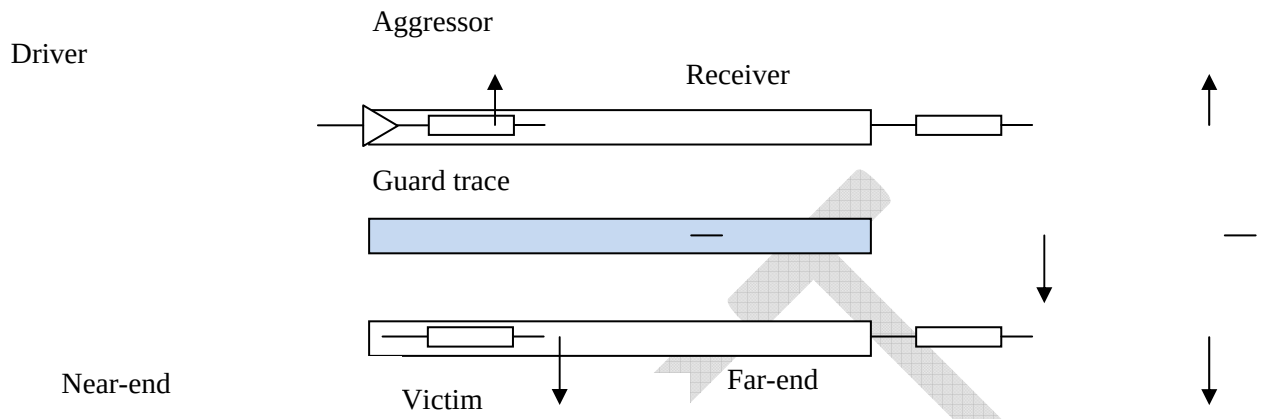


Figure 3.4 shows the guard trace

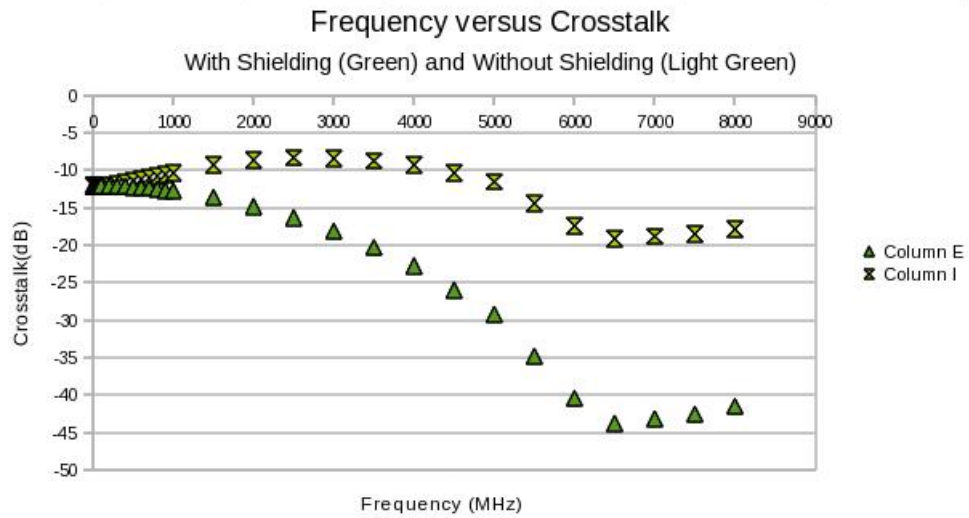


Figure 3.5 Simulation result with and without shielding

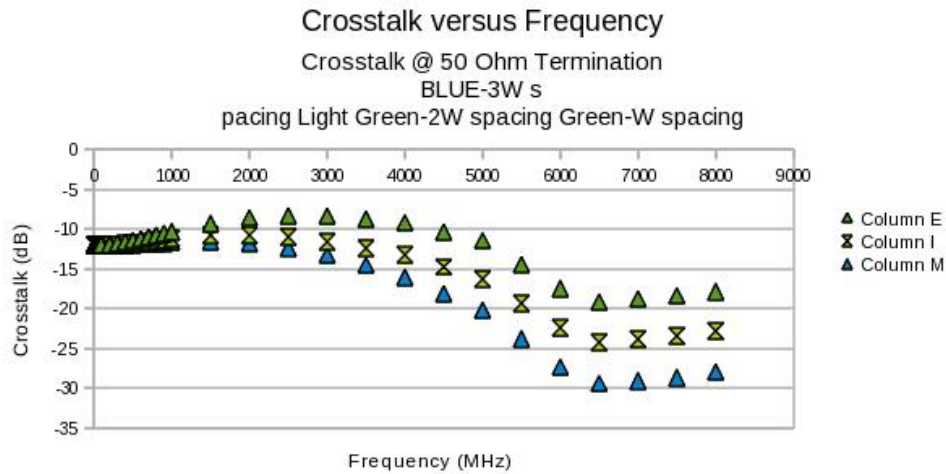


Figure 3.6 Simulation result with different spacing

3.1.5 Simulation Result

Figure 3.7 and 3.8 shows the crosstalk analysis result in frequency domain for different packages in the near end and far end with 50 Ohm and 120 Ohm termination. From the figure it is seen that crosstalk phenomenon varies significantly with the operating frequency. The analysis shows that near end crosstalk will be more compared to far end crosstalk. The same frequency domain crosstalk analysis is performed in a different package. The S-parameter macro model is extracted using 3D electromagnetic field solver (Sentinel™-PSI) and the analysis is performed using HSPICE® simulator. The frequency-domain results are plotted in figure 3.9 and 3.10. Table 3.1 shows the difference in crosstalk between frequency domain and time domain analysis.

Frequency =800MHz: 50Ohm Termination			
Frequency Domain Analysis		Time domain Analysis	
FEXT(dB)	NEXT(dB)	FEXT(dB)	NEXT(dB)
-38.44	-21.95	-33.21	-21.22

Table 3.1 shows the crosstalk difference between two domains

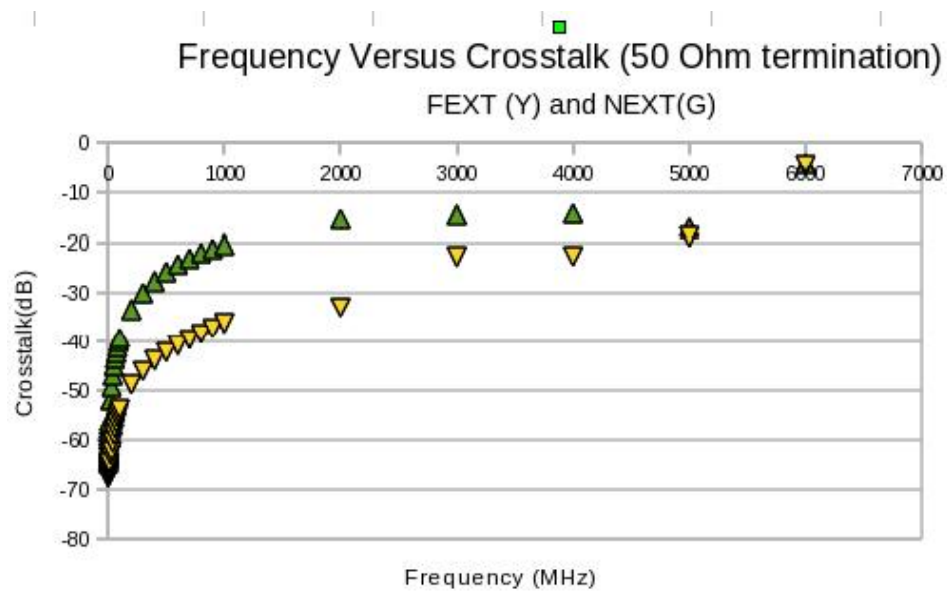


Figure 3.7 FEXT and NEXT with 50 Ohm termination

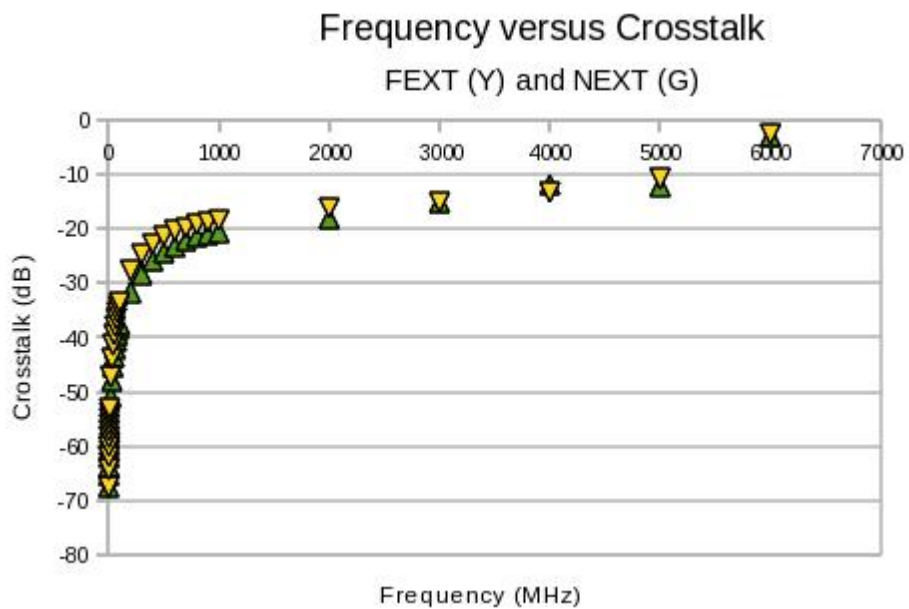


Figure 3.8 FEXT and NEXT with 120 Ohm termination

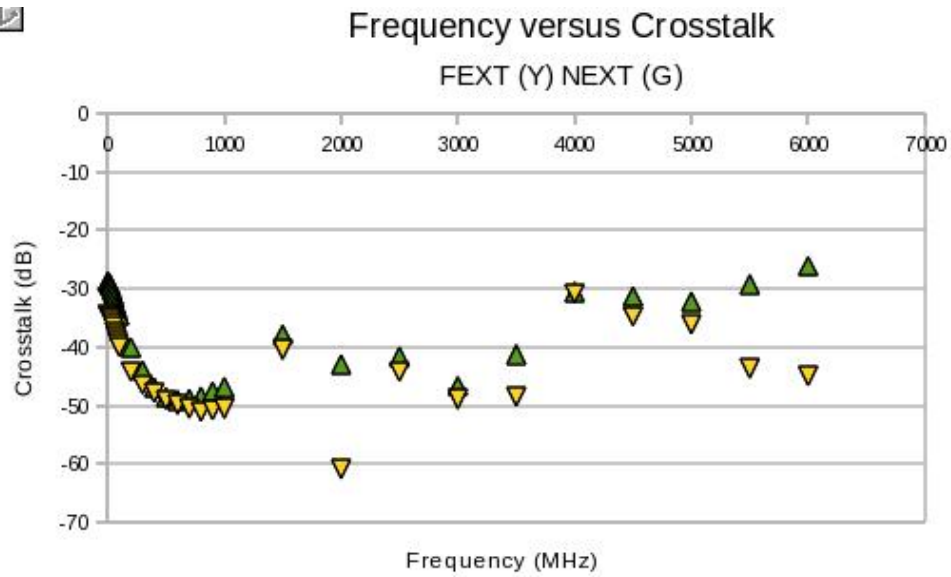


Figure 3.9 FEXT and NEXT with 50 Ohm termination

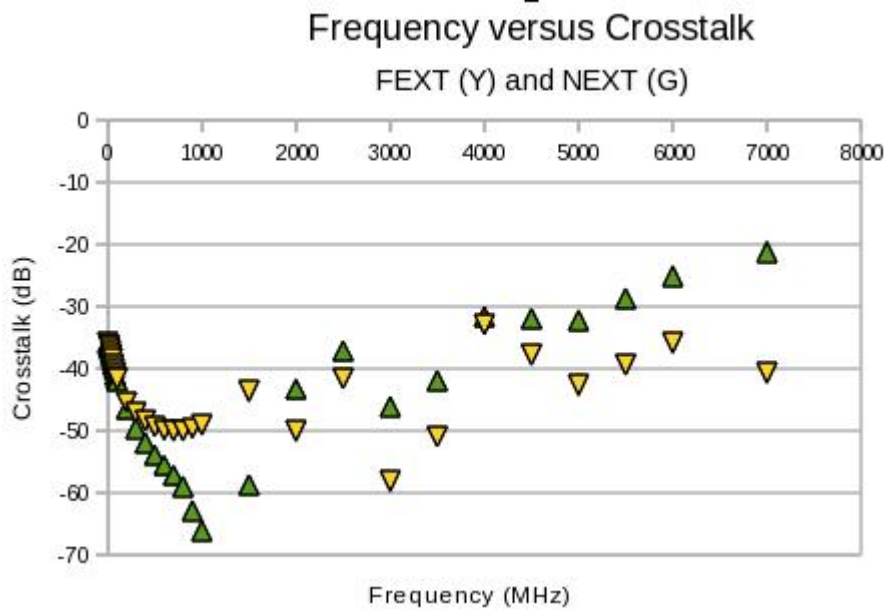


Figure 3.10 FEXT and NEXT with 120 Ohm termination

3.2 Jitter Analysis of different packages

Figure 3.11 and 3.12 shows the eye diagram of different packages. After extracting the S-parameter from 3D electromagnetic field solver, the transient analysis is performed in HSPICE®. From the eye diagram the jitter value for PKG1 is 59.12 ps and PKG2 is 22.30ps with the same Thevenin termination of 50 Ohm. This jitter value is used for the budget calculation of DDR3 interface.

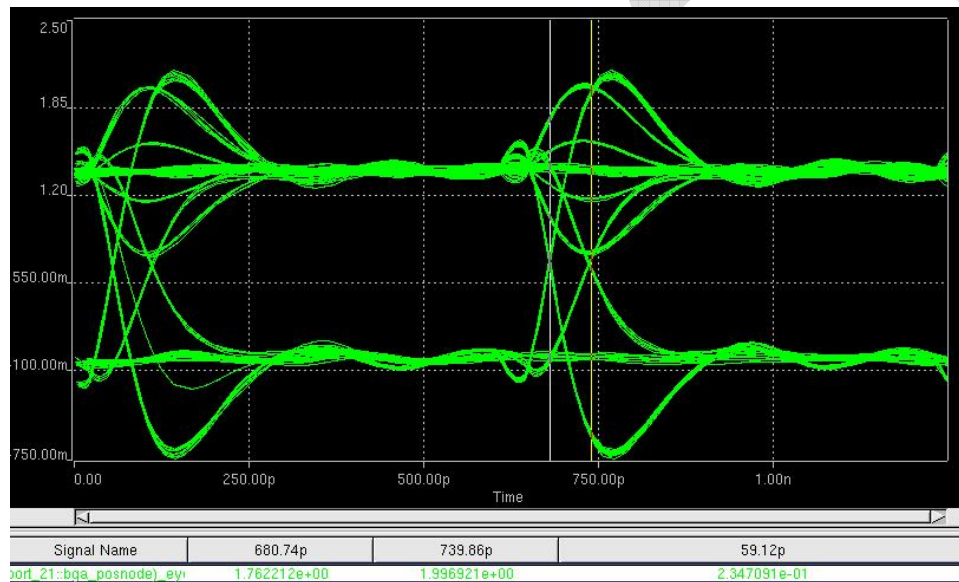


Figure 3.11 Eye diagram of PKG1

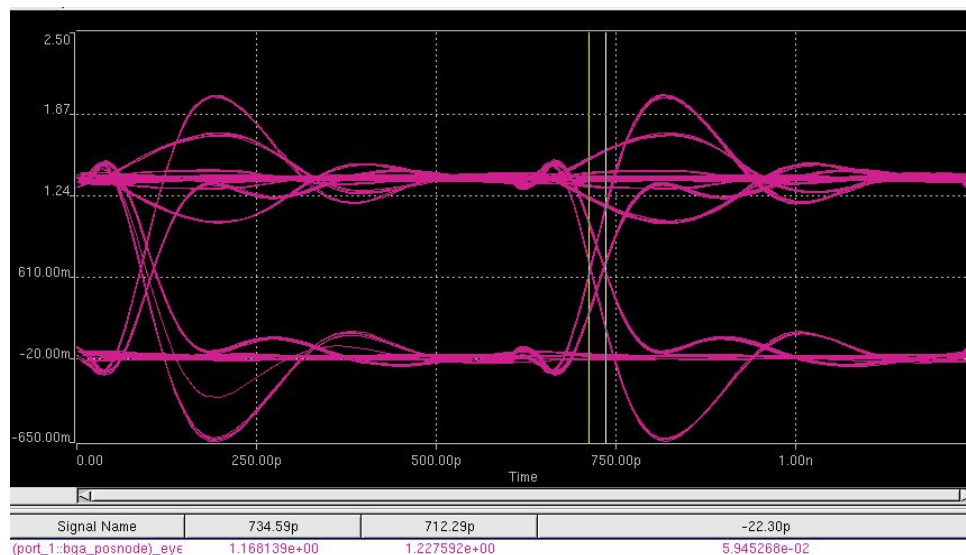


Figure 3.12 Eye diagram of PKG2

CHAPTER 4

DDR3 INTERFACE ANALYSIS USING HSPICE®

In DDR2 to DDR3 comparison, the greatest difference is the topology used from “Balanced-T” to “Fly-By” architecture. The Balanced-T topology is used to balance the delays to each SDRAM device. To down side of balanced T-line topology is that it will introduce additional skew because of the addition of multiple stubs and stub lengths for each individual net. The addition of multiple loads to address/control nets limits the bandwidth [8]. Skews between the address/control and data nets also introduce bandwidth limitations. The DDR3 “fly-by” architecture provides a benefit to layout and routing of control and address signals. In this topology each respective signal from the controller is sequentially routed from one SDRAM to the next thus eliminating the reflections associated with the stubs.

The main features of Texas Instruments (TI’s) DDR3 controller are Error Correction (ECC) which allows automatic detection and correction of single and double-bit errors, Read leveling, Write leveling, Change in pre-fetch size, ZQ calibration, and a reset pin [9]. The memory controller automatically corrects the delay skew between SDRAMs during write and read leveling. The ZQ calibration is used to control the On-Die-Termination (ODT) values and output drivers of the SDRAM. It is controlled by using a precision 240Ohm resistor. The differential DQS improves noise immunity and allows for longer signal path without compromising signal integrity.

A variety of software tools exists to model the high performance interfaces. The most common tool is SPICE® or HSPICE®. This analysis device uses two 32-bit DDR3 interfaces operating at 800 MHz. The DDR3 interface in this device comprises of 8-bit Data macro which consists of PHY data macro, DLL and the IOs and 11/9 + 2-bit Command macro which consist of PHY command macro and IOs integrated together. The analysis is done only for the Data WRITE (Transmit mode).

4.1 Block Diagram

Figure 4.1 shows the block diagram of DDR3 interface with the memory. It consists of DDR IOs, Package model, Board model and DDR memory model.

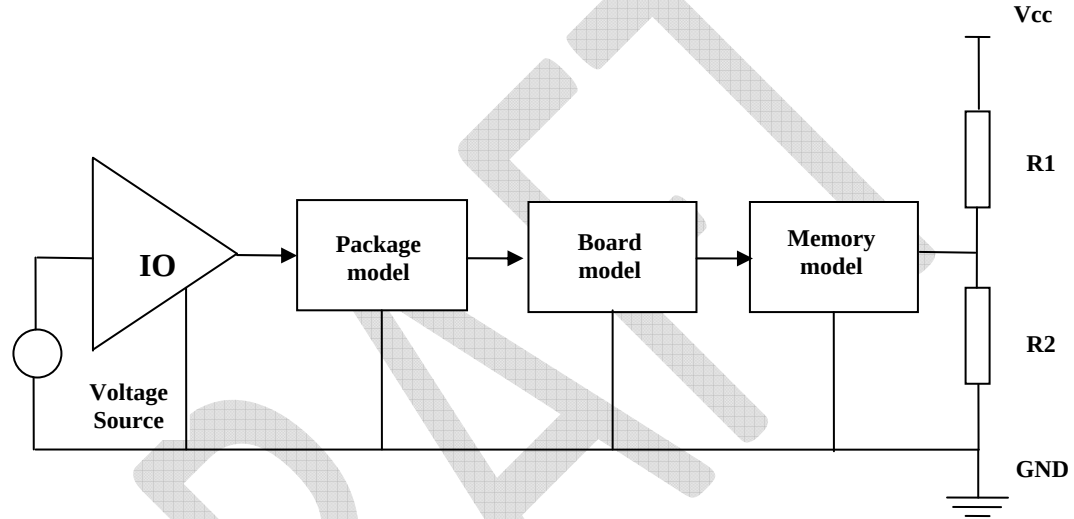


Figure 4.1 Block diagram

4.1.1 DDR IOs

This IO cell is a Process, Voltage and Temperature (PVT) compensated IO that uses binary and thermometer coded scheme for impedance control and on-die termination control. Dynamic and static update of the impedance of the drivers and terminations are possible. For impedance adjustment the IO cell receives a 6-bit binary code as input, which is internally converted to a thermometer code update within the IO cell. The dynamic update must guarantee that the termination must not cause significant added jitter when the impedance is updated. Apart from PTV compensation the driver can be configured to various output impedance levels. The functionality of this IO is capable of configured into various modes of operation. Various operating modes of the IOs are listed in the Table 2.1.

Symbol	Operating mode	Description
Tx	Transmit IO voltage interface signal	This mode can be selected to transmit DDR compatible signals
Rxvref	Receive IO voltage interface signal through Vref based receiver	This mode can be selected to receive DDR compatible signals
Rxvref + ODT	Receive IO voltage interface signal through Vref based receiver with On-Die Termination enabled	This mode can be selected to receive DDR compatible signals at higher speed.

Table 4.1 IO different operating modes [9]

Figure 4.2 shows the Bidi IO macro block schematic. This has primarily a transmitter, a receiver circuitry, with a tristate enabled control and a power-down feature to gate the transmitter and receiver respectively in order to drive the pad. This IO has internal circuitry for adjusting the on-die termination to full/half Thevenin termination for better signal integrity on the receiver end with proper mitigation of far-end Xtalk effects. The on-die termination is adjusted through odt* pins. The receiver is a differential comparator used for receiving the data from the memory with pad connected to the positive terminal and Vref connected to the negative terminal [9]. Normally Vref is tied to half of the IO voltage. Similar to the driver, the receiver is also ODT controlled for better system level signal integrity and performance.

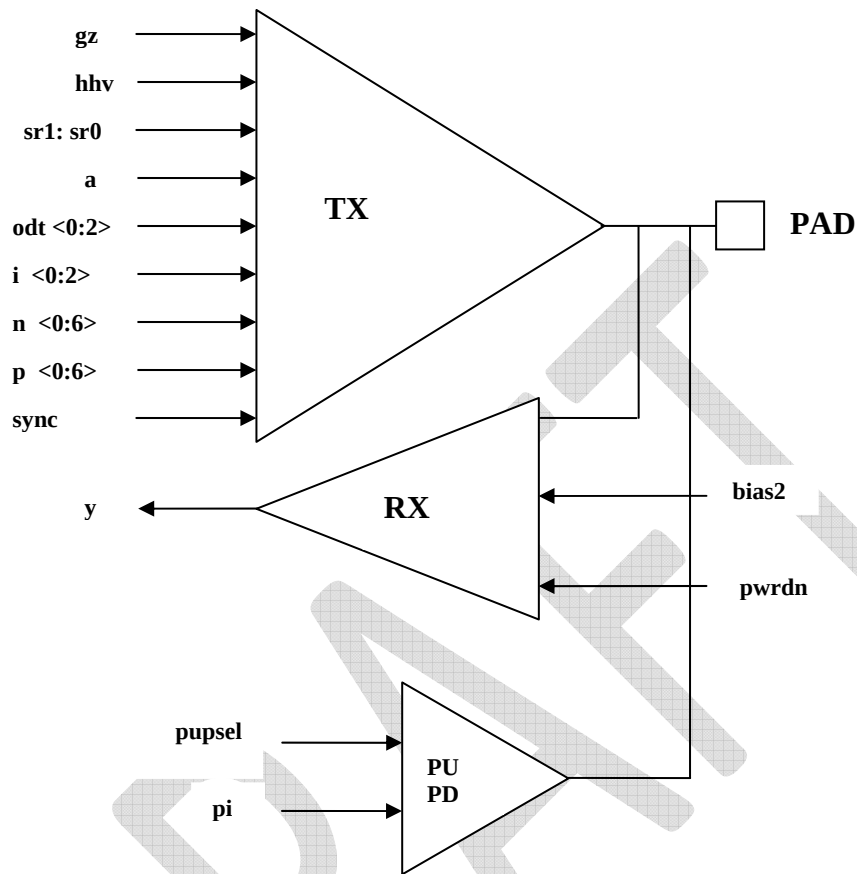


Figure 4.2 IO block schematic [9]

The power-up sequencing of the IO cell is independent; either core power supply (VDD) or IO power supply (VDDS) is powered up first. To avoid huge power-up current when VDDS is powered first the hhv pin should be tied to VDDS so that the output buffer is tri-stated and the pad is pulled low through a weak resistor.

Symbol	Description	Interface	Voltage
VDDS	Output supply voltage	1.5V DDR3	1.5 V
VDD	Core supply voltage	NA	NA

Table 4.2 Operating voltage levels requirement at package-pin/BGA [9]

4.1.1.1 Transmit mode (Tx)

This mode can be selected to transmit DDR compatible signals. In this mode the power down signal will be set to high to save static power.

hhv	gz	a	pad
1	X	X	Weak low
0	1	X	High impedance
0	0	0	0
0	0	1	1

Table 4.3 shows the driver functionality [9]

In the transmit mode of operation, the driver is provided with pin controls to program the output driver impedance and slew rate. The pins $ip<0:2>$, $in<0:2>$ and $i<0:2>$ are used to program the output impedance of the driver. The output impedance of the driver can be varied by the input settings of the 7-bit PVT code ($p<0:6>$ and $n<0:6>$). For getting minimum noise/frequency trade off the slew rate of the output signal is also programmed using the slew rate control pins ($sr0$ and $sr1$). The driver supports real-time dynamic Voltage, Temperature and Process (VTP) compensation. The VTP controller sends out VTP information bits ($p<0:6>$, $n<0:6>$) which are then decoded by code decoder block. The decoded bits control the impedance or drive strength of the driver based on impedance selection bits and VTP variations. The synchronization signal 'sync' is required to support dynamic impedance compensation and it is a clock signal for synchronizing p/n codes and is generated within the VTP controller [9].

4.1.2 Package model

This device uses 6-layer Flip Chip Ball Grid Array (FCBGA) package which replaces the wirebond package as the demands of high speed signaling interfaces have exceeded the capabilities of standard wirebond package. Thicker packages with additional build up layers offer better designed power distribution networks and lower routing density to minimize crosstalk. The 6-layer design is clearly superior from an electrical perspective allowing high signaling speeds but it is more expensive compared to 4-layer FCBGA [10]. High Frequency Structure Simulator (HFSS) tool is used for modeling the package. For the other power nets VDDS and VDD, only the ports required for an IDID macro is used. The DATA signals (DQ0-DQ7, DQS/DQSN and DQM) and ADDR/CMD signals are modeled

up to 3GHz. The S-parameters can be obtained from HFSS after that the extraction converges. This can be directly used in HSPICE®.

The IO ring parasitic and decoupling capacitance is modeled. The corner specific resistors were modeled from the metal layer dimensions. The capacitance and Equivalent Series Resistance (ESR) of the power pad cells is modeled using REDHAWK APL utility from Apache. Additional decap estimation is done on the preliminary package. The bump parasitic is extracted using STAR-XT and signal nets as R and C in the SPICE setup.

4.1.3 Board model

The PHY BGA assignment depends on the Printed Circuit Board (PCB) routing topology and DDR3 memory placement. Since DDR3 memory pin-out is fixed, the system designer must design a PCB layout topology to minimize the routing complexity and PCB area constraints [11]. This device uses 4-layer PCB stack up. Signal routing is constrained to two layers and by selecting the layout topology for the signal routing the routing congestion is reduced which minimizes the crosstalk and phase mismatch. The board model for this device is extracted using HFSS. For DATA the signal routes in the board matched within 2.5mm. The ADDR/CMD layout in the board is large; the HFSS takes lot of time for convergence. So W-element modeling is used for the board traces. The result used for the W-element modeling was optimistic; an additional margin of 50% is used for compensating the result.

4.1.4 DDR3 memory model

The DDR3 SDRAM is a high speed dynamic random access memory and is internally configured as an eight bank DRAM. It uses an 8n pre-fetch architecture to achieve high operation speed. The interface is designed to transfer two data words per clock cycles at the I/O pins. Read and write operation to DDR3 SDRAM is burst oriented or a chopped burst of four in a programmed manner [12]. The On-Die-Termination (ODT) is an additional feature of DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQSN and DM and is controlled through ODT control pins. The ODT feature is designed to improve the signal integrity of the memory channel.

Two memory loads are used for each DQ signal. The ODT values of 60Ohm used for the active memory and 120 Ohm is used for the idle memory. The load capacitance values are taken from the MICRON Input/output Buffer Information Specification (IBIS) model and are also depend on the ODT settings.

4.1.5 Data Write Simulation

4.1.5.1 IO Setup

- Slew rate setting used: sr1=0,sr0=0 (fastest)
- Output impedance settings: 50Ohms (i2=1,i1=0,i0=0)
- On-Die Termination settings (odt2=0,odt1=0,odt0=0)
- Tristate control during power sequencing (hhv) =0
- Synchronization signal for output impedance update from VTP-controller (sync) =0
- Tri-state control (gz) =0
- Inhibits weak pull-up /pull-dn (pi) =0

4.1.5.2 Input Vectors

The input used for running the HSPICE® simulation is Pseudo Random Binary Sequence (PRBS) input vectors. In this vector the values of an element is independent of the values of the any other element and the values are deterministic. After N-element the pattern will repeat itself. It is generated as the output of a linear shift register. The simulation is run for 125ns with PRBS input vector applied to all the DQ and DQM signals. The ODD mode Jitter values are calculated, which means all aggressor are switching in the same direction and the victim line is switching in the opposite direction.

PRBS example:

```
param td=0n tr =40ps tf=40ps ts=0.625n datarate=1600e6
Vdq7 indq7 0 PAT PVDD PVSS td tr tf ts b1 rb=1 r=39
b0111101010001001110000011001011011110101 rb=1 r=1
b1000010101110110001111100110100100001010 b1 rb=1 r=39
```

4.1.6 Result: The worst case timing (T=125, VDD=0.95v and VDDS=1.425v) is observed for the signals switching opposite to the other signals. Figure 4.3 below shows the eye diagram for the DQ0 and DQ7 signals at the Far End side (memory). The setup and hold jitter value is calculated from the data (DQ7) and differential clock (DQS0 and DQSN0). The output signal and differential clock signal waveform are show in figure 4.4. The maximum frequency possible from the current WRITE simulation is **720MHz**.

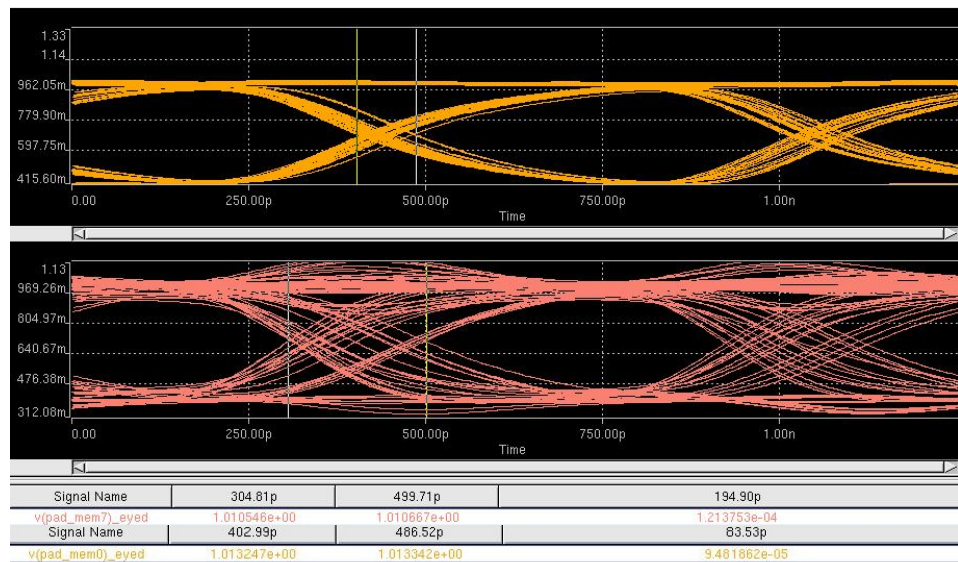
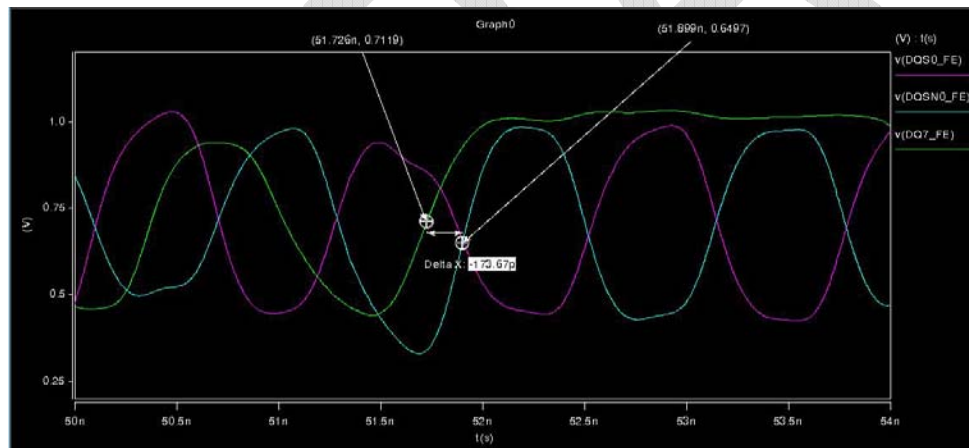
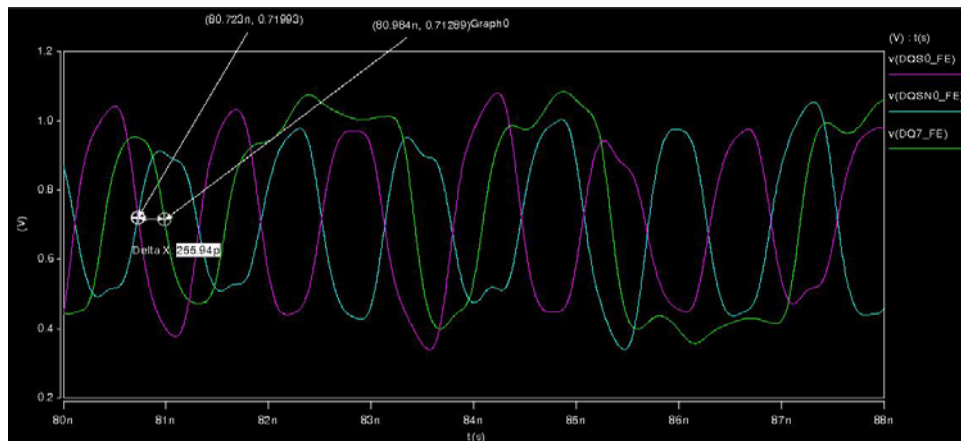


Figure 4.3 Eye diagram of PAD_MEM0 and PAD_MEM7 (FE signal)



$$\begin{aligned}
 \text{Setup jitter} &= \text{Ideal setup time} - \text{actual setup time} \\
 &= 0.3125\text{ns} - 0.17367\text{ns} \\
 &= 0.13883\text{ns} \\
 &= 138.83\text{ps}
 \end{aligned}$$



$$\begin{aligned}
 \text{Hold jitter} &= \text{Ideal hold time} - \text{actual hold time} \\
 &= 0.3125\text{ns} - 0.255\text{ns} \\
 &= 0.0575\text{ns} \\
 &= 57.5\text{ps}
 \end{aligned}$$

Figure 4.4 Output signal and differential clock signal

CHAPTER 5

DDR3 INTERFACE ANALYSIS USING SENTINEL™-SSO

5.1 Introduction

Sentinel™-SSO (Simultaneous Switching Output) is a high capacity signal-integrity analysis tool for Input/output (IO). It can simulate the entire bank of IO (eg: DDR) under simultaneous switching condition with good accuracy. The main challenge of Sentinel™-SSO is to drive off-chip loads in package and PCB. The switching current produced at the chip output driver will be very high compared to the switching current of signals inside the chip. The simultaneous switching of multiple output drivers will produce noise on the IO supply and ground. Sentinel™-SSO simulation covers all sources of noise by accurately modeling IO cells, decoupling capacitor, power distribution network (PDN), crosstalk noise coupling, package, and PCB parasitic [13].

Sentinel™-PSI (Power and Signal Integrity) is a fully integrated, power integrity (PI) and signal integrity (SI) analysis tool for packaging and PCB designs. Using 3D-modelling and finite element method (FEM) analysis, it performs 3D- full wave model extraction for SI analysis. The main features of Sentinel™-PSI are

- 3D-full wave network extraction for SI and PI analysis.
- DC (static), AC and transient analysis.
- Electromagnetic Interference (EMI) simulation.
- Macro model generation based on S-parameters.
- Wide-IO channel-model generation for SSO analysis of package and PCB

5.2 Sentinel PSI-SSO link

PSI-SSO link provides an interface between Sentinel™-PSI and Sentinel™-SSO for noise and timing analysis of an IO channel across Die, package (PKG) and PCB system. It comprises two parts, SSO Channel Builder (SCB) in Sentinel™-PSI and Channel Model Extractor (CME) in Sentinel™-SSO. The SCB generates an entire channel model with 3D-full wave electromagnetic characteristics. The channel model includes both signal and Power/Ground (PG) nets associated with the IO interface from both package and PCB. From the channel builder, the model extractor extracts an optimized channel model customized for the user specified SSO simulation, so that it will significantly reduces the simulation time with maintaining the accuracy. The PSI-SSO link provides the following advantages.

- 3D-full wave accuracy for PKG/PCB

- Automated connection for partial channel models
- Speed up SSO transient simulation

5.3 Sentinel™-SSO-Functional Overview

5.3.1 Sentine™-SSO subsystem

Figure 5.1 shows a Sentinel™-SSO subsystem. It consist of IO, on-die PG network, package and PCB models. Sentinel™-SSO generates the subsystem by building macro models of the IO cells, extracting the PG net, adding the package and PCB models.

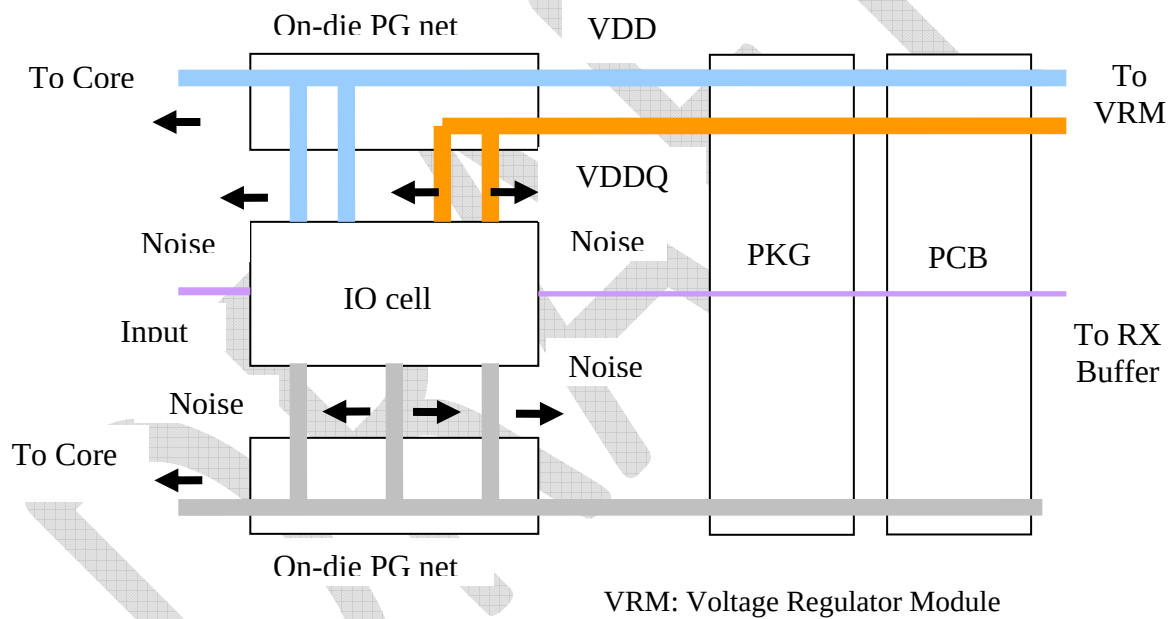


Figure 5.1 Sentinel™-SSO subsystems [13]

5.3.2 Sentinel™-SSO workflow

Figure 5.2 shows the functional block diagram of Sentinel™-SSO workflow. The inputs required for running Sentinel™-SSO are

- Physical Design of the IO subsystem (described by GDS/LEF/DEF files)
- IO spice netlist
- Package and PCB SPICE models (these models can be distributed RLCK model or broadband S-parameter model)

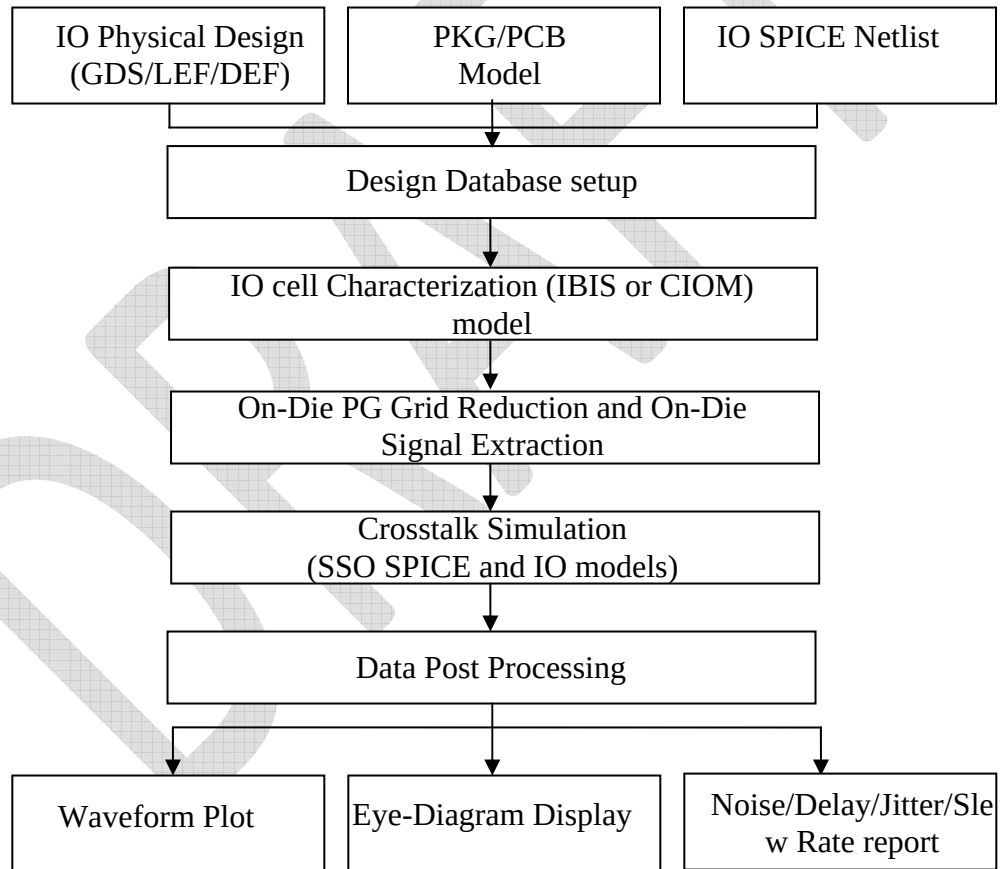


Figure 5.2 Functional Block diagram of Sentinel™-SSO [13]

After completing the setup, Sentinel™-SSO executes the analysis according to the advanced Macromodeling flow (AMF). The main advantage of AMF is it will consider the effect from total IO bank (not the nearest neighboring IO cells), PG and signal coupling in the package/PCB. Figure 5.3 shows advanced macromodeling flow diagram. It will first build Chip IO macro models (CIOM) of all the IO cell instances from the converted user-supplied design files. It generates the models by applying user specified stimulus and connecting the PKG/PCB model to the IO cell instance [13]. CIOM are non-linear IO cell macro model that achieve transistor level accuracy, reduce circuit complexity, fast and high capacity SSO analysis. From the physical design data Sentinel™-SSO generates an equivalent SPICE model of the on-die PG grid. The final step of Sentinel™-SSO is to assemble the following components and do the simulation. The components are

- Transistor level victim and neighbor IO cells
- CIOM power aggressor models of the other IO cells in the bank
- User-defined input stimuli
- PG SPICE model
- Extracted signal model
- Original coupled signal and PG PKG/PCB SPICE model.

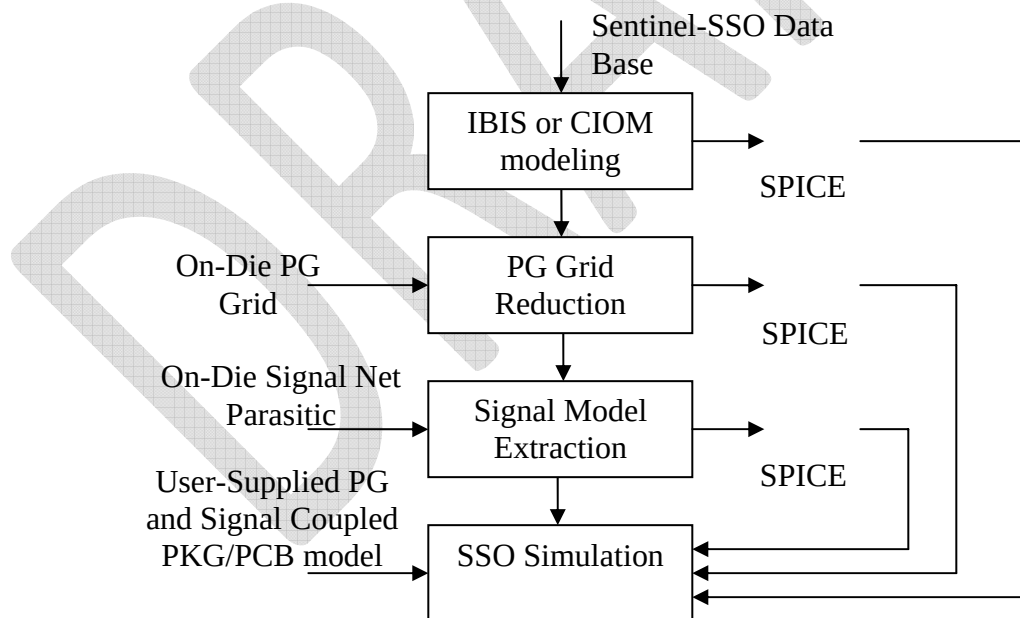


Figure 5.3 Advanced Macromodeling Flow (AMF) diagram [13]

Sentinel™-SSO generates the reduced on-die PG grid model from the exposed PG pads, the internal IO cell connections to the PG pins that connect to PKG PG nodes, the transistor-level IO PG pins and CIOM models [13]. CIOM model replaces all the transistor level non-victim signals which is not the neighbor aggressor IO cells in the IO bank which reduces the simulation time for the SSO. These distant transistor-level aggressor IO cells cause less crosstalk effect on the victim IO. Near neighbor aggressor cells remains as transistor level model and those IO behaves as crosstalk aggressors. These can be controlled through Tcl commands during SSO simulation.

Sentinel™-SSO generates the reduced on-die PG grid model and it has high equivalency with the original PG grid RLC model. This will reduce the complexity, which will enhance the capacity and performance of Sentinel™-SSO.

5.4 Data collection and preparation

A Tcl-scripted command file with user specified design data and simulation conditions set in a configuration file executes the Sentinel™-SSO flow. The inputs required for running Sentinel™-SSO are

- Design layout files (Cadence Design Exchange Format –DEF)
- Cell library files (Cadence Library Exchange Format-LEF)
- Technology file that defines the dimensional and material properties of the design layers.
- Timing library files or PG arc files.
- GDSII-format cell physical layout file
- Apache Power Library (APL) files
- Decoupling capacitor parameters.
- IO SPICE netlist and
- Bias setting

Sentinel™-SSO supports three types PKG/PCB models.

- Decoupled
- Coupled and
- Prototyped

Table 5.1 shows how Sentinel™-SSO uses the PKG/PCB model types. [13]

Model type	Model Description
DECOUPLED	Signal and PG SPICE models decoupled
COUPLED	Signal and PG SPICE model coupled
PROTOTYPED	Package/PCB model unavailable; simple decoupled signal and PG models generated for the simulation.

These models have to be specified in the configuration file. In our design for SSO simulation, a Coupled model is used. It provides faster execution with good simulation accuracy. The method for modeling a coupled PKG/PCB is to use PSI-SSO link, first combine the separate PKG and PCB models in Sentinel™-PSI and then the resulting channel model is used in the Sentinel™-SSO simulation.

5.5 Sentinel™-PSI-Functional Overview

Sentinel™-PSI imports the physical data base of a design from various CAD tools. It discretizes the 3D physical model and then solves the Maxwell's equation to extract resistive SPICE model or broad band S-parameter from the geometry. Basically for generating the accurate 3D physical model, it generates the electric and magnetic field characteristics for the package and PCB. Sentinel™-PSI 3D extraction produces highly accurate S-parameter values that closely model the actual physical design [14]. The Sentinel™-PSI provides the following types of output.

- S-parameters as touchstone file
- SPICE wrapper around the touchstone file
- SPICE macro model which contains the equivalent circuit of the S-parameters.

Sentinel™-PSI is full wave electromagnetic field solver, offers accurate, high performance, high capacity result. In the case of quasi-static field solver, the displacement current is not included when solving Maxwell's equation, which will lose the accuracy in very high frequency (GHz). Sentinel™-PSI provides the following types of analysis.

- DC resistance
- S-parameter extraction
- Transient analysis and
- Electromagnetic Interference (EMI) analysis

5.6 S-parameter extraction

SI analysis is to extract the network parameter of power and signals over a wide range of frequency. Sentinel™-PSI applies 3D full wave and Finite Element Method analysis for S-parameter extraction. It will give accurate models over a wide range of frequency (100 Hz to few GHz) with less simulation time. It will export the S-parameter as a touch stone file for further SPICE simulations. It will also generate a macromodel from the S-parameters and its behavior is almost identical to that of the original S-parameter model. Sometimes the S-parameter model will not converge, since it is hard to find the dc operating point. However the macro model is easily converged and it is friendlier for SPICE simulation.

Figure 5.4 shows the input port voltage (DIE side) reflection coefficient (S_{11}) of the analysis device over the frequency range. S-parameters can be viewed using S-utility application software. The reflection coefficient value will be normally in between 0 and 1.

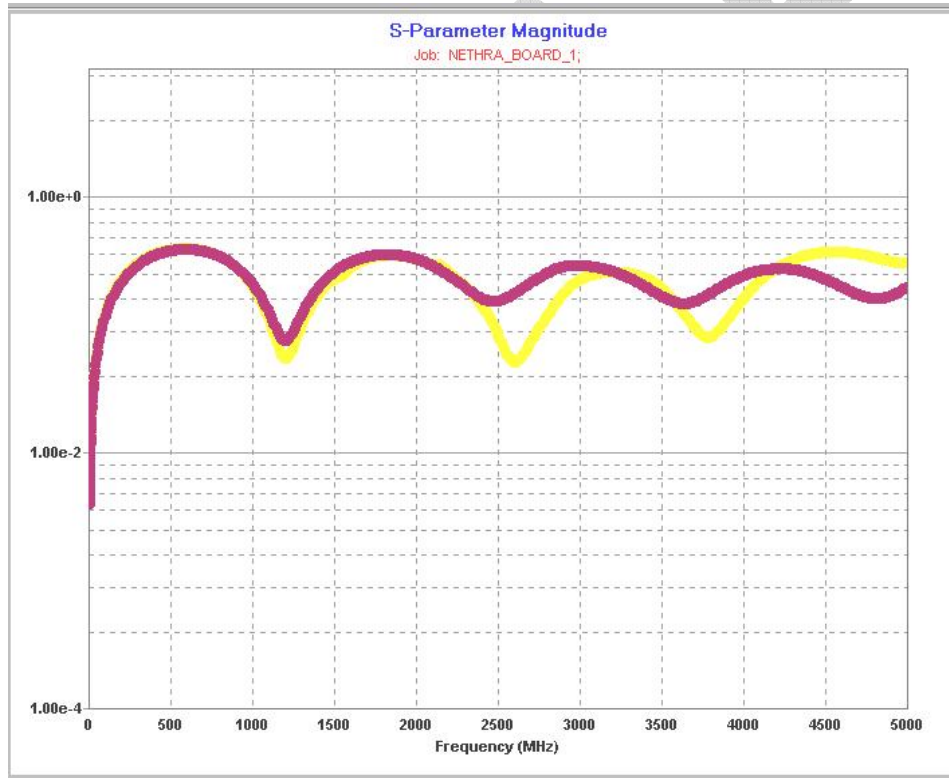


Figure 5.4 Input reflection (S_{11}) Coefficient of D0 and D7

5.7 Simulation Result

Figure 5.5 below shows the eye diagram for the DQ0 and DQ7 signals at the Far End side (memory), which is almost same as the result obtained through HSPICE® simulation. The main advantages of Sentinel™-SSO compared to HSPICE® simulation are

- Capacity for full-chip IO SSO analysis
- Run time will be less compared to HSPICE® and easily converged.
- Tool Command language (Tcl) script based execution and Graphical User Interface (GUI) based viewing of results, analysis and debugging.
- Waveform and eye-diagram display.

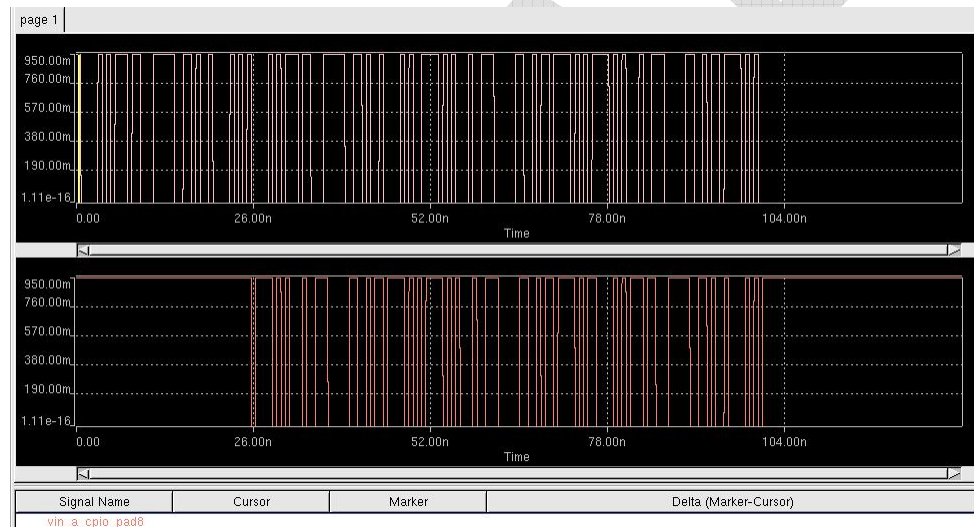


Figure 5.5(a) PRBS input waveform

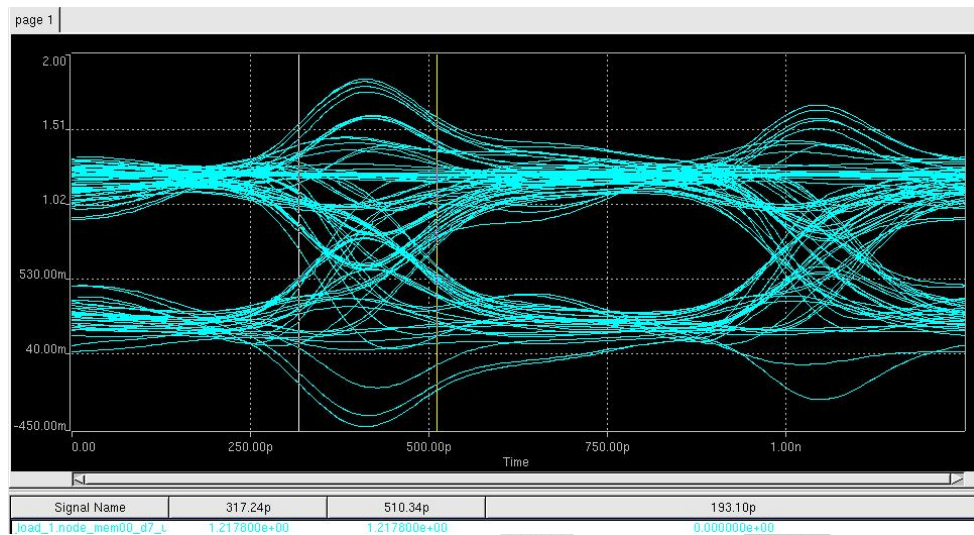


Figure 5.5(b) Eye-diagram of victim signal (DQ7) at Far end.

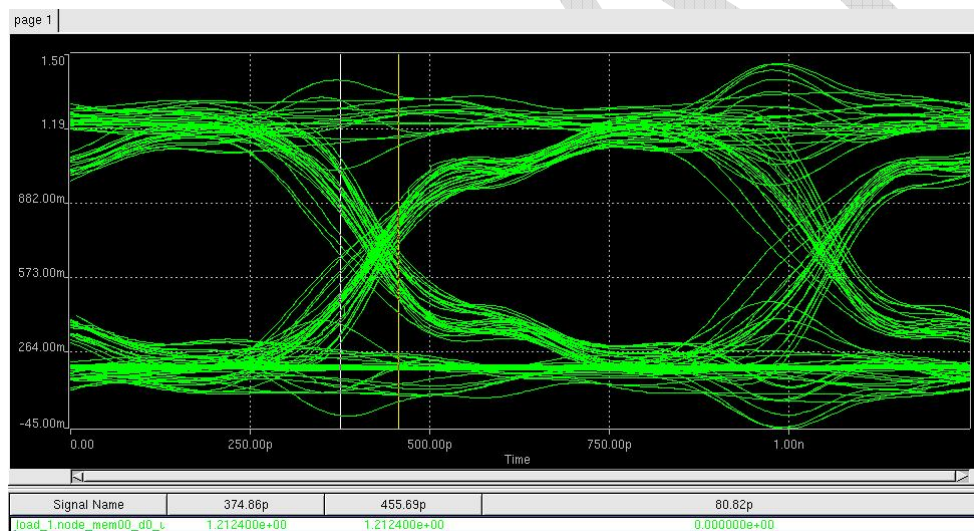


Figure 5.5(c) Eye-diagram of aggressor signal (DQ0) at Far end.

Table 5.2 shows the simulation comparison result between Sentinel™-SSO and HSPICE®.

	Extraction: HFSS Simulation: HSPICE®	Extraction: Sentinel™-PSI Simulation: Sentinel™-SSO
DQ0 FE Eye-diagram	83.53ps	80.82ps
DQ7 FE Eye-diagram	194.90ps	193.1ps

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

The simulation examples and results within this thesis have shown how the design of the package and board of the entire DDR3 sub-system can adversely affect the signal integrity of the link.

First we analyzed a 4-layer PCB implemented in 2D field solver and jitter analysis in time domain is performed by varying track dimensions, microstrip versus stripline geometry and input pattern. The analysis result shows that when the trace length increases, the jitter value will increase approximately 3ps per inch. The delay introduced is approximately 180ps per inch. The recommendation for reducing the jitter is to increase the spacing between the traces which will reduce the jitter by approximately 1ps per mil. It is also recommended to provide shielding/guard trace which will reduce the deterministic jitter. However this will introduce routing congestion and waveform distortion for the aggressor line. Jitter will be also caused due to the improper terminations and if the termination is not properly, the jitter will increase due to reflection. This can be avoided by properly terminating the receiver side with the characteristic impedance. This thesis discusses about different terminations techniques and the recommendations given to the DDR3 sub-system is to use Thevenin termination.

Next the crosstalk analysis in frequency domain is performed for different design packages (6 L and 7L). The frequency domain analysis is done by extracting the S-parameter model from the package design file (mcm), which is simulated using HSPICE® software. The analysis result shows that near end crosstalk will be more compared to far end crosstalk for the same termination. Crosstalk effect is a frequency dependent phenomenon and this analysis will be more accurate compared to transient analysis. The remedies for reducing crosstalk are to increase the spacing between the aggressor and victim line, and adding the grounded conductor shielding in the victim line. The jitter analysis of different packages is performed and concluded that package jitter will be more compared to board jitter. Using the analysis result for jitter and channel we analyzed a DDR3 sub-system timing budget to verify that the PHY will operate reliably at the target data rate using memory model. The DDR3 PHY and memory interface is designed in a 6-layer ball grid array package and 4-layer PCB. The system achieves a reliable memory operation (WRITE) of 720MHz. The expected frequency of operation

will be 800MHz and there is a 10% reduction in the expected frequency of operation. During the analysis the assumption that all the extraneous parameters are linearly accounted in to the link layer timing calculation, but from a Gaussian distribution curve the effective impact is root-sum-square of the results obtained.

CHAPTER 7

FUTURE WORK

We can extend the analysis for data READ, ADDR/CMD simulations. The comparative study of the performance of different layer FCBGA packages designed to support DDR3 interface and the correlation between simulations and silicon measurements predicts the performance which helps to improve the future decisions based on tradeoffs between cost and performance. The package and board analysis of DDR sub-system can be extended from the current DDR3 (1.6Gbps) to next level of DDR (3.2Gbps). This will be helpful for the timing budget calculation. Analysis can be extended to Wide IO's .Wide IO is used to reduce power and increase the bandwidth at a relatively low cost.

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[19] HSPICE® User Guide: Simulation and Analysis.

DRAFT

APPENDIX A

A.1 2DFS Implementation of stripline

```
.inc 'spice_options.inc'
.inc 'ioring_parasitics.inc'
.inc 'prbs_all_125ns.inc'
.inc 'probe.inc'
.include 'bshtltcscdvvpbfz_nocodeconv.c.cworst.-40.netname'
.include 'ss_eol_125_1.35_50.truecode'
Xbhst0 indq0 gz hhv i0 i1 i2 NN N0 N1 N2 N3 N4 N5 odt0 odt1 odt2 PP P0 P1
P2 P3 P4 P5 pad0 pi pupdsel pwrdrn sr0 sr1 sync y0 vss vss vdd vdds bias2 vdds
vss vss bshtltcscdvvpbfz_nocodeconv
.inc 'qc_max_params_morecap.inc'
.inc 'qc_max_ptv_write.inc'

.param mil2meter=2.54e-5
Rto1 out0 vdds 240
Rto2 out0 gnd 240
.OPTION PROBE POST
W1 pad0 gnd out0 gnd FModel=cond2_sys N=1 l=0.5 delayopt=3
.MATERIAL diel_1 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_2 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_3 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL copper METAL CONDUCTIVITY=57.6meg
.SHAPE rect RECTANGLE WIDTH=0.1016mm HEIGHT=1mil
.LAYERSTACK stack_1
+ LAYER=(copper,1mil), LAYER=(diel_1,3mil), LAYER=(copper,1mil)
+ LAYER=(diel_2,52mil), LAYER=(copper,1mil),LAYER=(diel_3,3mil)
+ LAYER=(copper,1mil)
.FSOPTIONS opt1 PRINTDATA=YES
.MODEL cond2_sys W MODELTYPE=FieldSolver
+ LAYERSTACK=stack_1, FSOPTIONS=opt1
RLGCFILE=onecond_strip_line.rlgc
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(0,30.5mil))
.PROBE v(out0)
.measure vout0_max max par('abs(v(out0))')
.measure vout0_min min par('abs(v(out0))')

.measure peak_vout0 pp par(' abs(v(out0)) ')
.measure TRAN trout trig v(out0) val='vout0_min+peak_vout0*0.1' rise=1
+targ v(out0) val='vout0_min+peak_vout0*0.9' rise=1
```

```
.measure TRAN tfout trig v(out0) val='vout0_min+peak_vout0*0.9' fall=1
+targ v(out0) val='vout0_min+peak_vout0*0.1' fall=1
.tran 10ps 125ns
.end
```

A.2 2DFS Implementation of microstrip

```
.inc 'spice_options.inc'
.inc 'ioring_parasitics.inc'
.inc 'prbs_all_125ns.inc'
.inc 'spicedeckfiles/probe.inc'
.include 'bshtltcscdvpgbfz_nocodeconv.c.cworst.-40.netname'
.include 'ss_eol_125_1.35_50.truecode'

Xbhst0 indq0 gz hhv i0 i1 i2 NN N0 N1 N2 N3 N4 N5 odt0 odt1 odt2 PP P0 P1
P2 P3 P4 P5 pad0 pi pupdsel pwrdrn sr0 sr1 sync y0 vss vss vdd vdds bias2 vdds
vss vss bshtltcscdvpgbfz_nocodeconv
.inc 'qc_max_params_morecap.inc'
.inc 'qc_max_ptv_write.inc'
.param mil2meter=2.54e-5
Rto1 out0 vdds 240
Rto2 out0 gnd 240
.OPTION PROBE POST
W1 pad0 gnd out0 gnd FSmodel=cond2_sys N=1 l=0.5 delayopt=3
.MATERIAL diel_1 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_2 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_3 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL copper METAL CONDUCTIVITY=57.6meg
.SHAPE rect RECTANGLE WIDTH=0.1016mm HEIGHT=1mil
.LAYERSTACK stack_1
+ LAYER=(copper,1mil), LAYER=(diel_1,3mil), LAYER=(copper,1mil)
+ LAYER=(diel_2,52mil), LAYER=(copper,1mil),LAYER=(diel_3,3mil)
.FSOPTIONS opt1 PRINTDATA=YES
.MODEL cond2_sys W MODELTYPE=FieldSolver
+ LAYERSTACK=stack_1, FSOPTIONS=opt1
RLGCFILE=onecond_microstrip.rlgc
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(0,61mil))
.PROBE v(out0)
.measure vout0_max max par('abs(v(out0))')
.measure vout0_min min par('abs(v(out0))')
.measure peak_vout0 pp par(' abs(v(out0)) ')
.measure TRAN trout trig v(out0) val='vout0_min+peak_vout0*0.1' rise=1
+targ v(out0) val='vout0_min+peak_vout0*0.9' rise=1
.measure TRAN tfout trig v(out0) val='vout0_min+peak_vout0*0.9' fall=1
```

```

+targ v(out0) val='vout0_min+peak_vout0*0.1' fall=1
.tran 10ps 125ns
.end

```

A.3 Two transmission line ac analysis

```

.inc 'spice_options.inc'
.param td=0n tr=40ps tf=40ps ts=0.625n datarate=1600e6
*Vdq0 pad0 0 PAT PVDD PVSS td tr tf ts
b1000010101110110001111100110100100001010 rb=1 r=1
b0111101010001001110000011001011011110101 rb=1 r=1 b0 rb=1 r=39
*Vdq1 pad1 0 PAT PVDD PVSS td tr tf ts
b1000010101110110001111100110100100001010 rb=1 r=1
b0111101010001001110000011001011011110101 rb=1 r=1 b0 rb=1 r=39
Vdq0 pad0 0 AC 1.425
.AC DEC 10 10 8000MEG
.PRINT AC VDB(pad0) VDB(out0)
Rtpupad1 pad1 vdds 100
Rtpdnpad1 pad1 gnd 100
*.inc 'prbs_all_125ns.inc'
.inc 'probe.inc'
.inc 'qc_max_params_morecap.inc'
Rout01 out0 vdds 100
Rout02 out0 gnd 100
Rout11 out1 vdds 100
Rout12 out1 gnd 100
.OPTION PROBE POST
W1 pad0 pad1 gnd out0 out1 gnd FSmodel=cond2_sys N=2 l=0.01 delayopt=3
.MATERIAL diel_1 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_2 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_3 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL copper METAL CONDUCTIVITY=57.6meg
.SHAPE rect RECTANGLE WIDTH=15mil HEIGHT=1mil
.LAYERSTACK stack_1
+ LAYER=(copper,1mil), LAYER=(diel_1,3mil), LAYER=(copper,1mil)
+ LAYER=(diel_2,52mil), LAYER=(copper,1mil),LAYER=(diel_3,3mil)
.FSOPTIONS opt1 PRINTDATA=YES
.MODEL cond2_sys W MODELTYPE=FieldSolver
+ LAYERSTACK=stack_1, FSOPTIONS=opt1
RLGCFILE=twoconductor_0.1.rlgc
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(0,61mil))
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(60mil,61mil))
.PROBE v(*)
*.tran 10ps 125ns

```


.end

A.3 Two transmission line ac analysis with shielding

```
.inc 'spice_options.inc'
.param td=0n tr=40ps tf=40ps ts=0.625n datarate=1600e6
*Vdq0 pad0 0 PAT PVDD PVSS td tr tf ts
b1000010101110110001111100110100100001010 rb=1 r=1
b0111101010001001110000011001011011110101 rb=1 r=1 b0 rb=1 r=39
*Vdq1 pad1 0 PAT PVDD PVSS td tr tf ts
b1000010101110110001111100110100100001010 rb=1 r=1
b0111101010001001110000011001011011110101 rb=1 r=1 b0 rb=1 r=39
Vdq0 pad0 0 AC 1.425
.AC DEC 10 10 8000MEG
.PRINT AC VDB(pad0) VDB(out0)
Rtpupad1 pad1 vdds 100
Rtpdnpad1 pad1 gnd 100
*.inc 'prbs_all_125ns.inc'
.inc 'spicedeckfiles/probe.inc'
.inc 'qc_max_params_morecap.inc'
Rout01 out0 vdds 100
Rout02 out0 gnd 100
Rout11 out1 vdds 100
Rout12 out1 gnd 100
Rpad1s1 pad1s1i gnd 1.000E-05
Rpad1s1o pad1s1o gnd 1.000E-05
.OPTION PROBE POST
W1 pad0 pad1s1i pad1 gnd out0 pad1s1o out1 gnd FSmodel=cond2_sys N=3
l=0.01 delayopt=3
.MATERIAL diel_1 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_2 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL diel_3 DIELECTRIC ER=4.50 LOSSTANGENT=0.035
.MATERIAL copper METAL CONDUCTIVITY=57.6meg
.SHAPE rect RECTANGLE WIDTH=15mil HEIGHT=1mil
.LAYERSTACK stack_1
+ LAYER=(copper,1mil), LAYER=(diel_1,3mil), LAYER=(copper,1mil)
+ LAYER=(diel_2,52mil), LAYER=(copper,1mil),LAYER=(diel_3,3mil)
.FSOPTIONS opt1 PRINTDATA=YES
.MODEL cond2_sys W MODELTYPE=FieldSolver
+ LAYERSTACK=stack_1, FSOPTIONS=opt1
RLGCFILE=twoconductor_0.1.rlgc
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(0,61mil))
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(30mil,61mil))
+ CONDUCTOR=(SHAPE=rect, MATERIAL=copper, ORIGIN=(48mil,61mil))
```

```
.PROBE v(*)  
*.tran 10ps 125ns  
.end
```

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