Master of Science Thesis

A 1 MHz Bandwidth, 90 nm CMOS Fractional-N Synthesizer Using Hybrid-ΔΣ-DAC-Based Phase Noise Cancellation Technique for LTE FDD/TDD

By

Dawei Ye

Supervised by Dr. Ping Lu, Lund University

Examined by Prof. Pietro Andreani, Lund University

Department of Electrical and Information Technology

Faculty of Engineering, LTH, Lund University

SE-221 00 Lund, Sweden

To my dear aunt and mother

Abstract

In this project, a 1MHz bandwidth, ΔΣ fractional-N PLL using phase noise cancellation path is designed as the frequency synthesizer for LTE FDD/TDD, where the phase noise cancellation path is composed of a ΔΣ DAC with equivalent 9 output bits. Nevertheless, the actual performance of this phase noise cancellation technique is limited by the mismatch, nonlinear distortion and additive noise in the charge pump and ΔΣ DAC, respectively. Hence some advanced circuit topologies are developed to improve the system performance. At the first, the charges mismatch between the charge pump and current-steering DAC outputs can be decreased by introducing the digital shaped signals which are capable of increasing the overlapped region between their current pulses. Secondly, the timing offset pulses from the retiming circuit are fed to the charge pump in order to avoid the noise folding issue. Finally, a novel hybrid ΔΣ DAC with fine output resolution is creatively designed in order to reduce its quantization noise which will inject into the PLL when enabling the phase noise cancellation path.

The performance and functionality of the proposed PLL are verified by both the behavioral and transistor-level simulated results. The synthesizer is integrated in a 90 nm CMOS process and the PLL core and I/Q generators consume 14mA and 6.96mA from a 1 V supply, respectively.

Acknowledgements

Firstly, I would like to thank my daily supervisor Ping Lu for her endless patient helps in my thesis work. She also is the supervisor of my IC project course. Her insight experiences guide me to start my research life for the analog/mixed-signal IC design. Secondly, I want to deeply thank my thesis promoter Prof. Pietro Andreani for giving me freedom to organize and enjoy my research. He also gives me invaluable guidance. His respectable attitude toward the scientific work encourages me to challenge myself in the future work. I would like to thank Prof. Henrik Sjöland. His useful and innovative advices have inspired me in the IC project design. It is my honor to be a student under his supervision.

Finally, I will dedicate this master thesis to my beloved family. Without their unconditional support and encouragement, I could not smoothly continue my master study over the last three years.

Dawei Ye
Lund, March 2012

Contents

List of figures

List of tables

CHAPTER1

1 Introduction

The coming of 4th generation wireless communication standards brings up new challenges to the synthesizers design because of its flexible channel bandwidth and multi frequency bands. For instance, In the case of Long Term Evolution (LTE), the selectable channel bandwidth includes 1.4, 3, 5, 10, 15 and 20MHz, while the frequency bands reserved for LTE deployment are allocated from 700 to 2700MHz [1]. In addition, since LTE supports both Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) techniques, the targeted synthesizers should meet the specific requirements for different LTE divisions. Meanwhile, low power and low noise are the other two aspects which should be concerned in the related design. As a result, a compromise has to be made carefully when focusing on these technical issues in the practical design of the synthesizer for LTE.

The objective of this master work is to develop a high performance frequency synthesizer for LTE applications. Normally, most of the synthesizers are based on the Delta-Sigma (DS) fractional-N Phase-Lock-Loop (PLL) because of its fine frequency resolution, acceptable settling time and good noise performance. However, due to its inherent limitation, traditional DS fractional-N PLL is hard to follow the technical evolution for the newest generation wireless communication standards. Hence some advanced PLL structures with faster settling time and better noise performance were developed in recent years and a novel PLL based on these previous researches will be designed in our project.

The thesis is organized as follows. Chapter 2 introduces the specifications of the frequency synthesizer for LTE systems. Chapter 3 illustrates the main issues and relative solutions in high-level design. The corresponding behavioral

simulated results are also attached in the end. Chapter 4 shows the circuit details in each of the system blocks and their relative transistor-level simulated results. Finally, the conclusion will be made and the future works will be suggested in chapter 5.

CHAPTER 2

2 Synthesizer basics for LTE

2.1 Frequency synthesizer for LTE FDD/TDD

There are two LTE divisions –TDD and FDD, each type has its specific RF front end for signal transmission. It therefore means the required synthesizer should be capable of working for both the transceiver architectures (TDD and FDD). Figure 2.1 shows the two transceiver architectures for different LTE divisions. The block diagram in figure 2.1 (a) describes the transceiver for FDD technique. In principle, the RX and TX paths work simultaneously, thus two synthesizers are needed to demodulate the receiving RF signals and modulate transmitting base-band ones at the same time. Furthermore, a duplexer is adopted to separate the RX and TX signals and hence reduce the interference between them. However, due to the limited signal separated ability in the practical duplexer, the noise will leakage from TX to RX at the duplex distance and deteriorates the noise figure in the whole RX. To ease the noise leakage problem, the Surface Acoustic Wave (SAW) filter with wide bandwidth and small gain loss can be inserted before the duplexer in order to suppress the noise at far out frequency offset (duplex distance). However, such an external and costly device is not suitable for the high integration design. Thereby the synthesizers should have better out-of-band phase noise performance in a SAW-less transceiver. Further, figure 2.1 (b) depicts the transceiver architecture for LTE TDD. Since the RX and TX will not wok simultaneously but in different time slots and the signal will be modulated or demodulated at a single frequency band, only one signal transmission path and frequency synthesizer is required for signal synthesis in TDD transceiver. For this to be true, the noise leakage issue in FDD architecture will not appear in the TDD RF front end.

Additionally, the settling time of synthesizer should be fast enough so that it is within the guard period for the downlink (uplink) to uplink (downlink) switched activities. Finally, except for the noise and settling time requirements, the minimum frequency resolution of the designed synthesizer should be higher than the channel spacing in the LTE standards.

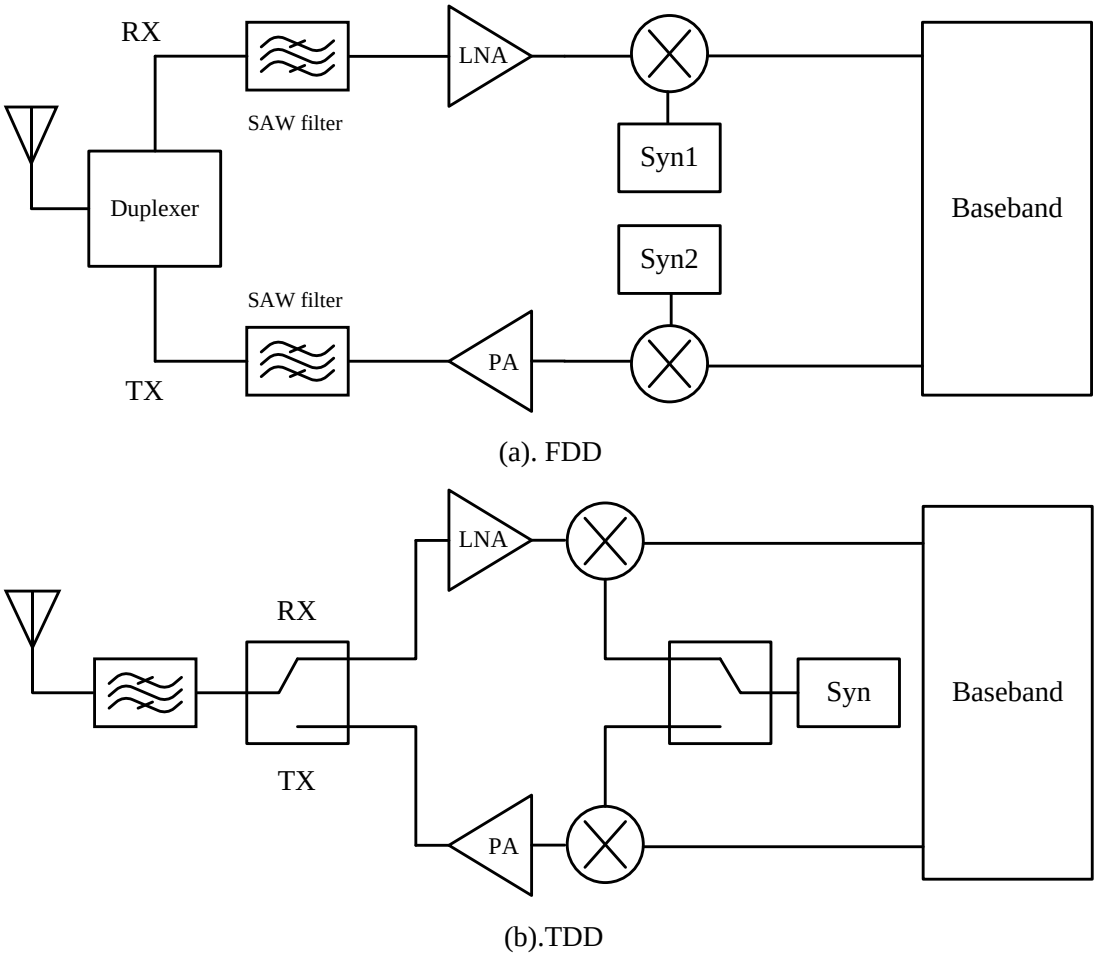


Figure 2.1 Transceiver architectures for LTE TDD/FDD.

In conclusion, the synthesizer designed for LTE should

A. cover multi-bands across a wide frequency range for deployment in different countries and regions;

B. have good phase noise both at in-band and far-out frequency and meet the requirement of extremely low integrated phase noise;

C. enable fast settling time between transmitting and receiving time slots for TDD mode;

D. have fine frequency resolution which supports the minimum channel spacing in LTE.

2.2 Frequency planning

Modu. Type	TX/MHz	RX /MHz	Relations With VCO	Available Channel Bandwidth / MHz	Duplex distances/ MHz
FDD	2500~2570	2620~2690	Fvco/2	5, 10, 15, 20	120
	698~716	728~746	Fvco/6	1.4, 3, 5, 10	30
	777~787	746~756	Fvco/6	1.4, 3, 5, 10	31
	704~716	734~746	Fvco/6	1.4, 3, 5, 10	30
TDD	2570~2620		Fvco/2	5,10	
	2300~2400		Fvco/2	5, 10, 15, 20	

Table 2.1 Frequency planning in this work.

Since multi frequency bands are reserved for LTE deployment, a good frequency planning is needed to ease the design difficulty. In this case, the synthesizer is applied for the direct conversion transceiver. One problem of such structure is the negative effect, namely Local Oscillator (LO) pulling, which will corrupt the VCO spectrum due to the undesired coupling of the high power level signal at the output of Power Amplifier. To alleviate this effect, the combination of VCO (which works at multiples of the desired frequency band) and frequency dividers can be adopted. This will allow the operating frequency of VCO (f_{VCO}) to allocate far away from the desired frequency band (Fvco/2, etc.), thereby mitigate the electromagnetic coupling effect. In addition, this structure also can increase the output frequency range and hence reduce the design difficulty of VCO with wide tuning range. Another problem is the phase noise requirement for the synthesizer. High phase noise of the LO will enhance

the reciprocal mixing which decreases the SNR of the demodulated signal. We will come to some theoretical derivations for the phase noise at different carrier offsets in the next section.

Due to the multi reserved frequency bands for LTE, an increment of difficulty to cover the available frequency range for a worldwide wireless application is inevitable. This requires the targeted synthesizer to works as the one for the multi-standards transceiver. Moreover, some frequency bands, 700MHz and 2600MHz, for instance, are favored to the LTE deployment. This is ascribed to the fact that 2500~2700MHz is a large clear band for potential users whereas band at 700MHz has high penetrating and hence provides wider coverage for rural regions. In the mean time, the supplementary band at 2300 ~ 2400MHz is also included in our planning. Table 2.1 lists the relationship between different frequency bands and outputs of the synthesizer. What's more, the available channel bandwidths at different frequency allocations and the duplex distances for FDD modulation are also listed.

2.3 Phase noise requirement for LTE

2.3.1 In-band phase noise

Error Vector Magnitude (EVM) is one of the most important parameters to describe the modulated quality of the transmitted signal. If EVM is low enough, the receiver will have a good ability of properly recovering the transmitted signal and hence have a higher quality of signal propagation in larger area due to the lower Bit Error Rate (BER). EVM depends on many nonlinear effects. One of the main contributors for the EVM is the phase noise. Good phase noise performance of the synthesizer is important in a RF system. Currently it can be estimated that the EVM of the overall transmitter system should be less than 3% while the PLL' s contribution to EVM should be less than 2% for 4G communication standards. This requirement means that the integrated phase noise has to be less than 1°. Moreover, the in-band interfering signals, so called blockers, have a high power level (often higher than the desired modulated signal) which will deteriorate the phase noise over the channel bandwidth. Poor

phase noise performance of the LO will cause a serious reciprocal mixing at a direct conversion transceiver and eventually corrupt the receiving quality of the modulated signals.

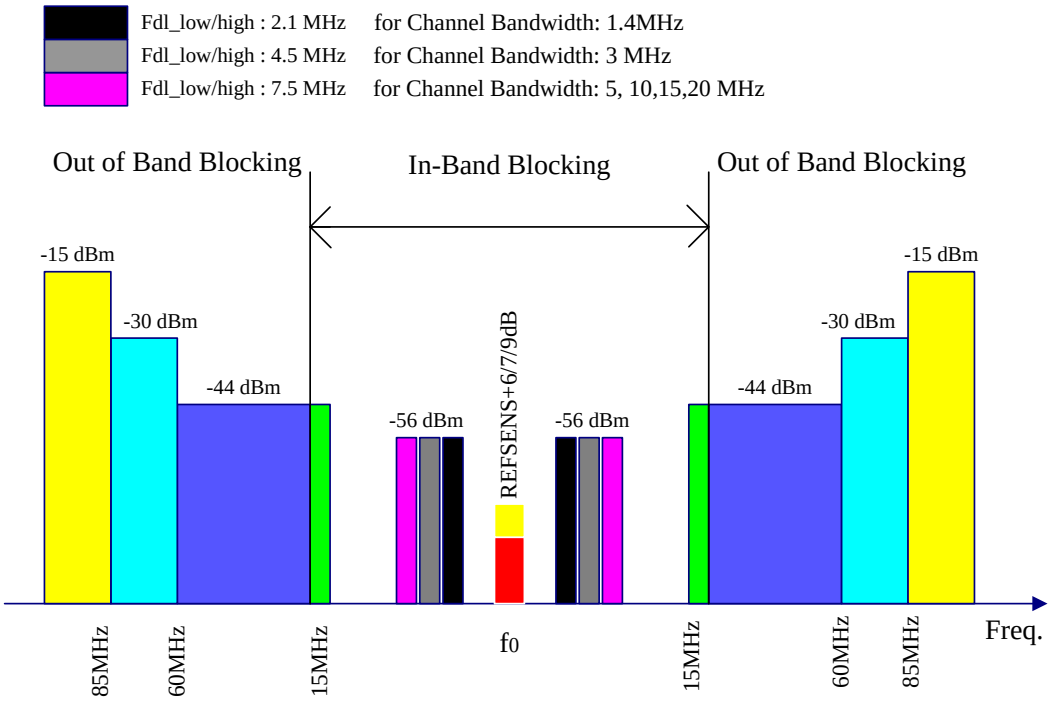


Figure 2.2 In-band blocking profile for LTE

Figure 2.2 displays the in-band blocking profiles of the LTE standard. To avoid the over deterioration of the demodulated signal, the minimum requirement for the phase noise at different frequency offsets should be meet. The phase noise of LO *L [dBc/Hz]* is calculated by the following formula:

$$L(\Delta f) \le P_{noise} - P_{blocker}(\Delta f) - 10\log(BW) \qquad (2.1)$$

and P_{noise} is given by:

$$P_{noise} = P_{REFSENS} + 6/7/9dBm - SNR \qquad (2.2)$$

where $P_{REFSENS}$ represents the reference sensitivity (REFSENS) of QPSK modulation, as shown in figure 1.2, SNR is the requiring signal-to-noise ratio

for given BER (here supposes 15 dB SNR corresponding with a 10^{-7} BER in QPSK). What ‘s more, for the channel bandwidth 1.4, 3, 5 and 10MHz, the desired modulated signal is 6 dB higher than the reference sensitivity, while for 15 and 20MHz, it is 7dB and 9dB above the sensitivity, respectively.

As known in [1], and with (2.1) and (2.2) derived above, the minimum requirement for the in-band (<20MHz) phase noise at different frequency offsets can be therefore calculated. Here we only concern the most stringent specification. It can be proved that the worst case occurs at the band 38 (TDD, 2570 ~2620MHz) with 10MHz channel bandwidth, and the relative results is given as following:

$$\begin{aligned} L(7.5MHz) &= -120dBc/Hz \\ L(15MHz) &= -132dBc/Hz \end{aligned} \tag{2.3}$$

2.3.2 Far-out phase noise

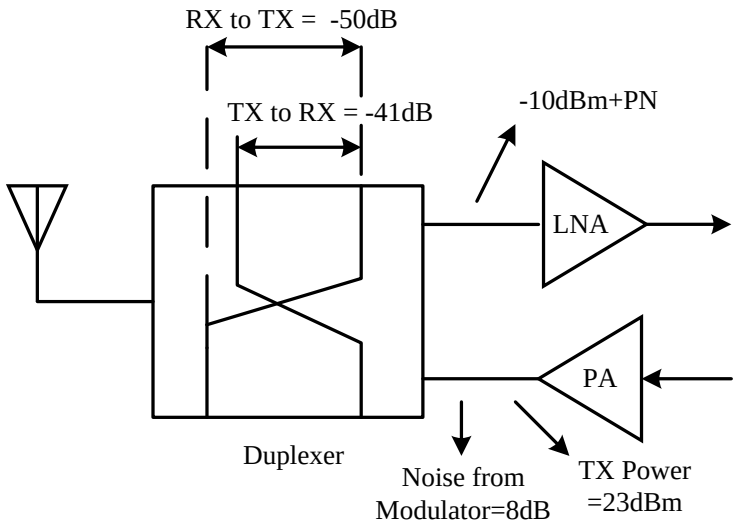


Figure 2.3 Principle of TX-to-RX noise leakage in SAW-less FDD transceiver.

In the classical design, the far out phase noise of LO can be neglected since the using of SAW filter can greatly filter out the phase noise beyond the maximum channel bandwidth (20MHz for LTE, etc.) while keeping a small gain loss at the RF frequency. However, to meet the stringent requirement for high

integration design, such an external and costly filter is welcome to be removed. This means that the far out phase noise of LO should be concerned carefully for a SAW-less transceiver.

As we described above, the saw filter is used to limit the impact of the transmitter noise on the receiver. If this filter is removed, the practical duplexer in FDD transceiver will result in the noise leakage from the TX to RX at the duplex distances (30MHz for 700MHz bands, etc.). Thereby the poor far-out phase noise of LO will degrade the noise figure of the whole RX. As shown in figure 2.3, at the first, we assume that the total TX power is 23dBm, the additional noise contribution from the Power Amplifier (PA) and modulator is 8dB, and the TX-to-RX attenuation is -41dB, respectively. Then we can know that the noise power density leaking to the input of Low Noise Amplifier (LNA) at the duplex distance (30MHz for 700MHz band, etc.) is

$$23dBm + 8dB - 41dB + PN = -10dBm + PN \qquad (2.4)$$

The industry standard noise reference is defined at 17 deg C, using Boltzmann's constant and in a 1Hz bandwidth, the ideal noise floor is therefore -174dBm/Hz. If we also assume that the noise figure for the whole RX is 4dB. Combining with (2.4), it can be known that,

$$\begin{aligned} -10dBm + PN &= -174dBm/Hz + 4dB \\ PN &\approx -160dBc/Hz \end{aligned} \qquad (2.5)$$

where PN is the required phase noise of LO at the duplex distances. By considering some noise margin for different channel bandwidths and more stringent noise figure for RX, the practical LO phase noise at the duplex distance should be 3~4 dB lower than -160dBc/Hz. On the other hand, such a noise leakage issue will not be concerned when designing the frequency synthesizer for LTE TDD since the TX and RX don't work simultaneously and hence the duplexer is not needed for the TDD transceiver.

2.4 Chapter summary

This chapter determines the specifications for the synthesizer in LTE systems. Firstly, the synthesizer should cover a wide frequency range from 698 to 2690MHz. The frequency dividers will be adopted to ease design difficulty of wide tuning range VCO. Further, to determine the phase noise requirement for the synthesizer, the blocking profile based on [1] is used to specify the in-band phase noise while the noise leakage effect from TX to RX dominates the phase noise at far out frequency. Finally, the required synthesizer should be fit for the TDD modulation also, which means its settling time is within the guard period between transmitting and receiving time slots.

CHAPTER 3

3 High-level design of the synthesizer

3.1 Synthesizer based on PLL

The PLL is widely used as the frequency synthesizer because of its fast settling time and fine frequency resolution. In general, the PLL can be classified into two categories – integer and fractional-N PLL. Compared to the integer-N PLL, the $\Delta\Sigma$ fractional-N PLL [2] is preferred to be used as the synthesizer due to its wider bandwidth (BW) and finer frequency resolution. As shown in figure 2.1, in the fractional-N PLL, the delta-sigma modulator (DSM) is adopted in order to control the divider to toggle its dividing ratio among some random integer numbers (N, N+1, N+2… etc.). The average value of this control sequence is equal to a targeted fractional number, which is given by:

$$f_{DIV} = \frac{f_{VCO}}{N + \frac{K}{2^B} + q[n]} \tag{3.1}$$

where K is the frequency control word, B is the bit width of DSM and N is the integer ratio for multi-modulus divider. Since the denominator of (3.1) includes fractional part $-\frac{K}{2^B} + q[n]$, and the control word K is selectable, a finer frequency resolution can be obtained. Moreover, unlike the integer-N PLL which has to keep a low reference frequency to guarantee a fine frequency resolution, with the advantage of fractional ratio, the reference frequency of fractional-N PLL can be chosen to any high values in principle, thus the PLL bandwidth can be wider until it reaches the limitation for the system stability

($BW < f_{REF}/10$). However, the main drawback for wide BW fractional-N PLL is the quantization noise from the DSM. It is well known that the DSM is capable of pushing its in-band quantization noise to high frequency offsets, resulting in lower in-band and higher out-of-band quantization noise. The quantization noise is fed into the PLL and finally converted to the phase noise. To alleviate the impact of quantization noise on the PLL performance, the loop bandwidth has to be narrow enough to ensure that the instantaneous error charge at the Charge Pump (CP) output, which is converted by the quantization noise, can be greatly suppressed before it disturbing the VCO. As shown in figure 3.2. (a), the phase noise contributed by DSM has less impact on the narrow BW PLL and hence good phase noise performance can be obtained at the PLL output. While in figure 3.2 (b), the PLL BW is wider and the phase noise from DSM can not be suppressed effectively, deteriorating the phase noise at the PLL output.

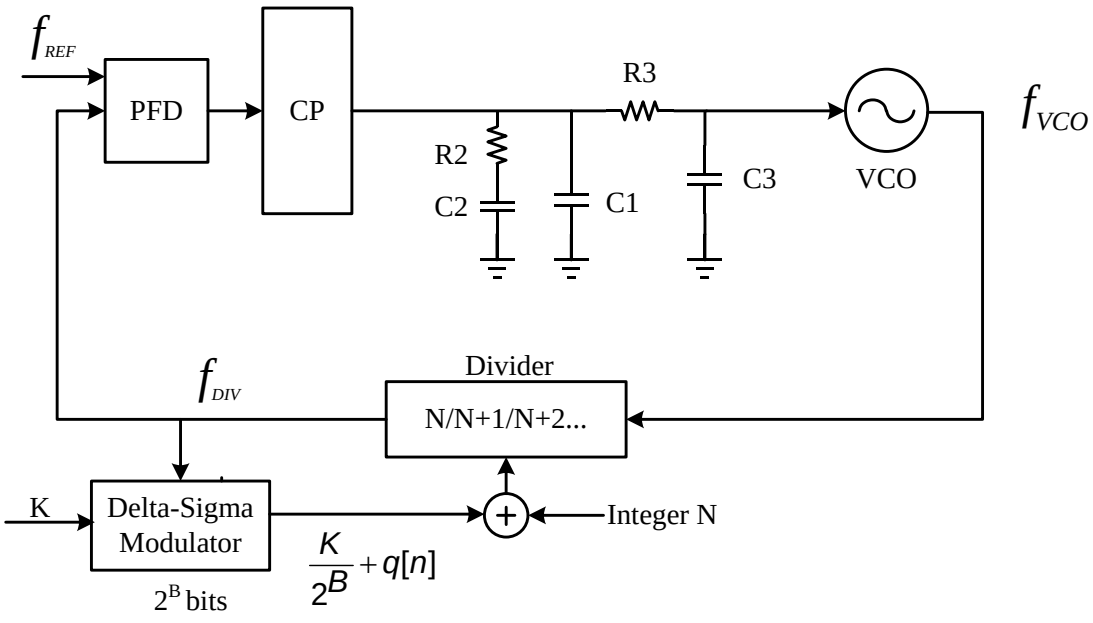


Figure 3.1. Classical delta-sigma fractional-N PLL

Meanwhile, to meet the requirement for LTE, the settling time of the synthesizer should be faster compared to the traditional fractional-N PLL. This means the PLL BW can not be too narrow. While in the classical design, the DSM quantization noise will hinder the increment of the PLL BW. To obtain a wider PLL BW while keeping reasonable phase noise, some advanced

architectures, which are developed based on the classical delta-sigma PLL, will be introduced in the next section.

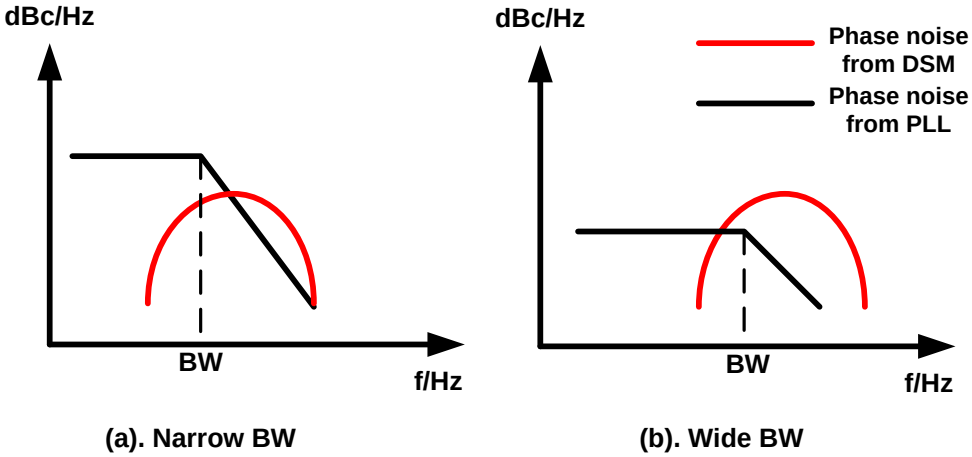


Figure 3.2 Influence of (a). narrow and (b). wide BW on phase noise in fractional-N PLL

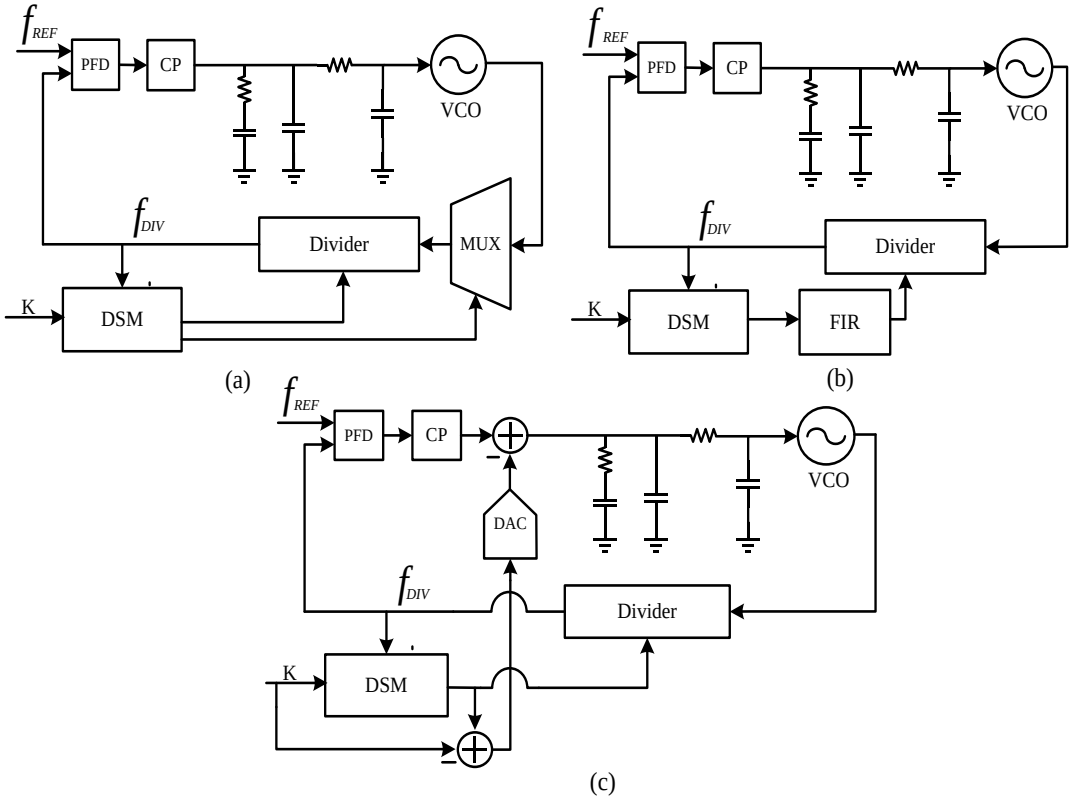


Figure 3.3 Architectures for wide BW fractional-N PLL: (a). Multiphase VCO, (b). FIR (embedded) filtering and (c). DAC cancellation.

3.2 Types of wide bandwidth fractional-N PLL

Wide BW PLLs can benefit in some aspects. First of all, fast settling time

enabled by wide PLL BW is important for the efficient signal transmission in wireless communication. Secondly, wide BW can help to reduce the DC gain of loop filter if the Gain Bandwidth Product (GBP) keeps the same (see figure 3.2). This will result in a significant reduction of in-band phase noise and hence ease the design difficulty of high performance PFD/CP and VCO. However, as described before, the phase noise contributed by DSM is the main limitation for wide loop bandwidth in fractional-N PLL. To overcome this issue, several advanced architectures are introduced in the previous researches [3]-[9]. Such architectures can be roughly divided into three categories – multiphase VCO, FIR (embedded) filtering and DAC cancellation, which are shown in figure 3.3, respectively.

Firstly, it is known that the multiphase VCO (which is often implemented by ring oscillators) shown in figure 3.3 (a) can be used to reduce the in-band phase noise [3], [4]. By introducing the multiphase VCO, the "fractional divider" which is made of multi-modulus divider and DSM can provide finer quantization steps, resulting in a great reduction of quantization noise. However, the phase mismatch in the multiphase VCO will increase the level of spurious tones at the output spectrum. The adoption of phase randomization technique can ease the spurious issue to some extent, while the in-band quantization noise will therefore increase as a trade-off.

The block diagram shown in figure 3.3 (b) describes the FIR filtering method to suppress the quantization noise in a wide BW fractional-N PLL. The basic idea of this technique is to insert a digital FIR filter between the DSM and frequency divider so that the high frequency quantization noise of DSM output can be suppressed before it enters the PLL [5]. However, due to the DC gain (which is integer and larger than 1) of the digital FIR filter, the quantization noise will also be amplifying at low frequency range. To avoid the increment of in-band noise when using a digital FIR filter, the FIR-embedded noise filtering method is adopted in [6]. In this approach, the FIR algorithm is embedded into the fractional-N PLL sophisticatedly so that the quantization noise both in-band and out-of-band can be suppressed at the cost of power consumption and complexity. As a result, when the FIR algorithm is implemented in the analog domain, the DC gain equal to 1 in the FIR topology is possible to be realized.

As we know, the output sequence of DSM is actually predictable and high-pass shaped. The error sequence $q(n)$ in (3.1) is therefore possible to be deleted before it disturbs the VCO. The third approach to widen the loop BW is refer to as the phase noise cancellation utilizing a feed forward path to delete the quantization error charges [7]-[9]. As shown in figure 3.3 (c), the quantization error is extracted by subtracting the DSM output from its input at the first, then we have it pass through the Digital-to-Analog-Converter (DAC) in order to convert it to the error charge in analog domain. Since the digital error sequence is predictable, its corresponding error charges after the DAC are correlated with the PFD/CP output. If the signal path (which is defined as the route from DSM to the loop filter) and the phase noise cancellation path are ideally matched, the instantaneous error charges due to the quantization noise can be eliminated completely. However, in the practical design, the main drawback for this approach is the mismatch between the signal and cancellation paths. In the mean time, the nonlinear effect in each of the two paths, such as the nonlinearity in PFD/CP and additive noise arising from the DAC itself, will also undermine the phase noise performance of the whole system.

In conclusion, each of these methods for wide BW fractional-N PLL has their own pros and cons. In our design, the topology using a DAC for noise cancellation will be adopted and developed. Some novel ideas and designed details will be introduced in the following sections.

3.3 Issues of wide bandwidth PLL using phase noise cancellation path

The details of wide BW fractional-N PLL using phase noise cancellation is described in figure 3.4. As we see, the DSM output including the quantization error $e_q[n]$ and DC component *K* is going to change to the instantaneous error charge $Q_q[n]$ when it arrives at the loop filter though the signal path (red dashed line). On the other hand, by introducing the noise cancellation path

(blue dashed line), $e_q[n]$ is extracted individually and converted to the charges $Q_{DAC}[n]$ by the high performance DAC. Then the charges $Q_q[n]$ and $Q_{DAC}[n]$ are about to make a subtraction before they pass trough the loop filter. If the matching between the two paths is perfect, nothing will be left to disturb the VCO, otherwise the residual charge $Q_r[n]$will degrade the phase noise performance to a certain extent.

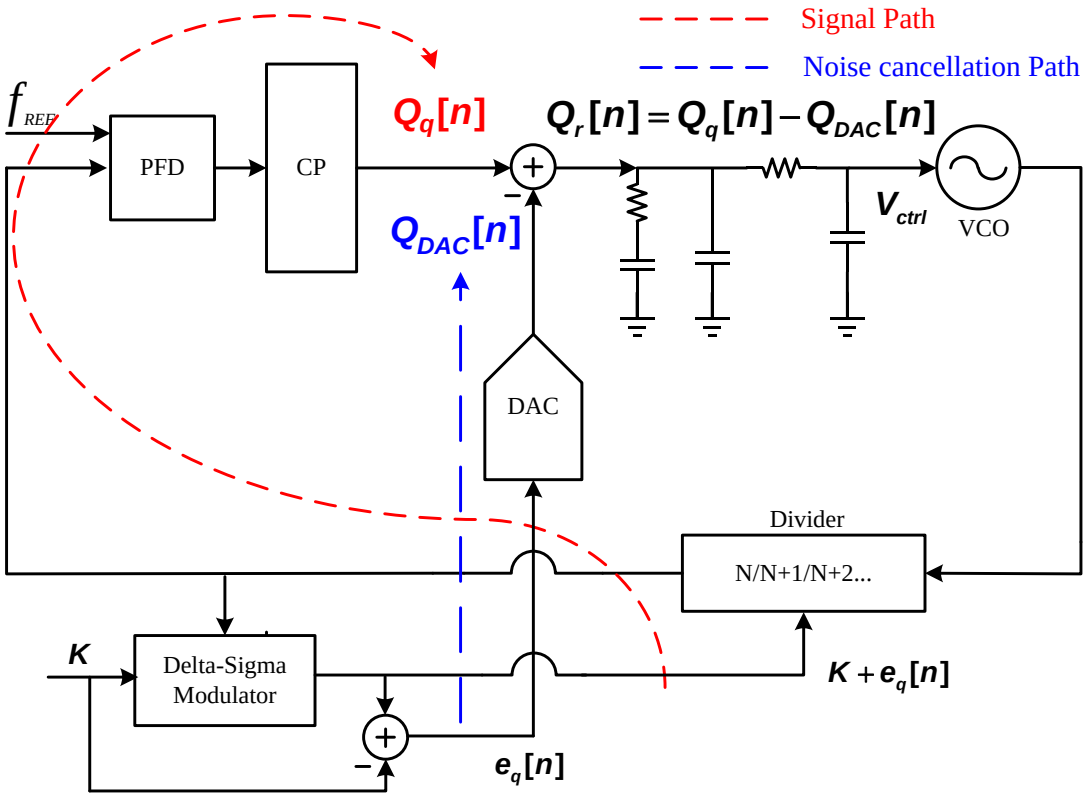


Figure 3.4 Issues of wide BW fractional -N PLL using phase noise cancellation path.

Now let us come to more details about the mechanism of phase noise cancellation. Based on the mathematical models developed in [10], we can know that the error charge $Q_q[n]$ is given by:

$$Q_q[n] = I_{CP}T_{VCO}\sum_{k=n_0}^{n-1} e_q(k) \tag{3.2}$$

where T_{VCO} is the nominal period of VCO output and I_{CP} is the nominal output

level of CP. Furthermore, the charge $Q_{DAC}[n]$ from the cancellation path is written as:

$$Q_{DAC}[n] = I_{DAC} T_{DAC} \sum_{k=n_0}^{n-1} e_q(k) \tag{3.3}$$

Likewise, I_{DAC} is the nominal gain level of the output pulse of the Current Steering (CS) DAC while T_{DAC} is the relative nominal duration. Obviously, to ensure that $Q_r[n]$ is zero, we must have

$$\begin{aligned} Q_q[n] &= Q_{DAC}[n] \\ I_{CP} T_{VCO} &= I_{DAC} T_{DAC} \end{aligned} \tag{3.4}$$

Equation (3.4) shows us a simple principle to cancel the quantization noise. However, in the practical design, the mismatch between the two paths is inevitable so that a portion of residual charges will always be added to the loop filter and cause phase noise. The $Q_r[n]$ can be expressed as:

$$Q_r = Q_q - Q_{DAC} = \alpha I_{CP} T_{VCO} \sum_{k=n_0}^{n-1} e_q(k) \tag{3.5}$$

where α is defined as the mismatch factor between the two paths. Practically, due to the nature of different modulation types in PFD/CP and CS-DAC, completed cancellation is impossible to be achieved. Further, other issues due to the nonlinear effects in the real circuits will also contribute to the phase noise. In general, such problems encountered in the phase noise cancellation technique can be classified into three aspects:

A. Error charge mismatch between the signal and noise cancellation path;

B. Nonlinearity in PFD/CP;

C. Additive noise in DAC.

Each of these problems will be analyzed respectively in the following sections.

3.3.1 Error charge mismatch

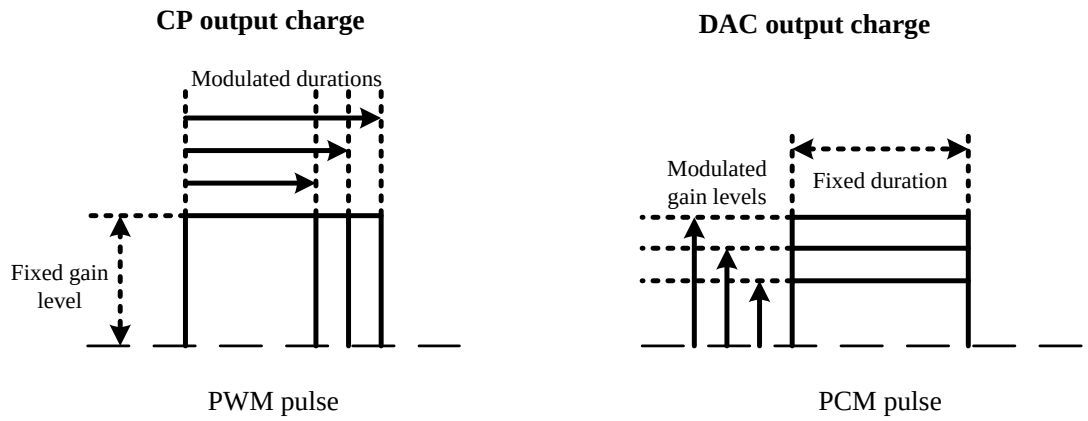


Figure 3.5 Output charge shapes of CP and DAC

In equation (3.4), we can find that the instantaneous error charge from DSM can be eliminated if the signal and cancellation path are perfectly matched. However, such condition is difficult to meet due to the fact that the two paths have different modulated characteristics for Digital-to-Analog (D/A) signal conversion.

Figure 3.5 describes the modulation types of CS-DAC and PFD/CP, respectively. As we see, the output charge of CP can be regarded as the Pulse-Width-Modulation (PWM) pulses which have fixed gain level and modulated durations. While for the CS-DACs, its output charge have fixed duration and modulated gain levels which are regarded as the Pulse-Code-Modulation (PCM) pulses. The output pulses with different modulation types determine that even if we suppose the charges of the two paths are equal in total (neglect the additive noise and nonlinear effect from the paths themselves), the residual charge $Q_r[n]$ will still be left to a certain extent and hence deposit on the loop filter, causing the undesired instantaneous phase errors.

The timing diagram shown in figure 3.6 illustrates this imperfect cancellation mechanism. Obviously, due to the problems of phase and modulation type, the error charge of CP can not be eliminated immediately when it is subtracted by

the DAC output. Hence the instantaneous residual charge $Q_r[n]$ is not equal to zero even though the total charges of each paths are supposed to be the same. Some spurs converted by $Q_r[n]$ are therefore added to the control voltage V_{ctrl}, leading to an increment of the instantaneous phase errors at the PLL output and causing phase noise. In the previous researches [8], [9], the main idea to improve the cancellation is to develop sophisticated circuits to shape the charge pulses for both CP and DAC at the expense of system complexity. Whereas in our design, in order to mitigate this mismatch while keeping reasonable complexity, a simpler idea presented in [11] will be adopted and introduced in section 3.4.1.

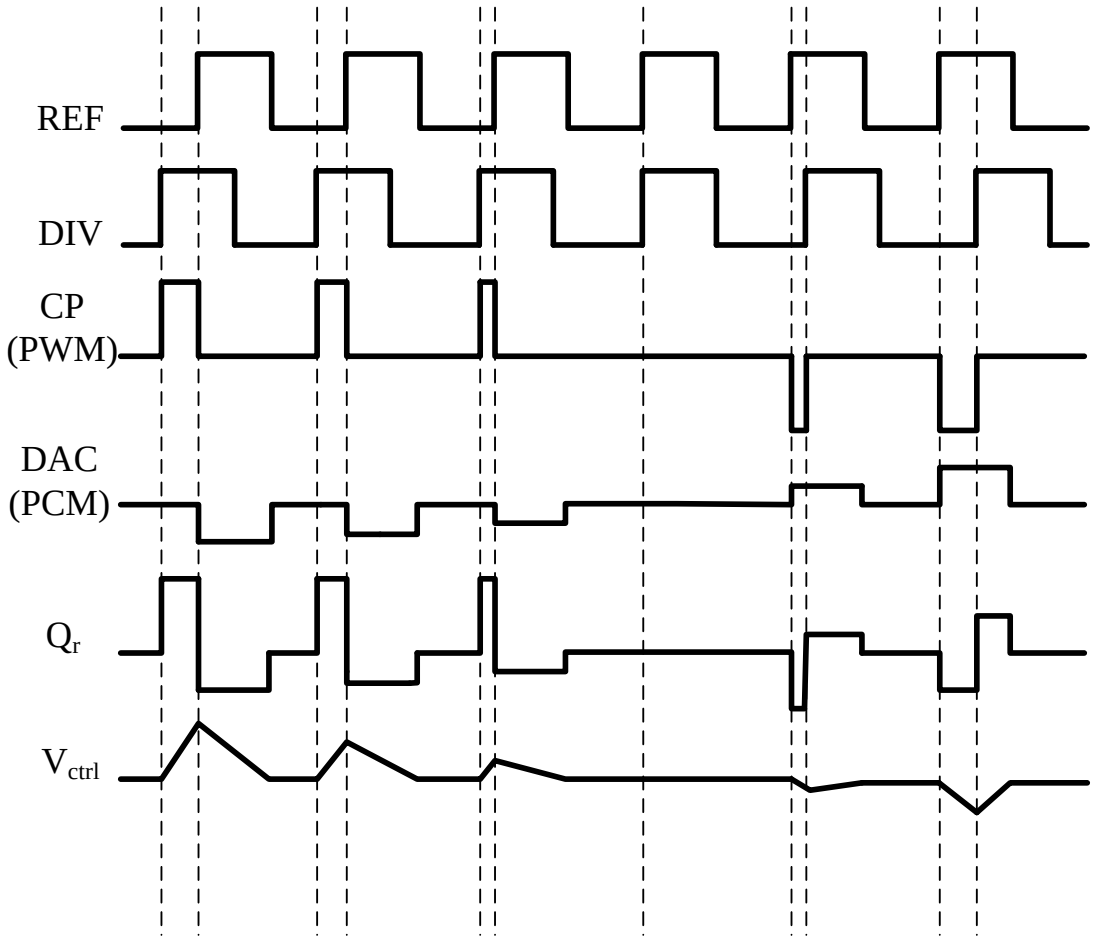


Figure 3.6. Timing diagram of delta sigma fractional-N PLL using phase noise cancellation path

Then, by understanding the noise cancellation mechanism, we can analyze the phase noise contributed by $Q_r[n]$ mathematically. First of all, it is well known that the phase noise contributed by the quantization noise in the conventional

$\Delta\Sigma$ fractional-N PLL [10] is given by:

$$S_{DS}(j2\pi f) = \frac{\pi^2}{3f_{REF}}\left|2\sin(\frac{\pi f}{f_{REF}})\right|^{2(k-1)} \times \left|H(j2\pi f)\right|^2 \qquad (3.6)$$

Where *k* represents the order of DSM, *f* is the frequency offset relative to the PLL carrier frequency and $H(j2\pi f)$ is PLL closed-loop transfer function. In our design, a third order passive loop filter shown in figure 3.1 is adopted, thus *H(s)* can be written as:

$$H(s) = \frac{NA(s)}{1+A(s)} \qquad (3.7)$$

where *A(s)* is the PLL open-loop transfer function, which can be expressed as:

$$\begin{aligned} A(s) &= \frac{K_V K_{CP}}{Ns} \bullet \frac{(1+sT2)T1}{(sC1(1+sT1)(1+sT3)T2)} \\ T1 &= \frac{R2C1C2}{C1+C2} \\ T2 &= C2R2 \qquad K_{CP} = \frac{I_{CP}}{2\pi} \\ T3 &= C3R3 \qquad K_V = VCO\ \ gain \end{aligned} \qquad (3.8)$$

Moreover, based on (3.5) and (3.6), if the DAC and PFD/CP are supposed to be ideal, the phase noise contributed by the DSM after the noise cancellation is shown in (3.9):

$$S_{Q_r}(j2\pi f) = \alpha^2 \frac{\pi^2}{3f_{REF}}\left|2\sin(\frac{\pi f}{f_{REF}})\right|^{2(k-1)} \times \left|H(j2\pi f)\right|^2 \qquad (3.9)$$

where α is the mismatch factor introduced by (3.5). Equation (3.9) illustrates how the residual charges after the noise cancellation affect the phase noise

performance at the PLL output. For instance, if α =0, the signal and cancellation path is matched perfectly. If α =1, equation (3.9) reduces to (3.7) which is used for the conventional $\Delta\Sigma$ fractional-N PLL and thus the noise cancellation path has no impact on the PLL performance.

3.3.2 Nonlinear effect in PFD/CP

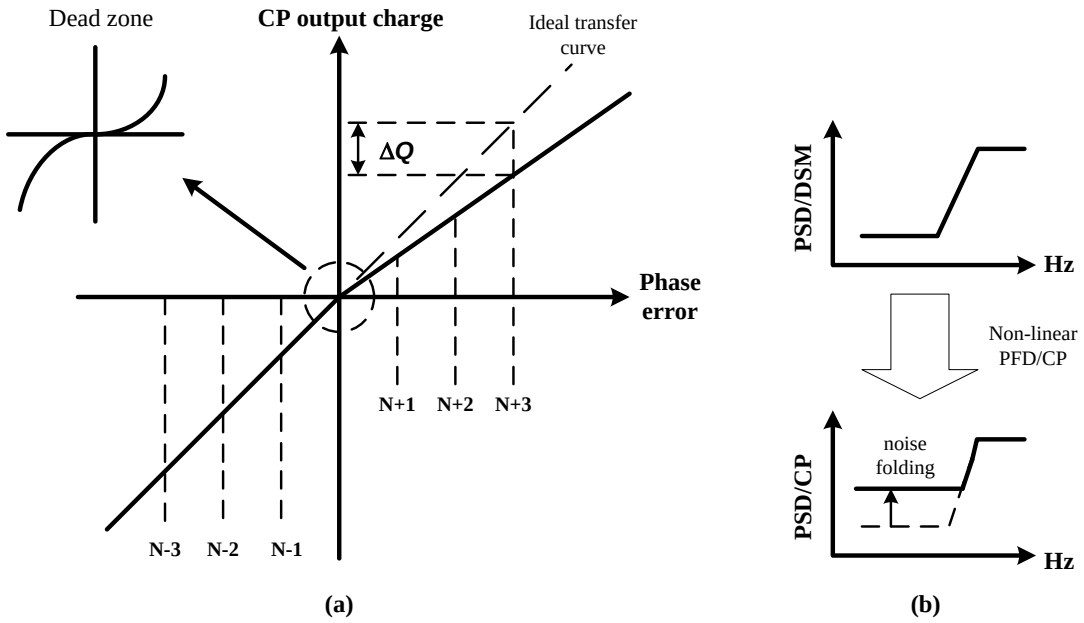


Figure 3.7 PFD/CP nonlinearity: (a). Sources of PFD/CP nonlinearity; (b). high frequency noise folding effect on PSD.

The PFD/CP-related nonlinearity and its influence on phase noise are depicted in figure 3.7. Figure 3.7 (a) shows the phase-error-to-CP-charge transfer function. Apparently, there are two reasons leading to the transfer nonlinearity. One is the dead zone resulted from the minimum settling time for the practical transistors. In order to reduce the dead zone range, some delays are usually added to guarantee that the designed devices have enough time to settle at the expense of an increment of the CP on-time. What's more, it is also known that the CP noise will inject into the loop filter when it is in the on state. Longer on-time means more CP noise will contribute to the PLL output. Therefore a compromise between the CP on-time and dead zone range should be made carefully. The other one is the current mismatch in the CP up and down currents. As we know, for the frequency divider in an integer-N PLL, the

dividing ratio will be fixed to a specific value when it is in the locked state and hence the system mainly suffer the dead zone issue while the current mismatch only affects the level of reference spur at the PLL output. However, the mechanism in locked state is quite different when it comes to the $\Delta\Sigma$ fractional-N PLL whose multi-modulus divider dynamically toggles its dividing ratio to gain the required fractional value. Thereby the nonlinear transfer curve due to the CP up/down current mismatch will result in an error charge ΔQ (as shown in figure 3.7 (a)), causing the negative effect of folding high frequency noise back to lower frequency [5], which is depicted in figure 3.7 (b).

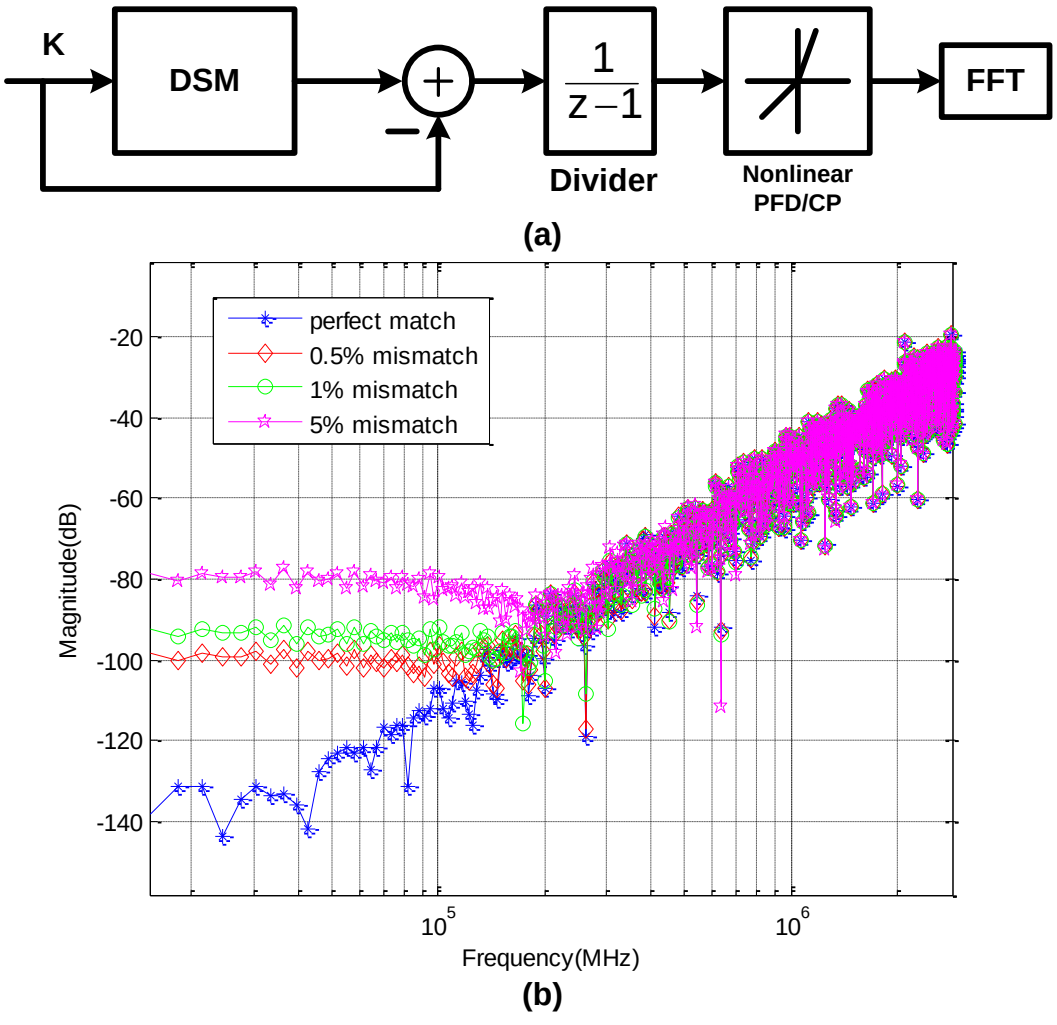


Figure 3.8 Behavioral model to examine the effect of PFD/CP nonlinearity on $\Delta\Sigma$ fractional-N PLL: (a). Schematic; (b). Simulated results.

To further understand the noise folding effect which is attributed to the PFD/CP nonlinearity, a mathematical model presented in [12], [13] is built in Simulink and used to study this intrinsic characteristic. Firstly, functional

diagram shown in figure 3.8 (a) is constructed. The DSM output is subtracted by its input in order to remove the DC component *K*, and then we have the quantization error $e_q[n]$ passing through the multi modulus divider which can be modeled as an integrator in the Z-domain [10]. Meanwhile, by referring to the figure 3.7, we find that the up/down current mismatch can be regarded as the gain (slope) variation in the nonlinear transfer function. By using this behavioral model, the relative results with 0, 0.5%, 1% and 5% current mismatches are shown in figure 3.8 (b), respectively. It is evident that when the current mismatch is increased, more high frequency noise will fold back into the lower frequency range, resulting in a great increment of the in-band noise. Therefore the PFD/CP nonlinearity is needed to be alleviated by some developed methods which will be introduced in section 3.4.2.

3.3.3 Additive noise in DAC

As shown in figure 3.4, the DAC in the noise cancellation path is used to convert the quantization error $e_q[n]$ to $Q_{DAC}[n]$ in order to cancel the instantaneous error charge $Q_{CP}[n]$ at the charge pump output. If the DAC is ideal, $e_q[n]$ can be converted perfectly and the only thing we should concern is the error charge mismatch due to the different modulation types which has been illustrated earlier. Otherwise some additive noise will inject into the loop filter accompanied with the imperfect D/A conversion. Actually such additive noise, which is mainly attributed to the DAC gain error, distortion and insufficient dynamic range, is inevitable in the practical system. So how to improve the DAC performance is the main target in this work.

As we know, to overcome the mismatches between the binary-weighted current banks of DAC, the Dynamic-Elements-Matching (DEM) algorithm combined with the thermometer-weighted current banks is preferred to be adopted. This means that for an N-bit input word, the required number of thermometer-weighted current banks will be up to 2^N. On the other hand, it is also known that to gain finer frequency resolution at the PLL output, the bit

width of the DSM should be wide enough (18 bits in our case, etc.) and hence the error sequence $e_q[n]$ has to require more current banks (2^{18} unit current banks, etc.) and complicated DEM circuit to process. However, due to the transistor size scaling, complexity and power limitations, the design of the DEM circuit and thermometer-weighted current units is actually impractical when the DAC input has more than 6 bits [14]. To break up the dilemma between the wide input bit width and system complexity, a digital DSM, which is defined as the requantized modulator in this work, can be used to truncate/requantize the error sequence $e_q[n]$ and then push the truncation/quantization noise to higher frequency. However, such typical high-pass shaped quantization noise will also inject into the loop filter and hence undermine the phase noise performance. As a result, how to improve the resolution of the $\Delta\Sigma$ DAC and reduce its quantization noise becomes our main issue when designing the noise cancellation path. In the following, we will further study the phase noise contributed by the requantized modulator.

Firstly, the requantized error is defined as $e_{rq}[n]$ in this work. If $e_{rq}[n]$ is supposed to be uniformly distributed from $-0.5\Delta_{RQ}$ to $0.5\Delta_{RQ}$, and has a variance of $\Delta_{RQ}^2/12$ where Δ_{RQ} is the minimum quantization step of the requantized modulator, the phase noise contributed by the requantization noise can be given by:

$$S_{RQ}(j2\pi f) \approx \frac{\Delta_{RQ}^2 \pi^2}{3 f_{REF}} \left| 2\sin(\frac{\pi f}{f_{REF}}) \right|^{2(L-1)} \times \left| H(j2\pi f) \right|^2 \qquad (3.10)$$

where L is the order of the $\Delta\Sigma$ modulator. Equation (3.10) shows us that the Δ_{RQ} and L determine the phase noise contributed by the requantized modulator. Hence it is essential that the L-order $\Delta\Sigma$ modulator should have enough output levels to reduce the minimum quantization step since $\Delta_{\mathrm{RQ}} = 1/\text{output levels}$. Reference [15] has proved that the requantization

noise has less impact on the PLL phase noise performance if the order *L* is equal to *K* or *K*+1 (where *K* is the order of DSM in the PLL) and output bits of requantized modulator are more than 8. The reasons for choosing such order and output levels of requantized modulator can be explained by figure 3.9.

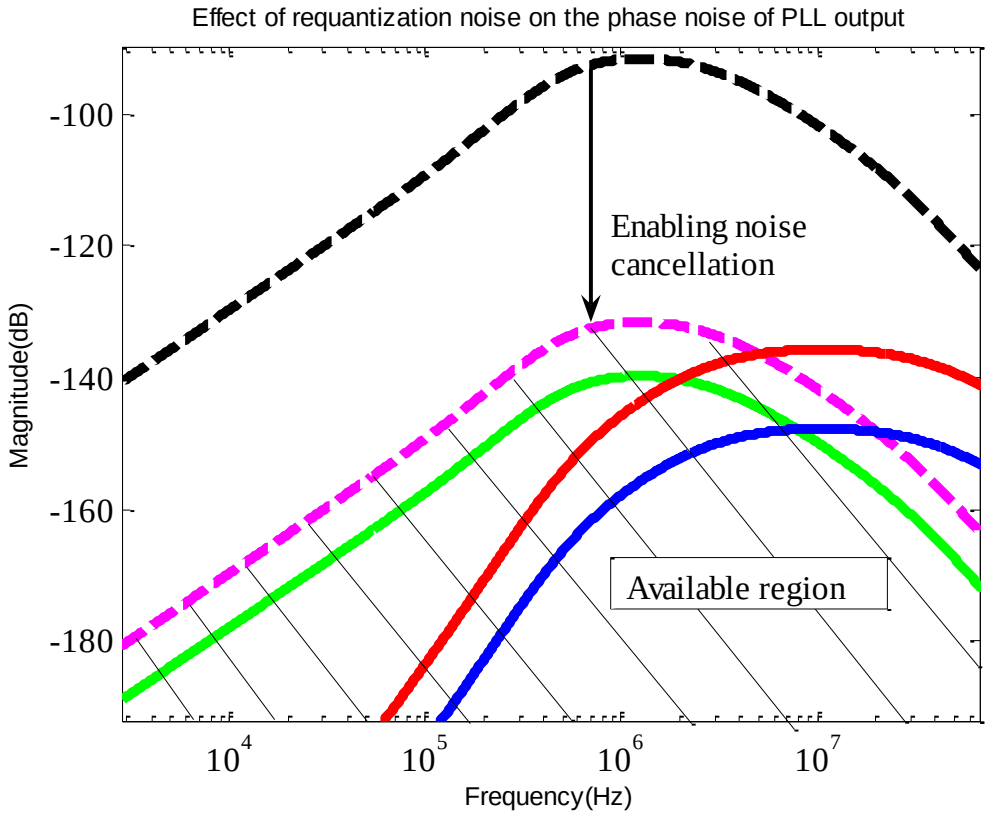


Figure 3.9 Effect of requantization noise on the phase noise of PLL output: (a). The phase noise contributed by the PLL DSM (second-order, 3 output bits) before the noise cancellation (black dashed line); (b). The phase noise contributed by the PLL DSM after noise cancellation with 1% error charge mismatch (magenta dashed line); (c). The phase noise contributed by the second-order, 8 output bits requantized modulator (green solid line); (d). The phase noise contributed by the third-order, 6 output bits requantized modulator (red solid line); (e). The phase noise contributed by the third-order, 8 output bits requantized modulator (blue solid line);

As seen in figure 3.9, the black dashed line expresses the phase noise of PLL DSM when disabling the noise cancellation path. The magenta dashed line expresses the phase noise of PLL DSM after noise cancellation with 1% error charge mismatch. It is worth nothing that the 1% charge mismatch can be regarded as a very pretty good result in the practical design of noise

cancellation path. The three solid lines express the phase noise contributed by the requantized modulators with different orders and output levels. Obviously, to ensure that the noise of the requantized modulator has less impact on (both in-band and out-of-band) PLL output, its phase noise contribution should be under the available region (shaded area in figure 3.9). For this to be true, the green and blue lines (8 output bits) therefore meet the phase noise requirement, while the red line will contribute more phase noise to the out-of-band frequency offset at the PLL output since only 6 output bits (256 output levels) are applied for the requantized modulator.

On the other hand, as described earlier, a high resolution (more than 6 output bits) $\Delta\Sigma$ DAC is difficult to be implemented by using normal modulator architecture. The segmented [16], [17] and cascaded [18] modulators can solve this problem while keeping reasonable system complexity and power consumption. In our design, a novel hybrid (segmented + cascaded) requantized modulator will be developed for the $\Delta\Sigma$ DAC to obtain high resolution (more than 8 bits) output while decrease the area and complexity simultaneously. More details about this issue will be discussed in section 3.4.3.

Finally, since the adoption of requantized modulator reduces the design difficulty of DEM circuit, the phase noise contributed by the mismatches between the unit current banks can therefore be improved by the implementation of DEM algorithm which is capable of high-pass shaping the mismatch error $e_{DAC}[n]$ [19]. Hence the phase noise contributed by $e_{DAC}[n]$ can be expressed as:

$$S_{DAC}(j2\pi f) \approx \frac{1}{f_{REF}} S_{e_{DAC}}(e^{\frac{j2\pi f}{f_{REF}}}) \times \left|H(j2\pi f)\right|^2 \qquad (3.11)$$

where $S_{e_{DAC}}$ is the PSD of $e_{DAC}[n]$. The high-pass shaped characteristic of $S_{e_{DAC}}$ can ensure that less noise closed to the carrier frequency will inject into the PLL bandwidth, which is similar to the mechanism of $\Delta\Sigma$ modulator.

3.4 Proposed wide bandwidth PLL

To solve the problem mentioned in the previous sections, an advanced architecture shown in figure 3.10 is proposed. The combinations of VCO and Divide-by-Two/Three circuits are used to guarantee that the output range can cover the desired frequency bands listed in table 2.1. The adoption of second order ΔΣ modulator with 18 bits DC input can ensure the PLL output has the required minimum channel spacing. Furthermore, the utilization of retiming circuit and synchronous divider can reduce the nonlinear effect in the PFD/CP on one side, and improve the error charge mismatch between the signal and noise cancellation paths on the other side. Finally, a novel hybrid ΔΣ DAC, which will be proposed in section 3.4.3, is developed to increase the DAC output resolution and decrease the system complexity and area cost simultaneously. Each aspects of this architecture will be analyzed in the following sections.

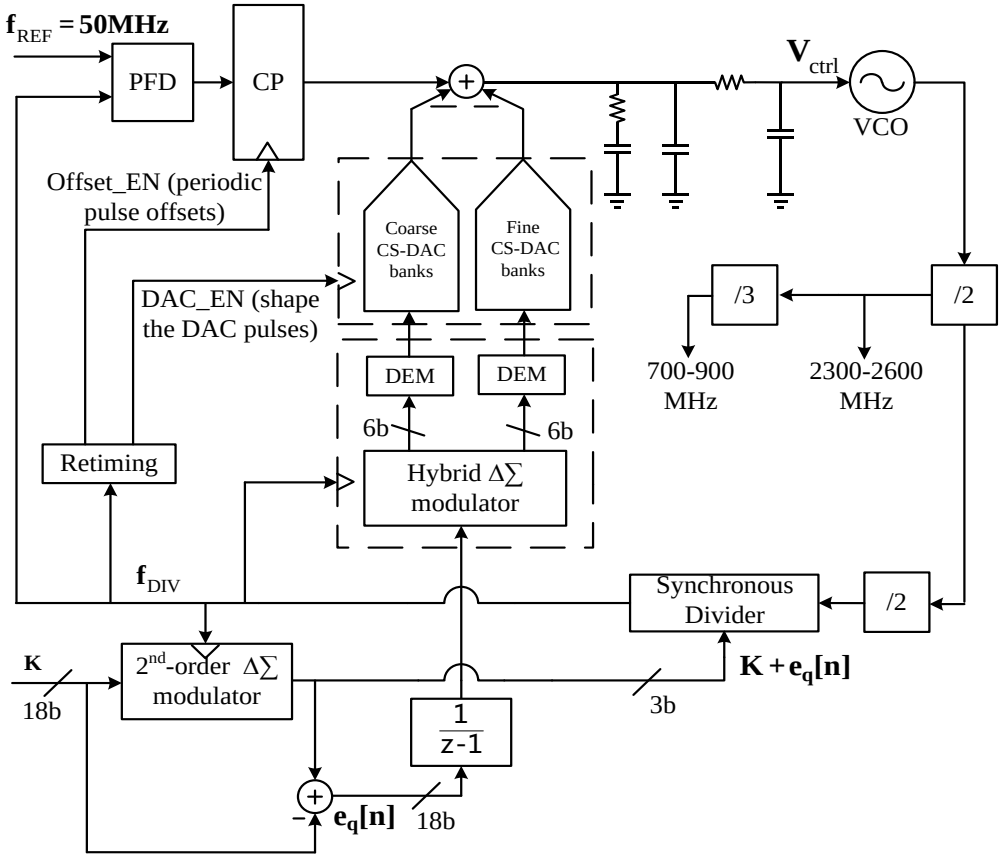


Figure 3.10 Proposed wide BW fractional-N frequency synthesizer utilizing hybrid - ΔΣ -DAC for phase noise cancellation.

3.4.1 Improvement of error charge mismatch between the signal and phase noise cancellation path

As the analysis in section 3.3.1, the error charge mismatch between the two paths is unavoidable since different signal modulation types (PCM and PWM) are used in different paths. This will result in undesired voltage spurs (see figure 3.6) after the loop filter even though the total error charge in each path are exactly the same.

The basic idea to solve this mismatch problem is to increase the overlap area between the CP and DAC output as much as possible. Therefore less residual charge will be converted to the voltage spur after enabling noise cancellation techniques. We know that the DAC pulse is typically aligned with the rising/falling edges of divider output. Hence, as shown in figure 3.6, the overlap area between CP and DAC output probably could be zero, resulting in a reduction of error charge canceling performance. To avoid such undesired condition, the retiming circuitry, which can be implemented easily when adopting the synchronous divider, is necessary to be used to ensure that the overlap area between the CP and DAC output is large and always exists.

On the other hand, it is known that the CP output are PWM pulses which have fixed gain level and variable durations. On the contrary, the DAC PCM output have fixed duration and modulated gain levels. To meet equation (3.4), the total charge of CP and DAC should be exactly the same. While this will not happen if T_{DAC} does not change with T_{VCO}. To solve this problem, the fixed duration T_{DAC} can be set to an integer number of VCO periods (i.e. $T_{DAC} = MT_{VCO}$, where *M* is an integer). Therefore when T_{VCO} is changed, the corresponding pulse duration of DAC output can be also changed. If the relationship between the gain levels of CP and DAC is $I_{DAC} = I_{CP}/M$, the total charge of DAC and CP can be equal theoretically. Then the following question is how to determine the integer number *M*? Figure 3.11 explains the effect of the DAC pulse

duration MT_{VCO} and overlap area between CP and DAC output on the error charge cancellation.

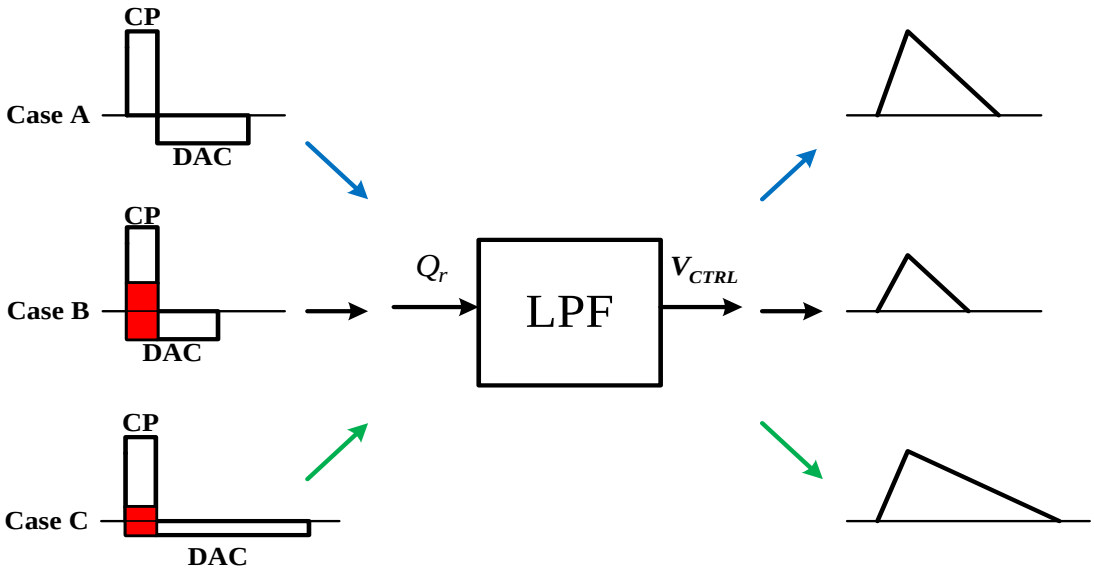


Figure 3.11 Effect of DAC pulse durations and overlap area (red regions) on the error charge cancellation.

Before the analysis, we suppose that the total charge from DAC and CP output is exactly equal and the low-pass filter is built by a simple capacitor. Then it is evident that when the overlap area is zero in case A, more residual charge will be left to the loop filter, leading to a high voltage ripple which will cause reference spur and phase noise at the PLL output. On the contrary, in case B and C, the overlap area between the CP and DAC output decrease the residual charge after the noise cancellation and hence smaller voltage spur can be obtained. Moreover, compared to case C, the pulse duration in case B is narrower and the error charge cancellation is more effective because of the smaller voltage transients. In conclusion, the narrower the DAC pulse, the smaller the undesired voltage spur.

The above analysis seems to be true if we don't concern the timing errors in the real circuitries. Actually the timing error, which is defined as ΔT_{DAC} in this work, will result in a normalized gain error $\Delta T_{DAC}/T_{DAC}$ at the DAC output. What's more, ΔT_{DAC} usually does not change accompanied with the variation of T_{DAC}. If T_{DAC} is too small, the gain errors induced by ΔT_{DAC} will

become larger and affect the noise cancellation performance. Thus a compromise should be made carefully to determine the integer number *M*. Researches in [9], [10] had proved that the empirical optimized value of *M* is 4 which will also be adopted in our design.

Then when concerning the DAC pulse duration effects on the phase noise of PLL output, the equation (3.9) should be modified as

$$S_{\mathbf{Q_r}}(j2\pi f) = \left\{ \alpha^2 + \left(\frac{\Delta T_{DAC}}{T_{DAC}} \right)^2 + (\pi f T_{DAC})^2 \right\} \times \frac{\pi^2}{3 f_{REF}} \left| 2\sin(\frac{\pi f}{f_{REF}}) \right|^{2(k-1)} \times \left| H(j2\pi f) \right|^2 \tag{3.12}$$

where $\pi f T_{DAC}$ reflects the contribution of DAC pulse duration to the PLL phase noise. The detailed derivation of the part $\pi f T_{DAC}$ can be found in [15].

Finally, we can derive the final equation for PLL phase noise contributed by the imperfect phase noise cancellation path.

$$S_{Cancel}(j2\pi f) = S_{RQ}(j2\pi f) + S_{DAC}(j2\pi f) + S_{Q_r}(j2\pi f) \tag{3.13}$$

where S_{RQ} , S_{DAC} and S_{Q_r} are given by equation (3.10), (3.11) and (3.12), respectively.

3.4.2 PFD/CP linearization technique

As analyzed earlier, the PFD/CP nonlinearity will deteriorate the phase noise performance at the PLL output because of the inherent mechanism of $\Delta\Sigma$

fractional-N PLL in the locked state. In figure 3.7, we can find that one simple and directed method to overcome this problem is to narrow the range of DSM output pattern, therefore have the dynamic dividing ratio toggling in a more linear region. However, smaller output pattern range will affect the stable input range of high order DSM, probably inducing the frequency dead band [20]. Typically, to avoid the frequency dead band at the PLL output, the DSM should have more than 3 output bits with the output pattern ranging from N-4 to N-3. Nevertheless, the noise folding effect attributed to PFD/CP nonlinearity will be amplified if the output pattern range becomes wider.

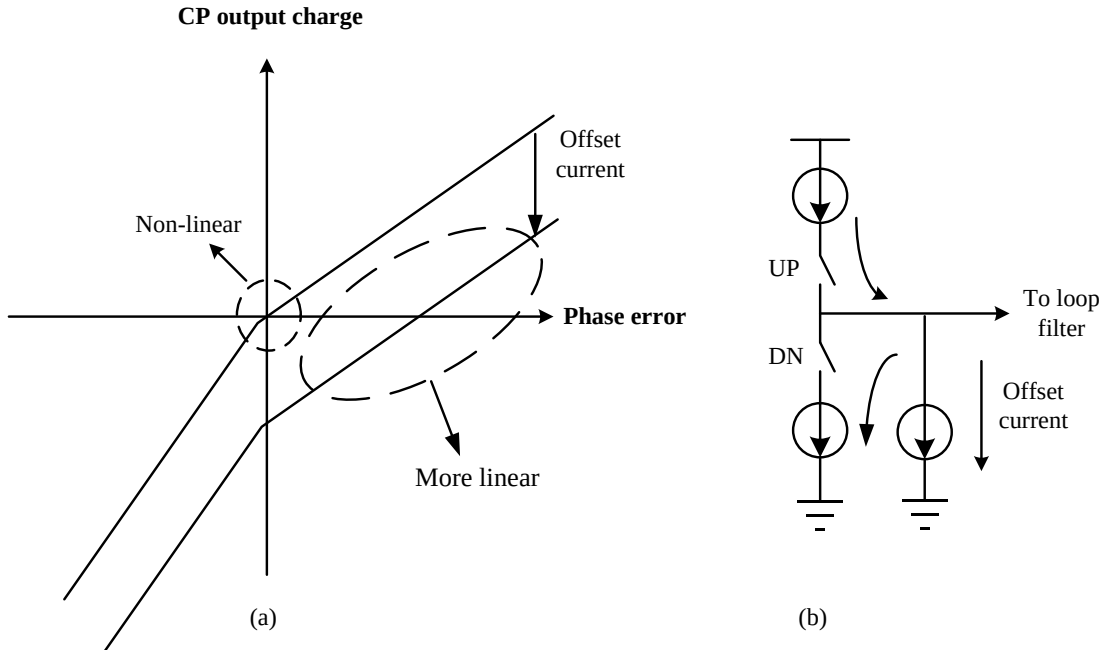


Figure 3.12. Effect of offset current on the PFD/CP transfer function: (a). Linearized PFD/CP transfer characteristic by using offset current; (b). CP schematic with offset current source.

To break up the dilemma between the PFD/CP nonlinear effect and DSM output pattern range, the additional offset current source presented in [13] can be added to decrease the sensitivity of PFD/CP to nonlinear distortions while keeping reasonable DSM output bits. As shown in figure 3.12, the transfer curve around the origin is often nonlinear. By adding offset current, the operation region of the transfer curve can be shifted up or down to its more linear part, alleviating the high frequency noise folding issue.

Conventionally, the added offset has a fixed value which can be easily implemented by a DC current source. However, such a fixed current will increase the gain level of undesired reference spur. As seen in figure 3.13, the net current I_{NET} after the subtraction between I_{CP} and fixed offset generates a

periodical ripple on V_{CTRL} which will modulate the VCO, resulting in an increment of reference spurious level.

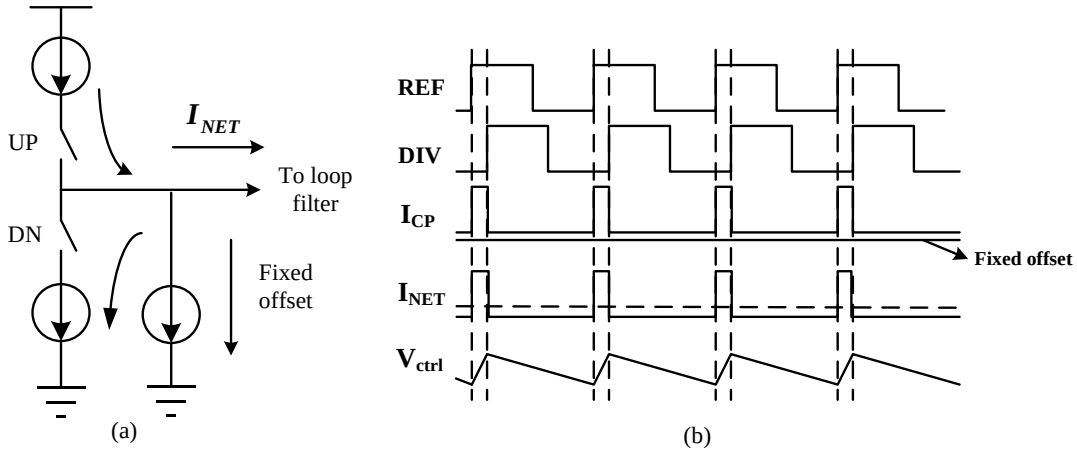


Figure 3.13. Effect of fixed offset current on the reference spurious levels: (a). Schematic; (b). Timing diagram;

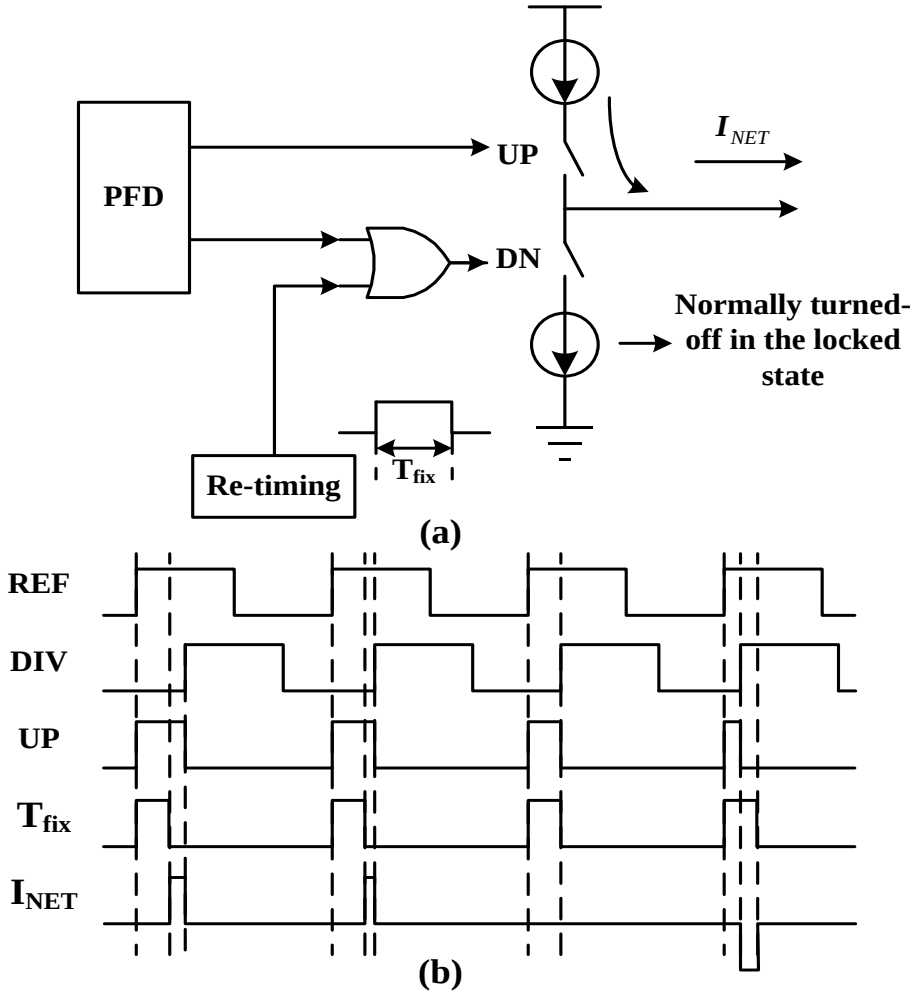


Figure 3.14. Proposed PFD/CP with fixed timing offset: (a). Schematic; (b). Timing diagram.

Instead of the linearization technique by using fixed current offset, the insertion of fixed timing offset pulse T_{fix} can greatly improve the reference spur performance. As shown in figure 3.14, the net current I_{NET} at the CP output, which will be further cancelled by the noise cancellation path, acts as the one without adding any linear offset. Furthermore, the pulse width of T_{fix} is set to guarantee that the final PFD output is capable of enabling a proper current pulse which has a large area overlapped with the CS-DAC output, resulting in an effective cancellation for the error charges. It is worth nothing that in this work the periodical timing pulses are provided by the retiming circuit proposed in figure 3.10. If the power and area budget is allowed, such timing offset approach can be replaced by the switch-controlled current source inserted before the loop filter.

3.4.3 Proposed architecture for high resolution DAC

In this section, a high resolution ΔΣ DAC will be proposed to construct the phase noise cancellation path. As described in section 3.3.3, the main issue is how to optimize the circuitry to ensure that the DAC output has more than 6 bits while keeping acceptable area cost and system complexity.

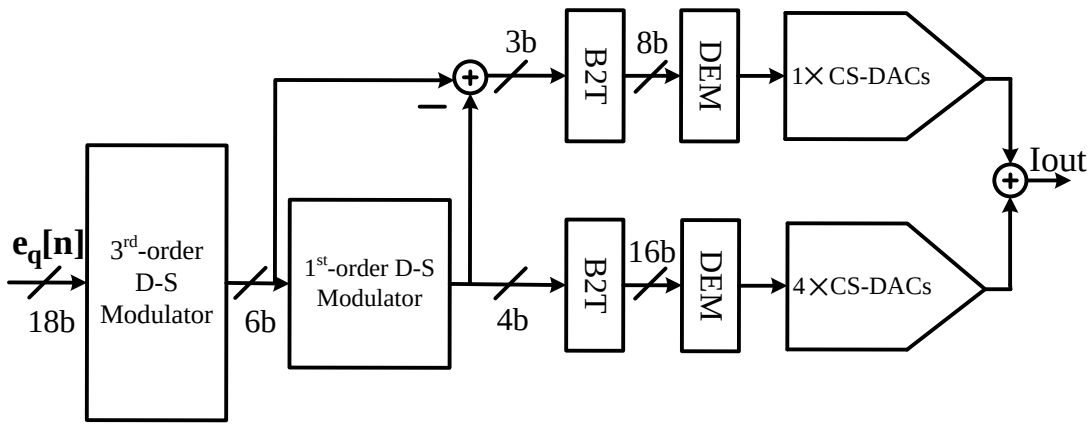


Figure 3.15. Segmented ΔΣ DAC with 6 bits modulator output

The segmented modulator [16] shown in figure 3.15 is popular to be adopted when designing multi-bits ΔΣ DAC. As we see, the third-order modulator has 6 bits output which will be divided into two parts for the subsequent processing.

The adoption of a first-order modulator can guarantee that the mismatch between the two separated bit patterns is inherently shaped by the first-order high-pass transfer characteristic, avoiding an undesired increment of the in-band noise. Additionally, since the 6 bits output of the first modulator is divided into two smaller parts, the implementation of their own DEM circuitries will become easier, compared to the normal ΔΣ DACs.

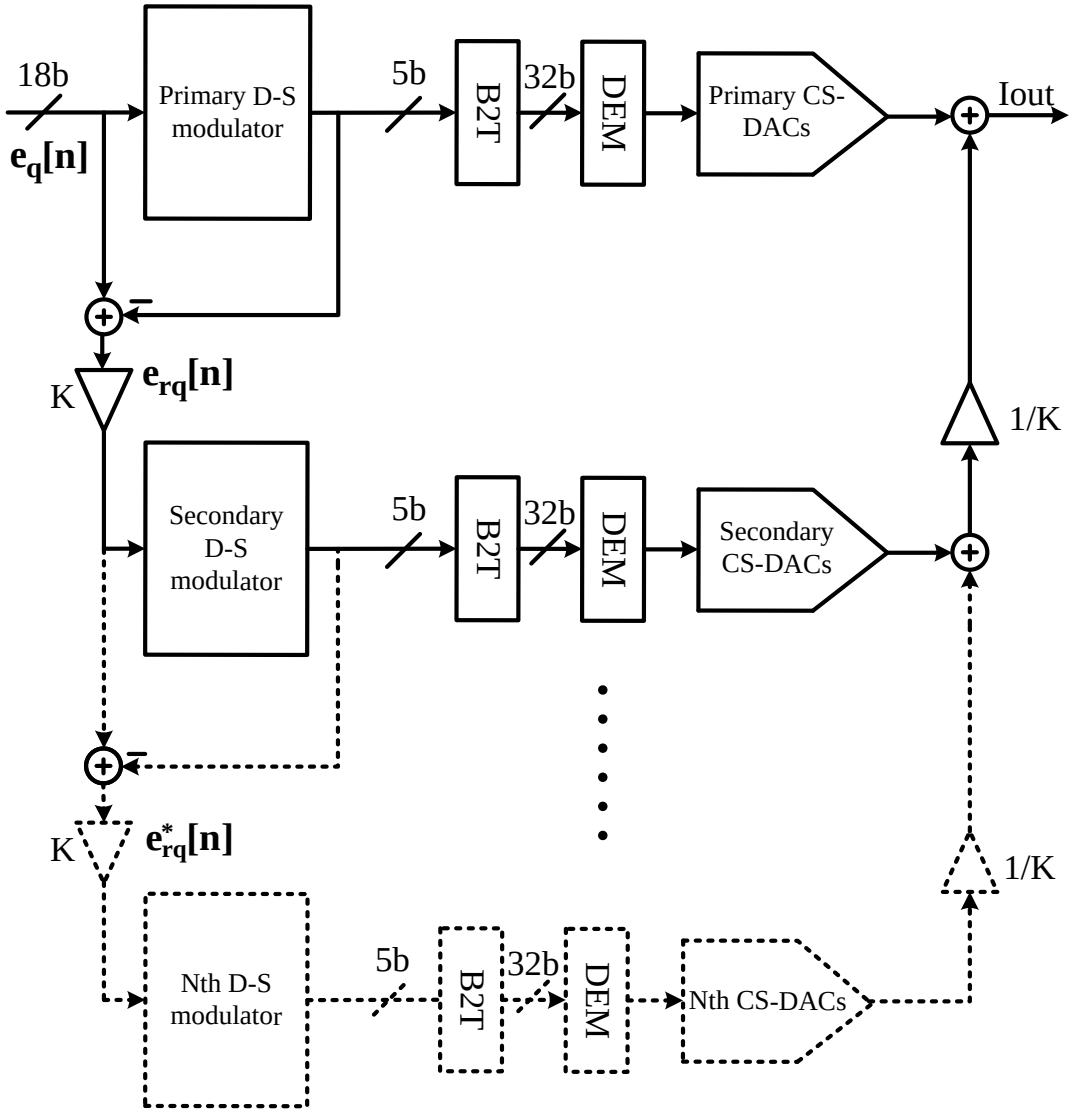


Figure 3.16. Cascaded ΔΣ DAC with more than 6 bits equivalent modulator output.

However, the classical ΔΣ DAC by using segmented noise-shaped DEM algorithm will still suffer the complexity problem when more than 6 output bits are required. The improved segmented noise-shaped DEM technique proposed in [17] can be alternatively chosen to widen the output bit width whereas a novel DEM algorithm and CS-DAC banks are needed to be developed.

Another choice to further increase the output resolution of ΔΣ DAC is the cascaded modulator architecture [18].

The cascaded modulator architecture is shown in figure 3.16. First of all, if we only concern on the primary stage, it is relative output in *Z*-domain can be expressed as:

$$Y_1(z) = STF_1(z)X(z) + NTF_1(z)E_{rq}(z) \qquad (3.14)$$

where $STF_1(z)$ and $NTF_1(z)$ are the signal and noise transfer function for the primary modulator, respectively. $E_{rq}(z)$ is the requantization noise from the primary ΔΣ modulator, which is expressed as $e_{rq}[n]$ in the time domain. Then extract $e_{rq}[n]$ by subtracting the output of primary modulator from its input, scale up $e_{rq}[n]$ by a factor of "*K*" and have it passing through the secondary modulator for the post processing. If $STF_1(z)$ is easy to be built (i.e. $STF_1(z)$ =1, in our case), the input signal $X(z)$ can be removed completely before $E_{rq}(z)$ enters into the secondary path. Therefore, the secondary modulator output is:

$$Y_2(z) = K \cdot STF_2(z)NTF_1(z)E_{rq}(z) + NTF_2(z)E_{rq}^*(z) \qquad (3.15)$$

where $E_{rq}^*(z)$ represents the requantization noise in the secondary modulator which is expressed as $e_{rq}^*[n]$ in the time domain. $STF_2(z)$ and $NTF_2(z)$ are the signal and noise transfer function for the secondary modulator, respectively. Note that the $STF_2(z)$ is designed to be 1 to simplify the matching work. Subsequently, the next step is to scale down $Y_2(z)$ by a factor of "*1/K*" and sum it with $Y_1(z)$ in the analog domain. Thus the final output is given by:

$$Y_{Total}(z) = STF_2(z)Y_1(z) + \frac{1}{K}Y_2(z)$$
$$= STF_1(z)X(z) + \frac{1}{K}NTF_2(z)E_{rq}^*(z) \quad (3.16)$$

Apparently, $E_{rq}(z)$ in the primary modulator is removed from the final output and what's left in $Y_{Total}(z)$ are the input signal and shaped noise $NTF_2(z)E_{rq}^*(z)$ multiplied by a scaled down factor "*1/K*". Therefore the quantization noise will reduce proportionally, which is equivalent to an increment of the DAC output resolution.

On the other hand, if there are some mismatches between the primary and secondary path, the transfer function in (3.16) will be changed as:

$$Y_{Total}(z) = STF_1(z)X(z) + (1 - \frac{K_D}{K_A})NTF_1(z)E_{rq}(z)$$
$$+ \frac{1}{K_A}NTF_2(z)E_{rq}^*(z) \quad (3.17)$$

where K_D and K_A represent the scaled factors in the digital and analog domain, respectively. If K_D is equal to K_A, equation (3.17) reduces to (3.16) and the two stages are perfectly matched. Otherwise the mismatch, which can be regarded as the difference between the scalded factors in different domains, will be reduced inherently by the part "$1 - K_D / K_A$" and hence have less impact on the modulator output.

Additionally, in principle there is no limitation for the number of cascaded stages. Hence more stages can be cascaded to obtain finer output resolution. If the scaled up/down factors between each stages are supposed to be equal,

equation (3.16) can be modified as:

$$Y_{Total}(z) = STF_1(z)X(z) + \frac{1}{K^N} NTF_N(z)E_{rq}^{**}(z) \qquad (3.18)$$

where N is the number of the cascaded stages, and $NTF_N E_{rq}^{**}(z)$ represents the shaped requantization noise in the N^{th} cascaded stage. Obviously, the scaled factor K before each stage will in turn increase the effective output resolution. Theoretically, K and N can be set to any high value until the designed system reaches to the minimum size limitation for the analog devices.

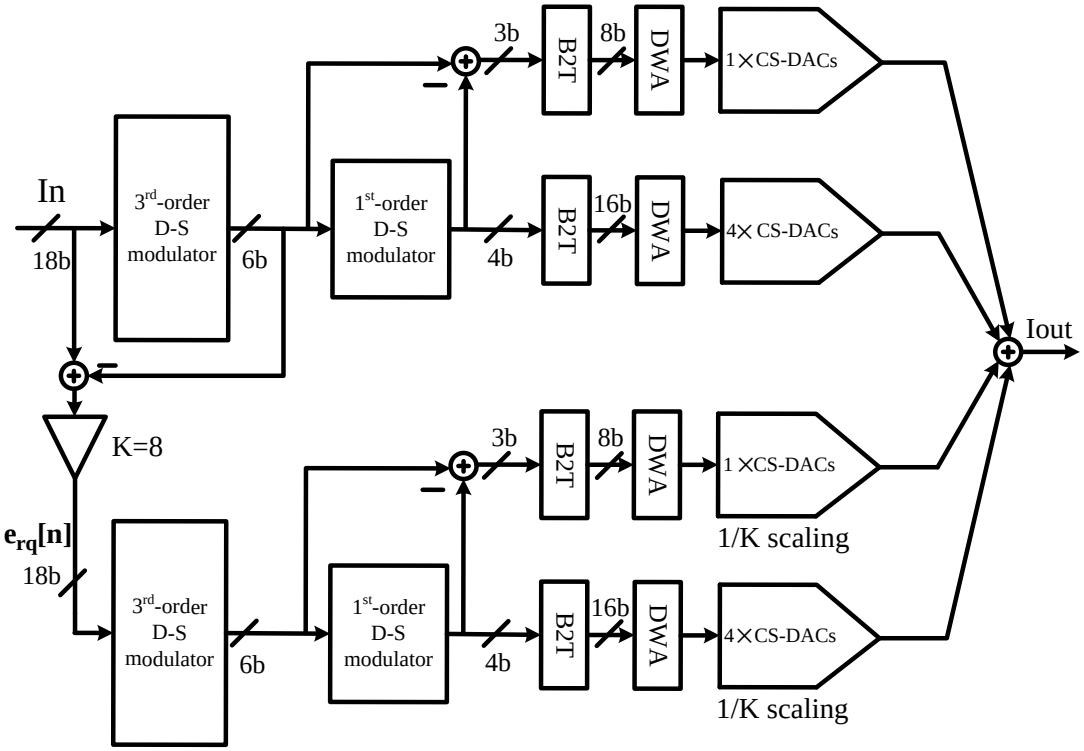


Figure 3.17. Proposed hybrid ΔΣ DAC with 9 bits equivalent output

As the above analysis, the segmented and cascaded modulators are capable of providing higher output resolution respect to the normal architectures. On the other hand, to further simplify the complexity while keeping higher resolution, a hybrid ΔΣ DAC shown in figure 3.17 is proposed in our design. As we see, the segmented modulator is adopted in each stage individually to ensure 6 output bits. On the other hand, the scaled up factor "*K*" is set to 8 in this case

which can be realized by a simple left-shifting bit operation whereas the factor "*1/K*" is implemented by scaling down the size of CS-DACs proportionally in the secondary stage. By referring to equation (3.16), we can know that the final equivalent output bits/levels is up to 9/512, which meets the requirement for the phase noise cancellation path. Further, the Data-Weighted-Averaging (DWA) is selected as the DEM algorithm in our design due to its simplification and power efficiency, whereas other newest DEM algorithms with more effective suppression for CS-DACs' distortion (such as [22]) can also be used alternatively to improve the PSD of S_{DAC} contributing to the PLL phase noise.

3.5 Simulated results in high-level design

3.5.1 Loop filter design

A third-order passive loop filter will be adopted in our design to implement a fourth-order closed loop transfer function for the whole system. By using the equation (3.8), we can guarantee that the setting parameters meet the stable and BW conditions. The targeted values of these parameters are given as follows:

$$C2 = 33.7\,pF \qquad R2 = 19.8k\Omega$$
$$C1 = 3.08\,pF$$
$$C3 = 0.8\,pF \qquad R3 = 5.3k\Omega$$
$$I_{CP} = 450\mu A \qquad K_{VCO} = 57MHz/V$$
$$BW = 1MHz \qquad f_{REF} = 50MHz$$

All of the above parameters have to be determined carefully after a compromised consideration for settling time, stability and noise. For instance, the CP output current should be high enough in the wide BW PLL in order to avoid an apparent growth of in-band noise. While the VCO gain should be small enough to ensure that the control voltage fluctuation has less impact on

VCO since this undesired voltage ripple will eventually contribute to the phase noise and spurious tones at the PLL output. On the other hand, the 1 MHz PLL BW can enable fast settling time while the relative reference frequency f_{REF} has to be high enough to make the system be far away from the instable condition ($BW < f_{REF}/10$).

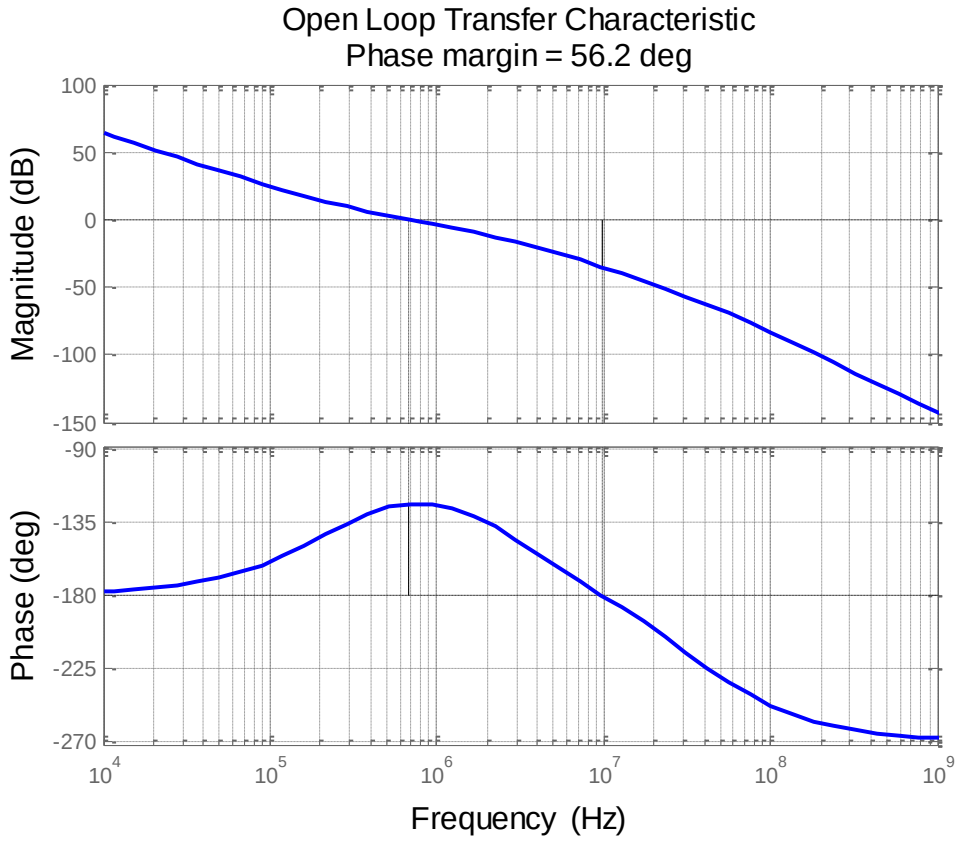


Figure 3.18. Open loop transfer characteristic of proposed PLL.

By using these predicted values mentioned above, now we can estimate the ideal transfer characteristics. Figure 3.18 depicts the open loop transfer characteristic of proposed system. Obviously, the phase margin is 56.2 degree and hence meets the requirement of system stability. Figure 3.19 shows the gain and phase of relative closed loop transfer function, it is evident that the system 3dB BW is around 1MHz which is capable of enabling fast settling time for our design target.

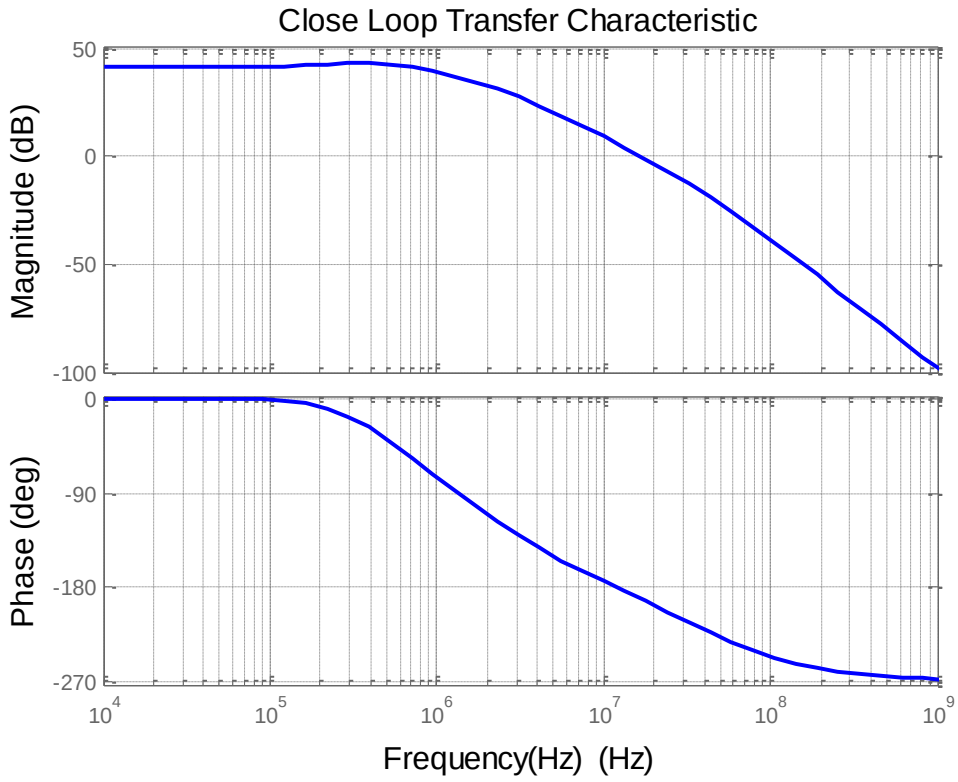


Figure 3.19. Closed loop transfer characteristic of proposed PLL

3.5.2 Simulated results for the proposed DAC

It is also necessary to estimate the performance of phase noise cancellation path before we come to the detailed circuit design. First of all, the behavioral model of proposed DAC is built in simulink. All the components are ideal and obtained from the default Matlab libraries. Secondly, two 3rd-order-single-loop $\Delta\Sigma$ modulators with the same architecture are designed in each cascaded stage respectively. A Linear-Feedback-Shift-Register (LFSR) with 25 bits is used to generate one-bit dithering for both the two modulators, which can mitigate the spurious tones by randomizing the Least Significant Bit (LSB) of proposed modulators [22]. Moreover, Instead of the quantization error $e_q[n]$ from PLL DSM, a DC word with 18 bits is setup to test the $\Delta\Sigma$ DAC performance. Since the schematic in simulink is ideal and what we mainly concern here is the quantization noise, the analog mismatch and distortion between the practical CS-DACs can be neglected to simplify the simulation work. The relative simulated results are shown in figure 3.21.

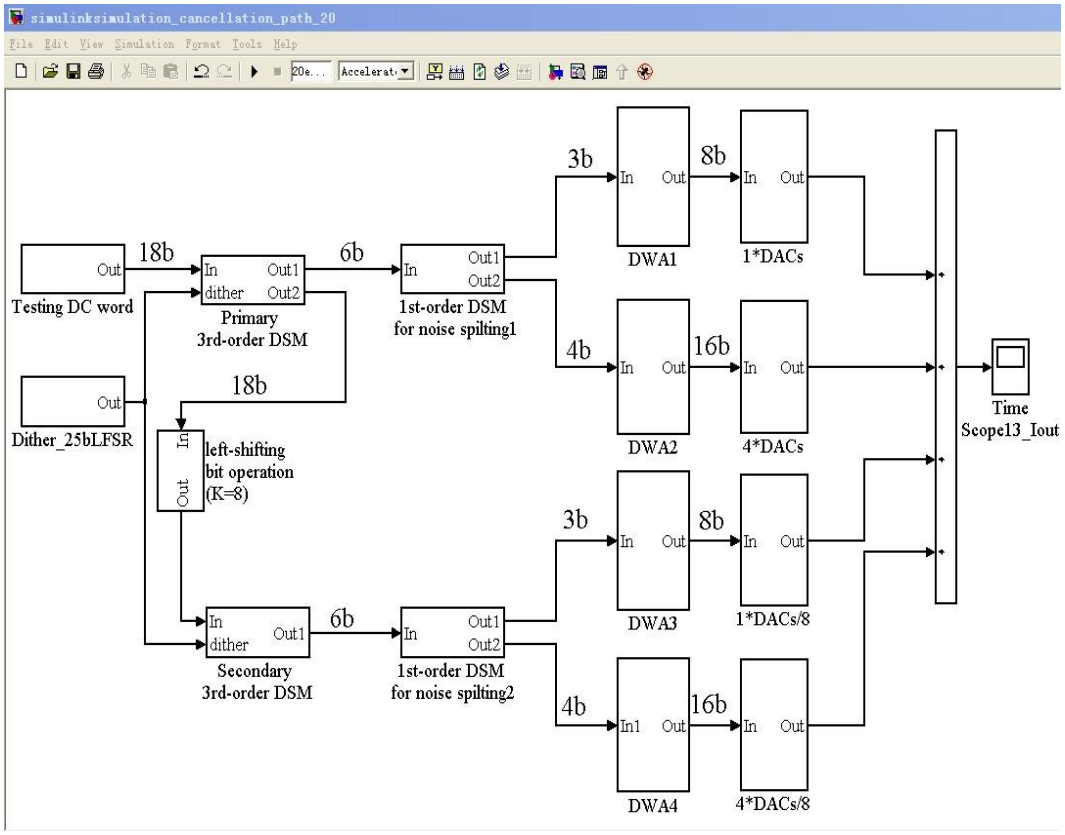


Figure 3.20. Behavioral model of proposed ΔΣ DAC built in Simulink

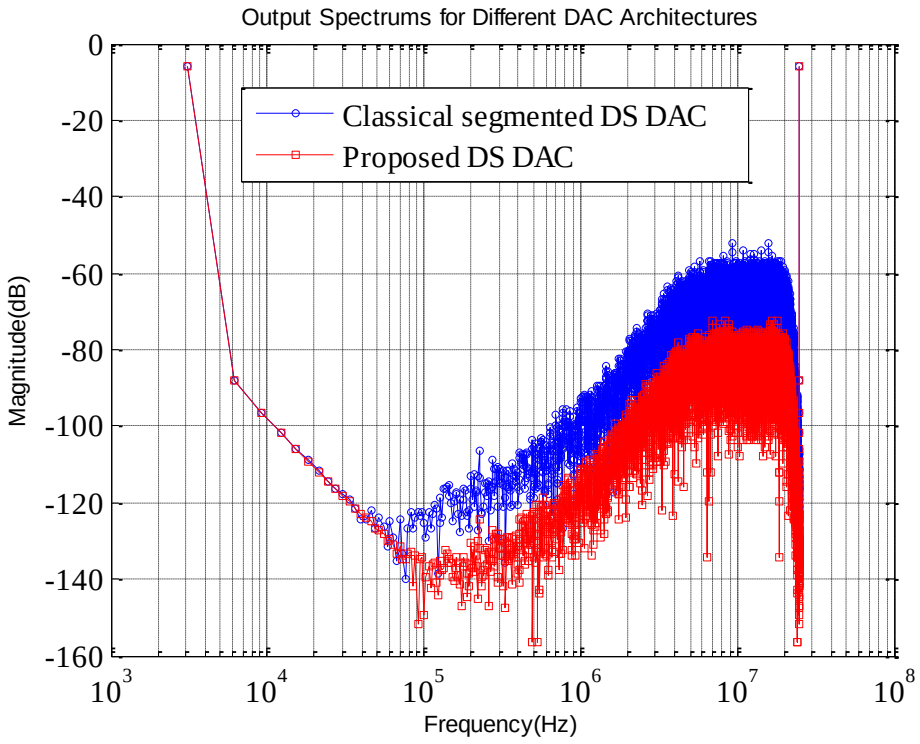


Figure 3.21. Output spectrums of behavioral models for different ΔΣ DACs (8192 points FFT).

In the beginning of the simulation, the secondary stage of the proposed architecture is disabled, the system will reduce to a classical segmented ΔΣ DAC and its corresponding output spectrum can be therefore obtained (blue line with circles). Then recover the proposed architecture and redo the simulation. Compared to the previous spectrum of segmented ΔΣ DAC [16], the relative result (red line with squares) shows that the quantization noise in the proposed architecture is greatly reduced by 18 dB since the equivalent output bits are increased from 6 to 9. With the analysis in section 3.3.3, we understand that less out-of-band quantization noise in the proposed ΔΣ DAC can ensure that its contribution to the phase noise is within the available region shown in figure 3.9, meeting the requirement for the additive noise in noise cancellation path.

3.5.3 Simulated results for the whole system

The behavioral model shown in figure 3.22 is built to examine the system functionality and impact of the quantization noise on the wide BW PLL. The basic parameters of the PLL have estimated in section 3.5.1 and will be used to specify the corresponding functional blocks. The ideal ΔΣ DAC verified in section 3.5.2 is adopted to construct the noise cancellation path. On the other hand, by referring to figure 3.10, the phase integrator between the PLL DSM and ΔΣ DAC is used to convert the quantization error to the phase error, matching the function of divider in signal path. What's more, just as the modulators in ΔΣ DAC, a one-bit dithering should be inserted into the LSB of the PLL DSM to avoid the spurious problem. In order to simplify the complexity, only one LSFR is adopted in the system, whose output bit stream is shared by all the ΔΣ modulators. Finally, the timing offset pulses from the retiming circuit is fed to the CP in order to force it operate in a more linear region. In the mean time, the retiming blocks also can increase the overlapped region between the CP and CS-DAC outputs, leading to a performance improvement of the noise cancellation technique.

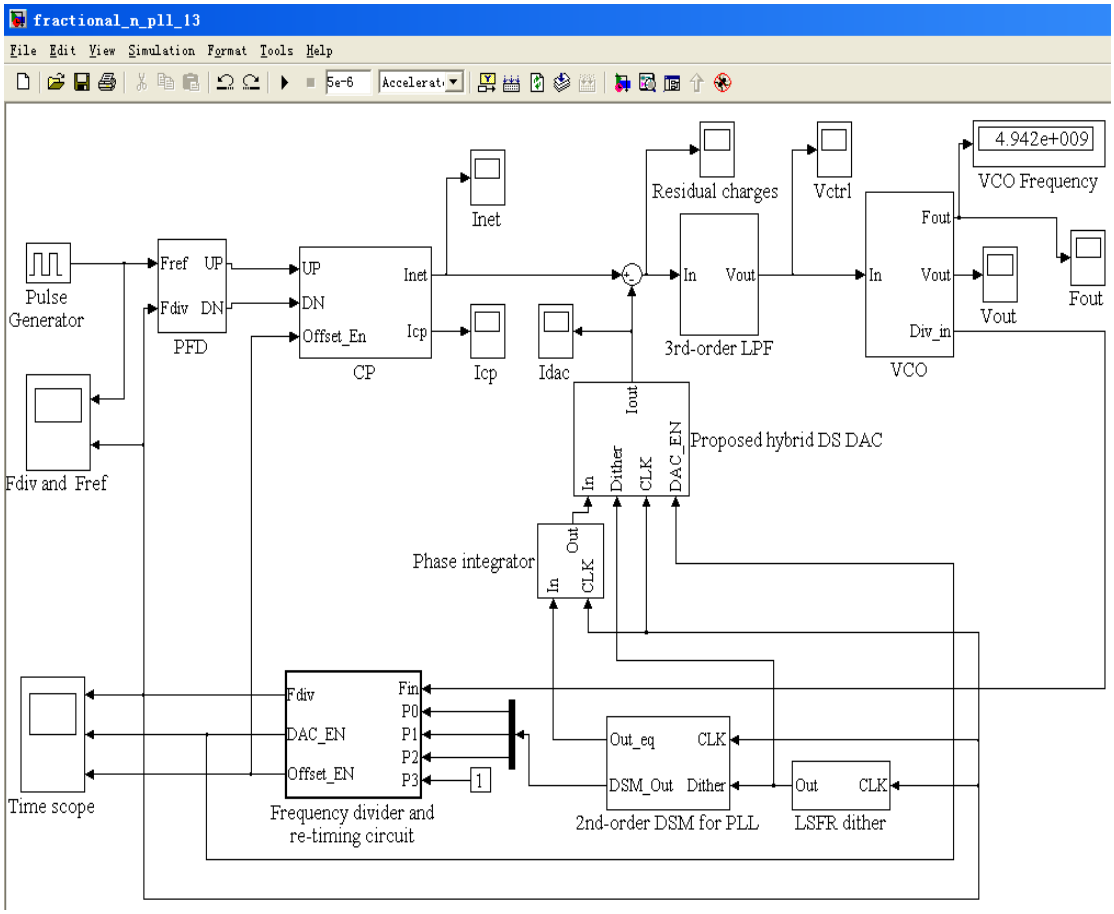


Figure 3.22. Behavioral model of proposed system built in Simulink

By using this behavioral model, we therefore can do the simulation to check its functionality and the impact of the proposed noise cancellation technique. At the first, the noise cancellation path is disconnected while keeping the BW unchanged. After the simulation, the relative results for the voltage transients is shown in figure 3.23 (a). It can be seen that the average level of control voltage V_{ctrl} is finally fixed to 0.64V at 2.5μS (≈ the PLL settling time) approximately. Hence, we can say that the functionality of the proposed PLL is correct. However, even though the average level of V_{ctrl} is locked, the instantaneous voltage error can be seen apparently on the control voltage which will deteriorate the phase noise at the PLL output. This is due to the fact that the quantization noise from the DSM will be converted to the related error through the signal path. The traditional method to solve this problem is to narrow the BW and hence suppress the instantaneous voltage error more effectively. However, this solution is not feasible in the proposed PLL since the wide BW is needed to be maintained. Then let's enable the noise cancellation path and redo the simulation. The related simulated result can be seen in figure 3.23 (b).

Obviously, with the assistance of the noise cancellation path, the instantaneous error charges are almost cancelled before passing through the loop filter. Thereby the voltage errors are mitigated significantly and only small ripples are left on V_{ctrl} . Such imperfect noise cancellation is due to the mismatch between the two paths and the requantization noise from the proposed DAC.

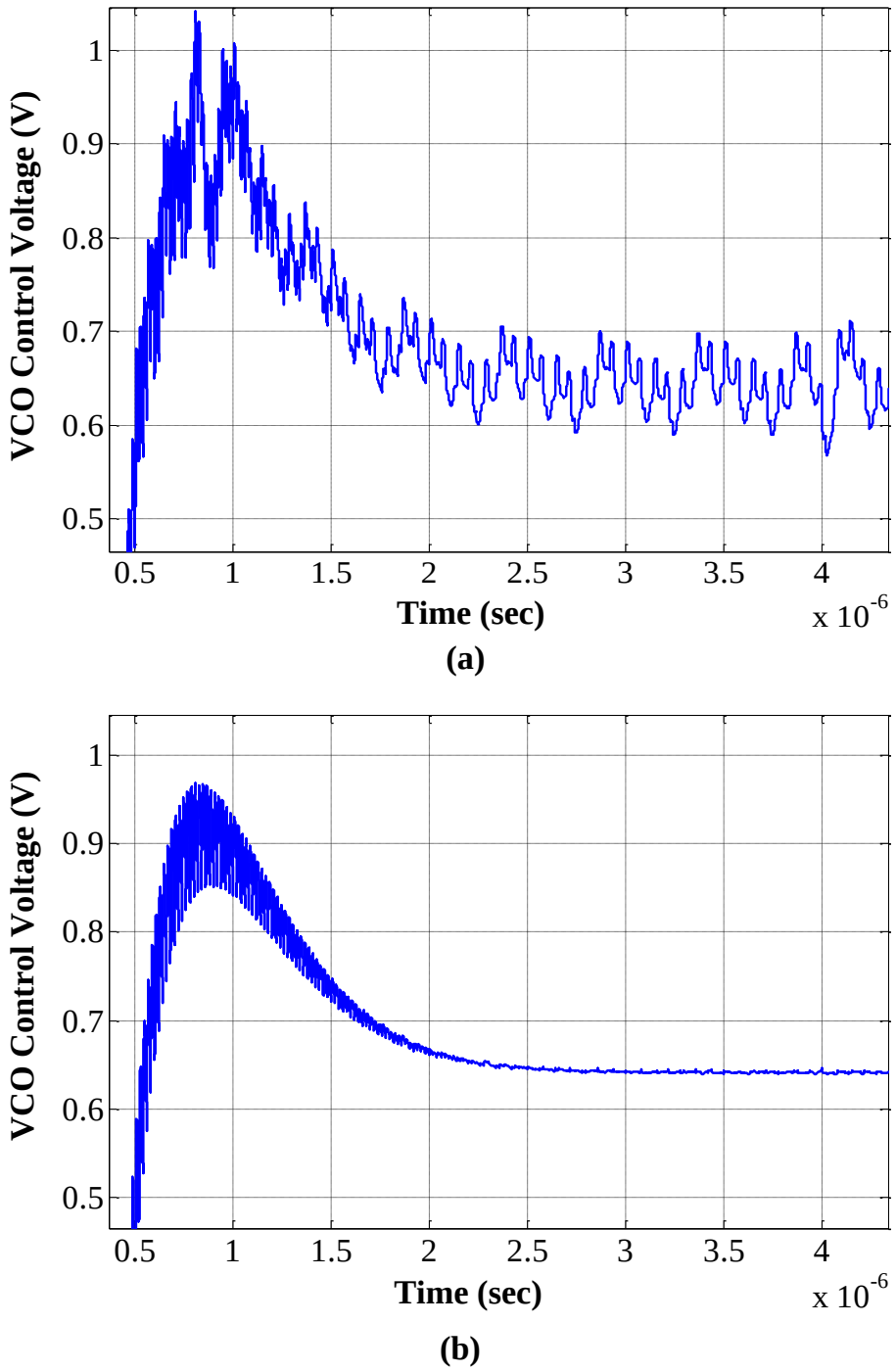


Figure 3.23. PLL transient response: (a). Disabling the phase noise cancellation path; (b). Enabling the phase noise cancellation path.

Let's zoom in the transients results for further analysis. As shown in figure 3.24 (a), the instantaneous voltage errors are reduced effectively from the magnitude of 100 mV to 5mV when enabling the noise cancellation path. While the CP and CS-DACs outputs with the residual charge $Q_r[n]$ shown in figure 3.24 (b) can verify that the correlation between the recovered error charges $Q_q[n]$ and $Q_{DAC}[n]$ is valid. This is easy to understand since the input signals of the two paths all contain the error sequence $e_q[n]$ and hence their corresponding converted error charges will be subtracted by each other in the analog domain. Even though there are some cancelled mismatches attributed to the imperfect D/A conversions in each paths and output signals with different modulated types.

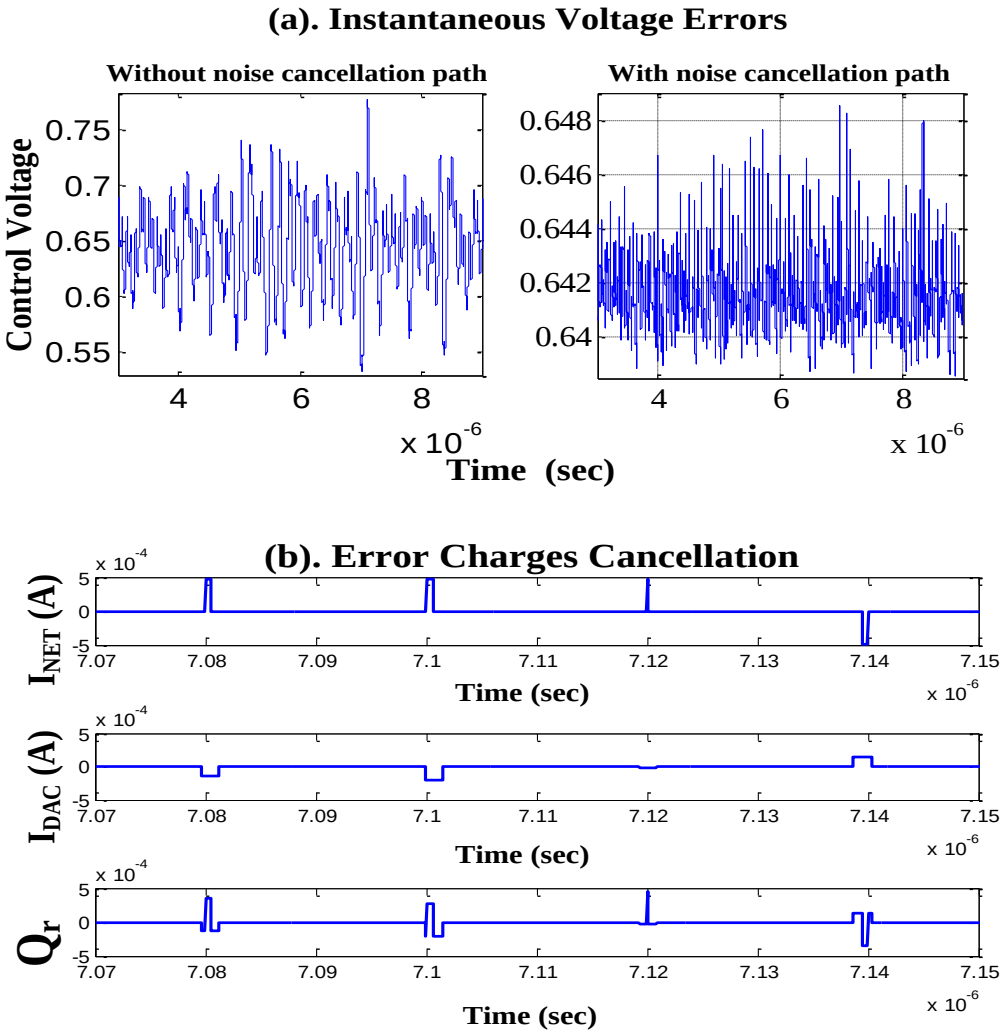


Figure 3.24. Simulated results for the impact of noise cancellation path on proposed PLL: (a). Instantaneous voltage errors; (b). Error charges cancellation.

3.6 Chapter summary

In this chapter, the high-level design for the required system is illustrated. The proposed synthesizer is based on the wide BW fractional-N PLL which can be divided into three categories. Each of the architectures is introduced comprehensively. While the fractional-N PLL with phase noise cancellation path will be selected as the basic architecture for further development in this work.

As we know, there are three main design problems for the fractional-N PLL using noise cancellation path:

A. Error charge mismatch between the signal and noise cancellation path;

B. Nonlinearity in PFD/CP;

C. Additive noise in DAC.

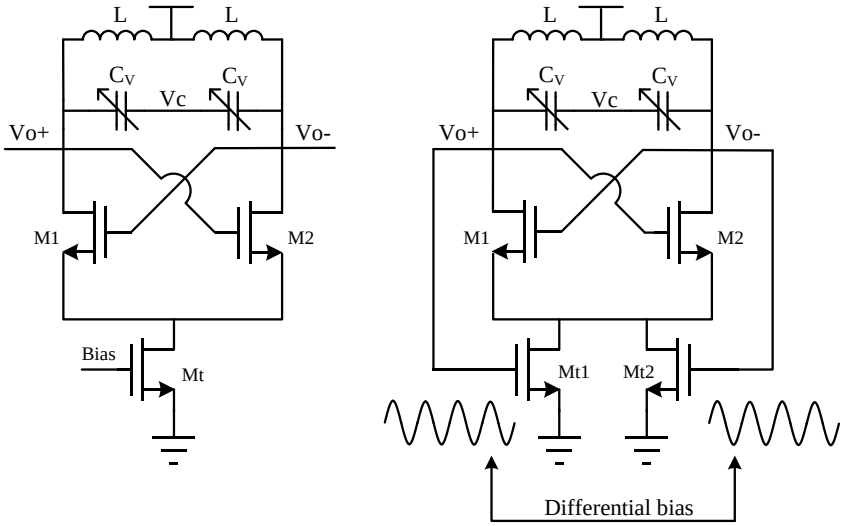
Each problem has been investigated and the corresponding solution is proposed. Based on these solutions, the proposed architecture is developed and the details for each sub-blocks is illustrated. First of all, the retiming circuit is adopted to increase the overlapped area between the CP and CS-DACs output, resulting in a significant reduction of the residual error charges. Secondly, to mitigate the nonlinearity in PFD/CP, the periodical timing offsets are fed to the CP input in order to shift the it up(down) to a more linear operation region, avoiding the high frequency noise folding effect. Moreover, a novel hybrid $\Delta\Sigma$ DAC, which is based on the segmented and cascaded modulator architectures, is developed to increase the equivalent output bits. As a result, the phase noise contributed by the proposed DAC is therefore reduced. Subsequently, the behavioral simulated results are shown in the end. The basic parameters are predicted and optimized to meet the system specifications. Further, the behavioral model of the hybrid $\Delta\Sigma$ DAC is built in simulink in order to verify its quantization noise performance. Finally, the behavioral model of the proposed fractional-N PLL is built to examine its functionality and the impact of the noise cancellation path.

CHAPTER 4

4 Circuit details and transistor-level simulated results

4.1 VCO

Compared to the ring oscillator, the LC structure shown in figure 4.1(a) has better noise performance and simple complexity and hence will be adopted in this work. However, no matter which structures will be used, how to minimize the power consumption while keeping good phase noise and required tuning range is the main problem in the VCO design. In section 4.1.1 and 4.1.2, the approaches for the design of the low power and low phase noise VCO will be introduced while in section 4.1.2, the proposed structure with its simulated results will be illustrated.



(a) (b)

Figure 4.1. LC VCO: (a). Classical architecture; (b). Switched biasing for phase noise reduction.

4.1.1 Low power design

For the LC VCO shown in figure 4.1 (a), if one assumes the input current of the LC tank is square wave (M1and M2 are supposed to be ideal switches), then at the frequency (w_0) of resonation, the harmonics of the input current will be rejected, leaving the fundamental to give rise to a differential output voltage swings $V_{O\pm}$, which is given by:

$$V_{O\pm} = \frac{4I_{bias}R_{eq}}{\pi} \tag{4.1}$$

where R_{eq} is the equivalent resistance contributed by the inductor, which is expressed as:

$$R_{eq} = w_0 LQ \tag{4.2}$$

where L and Q represent the inductance and quality factor of the LC tank, respectively. On the other hand, the minimum start-up gain A_{START} to guarantee the oscillation should be larger than unit, which is given by:

$$A_{START} = g_m R_{eq} = \frac{I_{bias}R_{eq}}{V_{OV}} = \frac{I_{bias}w_0 LQ}{V_{OV}} \geq 1 \tag{4.3}$$

where A_{START} can be set to 2-3 to have some margin. Equation (4.3) shows us that the bias current is inversely proportional to LQ. Therefore a large value of LQ product is necessary to be kept in order to minimize the power consumption [23].

4.1.2 Low phase noise design

In the early years, some researches [24], [25] had clarified that the tail current source may be the most significant contributor to the oscillator phase noise. To further illustrate, it can be recognized that the high frequency noise of the tail current source at twice the oscillation frequency ($2w_0 \pm \Delta w$) will be converted down to the oscillation frequency ($w_0 \pm \Delta w$) in a hard-switching oscillator,

while the other part, which is referred to as the low frequency noise closed to the carrier, will cause some other negative effects (AM-to-PM conversion of the nonlinear varactor, etc.) [26], [27] and eventually degrade the phase noise performance of the oscillator. Hence, the flicker noise in the tail transistor plays an important role in the phase noise conversion. In a word, how to suppress the flicker noise in the tail current source is the main issue in the oscillator design. Filtering technique for the tail current sources [28], which provides high impedance at the common source node of the differential pair and a directed path to ground for the noise of tail current source at $2w_0$, is an effective approach to reduce the converted flicker noise. However, the disadvantage of this filtering technique is that the passive reactive components used for noise suppression often occupies large area and hence is not friendly to realize a high integrated design.

Furthermore, it is well known that the origination of flicker noise is due to the carriers accumulated in the imperfect traps of the surface of the transistors and hence can be regarded as the "long-term memory" mechanism correlated to the time and practical physical process. Therefore, one effective approach to reduce such memory-related noise is refers to as the switched biasing [29], which provides periodical biasing pulses to the transistor gate in order to release the electronics stored in the surfaced traps periodically, resulting in an intrinsic reduction of the flicker noise. When this approach is applied to the tail transistors in the VCO [30], as shown in figure 4.1(b), the phase noise contributed by the flicker noise of $M_{t1/2}$ will be therefore reduced while the area-costing passive components [28] for noise filtering can be saved. On the other hand, thanks to the differential output of the VCO, the switched biasing current source can be "self-biased" by $V_{O\pm}$ and hence save the biasing circuits to the oscillator.

4.1.3 Proposed VCO

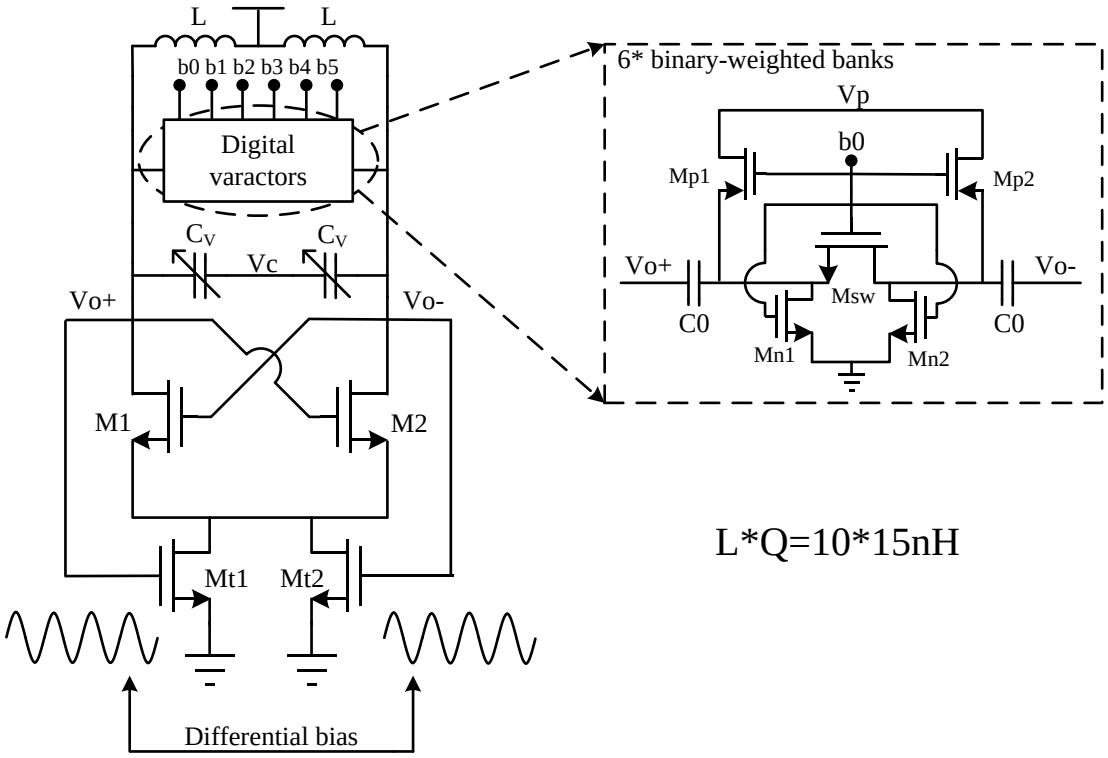


Figure 4.2. Proposed LC VCO architecture.

By considering the low power and low noise solutions, the proposed VCO is therefore developed shown in figure 4.2. The LQ product is set to 150nH in order to decrease the power consumption. The switched biasing is adopted to reduce the phase noise contributed by the flicker noise in the tail transistors.

Except for the noise and power considerations, it is also known that a large VCO gain can help to widen the output frequency range. However, the varactor with large gain will also increase the sensitivity to the fluctuation of control voltage and hence induce more phase noise. Even if the control voltage is noiseless, the varactor with large gain will also enhance the AM-to-PM conversion, resulting in phase noise degradation. In order to ensure that the VCO output range is sufficiently wide to cover the required frequency bands while keeping the varactor with small gain. The digital control capacitor banks with biasing circuits presented in [31] will be used here. As shown in figure 4.2, when the banks is enabled (b0 is high, etc.), transistor Msw is on and Mn1/2 will provide dc bias to the drain and source of Msw to keep the minimum

on-resistance and hence to maximize the on-Q factor. For this to be true, the size of Mn1/2 should be minimized to avoid the degradation of tuning ratio. When the bank is disabled, Msw and Mn1/2 are off in principle. However, due to the large output swing of VCO, the drain and source of Msw will swing below ground and thus be turned on slightly, leading to a poor off-Q. To avoid this negative effect, transistor Mp1/2 will be added to bias the drain and source of Msw by voltage Vp to ensure that Msw is certainly turned off when the bank is disabled. The widths of Mp1/2 are designed to be the minimum value while their lengths should be long enough in order to minimize the parasitic capacitances and keep high impedance between the bottom plate of the capacitors (C0, etc.) and Vp, respectively. Finally, transistor Msw with larger size can increase the on-Q by minimum on-resistance. However, this will result in a narrower tuning ratio and thus an optimization should be made for the size of Msw carefully.

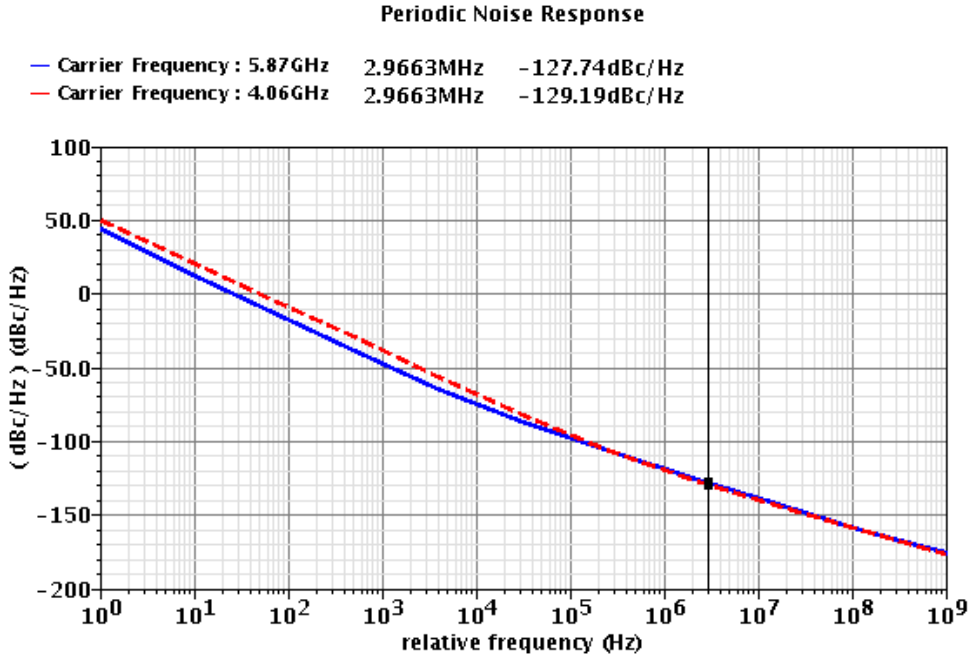


Figure 4.3. Transistor-level simulated results for VCO phase noise in the tuning edges of the output frequency.

The relative simulated result for the VCO phase noise in different frequency bands is shown in figure 4.3. As we see, when the output frequency is tuned to the maximum value (5.87GHz), the phase noise at 3MHz offset is -127.74dBc/Hz. When the output frequency reaches to the minimum point (4.06GHz), the related phase noise is -129.19dBc/Hz at 3MHz offset. Both the out-of-band phase noise performance (at 3MHz offset) meets the specification

for LTE system (refer to section 2.3.1). Furthermore, it is known that the PLL phase noise contributed by the VCO can be expressed as:

$$S_{PLL|VCO}(2\pi f) = S_{VCO} \times \left| \frac{1}{1 - A(2\pi f)} \right|^2 \tag{4.4}$$

Hence the VCO contribution to the PLL phase noise can be derived by the simulated data, as shown in figure 4.4.

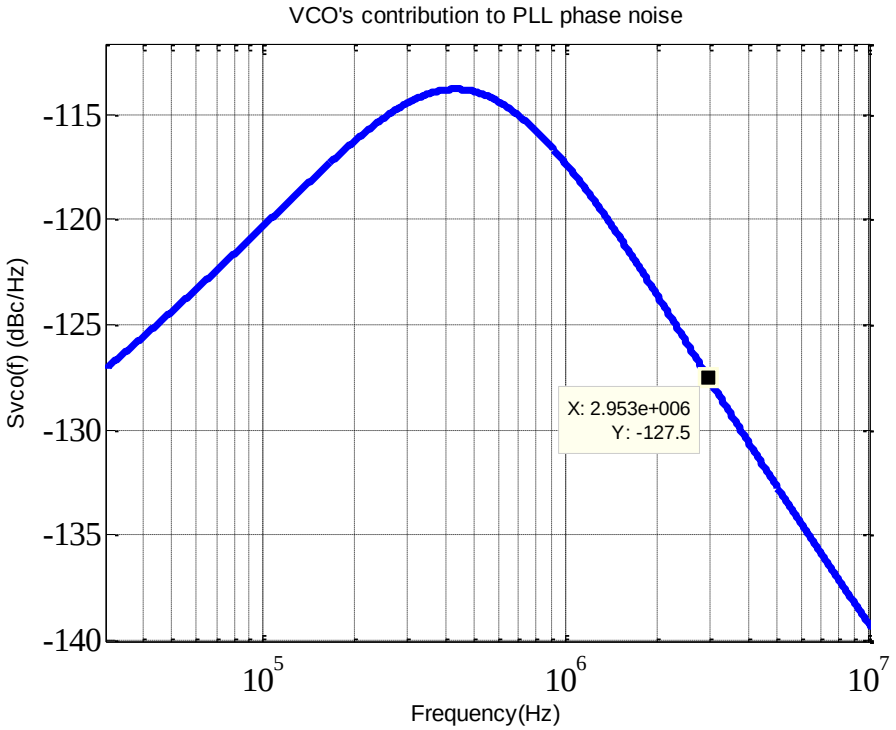


Figure 4.4. PLL phase noise contributed by VCO.

What's more, the tuning range of the proposed VCO is also can be simulated. Figure 4.5 depicts the relationship between the VCO output frequency and control voltage. As we expect, by using the digital tuning banks and post frequency dividers, the output range which is from 5.87 to 4.06 GHz is capable of covering the required frequency bands. Additionally, it is evident that the overlapped area between each tuning banks is always can be found, avoiding the dead band problem at the PLL output.

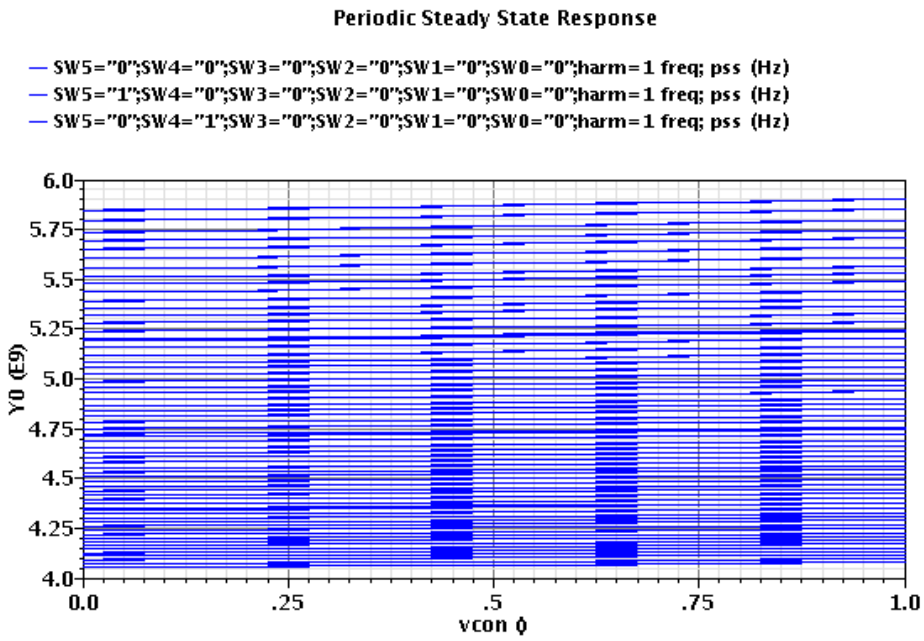


Figure 4.5. VCO output frequency VS. Control voltage.

The current consumption of proposed VCO is 1.18mA from a 1V supply when the output frequency is 5.87 GHz. Moreover, the Figure-of-Merit (FoM), which is described in equation (4.5), can also be adopted to estimate the VCO performance alternatively.

$$FoM = S(\Delta f) - 20\lg(\frac{f_0}{\Delta f}) + 10\lg(\frac{P_{total}}{1mW}) \qquad (4.5)$$

Finally, the transistor-level simulated results are collected in table 4.1

Phase noise	-127.84dBc/Hz @3MHz, carrier frequency: 5.87GHz -129.29dBc/Hz @3MHz, carrier frequency: 4.06GHz
Tuning range	4.06~5.87GHz with 64 coarse-tuning banks K_{VCO} ≈ 53MHz/V for fine tuning
Voltage supply	1 V
Current consumption	1.18mA for maximum output frequency 1.66mA for minimum output frequency
FoM	-193 ~ -189.7dB

Table 4.1. VCO performance summary

4.2 Charge pump

As we know, the mismatch and noise in CP will directly inject into the loop filter and hence corrupt the PLL performance. Hence some advanced architectures should be used to overcome these undesired results.

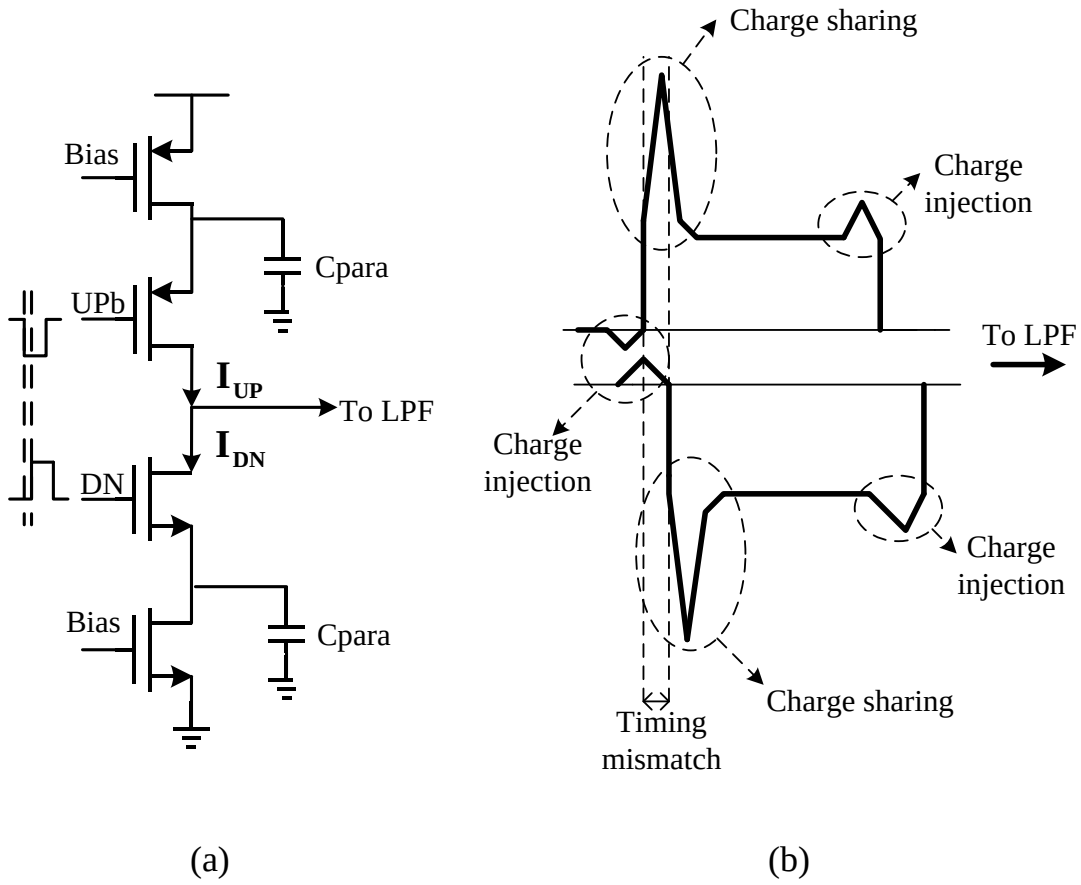


Figure 4.6. Non-linear effects of standard CP: (a). Schematic; (b). The relative up and down current pulses.

Firstly, the mismatch of the CP will be concerned. As analyzed earlier, the current mismatch will give rise to the spurious tones at the PLL output. Especially in the fractional-N PLL, any current mismatch will result in a high frequency noise folding problem at the PLL output spectrum and hence deteriorate the in-band phase noise, as shown in figure 3.7 and 3.8. What's more, nonlinear effects, such as the leakage current, timing mismatch in PFD and current mismatch between the up and down current sources [32] can be solved effectively by simple design tricky. For instance, by increasing the CP

output current, the leakage current can be greatly decreased when the CP is turned off. The timing mismatch in PFD can be reduced by adding proper delays into the up and down PFD branches. While another nonlinear effects including the charge sharing and injection are often hard to fight and will be mainly analyzed in the following.

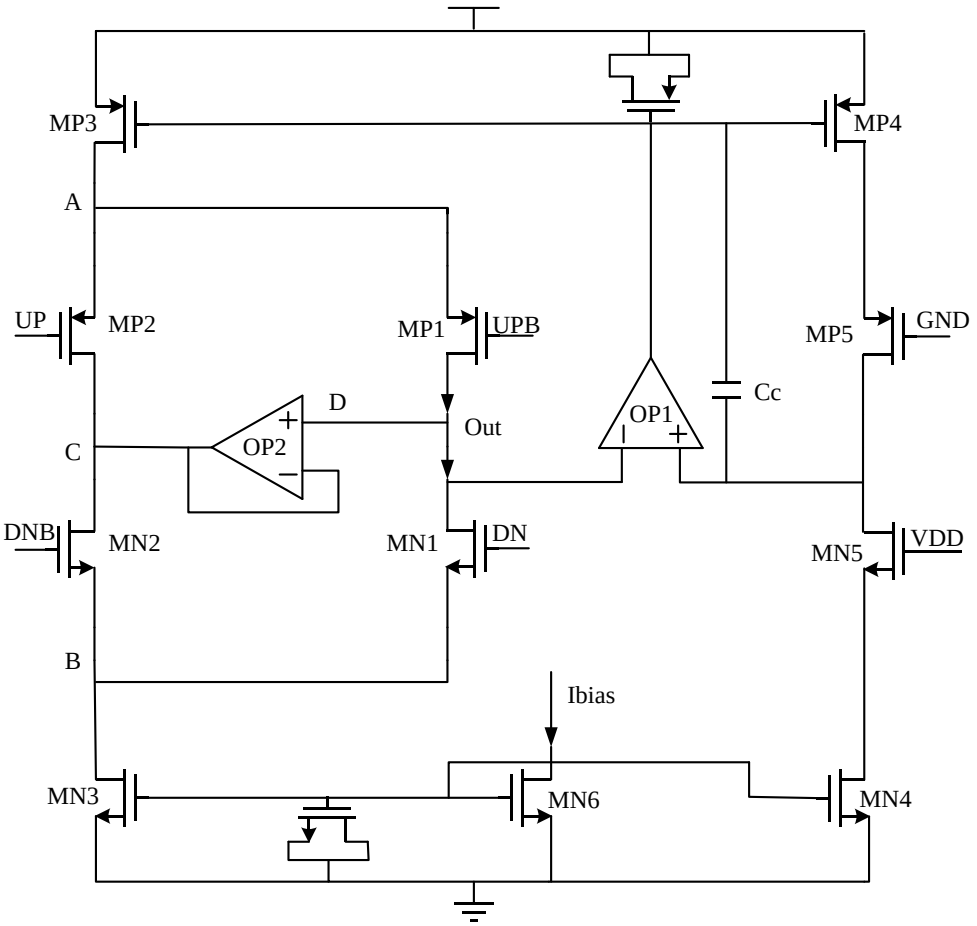


Figure 4.7. Schematic of a conventional current steering CP.

If the standard CP shown in figure 4.6 (a) is designed, the charge injection and sharing problems will become effective as shown in figure 4.6 (b). For example, when the up (down) switch is turned off, the relative output current will flow into the parasitic capacitance *Cpara* which is between the drain of the current source and the source of the switch. When the related branches is enabled again, the charge stored in the *Cpara* will inject into the loop filter and thus induce an high-level spike on the output current pulse, leading to an increment of charge mismatch between the up and down current sources. This is so-called charge sharing. On the other hand, when the switch is turned on,

the charge at the CP output will be pulled off the loop filter in order to form the inversion layer in the switch channel, inducing an initial downward (upward) spike. When the switch is turned off, the charge stored in the switch channel will be forced into the loop filter and hence give rise to another upward (downward) spike on the current pulse. Such effects are called charge injection.

The current-steering charge pump [32] can be adopted to mitigate these parasitic charge problems. As shown in figure 4.7, a replica branch which consists of MP2 and MN2 is used to improve the charge sharing. An unit gain voltage buffer OP1 is used to keep the voltage at replica node C the same as the output node D. Apparently, the charge sharing effect mainly occurs at the node A and B. When the output switches MP1 (or MN1) is turned off, the output current from the current sources MP3 (or MN3) will flow into the other branch since the switches MP2 (or MN2) is turned on by the inversed PFD enabled pulses simultaneously. For this to be true, the parasitic capacitances at node A and B will not be capable of storing the charge, minimizing the charge sharing issue. Furthermore, another replica branch composed by MP4-5, MN4-5 and OP2 are used to provide a feedback loop in order to maintain the equality between the up and down output currents.

The disadvantage of this architecture is that the timing mismatch between the enabled pulses of the output and replica (MN2 and MP2) branches is inevitable in the practical design. Some charges are therefore stored in the parasitic capacitance in the time slot between the enabled pulses for different branches, inducing the charge sharing problem. On the other hand, although the adoption of small size switches can alleviate the charge injection effect, the low voltage supply (1V) and high output current (450 μA) requirements in this work determine that the size of the switches have to be large to a certain extent. Otherwise the linear output range of the CP will be reduced. In order to overcome these disadvantages, the proposed architecture is therefore developed which is shown in figure 4.8.

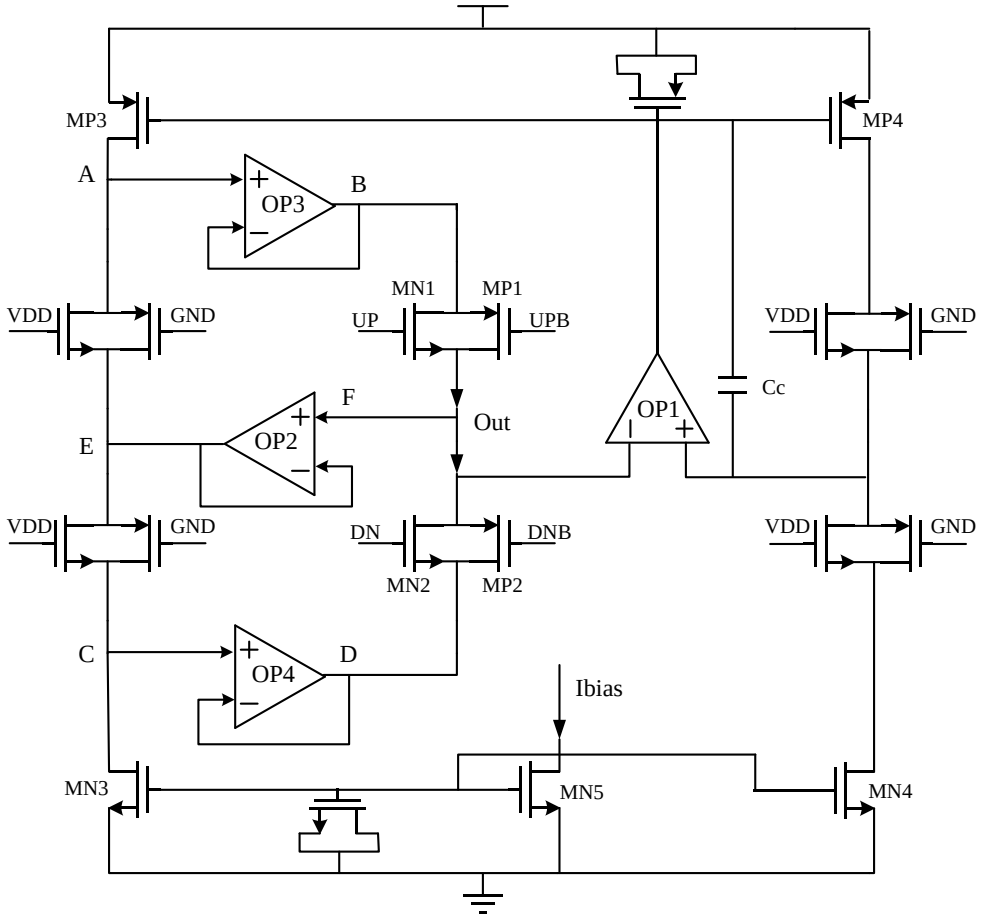


Figure 4.8. Schematic of proposed CP.

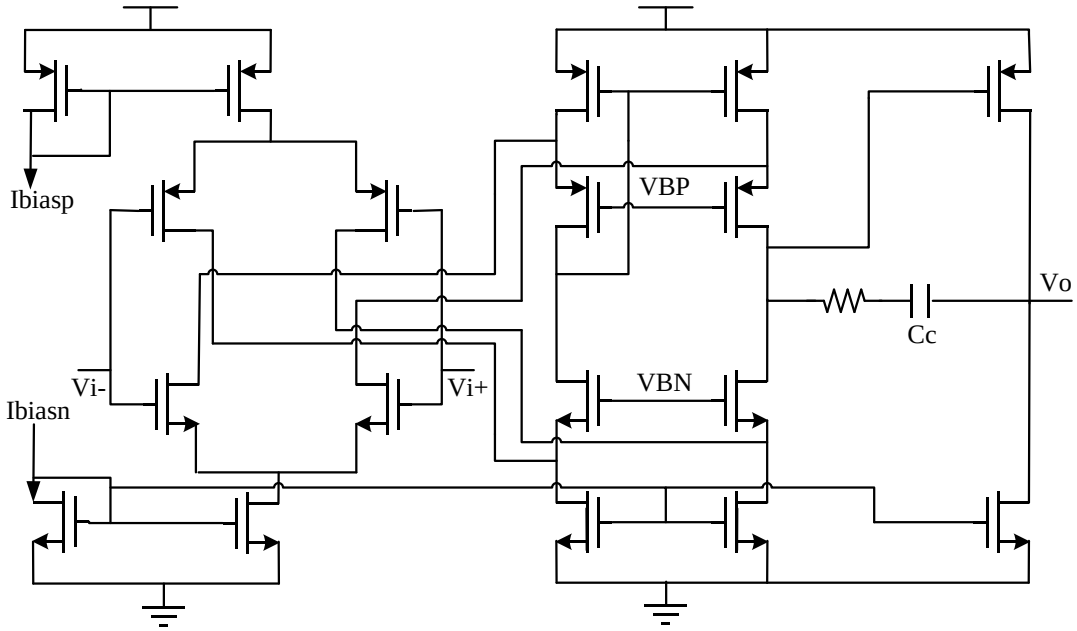


Figure 4.9. Schematic of OPAMP with rail-to-rail input stage for the unit gain voltage buffers-OP1 and OP2 in the proposed CP.

Compared to the conventional current-steering charge pump, two additional unit gain voltage buffer OP3 and OP4 are inserted between the output and the replica branches [33] in the proposed architecture shown in figure 4.8. By using the operational amplifier - OP3 (OP4) to buffer the drain voltage of the current transistors MP3 (MN3), the switches of the replica branch on the left side can be kept on at all times and hence avoid the timing mismatch between different branches. As a result, the charge sharing effect at node A (and C) can be eliminated completely. Moreover, in order to reduce the charge injection from the channels of the switch transistors, the complementary switch pairs [34] are utilized to replace the typical switches in all branches. Compared to its partner, the switch in the pairs has the proper sizing ratio and enabled pulse with inversed phase. This means that when one switch in the pair is turned off, the charge stored in its channel will not be pushed onto the loop filter but absorbed by the complementary one and vice verses. Finally, it is also known that the DC gain of OP1 and OP2 will be modulated by the CP output voltage, leading to an increment of the voltage offset between the replica and output branches which will result in a mismatch between the output current pulses. To mitigate this effect, the operational amplifier with rail-to-rail input stage shown in figure 4.9 is adopted for both OP1 and OP2. While the second stage of this amplifier are designed to maintain a high DC gain.

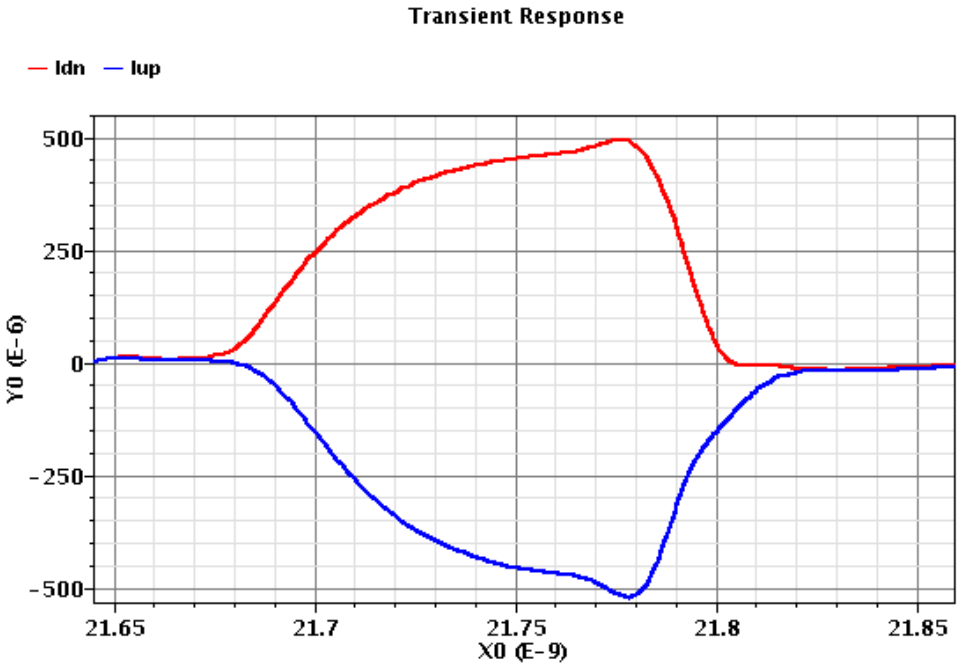


Figure 4.10. Simulated result of CP current pulses.

The transient responses of the output current pulses are shown in figure 4.10.

Compared to the predicted pulses in figure 4.6 (b), we can find that the charge injection and sharing effects almost disappear while the up and down current mismatch and timing mismatch in PFD is greatly improved by this sophisticated design.

Secondly, the noise performance of the proposed CP and its contribution to the PLL output will be investigated. It is well known that the phase noise contributed by the CP is expressed as:

$$S_{PLL|CP}(2\pi f) = S_{CP} \times \left| \frac{A(2\pi f)}{1 + A(2\pi f)} \right|^2 \tag{4.6}$$

where S_{CP} is:

$$S_{CP} = \overline{i_n}^2 \left(\frac{2\pi N}{I_{CP}}\right)^2 \tag{4.7}$$

where $\overline{i_n}^2$ is the intrinsic noise in the current sources of CP. It is worth nothing that when the CP noise is converted to the phase noise, it will amplify by N^2 times after entering the system loop. On the other hand, from equation (4.6) and (4.7), we can know that in the wide BW PLL, the CP output current should be large enough so as to avoid more noise to inject into the bandwidth and hence keep the integrated phase noise meet the specific requirement.

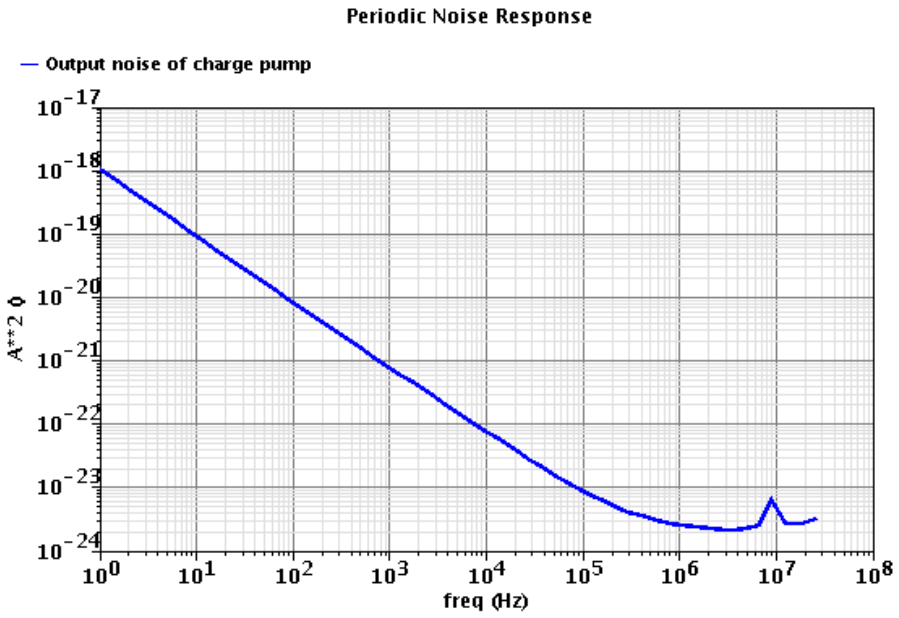


Figure 4.11. Simulated result of CP output noise.

The simulated result for the CP noise $\overline{i_n^2}$ is given in figure 4.11. By using equation (4.6) and (4.7), we can convert the simulated data of $\overline{i_n^2}$ to the PLL phase noise, which is shown in figure 4.12. As we see, the in-band phase noise contributed by CP is -112.1dBc/Hz at 100 kHz offset, which is mainly due to the amplification of the dividing ratio N.

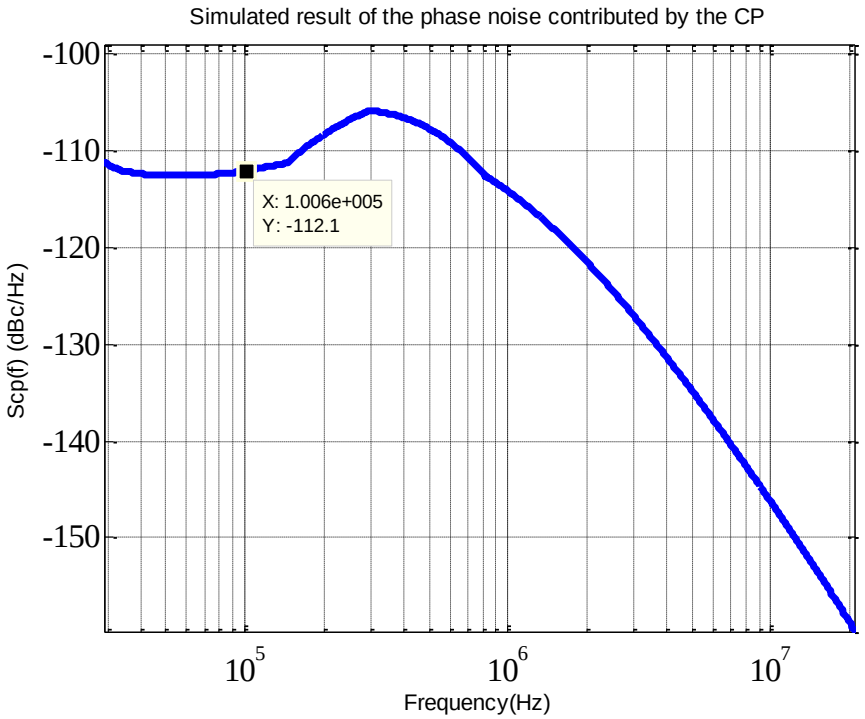


Figure 4.12. PLL phase noise contributed by CP.

In the end, the CP output current level is 0.45mA approximately. The total current consumption of the PFD/CP circuitry is 3.95mA from a 1V supply.

4.3 ΔΣ modulator

As analyzed earlier, the DSM should provide sufficient input bits to avoid the frequency dead bands at the PLL output while the switching intense determined by the output bits can be reduced by the offset current at the CP. Therefore, an 18 bits DC input will be used in our design in order to keep the minimum frequency resolution meet the requirement of the channel spacing in LTE system. Moreover, a one-bit dithering is inserted to randomize the LSB of

proposed modulator in order to alleviate the spurious tones at the relative output spectrum. The 2nd-order single-loop architecture will be chosen when considering available area (see figure 3.9) after enabling the noise cancellation path. The design work is done with the assistance of the Matlab Delta-Sigma Toolbox [35]. The proposed architecture is shown in figure 4.13.

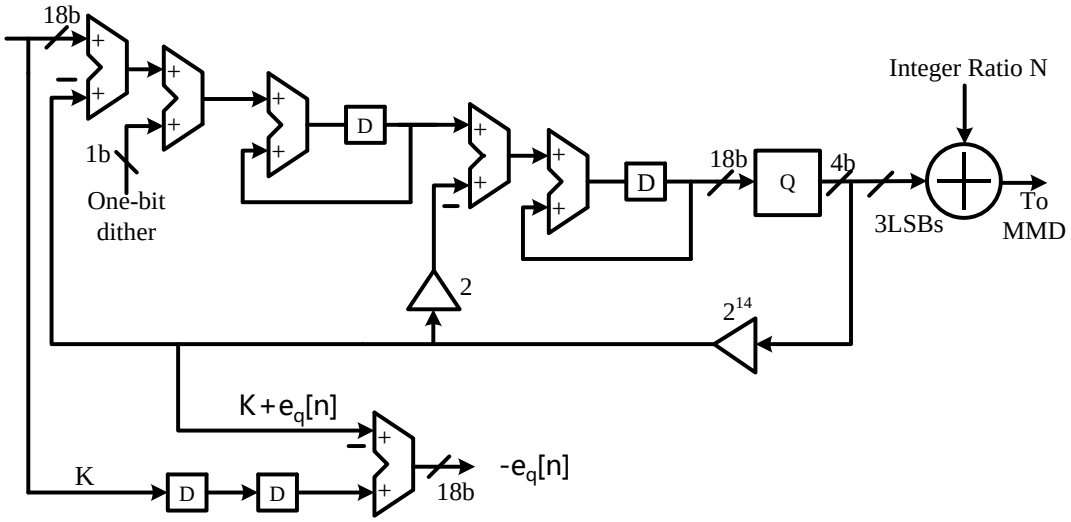


Figure 4.13. Proposed 2nd-order ΔΣ modulator for PLL

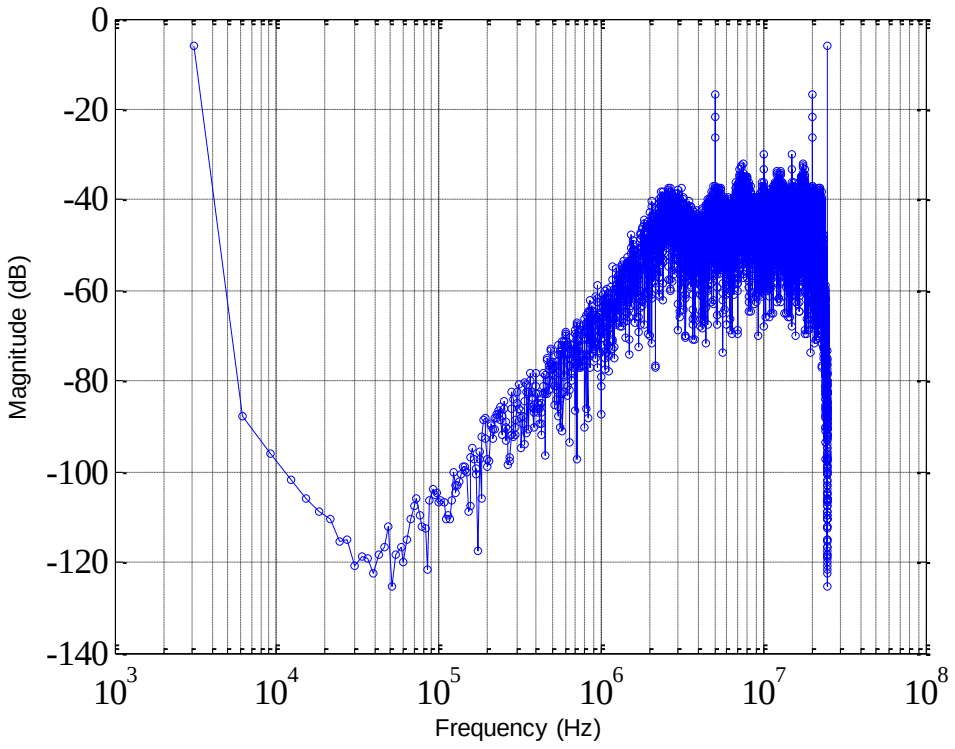


Figure 4.14. Transistor-level simulated result for the DSM output spectrum of DC input -0.1 (8192 points FFT).

The noise and signal transfer function of the proposed modulator are given by:

$$STF(z) = z^{-2}$$
$$NTF(z) = \left(1 - z^{-1}\right)^2 \tag{4.8}$$

By making a subtraction between the DSM output and input, the quantization error $e_q[n]$ can be extracted for the subsequent processing. Moreover, the multiple factors can be easily obtained by bit shifting operation in the digital modulator. Finally, the output bits combined with the integer bit pattern will be fed to the multi-modules divider.

The relative simulated result for the output spectrum is shown in figure 4.14. By using the equation (3.6) and the simulated data in figure 4.13, we also can estimate the phase noise contributed by DSM at the PLL output, which is given in figure 4.15.

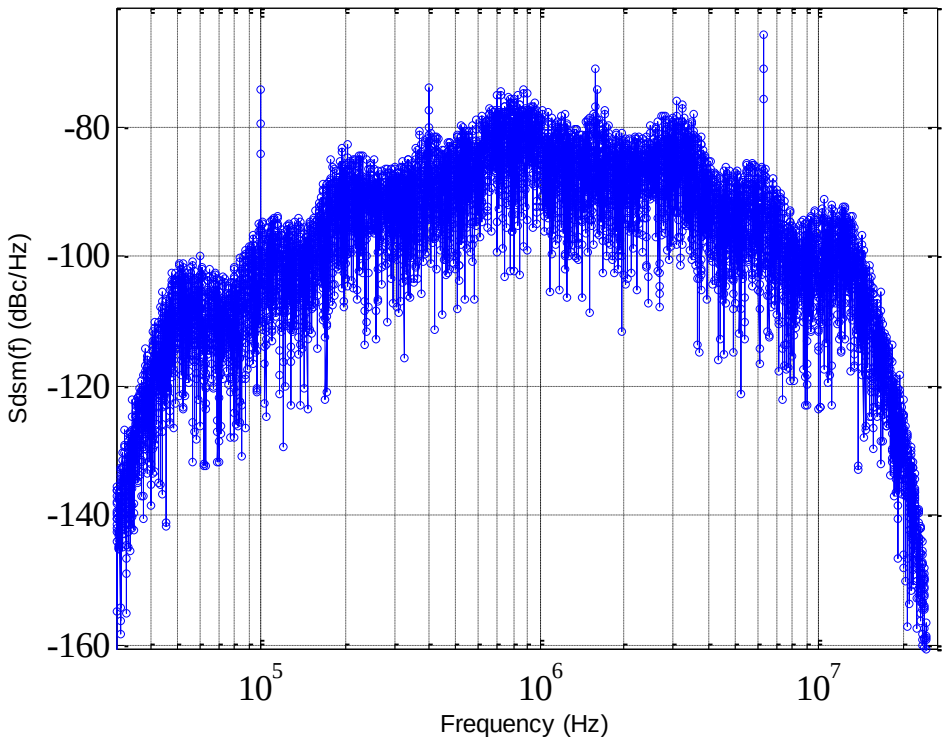


Figure 4.15. PLL phase noise contributed by DSM.

As we see in figure 4.15, some spurious tones are folded back into the PLL bandwidth. This is due to fact that the insufficient order of proposed modulator will give rise to some spurs at the high frequency of its output spectrum (as shown in figure 4.14), which will be folded into the lower frequency by multiplying the PLL closed loop transfer function (see equation (3.6)). But anyway, such undesired spurs will eventually be attenuated by enabling the noise cancellation path since they are correlated with the quantization error $e_q[n]$.

4.4 ΔΣ DAC

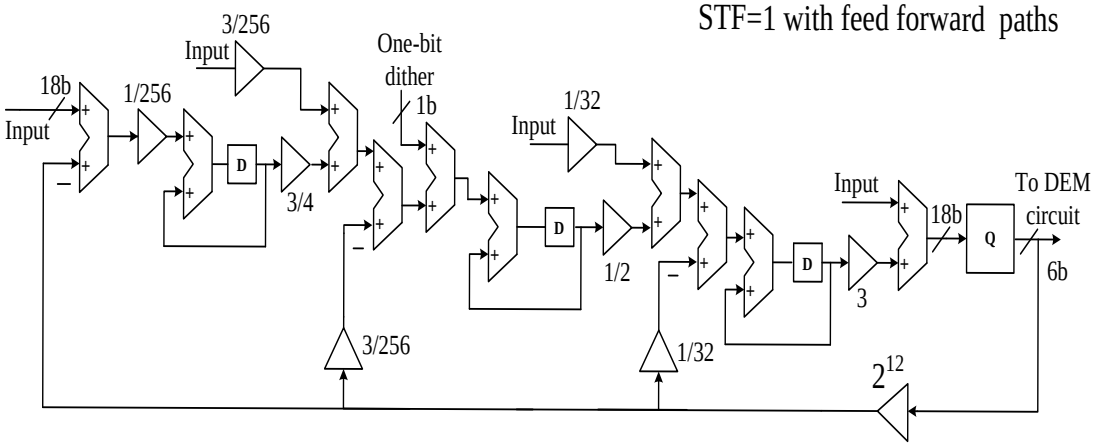


Figure 4.16. Proposed 3rd-order modulator with feed forward paths for ΔΣ DAC.

As analyzed in section 3.4.3. The 3rd-order single-loop modulator used in each path of the proposed ΔΣ DAC shown in figure 4.16 is developed. By referring to the equation (3.16), we know that the signal transfer function $STF(z)$ of proposed modulator should be easy to be constructed in order to ease the difficulty of extracting the shaped requantization noise $STF_1(z)E_{rq}(z)$ for the subsequent processing. The feed forward path in figure 4.16 is therefore adopted to ensure that the signal transfer function *STF* is equal to unit [14]. Furthermore, similar to the modulator used for providing the fraction ratio, the one-bit dither generated from the 25 bit LFSR is added to avoid the spurious tones at the output spectrum. The relative *NTF* and *STF* can be expressed as:

$$STF(z) = 1$$

$$NTF(z) = \frac{(z-1)^3}{(z-0.5)(z^2-0.5z+0.25)} \tag{4.9}$$

Note that the modulator in each path is not identical. For further improving the DAC performance, the modulator in primary path can be designed to guarantee the stability while the one in secondary path can have higher order for shaping the requantization noise more efficiently.

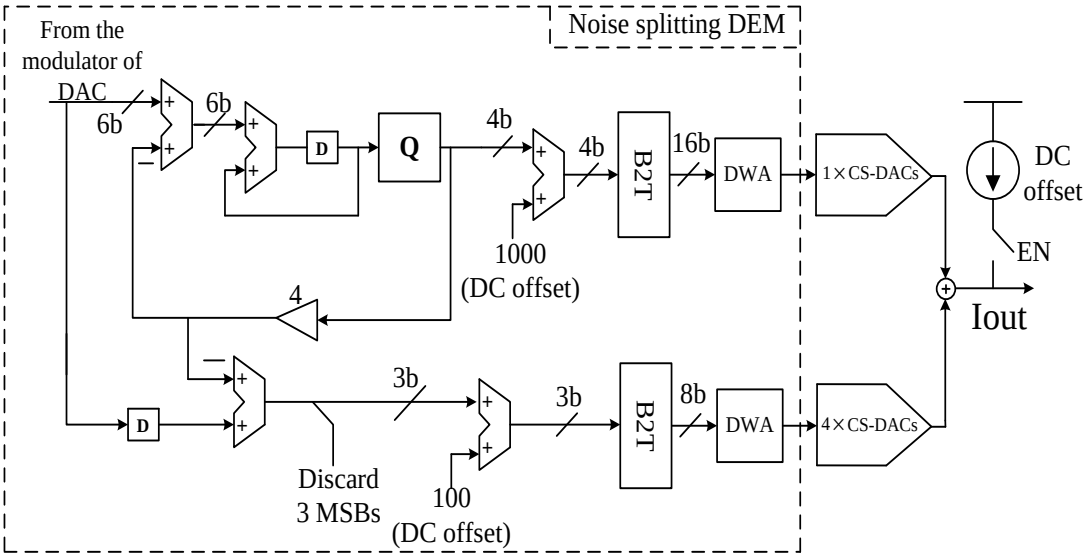


Figure 4.17. Schematic of noise splitting DEM.

As described earlier, the proposed ΔΣ DAC is the combination of the segmented [16] and cascaded [18] modulator architectures for increasing the output resolution while keeping achievable system complexity. In particular, the nose splitting DEM shown in figure 4.17 in each path of proposed DAC is analyzed as follows. Firstly, the adoption of the 1st-order modulator can reduce the mismatch between the segmented parts. This is due to the fact that the processing signal in the upper segmented part includes the signal from the former modulator and the shaped noise from the 1st-order modulator itself while the lower part only includes the extracted shaped noise. Hence when the two paths are summed in the analog domain, any mismatch between the analog devices will only affect the cancellation of the shaped noise from the 1st-order modulator whereas the recovering signal will almost keep its integrity.

Moreover, the digital DC offsets are added into the signals before they enter into the Binary-To-Thermometer (B2T) decoders in order to avoid the destruction of the digital waveforms in the progress of decoding. However, such digital DC offsets will affect the correction of the gain levels of the recovering signal at the CS-DAC output and hence will be eliminated by the compensated current banks controlled by the relative enabled logic.

After the processing of this DEM circuitry, the corresponding signals including the requantization noise will be converted to the current pulses by the CS-DAC banks, which are shown in figure 4.18.

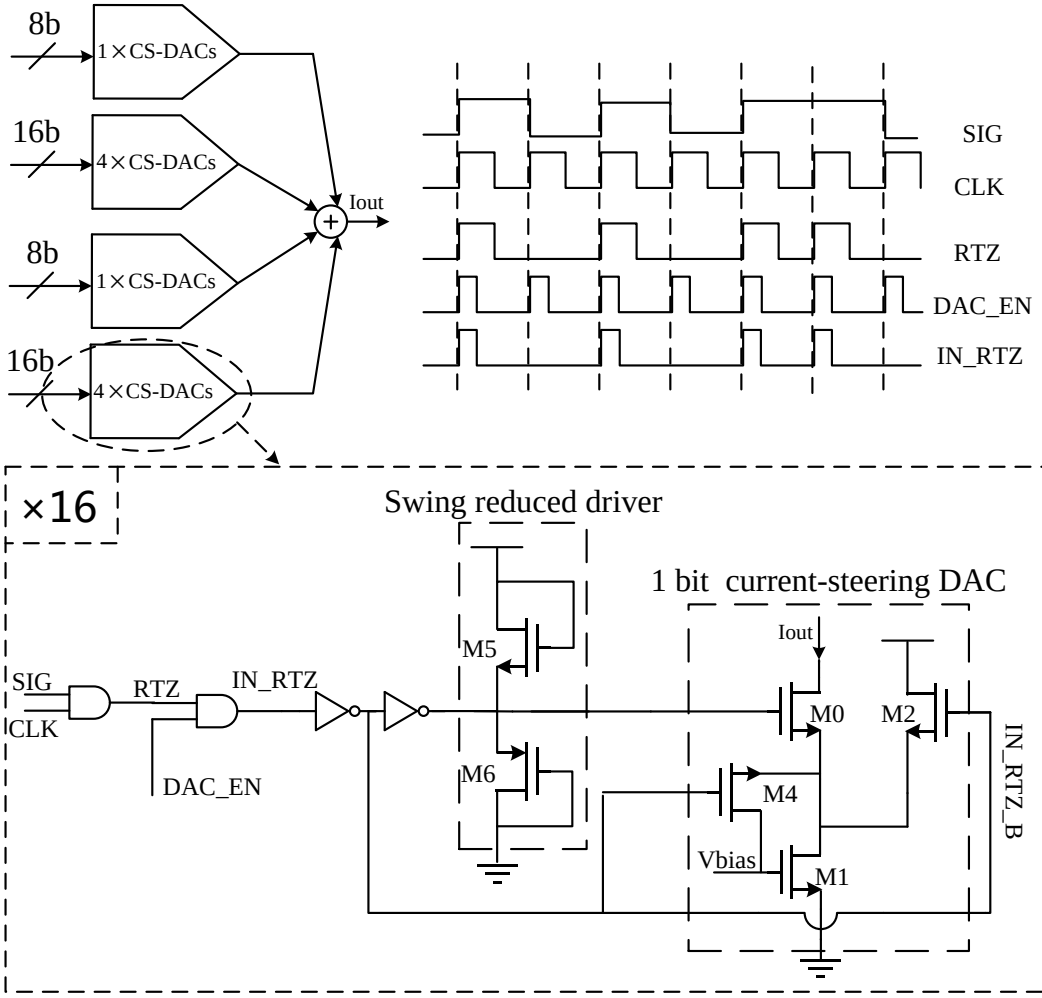


Figure 4.18. Schematic of proposed CS-DAC.

As we see in figure 4.18, before the digital signal comes to the current-steering DAC, some steps are needed to shape the signals to meet the requirement of

specific D/A conversion. First of all, we have the signal (SIG) "and" the system clock (CLK) from the divider output to generate the Return-To-Zero (RTZ) pulse, in order to minimize the Inter-Symbol-Interference (ISI) error [36]. Certainly, other advanced methods (ISI-shaper or sample and hold filter, etc.) can be adopted alternatively to further reject the ISI error [17], [21]. Subsequently, the DAC enabled sequence (DAC_EN) from the retiming circuit will be used to shape the duration of signal RTZ to 4 times VCO periods, following the specification mentioned before. Subsequently, the swing of the shaped signal (IN_RTZ) will be reduce by two diodes - M5 and M6, in order to mitigate the feed though effect which is due to the parasitic capacitance at the gate of the transistor M0. What's more, transistors M4 and M2 are used to alleviate the charge injection when M1 is turned on/off on one side, and keep the DC biasing voltage on the other side.

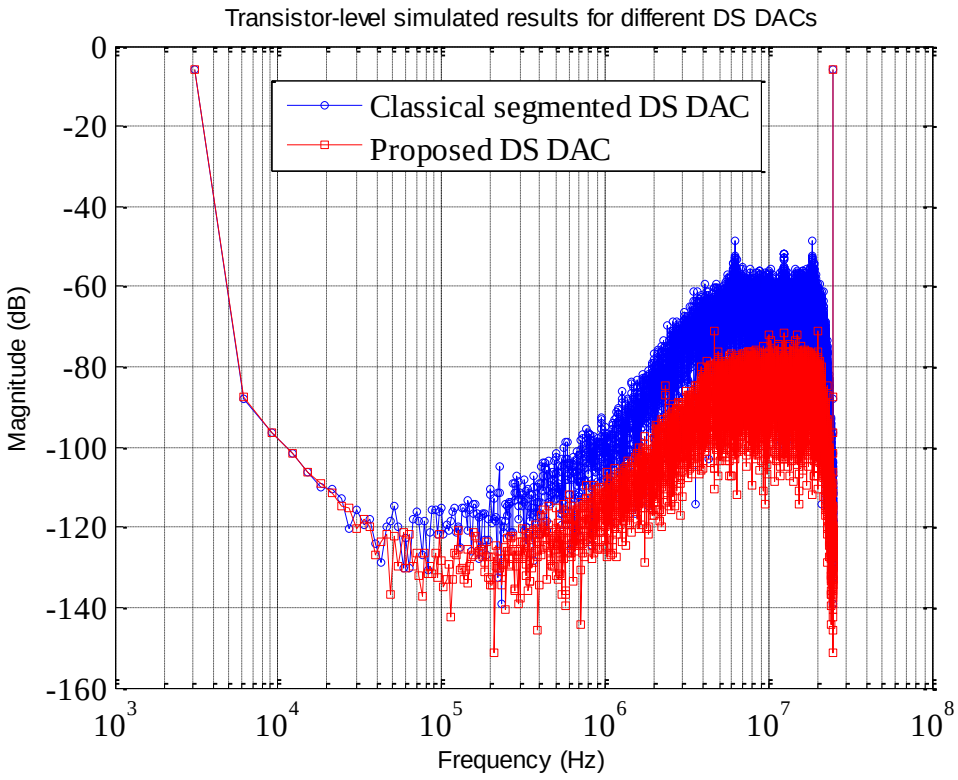


Figure 4.19. Transistor-level simulated results of output spectrums for different ΔΣ DACs (8192 points FFT).

Then the corresponding simulated results in transistor-level can be obtained. At the first, the output spectrums for different ΔΣ DACs are shown in figure 4.19.

Obviously, compared to the traditional segmented ΔΣ DACs (which is equivalent to the proposed DAC when disconnecting its secondary path), the quantization noise of the proposed DACs is decreased by 18 dB approximately at the high frequency. However, there is some differences from the behavioral simulated results obtained in figure 3.21, the in-band noise (<1MHz) of proposed DACs is increased by around 10 dB. This is mainly due to the analog mismatch between the primary and secondary path in the proposed architecture.

By using equation (3.10) and the simulated data from figure 4.19, we also can calculate the PLL phase noise contributed by the noise cancellation path, which is shown in figure 4.20.

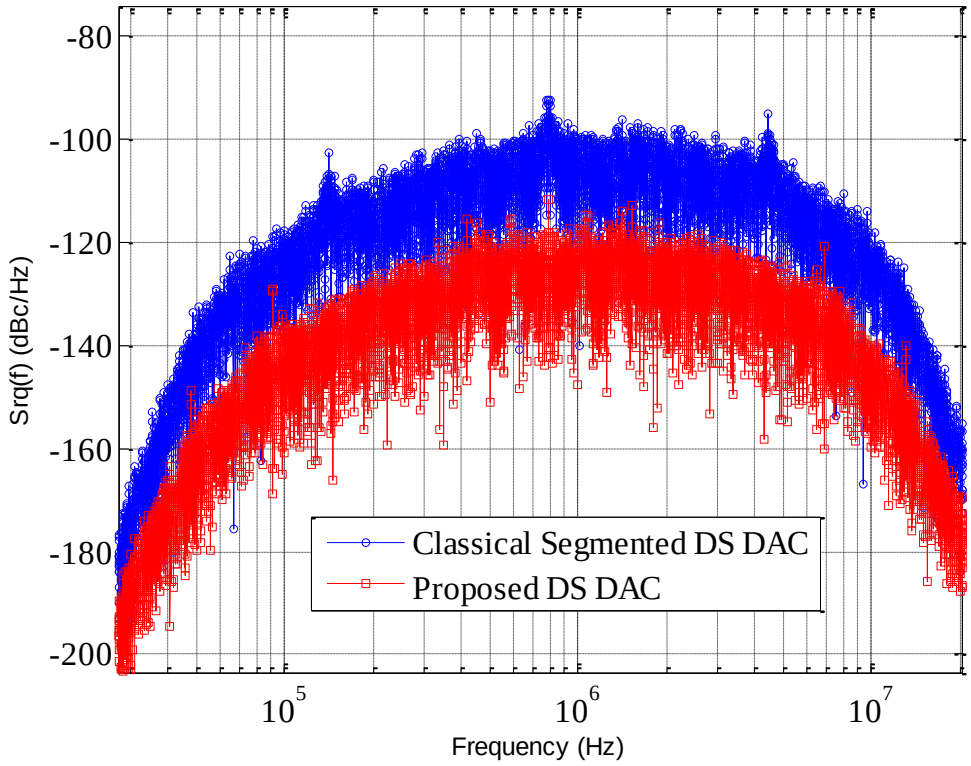


Figure 4.20. Transistor-simulated results of PLL phase noise contributed by different ΔΣ DACs.

4.4.1 Estimation of the impact of ΔΣ DAC on the PLL phase noise

In this project, verifying the functionality of the phase noise cancellation path to PLL is very time-consuming in transistor-level simulation and hence is not included in our work plan. However, since we have obtained the simulated results for the phase noise contributed by each important block, the impact of the noise cancellation path on the phase noise at the PLL output can therefore be estimated by using some mismatch assumptions introduced in the former sections. Note that the in-band phase noise performance is dominated by the PFD/CP while the phase noise contributed by the synchronous divider is low and hence can be neglected in this estimation.

First of all, by using the transistor-level simulated data, we can derive the PLL phase noise when disconnecting the noise cancellation path, which is shown in figure 4.21.

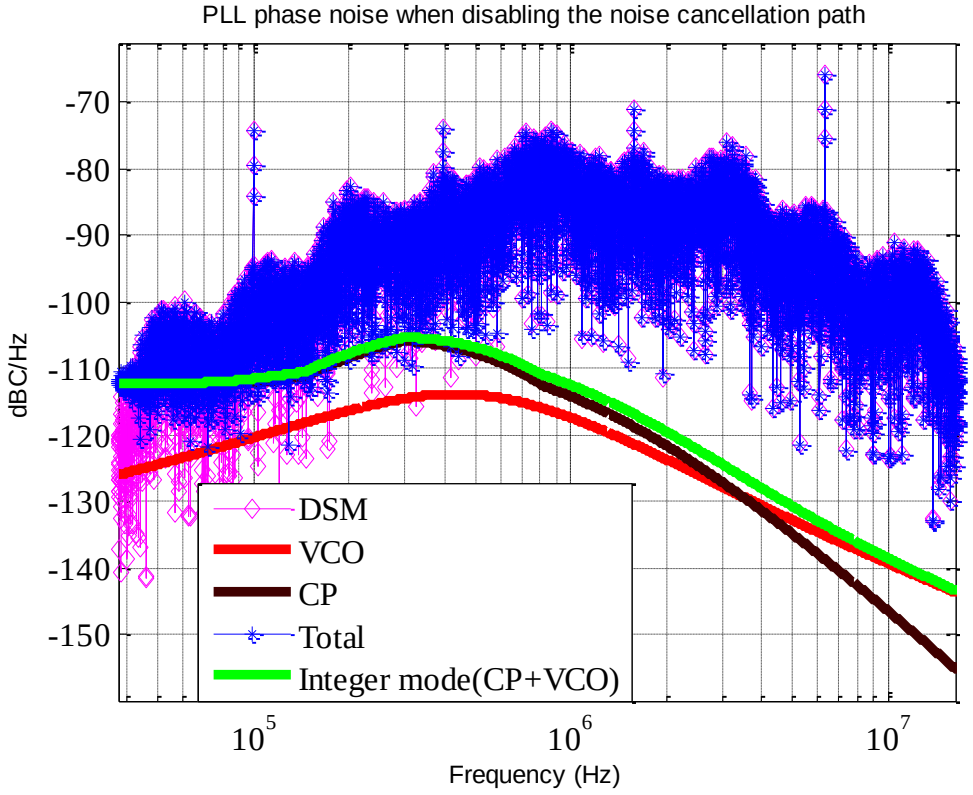


Figure 4.21. Estimation of PLL phase noise when disabling the noise cancellation path.

Apparently, Instead of the phase noise contributed by VCO, the out-of-band phase noise is dominated by the DSM since the wide loop bandwidth can not suppress the quantization noise effectively. If we assume that the noise cancellation path is ideal, its performance is only dependent on the error charge mismatch introduced in section. 3.3.1. We also assume that the mismatch factor α is 1%, and 10%, respectively. Then we can derive the available area (see figure 3.9) for the phase noise from the proposed DAC, as shown in figure 4.22.

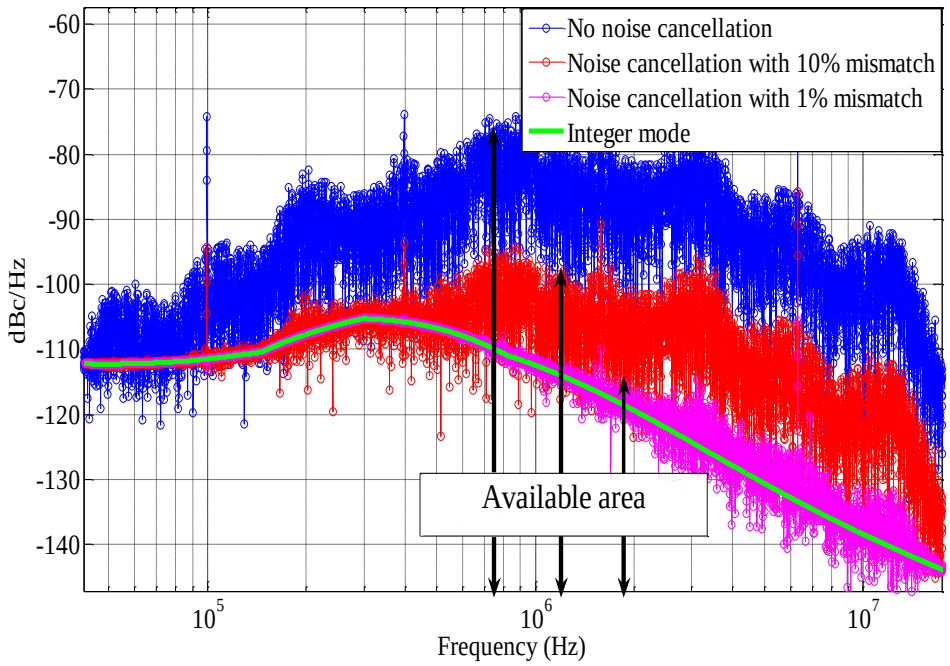


Figure 4.22. Available areas of DAC phase noise when the error charge mismatch between the signal and noise cancellation path is 10% and 1%, respectively.

As seen in figure 4.22, the less the error charge mismatch, the smaller the available area is reserved for the phase noise from the proposed DAC. In particularly, if the phase noise from the proposed DAC can still place in the available area when the error charge mismatch is only 1%, we can say that the proposed DAC meets the design specification. (Note that 1% error charge mismatch can be regarded as a pretty excellent result for this phase noise cancellation technique.)

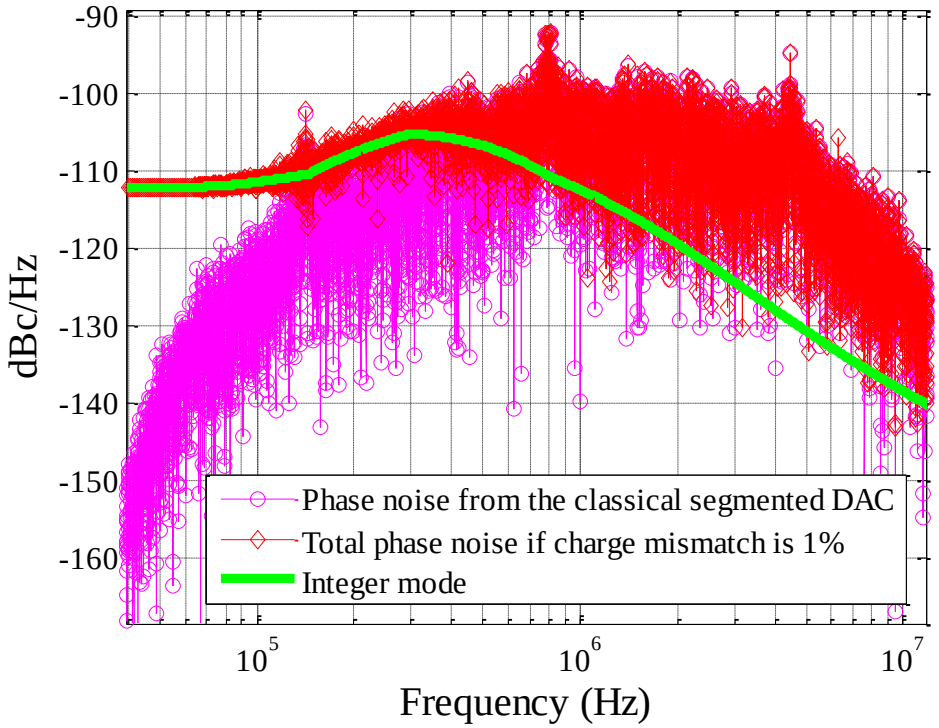


Figure 4.23. Impact of the phase noise of classical segmented DAC on the PLL phase noise when the error charge mismatch is assumed to be 1%.

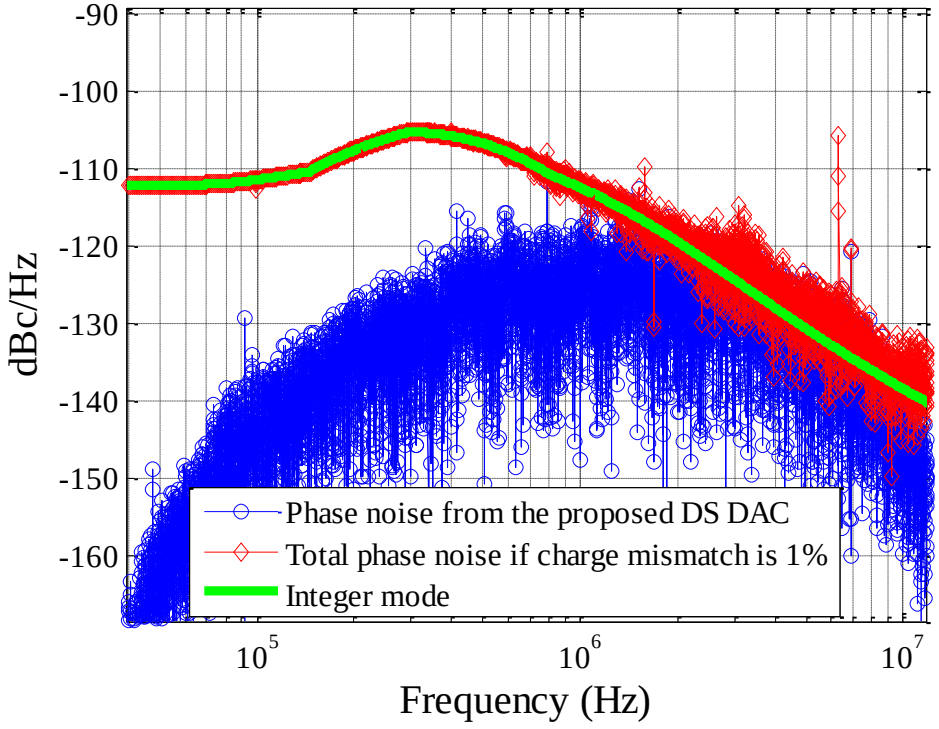


Figure 4.24. Impact of the phase noise of proposed DAC on the PLL phase noise when the error charge mismatch is assumed to be 1%.

Figure 4.23 depicts the impact of the classical segmented DAC on the PLL phase noise when the error charge mismatch is assumed to be 1%. Unfortunately, instead of the attenuated phase noise from the DSM, the phase noise from the segmented DAC dominates the out-of-band phase noise performance and hence deteriorates the integrated phase noise of the whole system. On the contrary, as shown in figure 4.24, the proposed DAC has less influence on the total phase noise even if the same assumption is made as before. As we expect, the phase noise from the proposed DAC almost locates within the available area and hence meet the design specification.

4.5 Frequency dividers

In the RF design, the Current-Mode-Logic (CML) frequency dividers are often used to process the ultra high frequency output of VCO in order to cover the specific frequency bands (see table 1.1). On the other hand, the CML divider is also capable of generating the quadrature signals with 90º phase difference, which is required by the direct conversion transceiver. However, due to the high power dissipation of such CML circuits, some optimizations are needed to be done [37], in order to reduce the power consuming while keeping the correct functionality. In this work, the divide-by-two [38] and divide-by-three [39] frequency dividers will be designed respectively as the former stages for processing the VCO output and generating the I/Q signals. Subsequently, the synchronous divider with retiming circuit will be proposed to reach the targets of proposed phase noise cancelled techniques.

4.5.1 Divide-by-two

The divide-by-two frequency divider is shown in figure 4.25, which is comprised of two CML D-latches (figure 4.25 (b)). The key drawback of this divider is the load resistors (MP1-2) in each unit cell. This is due to the fact that on one side a low load resistor is needed to maintain a small RC constant time in order to guarantee the functional correction. On the other side, the load resistor with high value is required to provide a wide output swing which is capable of driving the other unit cell and reducing the noise sensitivity at the

zero-crossing point. To break up this dilemma, the unit cell with dynamic load resistors was developed [38]. As shown in figure 4.25 (c), the enabled signal CLKb is moved from the gate of current source M6 to the load transistors MP1-2. Thereby, when the unit cell is in the flipping mode (signal CLK is high), MP1-2 are turned on and the related resistors are low, keeping a small RC constant time. When the unit cell come to the latched mode (CLK is low), MP1-2 are turned off and cause high load resistors, which in turn result in a wide output swing. The advantage of the D-latch with dynamic load resistors is that it only consumes current when CLK is high and hence effectively save the power by half.

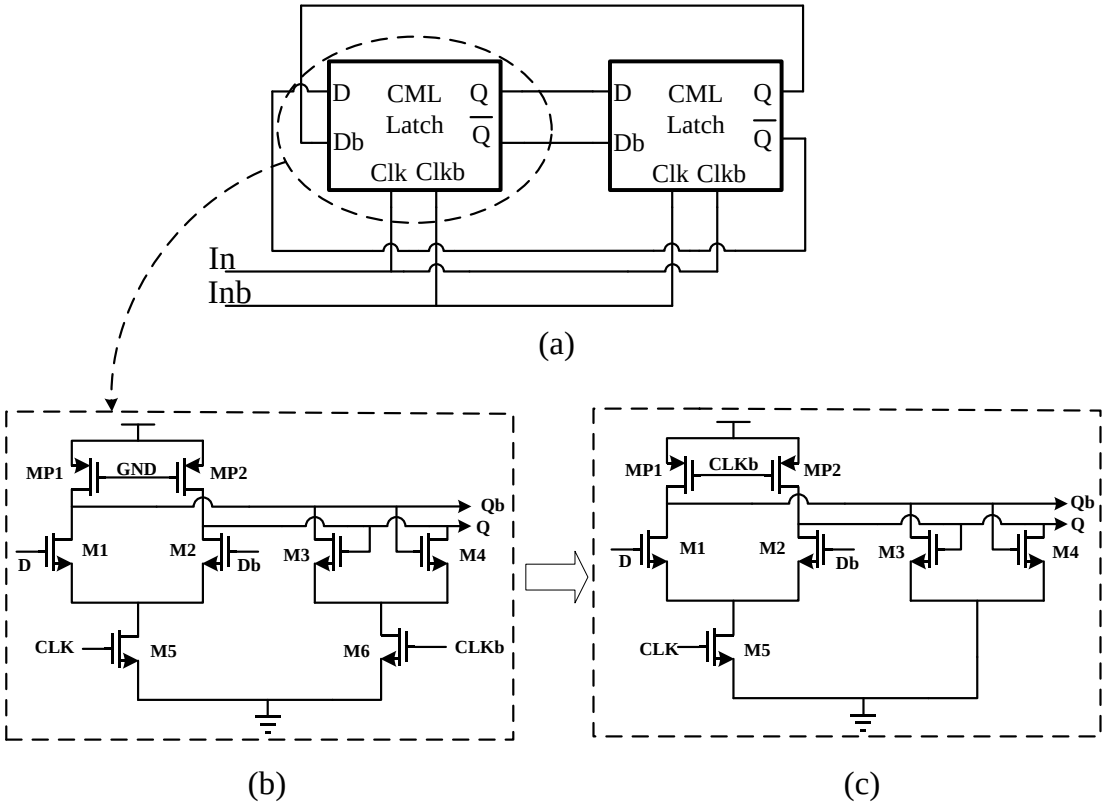


Figure 4.25. Divide-by-two frequency divider: (a). Top architecture; (b). Typical unit cell; (c). Improved unit cell with dynamic loads [38].

Finally, the far-out phase noise at the divider-by-two output should be concerned carefully since the TX-to-RX noise leakage will greatly undermine the noise figure of the whole RX when the phase noise performance of LO at the duplex distance is bad. As analyzed in section 2.3.2, the phase noise at the duplex distance should be better than -160dBc/Hz in order to obtain an acceptable noise figure for the whole RX path. Figure 4.26 depicts the phase noise at the divide-by-two divider output. Obviously, the far-out phase noise at

the required duplex distance (120MHz) is up to -160.2dBc/Hz when the carrier frequency is 2.63GHz and hence meets the design specification for the SAW-less transceiver.

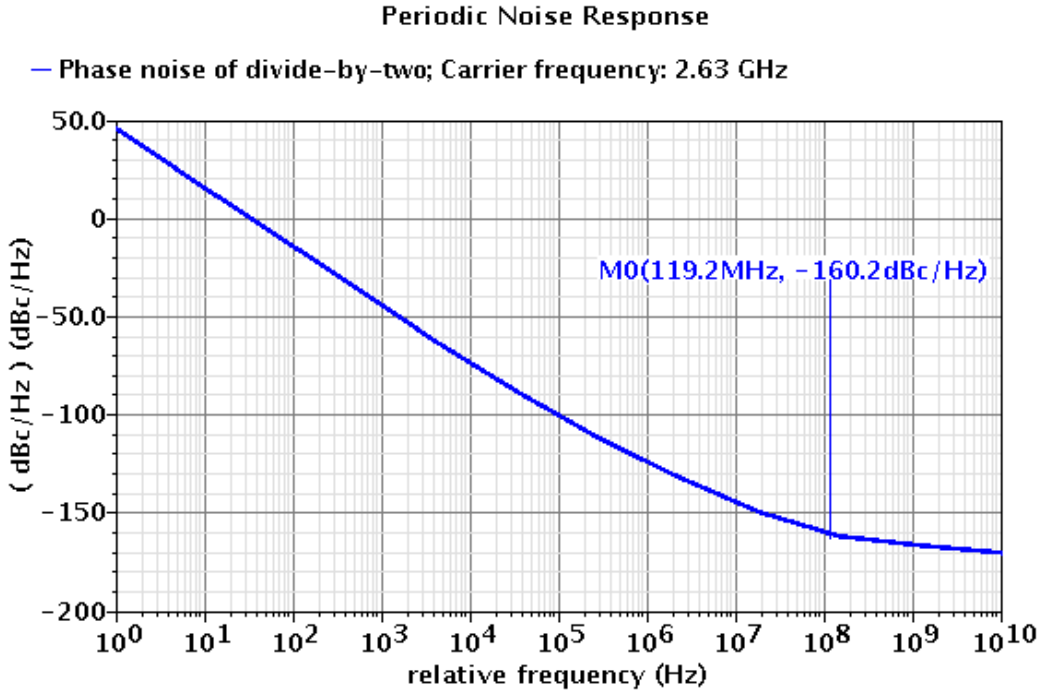


Figure 4.26 Phase noise at the output of divide-by-two frequency divider.

4.5.2 Divide-by-three

The divide-by-three frequency divider is designed in our work. Compared to the divide-by-four divider, the former topology can reduce the tuning range of the LC-tank in the VCO and hence ease the design difficulty of a low-noise, low-power and wide tuning range oscillator. However, the main drawback of the divide-by-three block is that the phase difference between the output signals of each unit cells is not 90º but 60º, which does not meet the phase requirement for I/Q signals in the direct conversion transceiver. Therefore a RC polyphase filter followed by the divide-by-three output is added to generate the quadrature signals. On the other hand, it is also known that if the input signals of polyphase filter contain strong harmonic components, the corresponding I/Q outputs will have effective phase mismatch. To solve this problem, the divide-by-three frequency divider with 50% duty cycle (shown in figure 4.25) is therefore designed [39], in order to suppress the harmonics by simply stage

between the divider and polyphase filter.

As shown in figure 4.27 (a) and (b), instead of the conventional D-latches based topology, the Phase-Switchable-Level-Sensitivity (PSLS) latches are used to construct the divide-by-three divider with 50% duty cycle. One benefit of this topology is that the combination of two outputs of these three PLSL latches can cancel the 3rd harmonics and hence result in a spectrally cleaner signal for subsequent processing (see figure 4.27 (c)). On the other hand, it is also important that the polyphase filter should have low attenuation and high image rejection for the input signals [40].

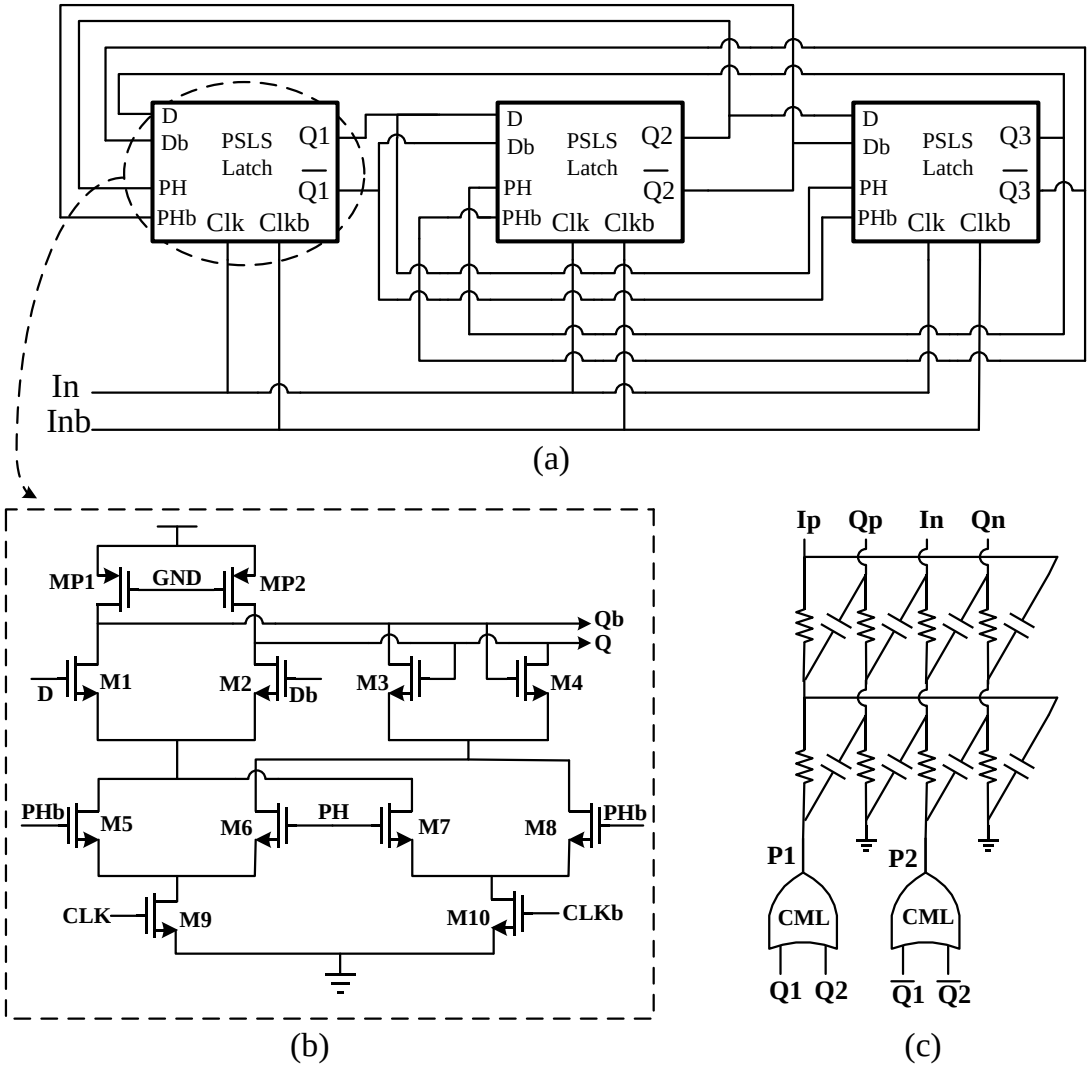


Figure 4.27. Divide-by-three frequency divider with 50% duty cycle [39]: (a). Top architecture; (b).Unit cell; (c). Output with I/Q generation.

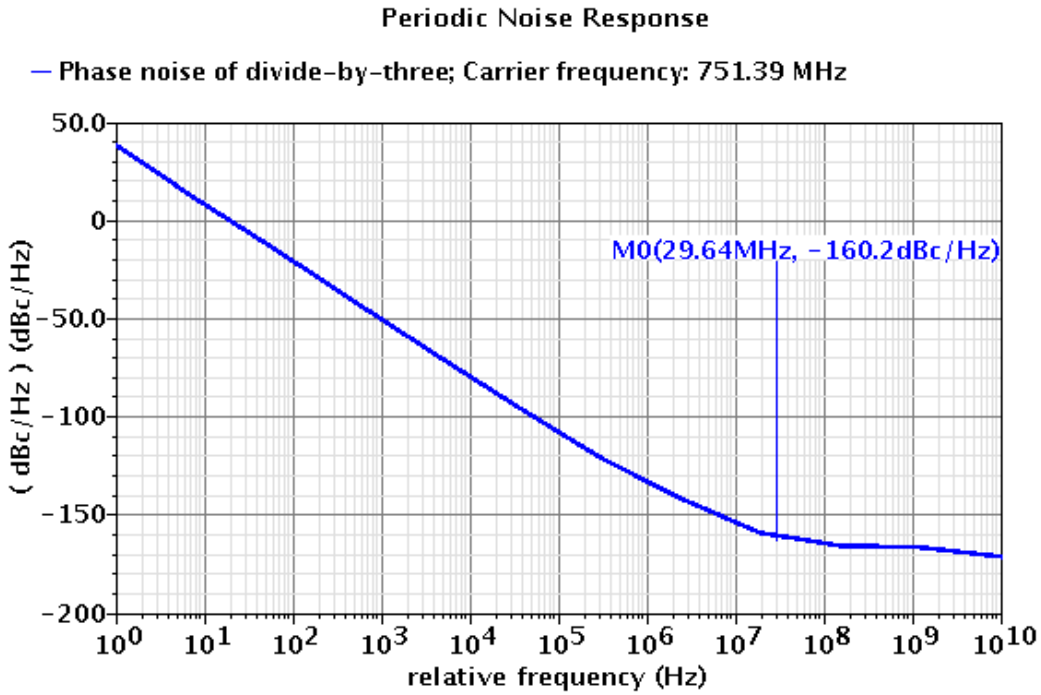


Figure 4.28. Phase noise at the output of divide-by-three frequency divider.

Moreover, similar to the divider-by-two block, the far-out phase noise of proposed divide-by-three divider is up to -160.2dBc/Hz at the duplex distance (30MHz) when the carrier frequency is 751.39MHz, meeting the far-out phase noise requirement for the proposed LO which is used in the SAW-less transceiver architecture.

4.5.3 Synchronous divider with retiming circuit

The proposed synchronous divider shown in figure 4.29 is developed based on the Vaucher's topology [41], which is composed of the divide-by-2/3 cells. The instant dividing ratio (/2 or /3) is individually controlled by the input bits (P0, P1, P2, P3, etc.) which are typically comprised of the fractional sequence (from DSM) and the integer word. On the other hand, similar to the fractional spurious issue in the nonlinear PFD/CP, the delays mismatch (i.e. systematic timing errors) in the multi-modulus divider will result in a spurious tone at $Frac*f_{ref}$, where *Frac* is the fractional ratio provided by DSM. Therefore some flip-flops are used to align the rising edge of the divider output to the rising edge of its input in order to avoid the unpredicted fluctuation of divider output

phase [20]. What's more, the retiming circuit followed by the synchronization flip-flops is used to generate the enabled and clock signals for signal and the noise cancellation paths (see figure 3.10), in order to improve the performance of proposed noise cancellation techniques.

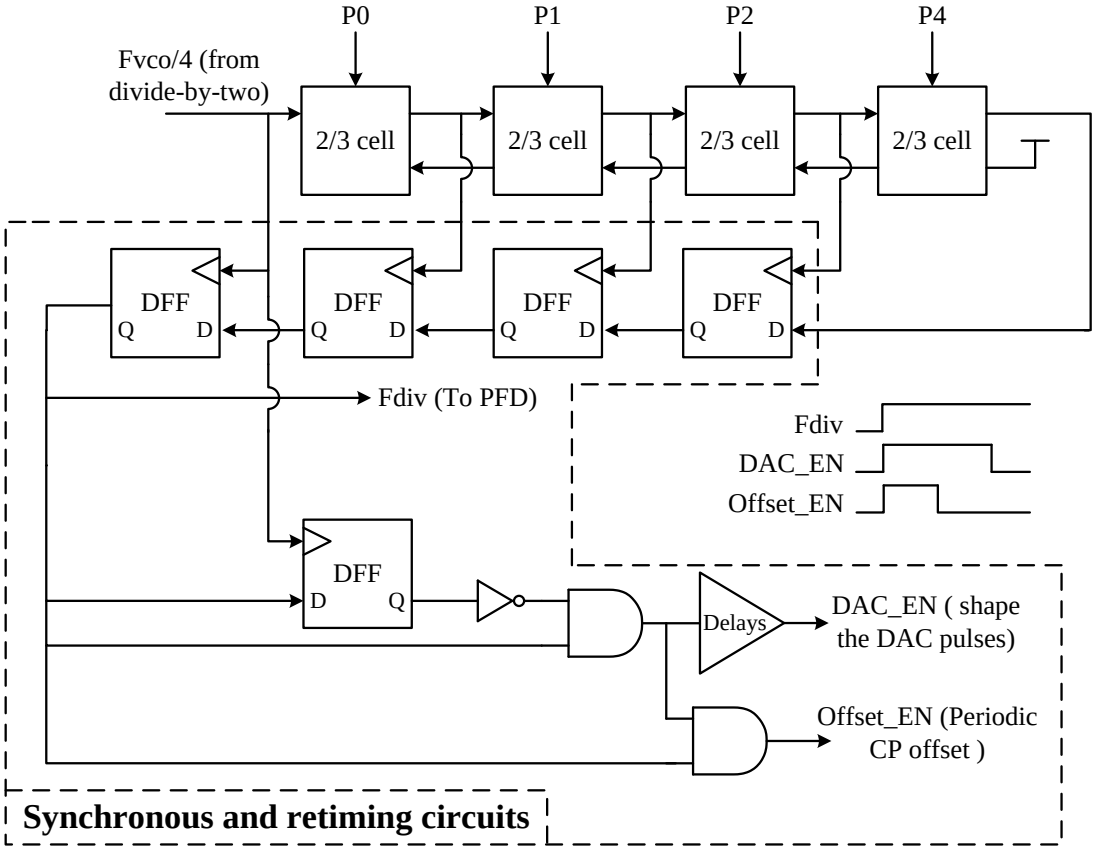


Figure 4.29. Proposed synchronous frequency dividers with retiming circuit.

4.6 Chapter summary

The circuit details and corresponding simulated results in transistor levels are shown in this chapter.

Firstly, the switched biasing VCO topology is adopted in order to reduce the nonlinear conversion of flicker noise from the tail transistors in VCO. Additionally, the digital controlled capacitors array is used to increase the output frequency range of proposed VCO. The high *LQ* product of LC tank is specified for low power design. As a results, a low-noise, low-power and wide tuning range VCO is obtained. Relative performance summary of this VCO can be found in table 4.1.

Secondly, a novel charge pump with complementary switches and additional voltage buffers are designed to overcome the charge sharing and injection problems. The phase noise from the proposed CP is -112.1dBC/Hz at 100 kHz offset.

What's more, a 2^{nd}-order single-loop $\Delta\Sigma$ modulator is used for the fractional-N PLL. Its order is determined by the phase noise contributed by the post modulator in the $\Delta\Sigma$ DAC (see figure 4.22). Subsequently, the details of the modulator architecture, noise splitting DEM and current-steering bank in proposed $\Delta\Sigma$ DAC are illustrated respectively. The comparison between the quantization/phase noises of different modulator architectures are shown to verify the effective reduction of quantization/phase noise by the proposed $\Delta\Sigma$ DAC. The transistor-level simulated result for the phase noise of proposed $\Delta\Sigma$ DAC ensures that it has less impact on the phase noise of PLL output even though the charge mismatch between the signal and noise cancellation path is only 1%.

Further, the divide-by-two with periodic biasing loads and divide-by-three with 50% duty cycles are designed as the I/Q generator. The corresponding simulated results for their far-out phase noise are also attached, which meet the phase noise requirement at the duplex distances. Finally, the synchronous divider with retiming circuit is proposed.

In the end, the simulated results for the current consumption of each block are summarized in table 4.2.

Proposed blocks		Current consumption (mA)
PLL Core	VCO	1.42
	PFD/CP	3.95
	Buffers + Dividers	4.41
	DSM + LFSR	0.60
	ΔΣ DAC	3.60
	Total	14
I/Q Generator	Divide-by-Two	1.37
	Divide-by-three	3.84
	Buffers	1.75
	Total	6.96

Table 4.2. Current consumption of proposed system from a 1V supply.

CHAPTER 5

5 Conclusion and future work

5.1 Conclusion

In this thesis, a frequency synthesizer for LTE FDD/TDD is designed based on the wide BW $\Delta\Sigma$ fractional-N PLL using phase noise cancellation techniques. The feature of LTE standard determines that the relative synthesizer should have fast settling time, fine frequency resolution, wide output range and good phase noise performance. The addition of the phase noise cancellation path in the classical $\Delta\Sigma$ fractional-N PLL can break up the designed trade-off between these above specifications. As we know, the purpose of the proposed noise cancellation technique is to eliminate the error charges converted by the quantization error included in the DSM output. Hence, the BW limitation due to the quantization noise of DSM can be greatly relaxed and fast settling time of PLL can be obtained.

However, in the practical design, the output mismatch, nonlinear distortions and additive noise in the signal and noise cancellation path will limit the effect of these phase noise cancellation techniques. Therefore, the corresponding solutions for improving these adopted techniques are developed and examined by both the behavioral and transistor-level simulated results. Firstly, to overcome the recovered charges mismatch between the signal and noise cancellation path, the retiming circuit are designed to increase the overlapped region between the CP and DAC current outputs. Secondly, the offset pulses from the retiming circuits can move the CP into a more linear operation region and hence avoid the noise folding issue in the CP of traditional

$\Delta\Sigma$ fractional-N PLL. Finally, a novel hybrid $\Delta\Sigma$ DAC with 9 equivalent output bits is creatively designed in order to decrease the requantization noise of proposed DAC, which will contribute to the phase noise at the PLL output.

The current consumption of proposed PLL core is around 14mA. While the I/Q generators consumes 6.96 mA approximately. The whole system is powered by a 1 V supply.

5.2 Future work

5.2.1. Spurious issue

The spurious issue including both reference and fractional spurs is very important in the fractional-N PLL design and hence is necessary to be investigated in the future. The reason for the reference spur is the currents mismatch in the nonlinear charge pump, which will leave some fixed residual charges to disturb the VCO in each periodic period and cause the spurious tones located at multiples of f_{ref} from f_{VCO}. In the practical design, such reference spurious tones can be effectively attenuated by using the PFD/CP linearization technique (introduced in section 3.4.2) and choosing the f_{ref} to be far away from the PLL bandwidth. Alternatively, the sample-and-hold operation embedded into the loop filter can be realized to reduce the fixed disturbance from the nonlinear CP to VCO in each reference periods and hence attenuate the reference spurs at the synthesizer output [9], [42].

On the other hand, compared to the reference spur, the fractional spur could be the main enemy in the fractional-N PLL. There are two distinct mechanisms giving rise to the fractional spurs. One is the nonlinear parasitic coupling path between the VCO output and the harmonics of the reference signal, the other is the sensitivity of DSM's output spectrum to the subsequent nonlinear circuitries (i.e. multi-modulus divider, PFD/CP, etc.).

In the first mechanism, it is well known that the harmonics of reference signal will be coupled to the VCO output via the nonlinear parasitic coupling path. In

particularly, such phenomenon will become more effective in the PFD and CP. The is due to the fact that the local power supply will be disturbed by the hard-switching activities within these blocks because of the bond wire inductance, resulting in an undesired modulation for the threshold voltage of relative digital switches. Similar to the reference spurious issue, the first mechanism arising from fractional spurs can be properly alleviated by providing offset current at the CP output because the additional fixed phase offset stemmed from the offset current in each reference period can ensure that the disturbances of the local power supply, which is due to the hard-switching of digital gates, have enough time to die out before modulating the delays and hence corrupting the phase difference measurement [7], [42].

Moreover, the digital DSM in the fractional-N PLL is regarded as the main contributor to the fractional spurs even if efficient dither has been applied to avoid the spurious tones at its output spectrum. This is due to the fact that the output of $\Delta\Sigma$ modulator is sensitive to the nonlinear distortions. Particularly in the $\Delta\Sigma$ fractional-N PLL, the output sequence of DSM will be converted to the analog pulse via the signal path (see figure 3.4) which is composed of some non-ideal blocks (multi-modulus divider, CP, etc.), hence leading to the fractional spurious issue. Unlike the first mechanism, the inherent sensitivity of nonlinear distortions for the DSM output requires very high linear subsequent circuits in the fractional-N PLL in order to reduce the fractional spurious level. Otherwise the sophisticated modulator topology [42], [43] or the addition of offset input to the DSM [44] can be alternatively utilized to alleviate the fractional spurious level. Therefore, how to increase the immunity of DSM output to the nonlinear distortion while keeping acceptable system complexity is necessary to be included in the future work.

5.2.2 Further suppression for quantization noise

As analyzed before, even though the signal and noise cancellation paths are assumed to be ideal, the performance of proposed noise cancelled technique is still subjected to the mismatch between these two paths. Hence the residual error charges caused by the quantization noise of DSM will be left to some extent after enabling the noise cancellation path, resulting in an imperfect

phase noise cancellation at the output spectrum of PLL.

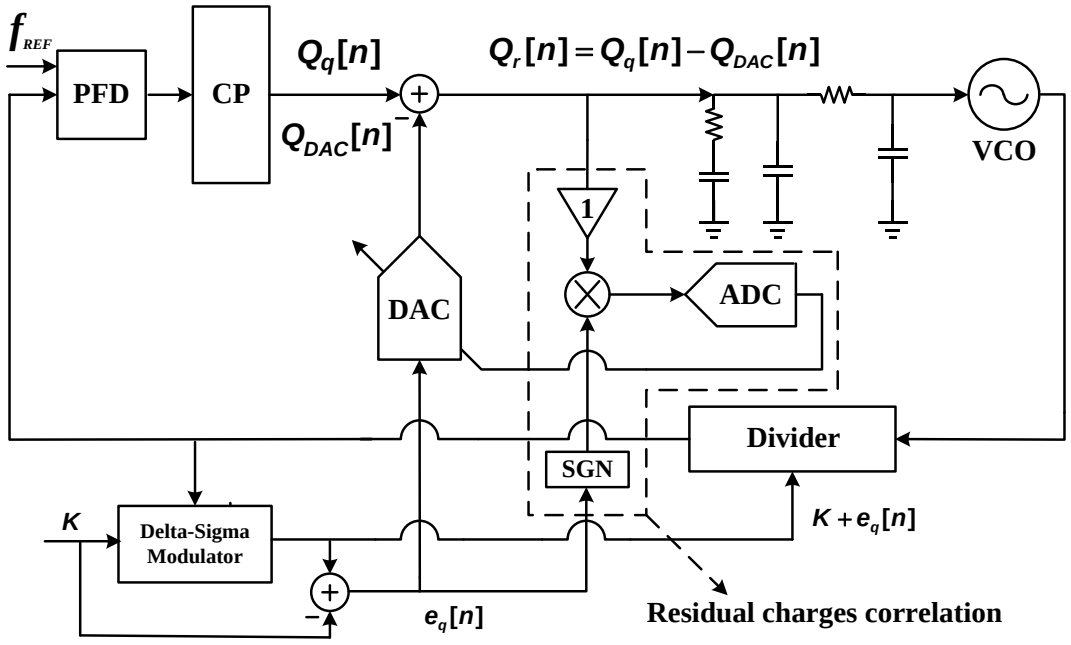


Figure 5.1. Adaptive phase noise cancellation technique.

As shown in figure 5.1, the adaptive phase noise cancellation technique for the $\Delta\Sigma$ fractional-N PLL, which was presented in [44] originally and developed in [11], can be used to further reduce the phase noise caused by $Q_r[n]$. The adaptive calibrated loop inserted between the noise cancellation path and loop filter converts $Q_r[n]$ to corresponding digital pulses which will dynamically adjust the output gain levels of proposed CS-DACs to the CP output. Hence, by supplementing this adaptive calibrated loop to the proposed PLL, $Q_r[n]$ will be minimized and the performance of the phase noise cancellation technique can be effectively improved.

5.2.3. Intrinsic noise

Since the quantization noise from the DSM is suppressed effectively when it enters into the PLL, the intrinsic noise will again become the mainly concerned area for the future research.

At the first, if we suppose the effect of the quantization noise on the PLL phase noise is negligible, the out-of-band phase noise at the PLL output will be dominated by the VCO. Hence the VCO noise performance will determine the possible noise improvement of PLL to a large extent. On the other hand, the in-band phase noise of PLL will be mainly contributed by the charge pump. In particularly, by reviewing equations (4.6) and (4.7) (shown as follows), we can find that the intrinsic noise of CP will be amplified by square of the dividing ratio *N*. Such amplification will greatly limit the further improvement of in-band phase noise at the PLL output, especially in the design of the PLL with large dividing ratio. For instant, the dividing ratio in our case can be up to 112, which will lead to a 41 dB increment of in-band phase noise for the proposed PLL

$$S_{PLL|CP}(2\pi f) = S_{CP} \times \left| \frac{A(2\pi f)}{1 + A(2\pi f)} \right|^2 \tag{4.6}$$

$$S_{CP} = \overline{i_n}^2 \left(\frac{2\pi N}{I_{CP}}\right)^2 \tag{4.7}$$

In order to remove *N* from equation (4.7), a new PLL topology is needed to be developed. The sub-sampling PLL presented in [46] introduces a novel solution to avoid the influence of *N* on the PLL phase noise. However, this topology is only suitable for the integer-N PLL and hence could not be applied for the frequency synthesis in wireless communication. Based on the sub-sampling PLL, the improved topology which is capable of providing finer frequency resolution can therefore be investigated in the future research.

References

[1] 3GPP TS 36.101 version 8.5.1 Release 8, Apr. 2009

[2] T. A. D. Riley, M. A. Copeland and T. A. Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis." in *IEEE J. of Solid-State Circuits*, Vol. 28, pp. 552-559, May, 1993

[3] C.-H. Heng and B.-S. Song, "A 1.8-GHz CMOS fractional-N frequency synthesizer with randomized multiphase VCO," in *IEEE J. of Solid-State Circuits*, vol. 38, no. 6, pp. 848-854, Jun. 2003.

[4] Miletic and R. Mason, "Quantization noise reduction using multiphase PLLs," in *Proc. Of ISCAS06*, pp. 4078-4081, May, 2006.

[5] T. A. D. Riley, N. Filol, Q. Du, and J. Kostamovaara, "Techniques for in-band phase noise reduction in $\Delta\Sigma$ synthesizers," *IEEE Trans. Circuits Syst. II*. vol. 50, pp. 794-803. Nov. 2003.

[6] X. Yu, Y. Sun, L. Zhang, W. Rhee, and Z. Wang, "A 1 GHz fractional-N PLL clock generator with low-OSR $\Delta\sum$ modulation and embedded FIR noise filtering," in *IEEE ISSCC Dig. Tech. Papers*, pp. 346–347, 2008.

[7] E.Temporiti, G. Albasini, I. Bietti, R. Castello, and M.Colombo, "A 700 kHz bandwidth $\Delta\Sigma$ fractional synthesizer with spurs compensation and linearization technique for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sep. 2004.

[8] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4 GHz delta-sigma fractional-N PLL with 1 Mb/s in-loop modulation," *IEEE J. Solid State Circuits*, submitted for publication. vol. 39, no. 1, pp. 49–62, Jan. 2004.

[9] S. E. Meninger and M.H. Perrott, "A 1-MHz bandwidth 3.6 GHz 0.18-um CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 966–980, Apr. 2006.

[10] M. H. Perrott, M. D. Trott, and C. G. Sodini, “A modeling approach for D-S fractional-N frequency synthesizers allowing straightforward noise analysis,” *IEEE J. Solid State Circuits*, vol. 37, pp. 1028–1038, Aug. 2002.

[11] A. Swaminathan, K. Wang, and I. Galton, “A wide-bandwidth 2.4 GHz ISM-band fractional-N PLL with adaptive phase-noise cancellation,” *IEEE J. Solid-State Circuits*, pp. 2639–2650, Dec. 2007.

[12] T.-H. Lin, C.-L. Ti and Y.-H. Liu, “Dynamic current-matching charge pump and gated-offset linearization technique for delta-sigma fractional-N PLLs” *IEEE Trans. Circuits Syst I.*Vol. 56, pp. 877 – 885. Feb. 2009.

[13] H. M. Chien, T. H. Lin, B. Ibrahim, L. Zhang, M. Rofougaran, A. Rofougaran, and W. J. Kaiser, “A 4 GHz fractional-N synthesizer for IEEE 802.11a,” in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2004, pp. 46–49.

[14] R. Schreier and G. C. Tees, “Understanding Delta-Sigma Data Converters,” Wiley-IEEE Press, Nov. 2004.

[15] S. Pamarti and I. Galton, “Phase-noise cancellation design tradeoffs in delta-sigma fractional-N PLLs,” *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 829–838, Nov. 2003.

[16] R. Adams and K. Q. Nguyen, “A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling,” *IEEE J. Solid-State Circuits*, vol.33, pp. 1871–1878, Dec. 1998.

[17] K. Nguyen, A. Bandyopadhyay, R. Adams, K. Sweetland, and P. Baginski, “A 108dB SNR, 1.1mW Oversampling Audio DAC with A Three-level DEM Technique,” *IEEE J. Solid-State Circuits*, vol. 42, no.12, pp. 2592-2600, Dec. 2008.

[18] R. Hezar, L. Risbo, H. Kiper, M. Fares, B. Haroun, G. Burra, and G. Gomez “A 110dB SNR and 0.5mW Current-Steering Audio DAC Implemented in 45nm CMOS,” *ISSCC Dig. Tech. Papers*, pp 304-305, Feb. 2010.

[19] I. Galton, “Why Dynamic Element Matching DACs Works,” *IEEE Trans. Circuits Syst. II: Express Briefs*, vol.57, no.2, pp.69-74, Feb. 2010.

[20] W. Rhee, B.-S. Song, and A. Ali, "A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-bit third-order ΔΣ modulator," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1453–1460, Aug. 2000.

[21] L. Risbo, R. Hezar, B. Kelleci, H. Kiper and M. Fares, "Digital Approaches to ISI-Mitigation in High-Resolution Oversampled Multi-Level D/A Converters," *IEEE J. Solid-State Circuits,* vol.46, no.12, Dec. 2011.

[22] I. Galton, "One-bit dithering in delta–sigma modulator-based D/A conversion," in *Proc. IEEE Int. Symp. on Circuits Syst.*, 1993, pp. 1310–1313.

[23] K. K. Lee, C. Bryant, M. Törmänen, H. Sjöland, "Design and analysis of an ultra-low-power LC quadrature VCO," Analog Integrated Circuits and Signal Processing, 2010.

[24] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential *LC* oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 717–724, May 1999.

[25] C. Samori, A. L. Lacaita, F. Villa, and F. Zappa, "Spectrum folding and phase noise in *LC* tuned oscillators," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 781–790, July 1998.

[26] C. Samori, A. L. Lacaita, A. Zanchi, S. Levantino, and F. Torrisi, "Impact of indirect stability on phase noise performance of fully-integrated *LC* tuned VCOs," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC) 1999*, Sept. 1999, pp. 202–205.

[27] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential *LC* oscillators," in *Proc. IEEE Custom Integrated Circuits Conf.*, Orlando, FL, 2000, pp. 569–572.

[28] E. Hegazi, H. Sjöland, and A. Abidi, "A filtering technique to lower oscillator phase noise," in *Proc. ISSCC 2001*, Feb. 2001, pp. 364–365.

[29] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van derWel, and B. Nauta, "Reducing MOSFET *1/f* noise and power consumption by switch biasing," *IEEE J. Solid-State Circuits*, vol. 35, pp. 994–1001, July 2000.

[30] C. C. Boon, M. A. Do, K. S. Yeo, J. G. Ma, and X. L. Zhang, "RF CMOS low-phase-noise LC oscillator through memory reduction tail transistor," *IEEE Trans. Circuits Syst. II*, vol. 51, no. 2, pp. 85–90, Feb.

2004.

[31] See Taur Lee, Sher Jiun Fang, David J. Allstot,, Abdellatif Bellaouar, Ahmed R. Fridi, and Paul A. Fontaine, "A quad-band GSM-GPRS transmitter with digital auto-calibration," *IEEE, J. Solid-State Circuits*, vol.39, no.12, pp.2200-2214, Dec. 2004,

[32] W. Rhee, "Design of high-performance CMOS charge pumps in phase locked loops," in *Proc. Int. Symp. on Circuits and Systems*, vol. 2, May 1999, pp. 545–548.

[33] C. Charles and D. Allstot, "A Buffered Charge Pump with Zero Charge Sharing," in *Proc. Int. Symp. Circuits Syst.*, Seattle, WA, May 2008, pp. 2633–2636.

[34] B. D. Muer and M. Steyaert, "CMOS Fractional-N Synthesizers: Design for High Spectral Purity and Monolithic Integration," New York: Springer, 2003.

[35] R. Schreier, The Delta Sigma Toolbox Version 7.0. Oct. 2004.

[36] R. W. Adams, "Design and Implementation of an Audio 18-bit Analog-to-Digital Converter using Oversampling Techniques," *J. Audio Engineering Society*, vol. 34, no. 3, pp. 153–166, March 1986.

[37] R. Nonis, E. Palumbo, P. Palestri and L. Selmi, "A Design Methodology for MOS Current-Mode Logic Frequency Dividers," *IEEE Trans. Circuits Syst I.* vol. 54, no. 2, pp. 245-254, Feb. 2007.

[38] H. Wang, "A 1.8V 3mW 16.8GHz Frequency Divider in 0.25 μm CMOS," *ISSCC Dig. Tech. Papers*, pp 196-197, Feb. 2000.

[39] R. Magoon, A. Molnar, J. Zachan, G. Hatcher and W. Rhee, "A Single Chip Quad-Band (850/900/1800/1900MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer," *IEEE, J. of Solid-State Circuits*, vol. 37, pp. 1710-1720, May 2002.

[40] F. Behbahani, Y. Kishigami, J. Leete and A.A. Abidi, "CMOS Mixers and Polyphase Filters for Large Image Rejection," *IEEE, J. of Solid-State Circuits*, vol. 36, no.6, pp. 873-887, Jun. 2001.

[41] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli and Z. Wang, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35μm CMOS Technology," *IEEE, J. of Solid-State*

Circuits, vol. 35, no. 7, pp. 1039-1045, Jul. 2000.

[42] K. Wang, A. Swaminathan and I. Galton, "Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz fractional-N PLL," *IEEE, J. of Solid-State Circuits*, vol.43, no. 12, pp. 2787-2797, Dec. 2008.

[43] A. Swaminathan, A. Panigada, E. Marry, and I. Galton, "A Digital Requantizer wit Shaped requantization noise that remains well behaved after non-linear distortion," *IEEE, Trans. Signal Process.*, vol. 55, no. 11, pp. 5382-5394, Nov. 2007.

[44] H.-Y. Jian, Z. Xu, Y.-C. Wu and M.-C. F. Chang, "A Fractional-N PLL for Multiband (0.8 - 6 GHz) Communications Using Binary-Weighted D/A Differentiator and Offset-Frequency $\Delta-\Sigma$ Modulator," *IEEE, J. of Solid-State Circuits*, vol. 45, no. 4, pp. 768-780, Apr. 2010.

[45] M. Gupta and B. S. Song, "A 1.8 GHz spur cancelled fractional-N Frequency Synthesizer with LMS based DAC gain calibration," *IEEE, J. of Solid-State Circuits*, vol. 41, no. 12, pp. 2842–2851, Dec. 2006.

[46] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N^2," *IEEE, J. of Solid-State Circuits*, vol. 44, no. 12, pp. 3253-3263, Dec. 2009.