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Master's Thesis

Two 500M-8GHz Wideband Balun-LNA-I/Q-Mixers

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ABSTRACT

Two wideband balun-LNA configurations have been designed in 65nm COMS technology. Both of them employ a single-to-differential (S-to-D) conversion topology composed of a common gate (CG) stage and a common source (CS) stage, providing output balancing and noise and distortion cancelling. One is inductorless and the other one exploits gain-boosting current-balancing topology. With 2.5V and 2.5V/1.8V supply the LNAs achieve voltage gains of 24.5dB and 22.8dB, noise figures of below or close to 3dB, input second-order intercept points (IIP2) of 31dB and 41.8dB, respectively. In addition, the sensitivity of IIP2 is deeply investigated.

Balun-LNA I/Q-mixers, which combine the balun-LNA cores and double-balanced mixers, are also designed in the same CMOS technology to resolve the bandwidth limitation in traditional direct-conversion receivers. With 2.5V supply, around 20dB conversion gain, 3dB DSB noise figure, 18.3dB IIP2 and -3dB IIP3 are obtained by the BLIXER using LNA.A over the bandwidth of 0.5 to 8GHz, while consuming 29mW DC power. The counterpart, the BLIXER using LNA.B, achieves around 20dB conversion gain, 4dB DSB noise figure, 38dB IIP2 and 2.8dB IIP3 over the same bandwidth while dissipating 15mW from 2.5/1.8V supplies.

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1

INTRODUCTION

In recent years, RF receiver designers made efforts on replacing analogue components with digital ones, striving towards the ideal software defined radio (SDR) where all signal processing is done in software. Such an ideal SDR platform may form an exceptionally flexible and reprogrammable receiver that can cope with many different standards, e.g., IS-95, GSM, UTMS, LTE and especially the various military standards. A software defined radio can also avoid the "limited spectrum" assumptions of previous kinds of radios by using spread spectrum and ultra-wideband techniques, which allow several transmitters to transmit in the

same place on the same frequency with very little interference, typically combined with one or more error detection and correction techniques to fix all the errors caused by that interference. Consequently, the demand of (ultra) wideband integrated RF building blocks with high performance has driven the market and research to explore an area of wideband CMOS RFIC designs for applications in a RF front-end transceiver.

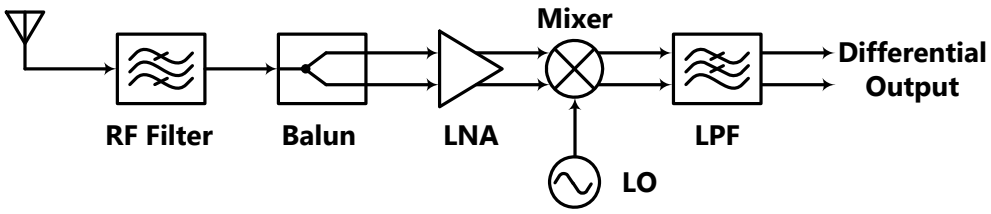

Figure 1.1 Block diagram of a RF receiver

Figure 1.1 shows a conventional direct conversion receiver front-end architecture. To take the advantages of differential LNA design, e.g. even order harmonic distortion rejection, a balun is commonly used to convert the single-end input signal from the antenna to a pair of balanced signal fed to the LNA. The balun is usually implemented on the PCB due to its large form factor. Therefore, proper impedance transformation and matching networks are often needed on the PCB, too, resulting in increased complexity and cost of the PCB. On the other hand, if the balun is implemented on chip, it consumes a lot of area which is very expensive in today's IC process. The evolution of circuitry provides the possibility to remove the balun, simultaneously keeping the single-end to differential conversion. This kind of circuit is the so-called Balun-LNA.

1.1 Project Overview

Two wideband balun-LNA configurations have been designed in STMicroelectronics 65nm COMS technology. Both of them employ a single-end-to-differential (S-to-D) conversion topology composed of a common gate (CG) stage and a common source (CS) stage, providing output balancing and noise and distortion cancelling. One uses g_m-scaling

technique and the other one exploits gain-boosting current-balancing topology. With 2.5V and 2.5V/1.8V supplies the LNAs achieve voltage gains of 24.5dB and 22.8dB, noise figures of below or close to 3dB, input second-order intercept points (IIP2) of 31dB and 41.8dB, respectively. In addition, the sensitivity of IIP2 is deeply investigated with Monte-Carlo analyses.

Then Balun-LNA I/Q-mixers, which combine the balun-LNA cores and double-balanced mixers, are also designed in the same CMOS technology to resolve the bandwidth limitation in traditional direct-conversion receivers. With 2.5V supply, around 20dB conversion gain, 3dB DSB noise figure, 18.3dB IIP2 and -3dB IIP3 are obtained by the BLIXER using LNA.A over the bandwidth of 0.5 to 8GHz, while consuming 29mW DC power. The counterpart, the BLIXER using LNA.B, achieves around 20dB conversion gain, 4dB DSB noise figure, 38dB IIP2 and 2.8dB IIP3 over the same bandwidth while dissipating 15mW from 2.5/1.8V supplies.

1.2 Thesis Organization

In this thesis report only the key points of the work are presented. The repetitive work and theories could be found in [4]. The thesis is structured as follows. Chapter 2 covers the main concepts and theories of RF receivers and circuits. The circuits of balun-LNAs designed in this work are introduced in Chapter 3. Chapter 4 describes the topology and implementations of the BLIXER. In Chapter 5, simulation results are given followed by discussions. The conclusion is drawn in Chapter 6.

2

THEORY FOR RF RECEIVERS

A RF receiver accurately extracts and selectively detects a desired signal in the presence of noise and interferers that are often several times than the desired signal. This is done through several operations, such as amplifying, filtering, demodulation, and analogue-to-digital conversion, with adequate signal-to-noise ratio (SNR) before digital signal processing. The received RF signal can be strong or extremely weak, while there can be a strong blocking signal(s) with a certain offset from the wanted frequency, which needs to be rejected. These translate into

requirements in terms of sensitivity, noise figure, dynamic range, and intermodulation performance.

In a radio receiver circuit, the RF front-end is a generic term for all the circuitry between the antenna and the first intermediate frequency (IF) stage. It consists of all the components in the receiver that process the signal at the original incoming radio frequency (RF), before it is converted to a lower intermediate frequency.

In this chapter, the fundamentals of receivers are reviewed including architectures and parameters of performance. In addition, blocks which consist of RF front-ends are also briefly introduced.

2.1 Receiver Architecture

Traditional Superheterodyne receivers were the most widely used receiver architecture because of its excellent sensitivity and selectivity. However, the direct translation of the RF spectrum to the baseband eliminates the need of the expensive and bulky off-chip components, and allows the channel selection filtering to be performed by a simple on-chip low-pass filter. Specifically, the direct conversion takes advantage from the zero intermediate frequency (IF) since a zero IF implies that the image of the desired signal is itself. Compared with Superheterodyne architecture, therefore, there is no need for image rejection filters and thus circuits become easy to implement. Furthermore, it is possible to process subsequent signals at very low frequency with a zero IF. In addition, the flexibility inherent in digital approaches opens the possibility for a ‘universal’ receiver, one that can accommodate many different standards with one piece of hardware [3]. Therefore, direct-conversion approach can provide highly integrated, low-cost, and low-power solutions for wireless products, and has become the most actively explored architecture of receivers. In this work the direct conversion receiver topology is used.

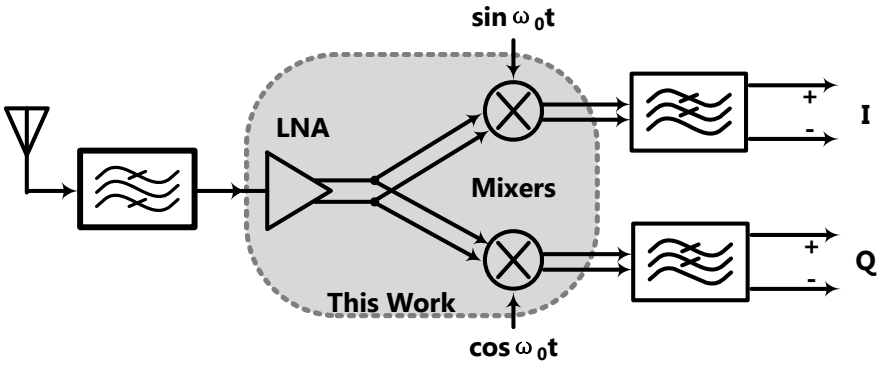

Figure 2.1 Block diagram of a Direct Conversion Receiver

A simple block diagram of homodyne (direct conversion) receivers is shown in Figure 2.1. The single-end signal received by the antenna is fed to the band-pass filter for band selection. Usually, there should be a balun [5] made of coils, which converts the single-end signal to differential, before the differential LNA. In this design, however, we use a topology of wideband balun-LNA with simultaneous output balancing, noise-cancelling and distortion-cancelling but without coils instead. The low noise amplifier amplifies the signal, also suppressing the noise contributed by the following stages along the signal path.

Then the differential signal is down-converted to the baseband by mixing with 0/90˚ phase shifted local oscillator frequencies to get a correct demodulated signal. Specifically, if the phases of RF and LO signal are coincident or anti-coincident, the demodulated signal at maximum strength is obtained; if the phases are quadrature, the demodulated signal is zero., Two mixers where quadrature LO signals are applied, therefore, are needed in order to provide arbitrary phase relationships between RF and LO signals. By combining the two outputs (I and Q), it is possible to obtain demodulated signal with arbitrary input phase.

2.2 Basic Receiver Performance Matrices

2.2.1 Receiver Sensitivity

Receiver sensitivity is the minimum signal strength ($P_{in,min}$) that a receiver is able to detect, and maintain a target bit-error-rate (BER).

$$P_{in,min}(dBm) = 10\,log(KT_0) + 10\,log(B) + NF_{rx} + SNR_{min}, \quad (2.1)$$

where K is the Boltzmann constant; T_0 is the temperature in Kelvin; B is the desired signal bandwidth; NF_{rx} is the total receiver noise figure and SNR_{min} is the minimum required signal to noise ratio. Since the SNR_{min} is determined by modems, codec schemes and target data rates, it is apparent that the noise figure becomes a significant item when evaluating the sensitivity.

2.2.2 Noise Figure

Noise Figure indicates the noise deterioration of a block. It is defined as the ratio of input signal-to-noise ratio (SNR_{in}) to output signal-to-noise ratio (SNR_{out}).

$$NF(dB) = 10\log(NR) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right), \quad (2.2)$$

where NF and NR stand for Noise Figure and Noise Ratio, respectively.

According to the Friis' Formula, the noise figure of a receiver can be approximately expressed as

$$NR_{Receiver} = NR_{LNA} + \frac{(NR_{Rest}-1)}{Gain_{LNA}}, \quad (2.3)$$

where NR_{Rest} is the overall noise factor of the subsequent stages of the LNA. From the equation 2.3, it is obvious that the overall noise figure of a receiver is primarily established by the noise figure of its first amplifying stage. Subsequent stages have a diminishing effect on signal-to-noise ratio.

For this reason, the first stage amplifier in a receiver is often called the low-noise amplifier (LNA). The overall noise figure is dominated by the noise figure of the LNA, if the gain is sufficiently high.

2.2.3 Harmonics and Intermodulation Distortions

A nonlinear system can be approximated by a polynomial.

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \cdots, \qquad (2.4)$$

where x denotes the input signal and y represents the output signal. Normally, the terms for higher orders diminish, as systems are only weakly nonlinear. So equation 2.4 can be truncated after the third-order term. Now consider that a single sinusoid $x = A\,sin(2\pi ft)$ is applied to the weakly nonlinear system as described in equation 2.4, the output is

$$\mathrm{y} \approx a_0 + a_1 A \sin(2\pi ft) + \frac{a_2 A^2}{2}\sin(4\pi ft) + \frac{a_3 A^3}{4}\sin(6\pi ft), \qquad (2.5)$$

This expression shows the harmonics distortions appear at the multiple of the fundamental frequency, as shown in Figure 2.2. Harmonic distortions can be reduced by filtering the output signal.

Another problem that is needed to consider is the intermodulation distortion (IMD). If there is a second received signal, whose frequency (f_1) is close to the frequency of interest (f_2), significant frequency components at $f_2 \pm f_1$ (2^{nd} –order IM) and $2f_2 \pm f_1$ (3^{rd} –order IM), and their images are produced by the nonlinear system, as shown in Figure 2.2.

If we see the diagram of input and output power, as shown in Figure 2.3, the fundamental frequency has a slope of one, the 2^{nd} –order and 3^{rd} –order intermodulation frequencies have slopes of two and three. In real systems, the curves saturate before intersection due to losses and nonlinearity in the systems. The extrapolated intersections of linear parts, however, are used as important parameters to measure the linearity of the system. The definitions of 2^{nd} –order input intercept point (IIP2), 2^{nd} –order output

intercept point (OIP2), 3rd –order input intercept point (IIP3) and 3rd –order output intercept point (OIP3) are summarized in Figure 2.3.

The IMDs are not easy to be filtered as the created IM frequencies could be very close to the desired signal, e.g. the 3rd-order IM shown in Figure 2.2. Furthermore, in a direct conversion receiver the 2nd-order IM also becomes problematical due to the feedthrough of mixers, which will be discussed later.

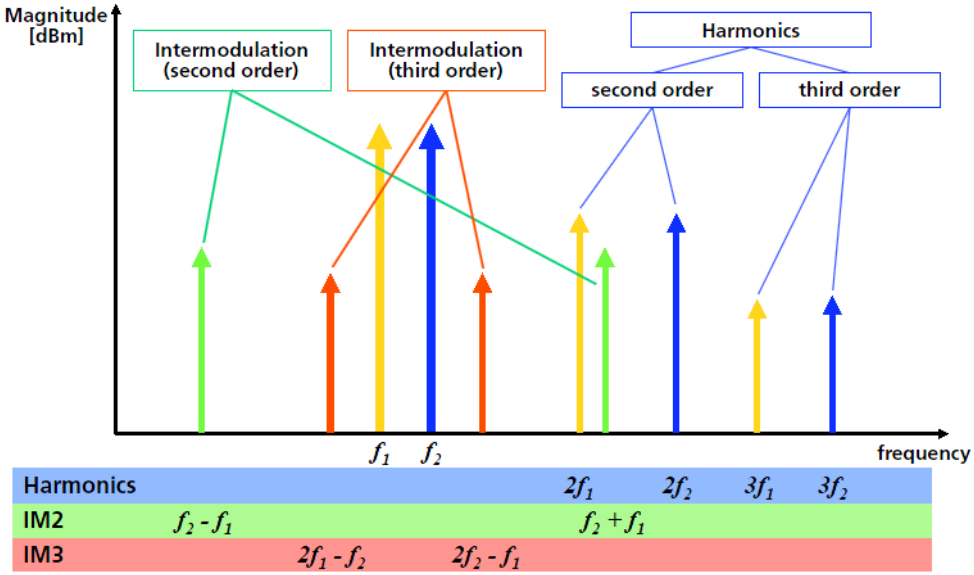

Figure 2.2 Harmonics and Intermodulation [1]

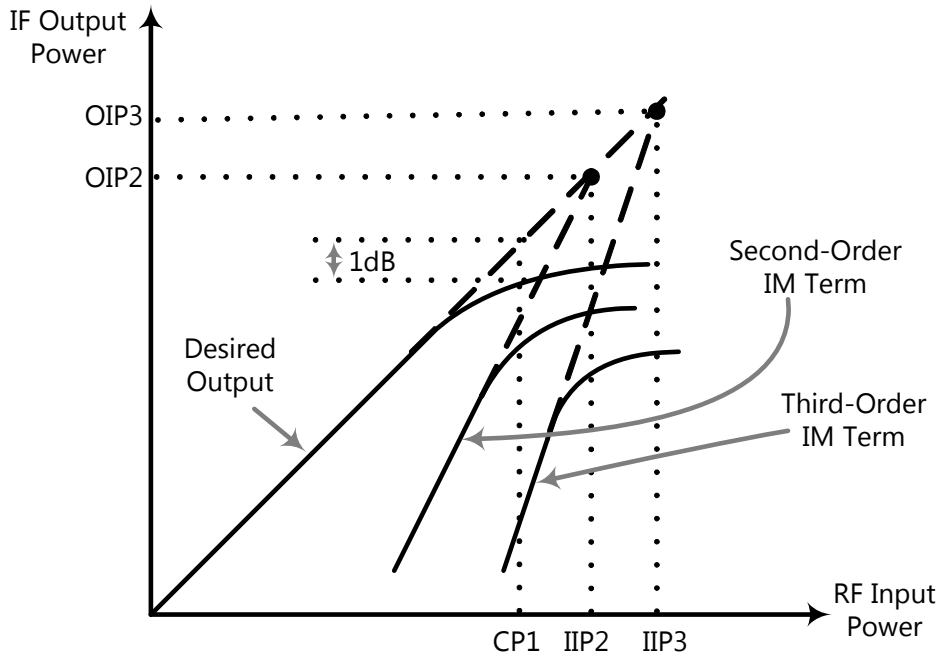

Figure 2.3 Definition of receiver linearity parameters

2.2.4 1-dB Compression Point (CP1)

Under linear operation, the conversion gain (loss) of the mixer will be constant, regardless of input RF power. If the input RF power increases by 1 dB, then the output IF power will also increase by 1dB. However, as the RF power becomes too large, the amplification of signals is eventually going into saturation when applying increasing input power. The 1 dB compression point is a measure of the linearity of the receiver and is defined as the input RF power required to increase the conversion loss by 1 dB from ideal; see Figure 2.3.

2.3 Design Issues for Direct Conversion Receivers

2.3.1 DC Offsets

A direct conversion receiver down-converts the desired signal to zero frequency or close to zero frequency. Therefore, a strong, nearby signal,

including the receiver's own LO, can mix with itself down to zero-IF (this is known as “self-mixing”) and generate a dc level that appears as interference at the center of the desired band. This could corrupt the signal and, more importantly, saturate the following stages. Specifically, the gain of the variable gain amplifier (VGA) provides very high voltage gain, e.g. 60dB. If the DC offsets exists at the output of the mixer, it would be amplified by the VGA and appear at the input of the ADC. As a result, this amplified offset would saturate the ADC, thereby prohibiting the process of the desired signal.

There are two main mechanisms of self-mixing, namely LO leakage and interfere leakage. Figure 2.4 shows self-mixing of LO due to the finite isolation typical of silicon-based ICs between the LO and RF ports of a mixer. Since the LO is typically a strong signal in order to provide sufficient drive for the mixer switching transistors, the LO can leak with sufficiently high amplitude through these unintended paths back to the frontend LNA. Therefore, the LO signal can reflect off the LNA output back into the mixer RF input and mix with itself, thereby generating a static DC level. The situation is exacerbated if the LO signal leaks back to the LNA input and is amplified before reaching the mixer input. Likewise, as shown in Figure 2.5, a strong nearby interferer, such as another user’s LO, can also generate DC offsets by finding a path to the mixer LO port and mixing with itself [18].

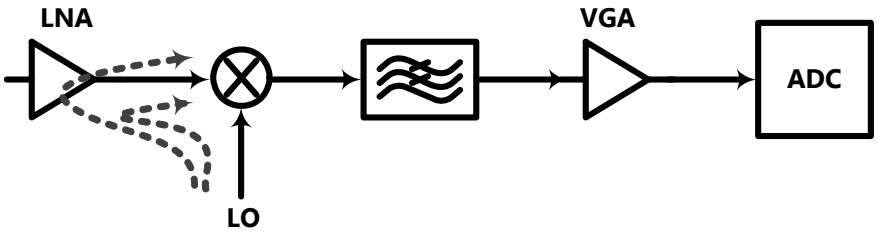

Figure 2.4 Self-mixing of LO (LO Leakage)

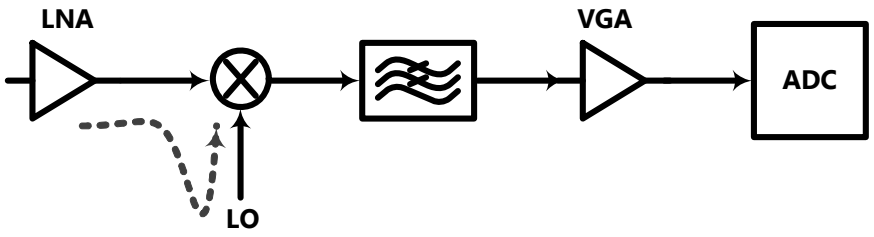

Figure 2.5 Self-mixing of interferes (Interferes Leakage)

2.3.2 I/Q Mismatch

Usually, the Direct Conversion Receiver requires quadrature LO frequencies for down-conversion. A 90˚ shifted LO (Q signal) frequency must be applied to the mixer together with a non-shifted one (I signal). The errors in the 90˚ phase shift as well as mismatches in the amplitudes of the I and Q LO frequencies corrupt the down-converted signal constellation, thereby raising the bit error rate. To minimized the I/Q mismatches some I/Q calibration techniques have been developed, as stated in [2].

2.3.3 Even-Order Distortion

In DCRs even-order distortion, which is normally dominated by the second-order distortion, becomes problematic. If there are two strong interferers close to the signal of interest, they would create a low frequency interferer beat in the presence of the 2^{nd}-order distortion. Ideally, this low frequency interferer is ignorable. In reality, however, mixers always exhibit a finite direct feedthrough from RF port to IF port, as illustrated in Figure 2.6. The low frequency 2^{nd}-order intermodulation would present at the IF port without any frequency translation, thus distorting the desire signal. The second-order nonlinearity can be characterized using 'second intercept point,' IP2.

Even-order distortion can be alleviated by using fully differential circuits. The signal taken from the antenna, however, is always single-end. Thus a single-end to differential conversion is required. In addition, more power is

dissipated by differential pairs. Therefore, in direct conversion receivers an LNA should have both good IP2 and IP3 performances.

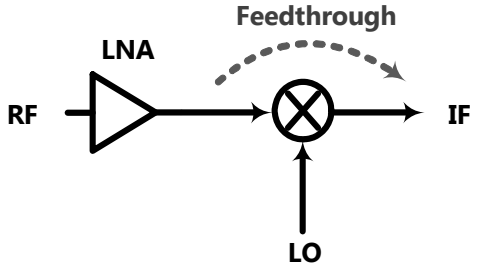

Figure 2.6 Feedthrough from RF to IF

2.3.4 Flicker ($1/f$) Noise

Flicker noise is inherently associated with MOS transistors with a $1/f$, or pink power density spectrum. The mean-square $1/f$ drain noise current is given by

$$\overline{i_n{}^2} = \frac{K \cdot g_m{}^2}{WLC_{ox}{}^2} \cdot \frac{1}{f} \cdot \Delta f, \qquad (2.6)$$

where K is the process-dependent constant, W and L are channel width and length, respectively.

The flicker noise dominates at low frequency, close to DC. Thus, it acts as the same as the DC offsets, thereby corrupting the desired signal after mixing. The effects of flicker noise can be reduced by applying blocks with very large devices after the mixer since the signal after mixing operates at low frequency. In addition, periodic offset cancellation technique that is introduced in the section of DC offset can also suppress the flicker noise.

2.4 Low Noise Amplifiers

Using an LNA, the effect of noise from subsequent stages of the receiving chain is reduced by the gain of the LNA, while the noise of the LNA itself

is injected directly into the received signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, so that the retrieval of this signal is possible in the later stages in the system. A good LNA has a low NF, a large enough gain and should have large enough intermodulation and compression point (IIP2, IIP3 and CP1). Further criteria are operating bandwidth, gain flatness and stability.

Basically, LNAs can be categorised into two configurations: common-source (CS) and common-gate (CG), as shown in Figure 2.7. The common-gate configuration is known as its robustness and simplicity. The input impedance of the circuit is determined by the transconductance of the input transistor, which provides possibility of wideband impedance matching. However, a g_m=20mS is required for most applications to match the input impedance of 50 Ω. Such a g_m results in high power consumption for a given process. Although there are methods that make use of transformers to reduce g_m [3], they are not easy to achieve with on-chip coils for standard CMOS technology due to limitation of the Q factor.

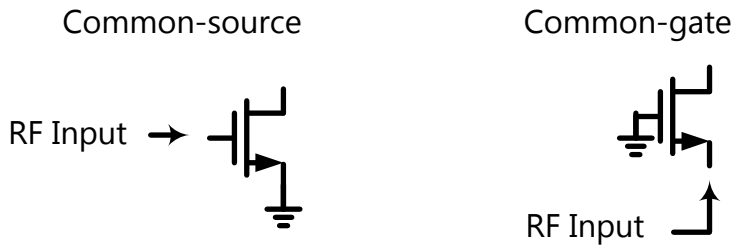

Figure 2.7 Simple CS and CG LNA Configurations

The common-source configuration is power saving compared with the CG configuration. It also provides much better isolation due to the small parasitic capacitance C_{gd}. In addition, input matching can be achieved using inductive degeneration. For those reasons, the CS configuration is very popular in narrow band designs.

In this design we take advantages of both CG and CS configurations by using an LNA topology which combining them together. That will be discussed later.

2.4.1 Impedance Matching

In the case of a complex source impedance Z_S and load impedance Z_L as shown in Figure 2.8, maximum power transfer is obtained when

$$Z_S = Z_L^*, \tag{2.7}$$

where * indicates the complex conjugate. Minimum reflection is obtained when

$$Z_S = Z_L. \tag{2.8}$$

In an LNA, the input impedance matching is important. For instance, the frequency response of the antenna filter that precedes the LNA will deviate from its normal operation if there are reflections from the LNA back to the filter. Furthermore, undesirable reflections from the LNA back to the antenna must also be avoided. The quality of the termination is defined by the reflection coefficient (Γ).

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{2.9}$$

Usually, the performance of the impedance matching is measured by S11 parameter.

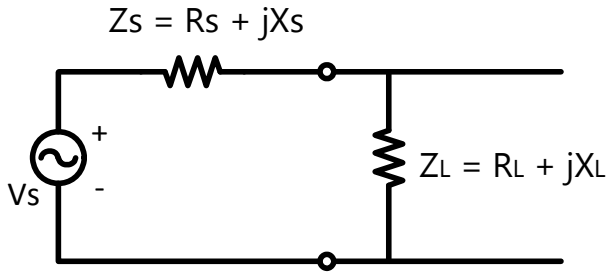

Figure 2.8 Simple network for impedance matching

2.4.2 Noise

2.4.2.1 Thermal noise of resistors

The thermal noise of a resistor can be modelled as a voltage noise source in series with a noiseless resistor, as displayed in Figure 2.9.

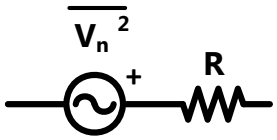

Figure 2.9 Example of resistor thermal noise model

The noise power of the voltage source is

$$\overline{v_n^2} = 4KTR\Delta f, \tag{2.10}$$

where K is Boltzmann's constant, T is the absolute temperature in kelvins, and Δf is the noise bandwidth in hertz.

2.4.2.2 Drain Current Noise in MOSFETs

The drain current noise in MOSFETs is commonly modelled as current source across the drain and source in shunt with the transconductor of the transistor. The noise has a power given by

$$\overline{i_n^2} = 4KT\gamma g_m\Delta f, \tag{2.11}$$

2.4.2.3 Other Noise Sources

There are a lot of noise sources in MOSFETs, for instance, shot noise popcorn noise as well as the flicker noise described in 2.3.4.

2.4.2.4 Noise Figure

The noise factor of an LNA is defined as

$$NR = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source}. \quad (2.12)$$

The noise figure is defined as

$$NF = 10 \log NR \quad (2.13)$$

2.4.3 Linearity

As illustrated in section 2.2.3, there would be harmonics and interferes during the receiving operation. An LNA must not only simply amplify signals without adding much noise, but also remain linear even when strong signals are being received. The parameters that are most commonly used to measure the linearity of an LNA are IP3 and CP1. Due the even order distortion issue in DCR, IP2 is also needed to take into consideration.

2.5 Mixers

In a RF front-end the mixer receives the signal from the LNA and mixes it with the signal from a local oscillator to convert the signal to a lower frequency called intermediate frequency.

2.5.1 Conversion Gain (Loss)

The conversion gain of a mixer is defined as the ratio of the desired IF output to the value of the RF input.

2.5.2 Noise Figure

Noise Figure is defined as

$$NF = 10 \log NR = 10 \log \frac{SNR_{input(RF)}}{SNR_{output(IF)}}. \quad (2.14)$$

Two representation of noise figure are used, namely single-sideband (SSB) NF and double-sideband (DSB) NF. When the desired signal only resides at one frequency, SSB NF is used to measure the performance of a mixer. In

cases where desired signals are found in both sidebands of the input, the DSB NF is applicable.

It is obvious that the SSB NF will be normally 3dB greater than the DSB NF, since both have the same IF noise but the former has signal power in only a single sideband.

2.5.3 Linearity and Isolation

Since a mixer cannot be absolutely linear, it also suffers from the problems of harmonics and intermodulation. The parameters, IP3 and CP1, described in section 2.2.3 can be used to measure the linearity of a mixer as well.

Another problem for a mixer is isolation. As discussed in 2.3.1 and 2.3.3, if there are leakages among the three ports of a mixer, signals will mix with itself or feedthrough, causing DC offsets or even-order distortions, thus degrading the performances of a down-conversion receiver. Unfortunately, there will always be some small amount of power leakage among the RF, LO and IF ports. The isolation is usually measured by the S12 parameter. Typically, 25-35dB, 20-30dB and 25-35dB isolation is required for LO to RF, LO to IF and RF to IF, respectively.

2.5.4 Double-Balanced Mixer

Figure 2.10 shows a typical double-balanced mixer. The transistors driven by LO signals switch alternatively to form a multiplication function, multiplying the linear RF signal current from with the LO signal. The circuit in Figure 2.10 consists of two single-balanced mixers that are connected in antiparallel. Consequently, this type of mixer provides a high degree of LO-IF isolation by summing the LO to zero at output. Typically, 40-60dB of LO-IF isolation is achievable. On the other hand, since the switches are driven by the LO signal, v_{LO} must be chosen large enough.

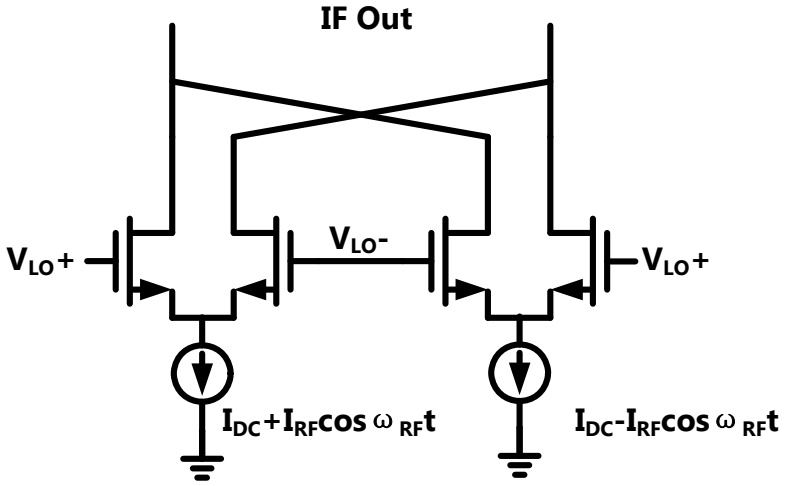

Figure 2.10 Double-balanced mixer

3

WIDEBAND NOISE CANCELLING BALUN-LNAS

The rapid downscaling of CMOS technology has led to more compact and faster RF circuits. Application examples are Bluetooth standard (2.4, 3.6 and 5 GHz) and satellite (0.95-2.15GHz). A wideband LNA can replace several LC-tuned LNAs typically used in multiband and multimode narrow-band receivers, improving chip area effectiveness and fitting better with the trend towards flexible radios with as

much signal processing as possible in the digital domain (toward "software defined radio") [16]. There are two key challenges associated with wideband LNAs: 1) the broadband characteristic, i.e., relatively flat gain, low noise figure (NF) and impedance matching over the covered frequency band; 2) the linearity. A high linearity is essential to minimize unwanted mixing of in-band blockers, which can consume much more power than the desired frequency.

In addition, differential signal is preferred in the receiving chain to reduce 2^{nd} –order distortion and to reject power supply and substrate noise. The signal received from the antenna, however, is always single-end. Therefore, it is inevitable to convert the single-end signal into differential before the LNA. Off-chip baluns with low losses are typically solution for narrowband applications, which calls for several off-chip devices in case of wideband operation. On the other hand, wideband passive baluns typically have high loss, degrading the overall NF of a receiver significantly [11].

Recent works on wideband low noise amplifiers based on single-to-differential (S-to-D) topology [9][10] with noise cancelling scheme have shown reliable RF performances such as output balancing, moderate noise figure, high linearity and broadband input matching. In this chapter, two wideband Balun-LNAs using the S-to-D topology designed in 65nm CMOS technology are going to be introduced followed by in-depth discussion of each performance.

3.1 Topology

3.1.1 Output Balancing (Balun Operation)

The S-to-D topology serves as a useful single ended to differential converter, which takes input from the antenna and drives the differential inputs of the mixer. It combines a common gate (CG) stage and a common source (CS) stage, as shown in Figure 3.1. The CG stage provides wideband input matching and an in-phase gain

$$A_{v,CG} = g_{m,CG} \cdot R_{CG}. \quad (3.1)$$

where $g_{m,CG}$ represents the transconductance of the common-gate stage. While the CS stage provides an anti-phase gain

$$A_{v,CS} = -g_{m,CS} \cdot R_{CS}. \quad (3.2)$$

When the gains of the two stages are equal the functionality of a balun is realized.

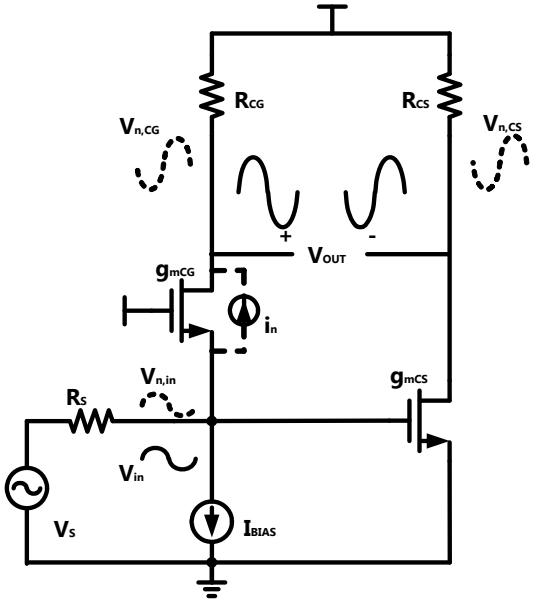

Figure 3.1 The basic common-gate-common-source single-to-differential topology

3.1.2 Noise Cancelling

It is well known that the CG amplifier presents a high noise figure, which is usually greater than 3dB due to the impedance matching and a g_m of 20mS. This topology addresses the problem by using a properly designed CS stage to cancel the noise of the CG transistor, which dominates in the CG stage. As shown in Figure 3.1 where solid and dashed lines represent signals and noise, respectively, the noise current due to the CG transistor generates an

in-phase noise voltage on the source resistor ($v_{n,in}$) and an amplified anti-phase noise voltage across R_{CG} ($v_{n,CG}$).

$$v_{n,CG} = -A_{v,CG} \cdot v_{n,in}. \quad (3.3)$$

The CS stage also amplifies the noise voltage ($v_{n,in}$) leading to an anti-phase noise voltage ($v_{n,CS}$), which is fully correlated with $v_{n,CG}$, across R_{CS}.

$$v_{n,CS} = A_{v,CS} \cdot v_{n,in}. \quad (3.4)$$

For equal CS and CG gain, the noise due to CG transistor is fully cancelled by differential sensing.

3.1.3 Transconductance-Scaling

According the previous work [11], there are three main configurations to implement the balun-LNA, as follows.

1) The transconductance of the CS and CG transistors are equal and the load resistors are equal, too. In this situation, $g_{mCG}=g_{mCS}$ and $R_{CG}=R_{CS}$.

2) The g_m of CS stage is scaled up n times while keeping that of CG not changed. The loads are kept equal, therefore, $g_{mCS}=n \cdot g_{mCG}$ and $R_{CG}=R_{CS}$.

3) The g_m of CS stage is n times bigger than that of CG, however, the load resistor of CS stage is n times smaller than the load of CG stage, leading to $g_{mCS}=n \cdot g_{mCG}$ and $R_{CS}=n \cdot R_{CG}$.

Figure 3.2 [11] displays the noise figure, voltage gain (A_v) and gain imbalance (ΔA_v) versus the scaling factor n for the three configurations. Configuration 1) fails to achieve low noise though the noise of CG is cancelled. One of the reasons is that this configuration cannot provide high GBW since the transconductance of the two transistors are fixed to 20mS for input matching. Thus, in wideband applications, there is not enough gain to suppress the noise. Another reason is the noise from CS stage becomes significant due to its low g_m ($\approx 1/R_s$) and is magnified by the voltage division of ½ by R_s and R_{in}. However, this configuration is still

attractive due to its equal DC level at the output. A gain-boosting scheme is invented to overcome the problem of gain and noise, which will be introduced in section 3.3.

Configuration 2) provides decreasing NF and growing voltage gain when the factor *n* increases. Although the noise of CG is not fully cancelled, the configuration takes advantage of increased transconductance of the CS stage, suppressing the total noise figure. The gain imbalance, however, is unacceptable.

Configuration 3) shows an even faster decrease gain of NF with increasing *n*. this is because the noise of CS transistor shrinks and the gain and gain imbalance remain constant with respect to *n*. In this case, due to the fully cancelled noise of CG transistor and increased transconductance of CS transistor, it is possible to obtain a NF below 2dB with a big *n* value. In addition, the gain and gain imbalance maintain at a constant level with respect of *n*. For the advantages above, this configuration is used to design one of the LNAs in this work (LNA.A).

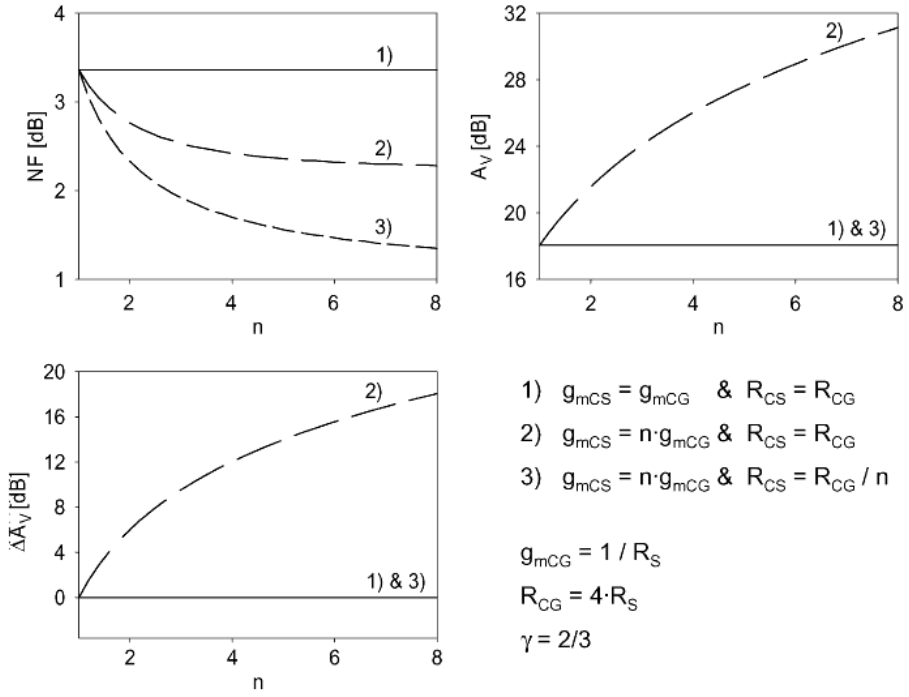

Figure 3.2 Noise Figure (NF), voltage gain (*Av*) and gain imbalance (*ΔAv*) versus impedance scaling factor 'n' for three different cases [11]

3.1.4 Distortion Cancelling

Not only the noise, but also the distortion of CG transistor is cancelled, providing remarkably enhanced IIP2 and IIP3 for the LNAs.

Figure 3.3 shows the small signal equivalent circuit of the CG stage of the LNA. Weakly nonlinear behaviour is assumed and distortion is assumed to originate only from the nonlinear memory-less voltage to current conversion of the matching device. Using a Taylor approximation, the nonlinear voltage (v_{in}) generated by the signal source (v_s) via R_S can be written as

$$v_{in} = \alpha_1 \cdot v_s + v_{NL}. \qquad (3.5)$$

where α_1 represents the first Taylor coefficients and v_{NL} represents all the nonlinear terms.

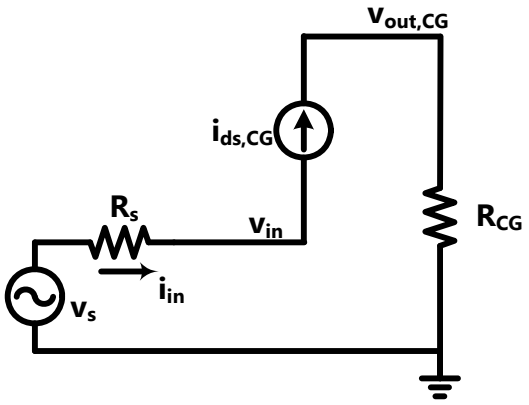

Figure 3.3 Small signal equivalent circuits of the CG stage

Obviously, the output

$$v_{out,CG} = i_{in} \cdot R_{CG} = \frac{v_S - v_{in}}{R_S} \cdot R_{CG} = ((1-\alpha_1) \cdot v_S - v_{NL}) \cdot \frac{R_{CG}}{R_S}. \quad (3.6)$$

Using the discussion in 3.1.1 and assuming the input impedance is perfectly matched ($R_S = 1/g_{m,CG}$), we obtain

$$v_{out,CS} = -v_{in} \cdot \frac{R_{CG}}{R_S} = -(\alpha_1 \cdot v_S + v_{NL}) \cdot \frac{R_{CG}}{R_S}. \quad (3.7)$$

As a result, the nonlinearity of the CG stage is subtracted by the differential sensing of the output,

$$v_{out} = v_{out,CG} - v_{out,CS} = -v_S \cdot \frac{R_{CG}}{R_S}. \quad (3.8)$$

Therefore, the distortion caused by the CS stage dominates in this kind of circuits. Unfortunately, high linearity is only available in a very small range of V_{gs} of the CS transistor. The stability of the IIP2, however, becomes a problem. In practical implementation, the IIP2 of this topology is also relatively sensitive to components mismatches.

One way to improve the stability of IIP2 is to adopt a differential current balancer (DCB) [12], consisting of cascaded amplifiers and cross-coupled capacitors, as the DCB shown in Figure 3.5. However, the current balancer cannot be employed on g_m-scaled circuits since the DCB requires equal output resistance of the cascaded transistors to cancel imbalances. But this is not possible for a scaled circuit.

3.2 Scaled-g_m Balun-LNA (LNA.A)

Figure 3.4 depicts the schematic of the Inducotrless Scaled-g_m Noise-Cancelling Balun-LNA (LNA.A). It employs the S-to-D conversion described in 3.1. In LNA.A, configuration 3) described in 3.1.3 is used. Both of the CG and CS stages are cascaded to provide better isolation leading to higher voltage gain. M_1 and M_3 have the same g_m as normal cascade configurations, and so do M_2 and M_4. The CG stage is biased using a resistor (R_{BIAS}) to avoid internal or external inductors. And the resistor can also provide a bias voltage to M_2.

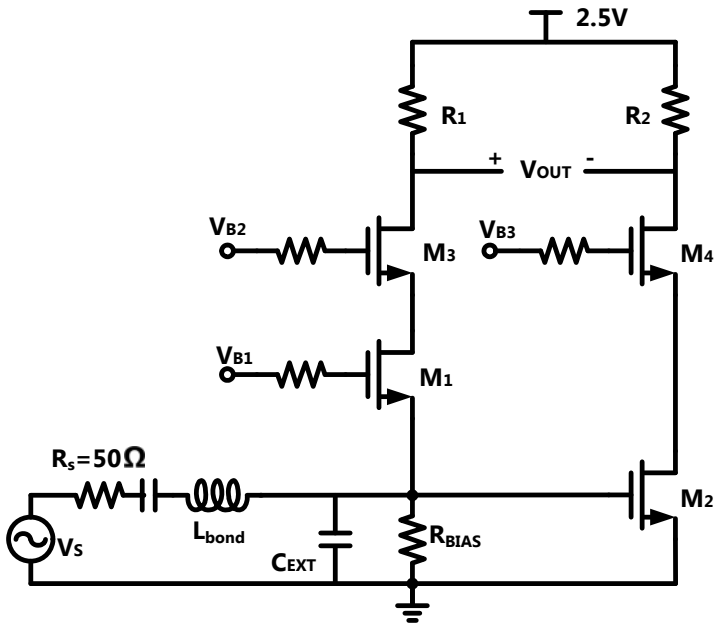

Figure 3.4 Inducotrless Scaled-g_m Noise-Cancelling Balun-LNA (LNA.A)

3.2.1 Input Matching

As discussed in 2.4, the input impedance of CG configuration is $1/g_m$ over a large range of frequency bandwidth. In this circuit, a bias resistor R_{BIAS} is connected in parallel with the CG transistor to provide DC current path for the CG transistor, so that the total input impedance becomes

$$R_{in} \approx \frac{1}{g_{m1}} \,//\, R_{BIAS}. \tag{3.9}$$

R_{BIAS} needs to be large to avoid affecting impedance and gain much; on the other hand, it cannot be too large, which consumes a lot of power. Typically, 350-500Ω is acceptable.

An external capacitor (C_{EXT}) is adopted to form a π-network, which helps to provide a broad input matching, together with the input bondwire inductance and the input capacitance. Depending on the application and requirement the C_{EXT} can be removed and the input matching would only be degraded by a few dB.

3.2.2 Gain and Noise Figure

The gain of the LNA is the differential of CS and CG stages.

$$A_V = g_{m1}R_1 + g_{m2}R_2, \tag{3.10}$$

Where g_{m1} and g_{m2} are the transconductance of M_1 and M_2, respectively.

To simplify the calculation of NF, only the thermal noise of the source and load resistor and of the CG transistors is taken into account assuming γ= 2/3, which is known to be optimistic for short channel devices. To begin with, the noise power generated by the source resistor at the output is given by

$$\overline{v_{n,s}{}^2} = 4KTR_s \cdot \left(\frac{R_{in}}{R_s+R_{in}}\right)^2 \cdot A_v{}^2. \tag{3.11}$$

The CG transistor generates a current noise source which can be converted into a voltage noise at the input of the CG and CS stages, namely $\overline{v_{n,in}{}^2}$, can be expressed as

$$\overline{v_{n,in}{}^2} = \frac{4KT\gamma}{g_{m1}}. \tag{3.12}$$

This noise voltage will be amplified by the CG stage, then generating a voltage noise power ($\overline{v_{n,CG}{}^2}$) via the load resistor R_1. This noise is given by

$$\overline{v_{n,CG}{}^2} = 4KT\gamma g_{m1} \cdot R_1{}^2 . \tag{3.13}$$

As the noise $\overline{v_{n,in}{}^2}$ is at the input of both CG and CS stages, it will also be amplified by the CS stage, leading to a noise ($\overline{v_{n,CS}{}^2}$) via the load resistor of CS stage (R_2). This noise is expressed as

$$\overline{v_{n,CS}{}^2} = \frac{4KT\gamma}{g_{m1}} \cdot g_{m2}{}^2 R_2{}^2. \tag{3.14}$$

Finally, the noise power ($\overline{v_{n,R}{}^2}$) caused by the load resistors is given by

$$\overline{v_{n,R}{}^2} = 4KT(R_1 + R_2) . \tag{3.15}$$

Using equation 2.11 and assuming $R_{in}=1/g_{m1}$, it is easy to calculate the noise factor of the circuit:

$$NR = \frac{\overline{v_{n,S}{}^2} + \overline{v_{n,CG}{}^2} + \overline{v_{n,CS}{}^2} + \overline{v_{n,R}{}^2}}{\overline{v_{n,S}{}^2}}$$

$$= 1 + \frac{\gamma \cdot g_{m1}(R_1 - R_S \cdot g_{m2} R_2)^2}{A_V{}^2} + \frac{\gamma g_{m2}{}^2 R_2{}^2 (1 + g_{m1} R_S)^2}{A_V{}^2 R_S} + \frac{\gamma (R_1 + R_2)(1 + g_{m1} R_S)^2}{A_V{}^2 R_S}, \tag{3.16}$$

where the second, third and fourth term of NR account for noise of M_1, M_2 and load resistors, respectively.

When the input impedance is matched to R_s, 3.16 can be written as

$$NR = 1 + \frac{\gamma(g_{m1}R_1 - g_{m2}R_2)^2}{{A_V}^2} + \frac{4\gamma g_{m2}{R_2}^2}{{A_V}^2 R_S} + \frac{4\gamma(R_1+R_2)}{{A_V}^2 R_S}, \quad (3.17)$$

3.3 Gain-Boosting Current-Balancing Equal-g_m Balun-LNA (LNA.B)

Figure 3.5 shows the schematic of the gain-boosting current-balancing equal-g_m Balun-LNA. It consists of an S-to-D amplifier, an inverter based gain-boosting amplifier (g_{mx}) and a differential current balancer (DCB).

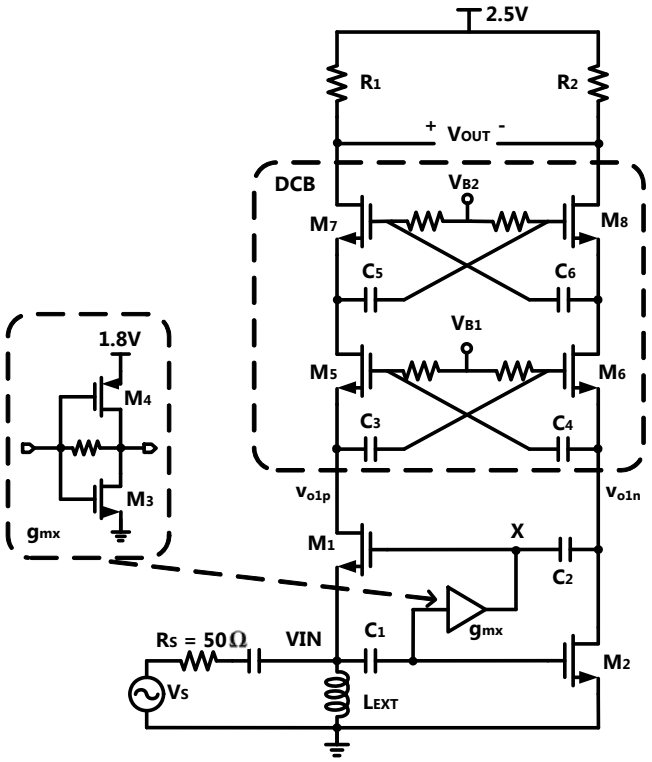

Figure 3.5 Gain-Boosting Current-Balancing Equal-gm Balun-LNA (LNA.B)

The S-to-D amplifier achieves output balancing while realizing wideband input impedance matching. Unlike the S-to-D topology of LNA.A, this

amplifier applies equal biased and sized transistors (equal g_m) for both common gate and common source stages, leading to better linearity.

The DCB, which corrects the errors of the two branches, can be applied on this topology. It can be treated as a current controlled current source with unity gain, offering the desired differential balancing inherently. Using the double cascaded amplifiers (M_5-M_8) with cross-coupled capacitors (C_3-C_6), the DCB significantly increases the precision of outputs balancing. The final differential imbalance should be just the residual of the original error so that distortions can be minimized. Moreover, the DCB improves the balun-LNA's reverse isolation and linearity by lowering the swing at v_{o1p} and v_{o1n}, where distortion arising from the nonlinear output resistance of M_1-M_4

The extra gmx can be seen as an amplifier with transconductance of g_{mx}. It enhances the gain of the circuit, helps to achieve good input matching and self-biases M_1 and M_2 simultaneously.

The circuit works as follows. The common source stage composed of gmx and M_2 generates an anti-phase output signal at point X. Assuming that the signal at X is $-A \cdot v_{in}$, v_{out+} is given by

$$v_{out+} = A_{v1} \cdot v_{in} = G_{m1} \cdot R_1 \cdot v_{in} = g_{m1} \cdot (1 + A) \cdot R_1 \cdot v_{in}. \quad (3.18)$$

The gain is boosted by this scheme and the noise and input resistance are reduced. Moreover, the negative output is given by

$$\begin{aligned} v_{out-} = A_{v2} \cdot v_{in} &= -G_{m2} \cdot R_2 \cdot v_{in} = -(g_{m2} + g_{mx}) \cdot R_2 \cdot v_{in} \\ &= -(g_{m2} + g_{m3} + g_{m4}) \cdot R_2 \cdot v_{in}. \end{aligned} \quad (3.19)$$

Thus, in order to balance the outputs,

$$A = \frac{g_{mx}}{g_{m1}} = \frac{g_{m3}+g_{m4}}{g_{m1}} \quad (3.20)$$

should be satisfied.

An external inductor is used to achieve a wideband impedance matching. The input resistance of the circuit is

$$R_{in} \approx \frac{1}{g_{m1}(1+A)}. \tag{3.21}$$

When $g_{m1}=g_{m2}$ and $R_1=R_2=R$, the voltage gain can be written as

$$A_v = \frac{v_{out+}-v_{out-}}{v_{in}} = 2 \cdot R \cdot (g_{m1} + g_{m3} + g_{m4}) \tag{3.22}$$

Similarly to the calculation for LNA.A, when assuming $G_{m1} \cdot R_s = 1$, the noise factor with respect to R_s becomes

$$NR = 1 + \frac{\gamma(G_{m1}R_1 - G_{m2}R_2)^2}{(A_{v1}+A_{v2})^2} + \frac{4\gamma G_{m2}{R_2}^2}{(A_{v1}+A_{v2})^2 R_S} + \frac{4\gamma(R_1+R_2)}{(A_{v1}+A_{v2})^2 R_S}, \tag{3.23}$$

where the second, third and fourth term account for M_1, M_2 and load resistors noise. The γ is assumed 2/3.

4

THE BLIXERS

The software defined radio (SDR) and ultra-wideband technique has become increasingly popular. The rapid development of these kinds of applications demands receivers operating over a large range of bandwidth, i.e. up to 6GHz for SDR or 10GHz for UWB. The bandwidth, however, is limited in traditional receivers. Specifically, active mixers have capacitance input impedance due to the gate-source parasitic capacitance. When a passive mixer is used, a voltage buffer or transconductance stage, which also loads the LNA capacitively, is often required between the LNA output and the input of mixer(s). The so-called BLIXER topology based on

the LNAs described in Chapter 3 resolves the bandwidth problem by lowering the impedance at RF nodes. In this chapter, the implementation of these circuits is introduced and analysed.

4.1 The Basic BLIXER Topology

Figure 4.1 shows the basic BLIXER Topology consisting of the balun-LNA core of Figure 3.1 with a cascaded double-balanced mixer which has been shown in Figure 2.10. The balun-LNA core is applied to provide input matching, single-end to differential conversion and amplification. The circuit also perform noise cancelling and distortion cancelling, but at IF outputs instead since the switching transistors are driven by the LO signals.

RF signals only appear at three nodes: the input and the drains of the two amplifying transistors, implying only the impedance of these three nodes limits the RF bandwidth. If these three nodes are loaded with low impedance, high bandwidth is achievable. For input matching, the input is loaded with 50Ω. Moreover, the impedance at drains of M_1 and M_2 equal $1/g_m$ of mixer transistors, which are similar to that of the amplifying transistor. Thus, the impedance at all the RF nodes is equal to or lower than 50Ω, allowing for high bandwidth. If only the gate-source capacitance of transistors is taken into account, the RF bandwidth of the BIXER is limited by the f_T of the switching transistors. f_T is given by

$$f_T = \frac{g_{m,switch}}{C_{gs,switch}}, \tag{4.1}$$

which is typically an order of magnitude higher than that of the balun-LNA with a voltage gain in the order of 20dB [17].

Moreover, the power efficiency of the BLIXER is also attractive since the mixer re-uses the current of the LNA, allowing for high conversion gain is available without dissipating a lot of power.

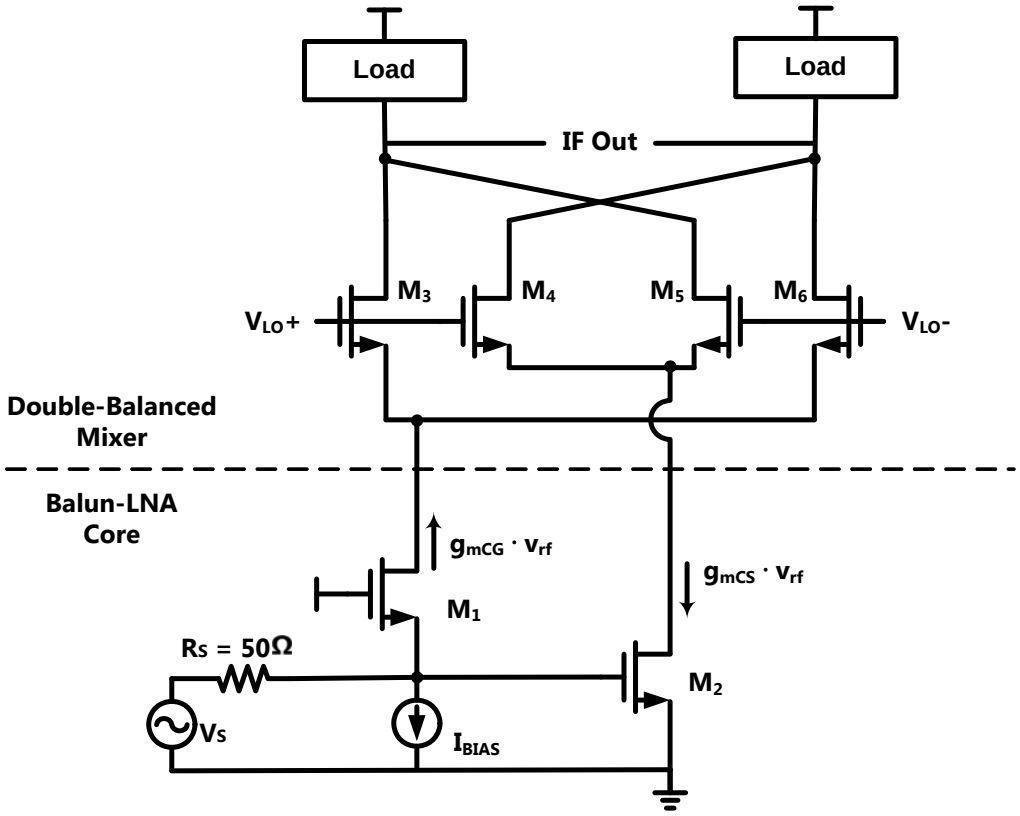

Figure 4.1 Basic BLIXER topology consisting of the balun-LNA core of Figure 3.1 with cascaded double-balanced mixer

4.2 The I/Q-BLIXER Implementations

4.2.1 I/Q-BLIXER using LNA.A

As discussed in 2.1, quadrature LO signals are required for down conversion receivers. In the I/Q-BLIXER, two double balanced mixers in parallel are employed. Figure 4.2 shows a completed schematic of I/Q-BLIXER using LNA.A driven by LO waveforms with 25% duty cycle. The LNA is slightly modified compared with that is shown in section 3.2. The bias resistor R_{BIAS} is replaced by a RF choke L_{BIAS} and moved off chip. This RF choke not only provides the path for DC current of CG stage, but also helps improve the input impedance matching at low frequency. An off

chip capacitor is also applied to form a π-network together with the bonding wire which can be modeled as inductor of 1~2nH.

The cascaded transistors are replaced by the mixers' switching transistors which are driven by the LO signals. Due to the application of quadrature LO signals, which has been explained in 2.1, two double-balanced mixers are used with parallel connection.

The LO signals applied to the mixers are square waveform with 25% duty cycle, as shown in Figure 4.3, making the voltage gain at IF of the I/Q-BLIXER is

$$A_{v,BLIXER} = \frac{\sqrt{2}}{\pi} \cdot A_{v,LNA.A} = \frac{\sqrt{2}}{\pi} \cdot (g_{m1}R + g_{m2} \cdot \frac{R}{n}) \quad (4.2)$$

where $\sqrt{2}/\pi$ equals the fundamental Fourier component of a 25% duty cycle LO signal.

There is a reduction of 7dB for the voltage gain due to the factor of $\sqrt{2}/\pi$. However, the DC voltage drop across the load resistors is

$$\overline{V_{Load}} = \frac{1}{4} \cdot (I_{CG} \cdot R_{CG} + I_{CS} \cdot R_{CS}) \quad (4.3)$$

since the CG and CS DC current flow through each load for only ¼ period with 25% duty cycle LO signals. This provides the opportunity to increase the load resistor to compensate the gain reduction. If the load resistors are doubled, extra 6dB voltage gain is obtained, consequently, only 1dB lower than that of the balun-LNA.

As the LNA.A uses the scaled-g_m topology, which means

$$g_{m2} = n \cdot g_{m1}. \quad (4.4)$$

Consider when V_{LO} I+ is high, there are two current paths from supply to ground, which are R_1-R_2-M_3-M_1 and R_3-M_4-M_2. The load for the CG stage is R1+R2 and that for CS stage is R3. In order to get the same gain for both

CG and CS stages, the loads need to be divided into two parts, as shown in Figure 4.2.

$$R_1 + R_2 = n \cdot R_3 \tag{4.5}$$

should be satisfied. In this design, we set $R_1=R_3=R_5=R_7=R/n$ and $R_1+R_2=R_3+R_4=R_5+R_6=R_7+R_8=R$, so that all the IF outputs are well balanced.

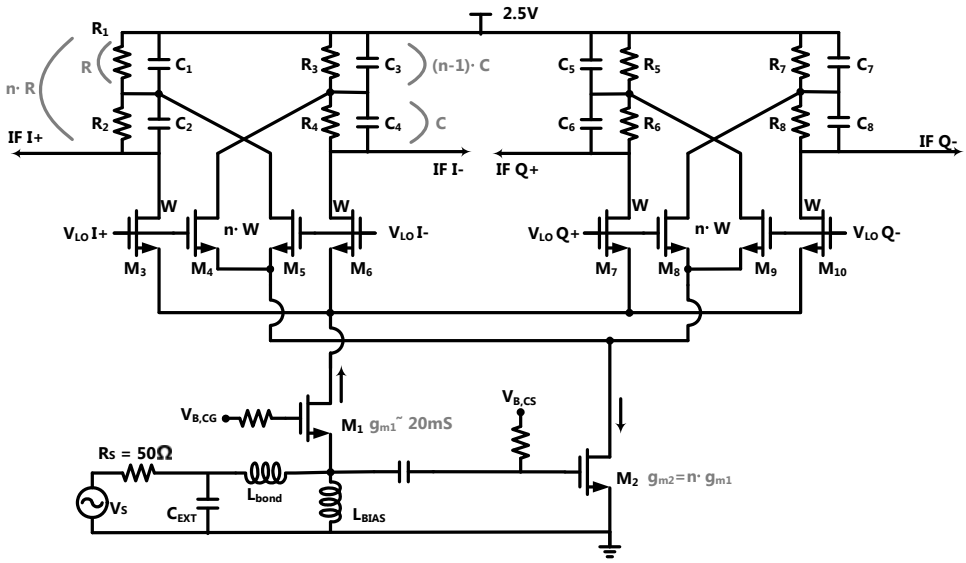

Figure 4.2 I/Q-BLIXER using LNA.A driven by LO waveforms with 25% duty cycle

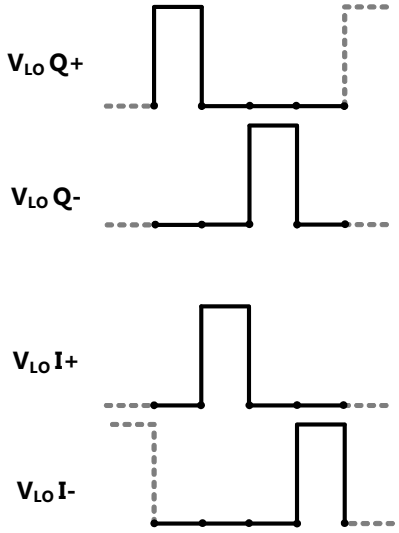

Figure 4.3 25% duty cycle LO waveforms

4.2.2 I/Q-BLIXER using LNA.B

Figure 4.4 shows the I/Q-BLIXER using LNA.B driven by LO waveforms with 25% duty cycle. The LNA core is the one described in section 3.3. Two double-balanced mixers are inserted between the loads and the double current balancer.

As the LNA.B employs equal gm amplifying transistors, the load resistors and capacitors are kept equal, so that there is no need to split them.

The same 25% duty cycle square wave LO signals, which is shown in Figure 4.3, are applied to the mixers' transistors. Thus, the voltage gain is given by

$$A_{v,BLIXER} = \frac{\sqrt{2}}{\pi} \cdot A_{v,LNA.B} = \frac{\sqrt{2}}{\pi} \cdot 2 \cdot R \cdot (g_{m1} + g_{m3} + g_{m4}). \quad (4.6)$$

Though 7dB is lost due to the factor of $\sqrt{2}/\pi$, we can double the load resistors to compensate it as described in the previous section.

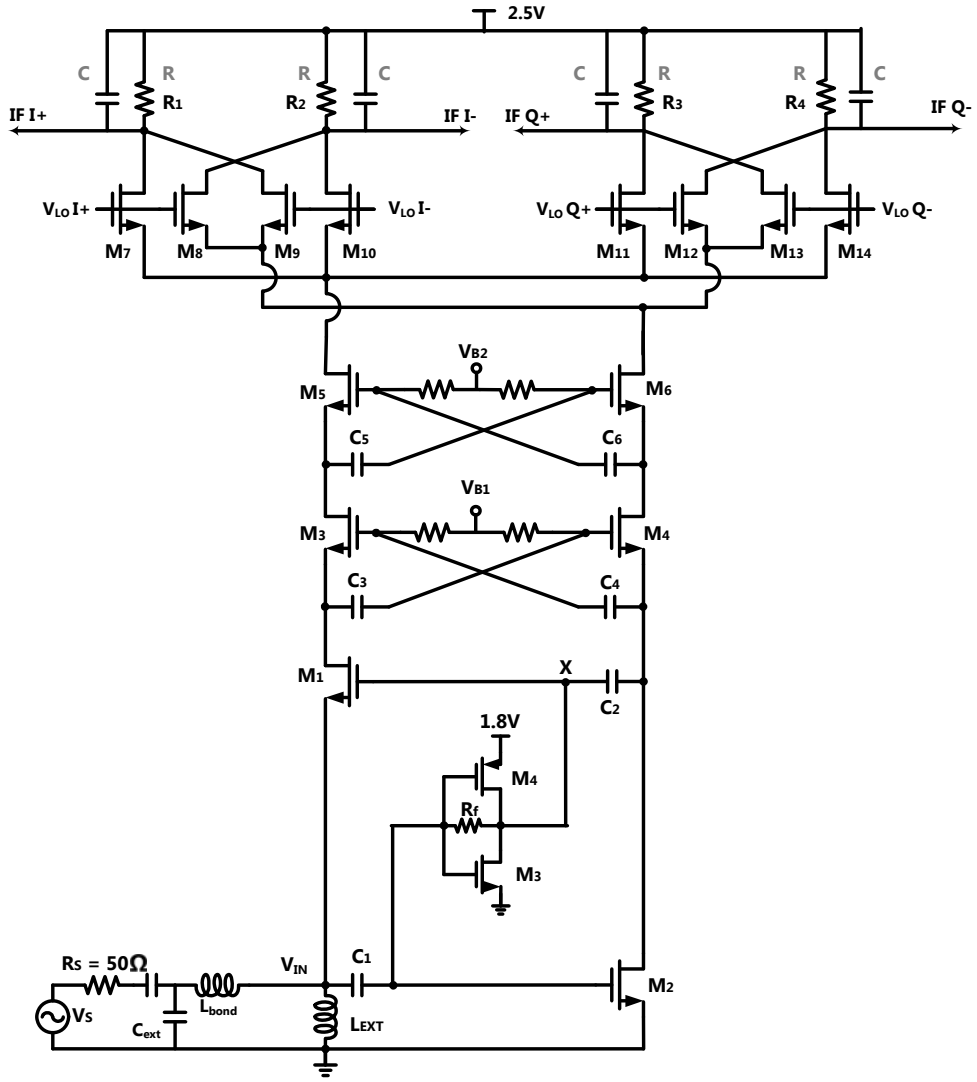

Figure 4.4 I/Q-BLIXER using LNA.B driven by LO waveforms with 25% duty cycle

5

SIMULATION RESULTS

5.1 Simulation Results for LNA.A

5.1.1 Gain, Noise Figure, Input Matching and DC Power Consumption

The circuits of LNAs have been designed in 65nm COMS technology and simulated with 50fF capacitive loads in the frequency range between 600MHz and 5GHz. Parameters of the circuits are shown in Table 5.1. The

LNA.A was simulated with CS transistor of 90μm width to compare the performance to LNA.B.

	LNA.A	LNA.B		LNA.A	LNA.B
W_1/L(μm)	66/0.06	26/0.06	g_{m1}(mS)	21.8	17
W_2/L(μm)	90/0.06	26/0.06	g_{m2}(mS)	59.7	17
W_3/L(μm)		10/0.06	g_{m3}(mS)		8.3
W_4/L(μm)		5/0.06	g_{m4}(mS)		3.2

Table 5.1 Parameters of the LNAs

The red curves in Figure 5.1 show the gain, noise figure and the S11 parameter of the LNA.A and the blue curves are for LNA.B. A voltage gain greater than 20dB is obtained for LNA.A up to 5GHz and a noise figure below 3dB is achievable up to 4GHz. The noise figure can be suppressed by enhancing the gain, however, a trade-off among power consumption, gain and bandwidth is always needed to take into consideration. In addition, S11 parameter is below -12dB, which provides good enough input matching.

The LNA consumes 10mA current from a 2.5V supply. The CG stage takes 2.5mA and the CS stage take 7.5mA since the transconductance of the CS transistor is set 3 times (~60mS) as that of the CG transistor.

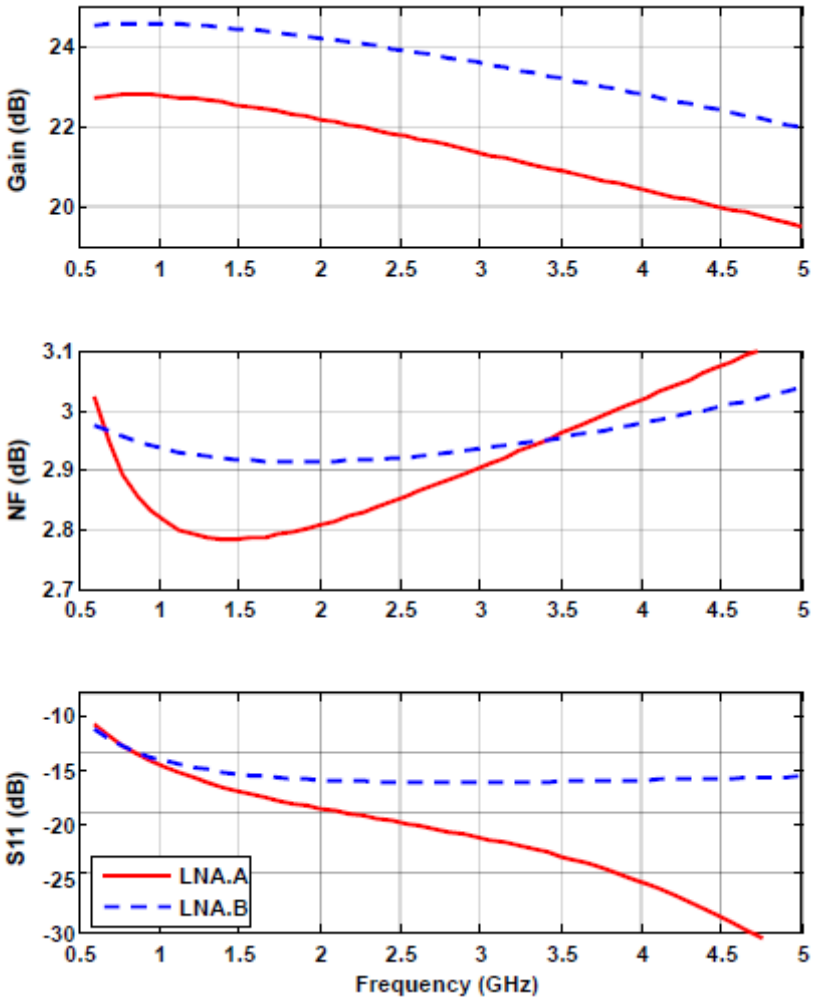

Figure 5.1 Simulation Results of the two LNAs

5.1.2 Linearity

Two sinusoidal tones located at 2.4 / 2.41GHz are chosen to simulate the linearity of the circuits. The LNA.A achieves 31dB for IIP2 and -2.1dB for IIP3; see Figure 5.2 and Figure 5.3.

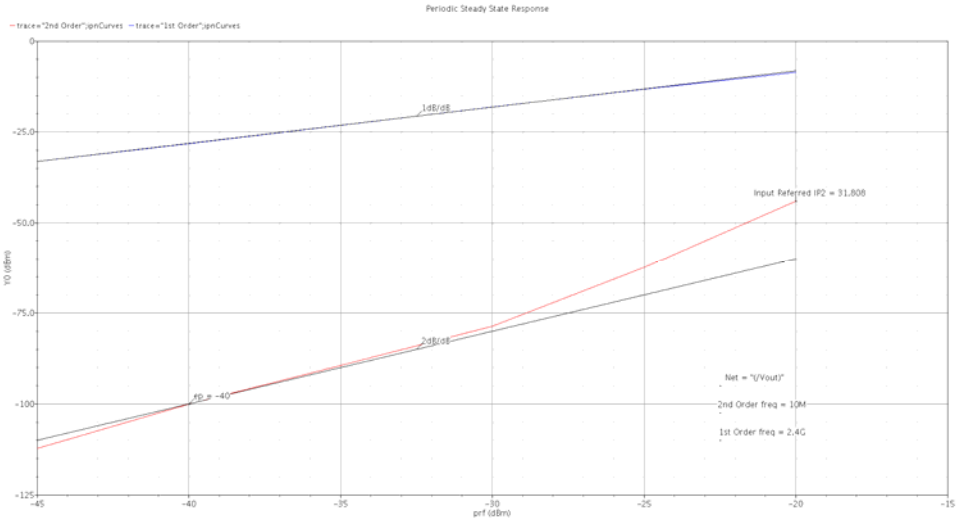

Figure 5.2 IIP2 simulation of LNA.A

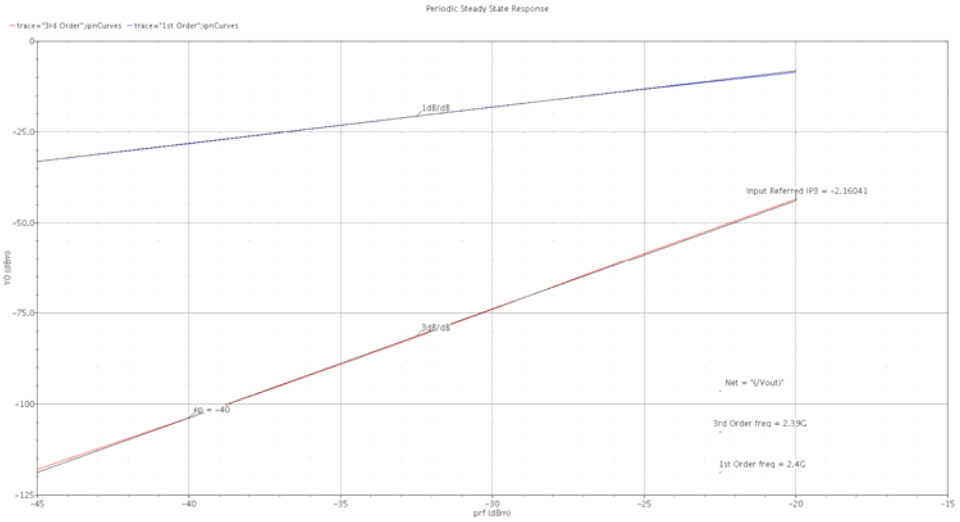

Figure 5.3 IIP3 simulation of LNA.A

Linearity simulations with two tone signals with 10MHz space from 0.5 to 6GHz are also implemented, as shown in Figure 5.4. As all the transistor dimensions and biases are optimized for 2.4GHz application, the LNA achieves the best IIP2 performance at 2.4GHz; nevertheless, the IIP2 is still above 20dB up to 3.5GHz.

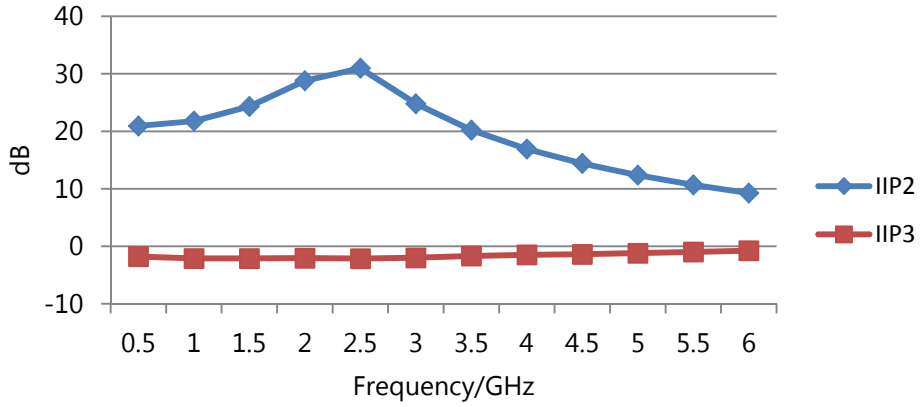

Figure 5.4 IIP2 and IIP3 versus input RF frequency for LNA.A

5.2 Simulation Results for LNA.B

5.2.1 Gain, Noise Figure, Input Matching and DC Power Consumption

The blue dotted curves in Figure 5.1 show the voltage gain, noise figure and the S11 parameter of the LNA.B. A voltage gain greater than 22dB is obtained up to 5GHz and a noise figure below 3dB is achievable also over this bandwidth. The S11 parameter is below -12dB.

The two circuits of LNA.A and LNA.B achieve almost the same NF, close or less than 3dB; however, the gain of LNA.B is higher. That implies that LNA.B requires higher gain to suppress the noise figure as discussed in 3.1.3.

The LNA.B dissipates 17mW from 2.5V/1.8V supplies. Each branch takes 3mA from 2.5V; and the gmx consumes 1.5mA from 1.8V supply voltage.

5.2.2 Linearity

The same two sinusoidal tones, which locate at 2.4 / 2.41GHz, are taken to simulate the linearity. The LNA.B, which benefits from the equal sized and

biased transistors as well as the current-balancing scheme, shows 40dB and 5.8dB for IIP2 and IIP3, respectively; see Figure 5.5 and Figure 5.6.

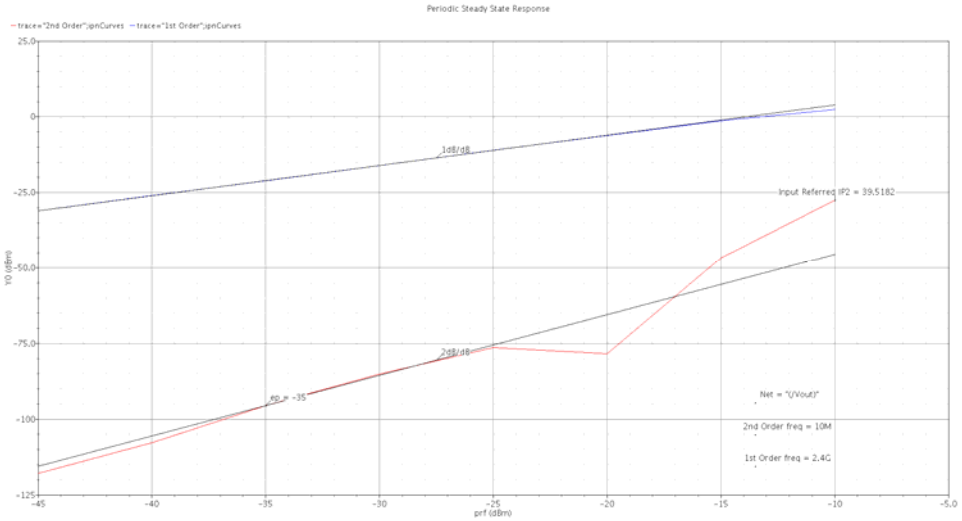

Figure 5.5 IIP2 simulation of LNA.B

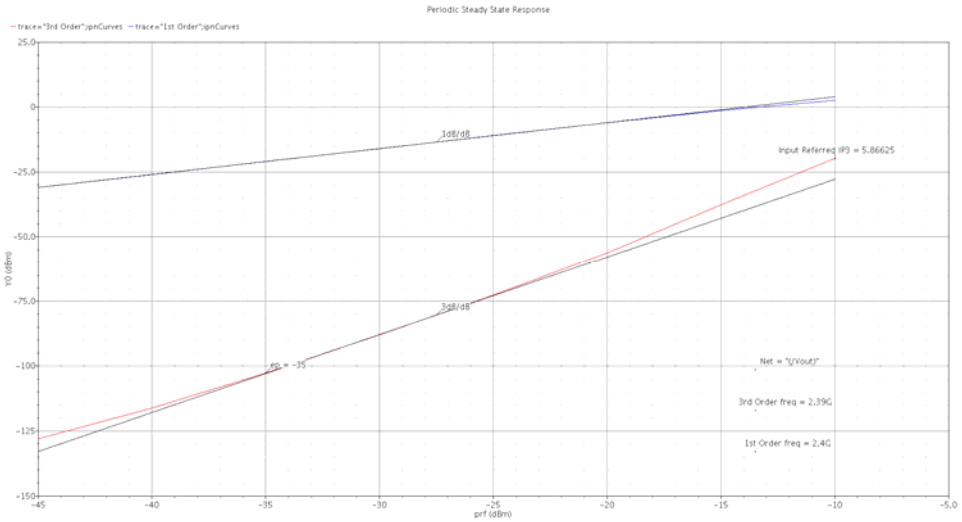

Figure 5.6 IIP3 simulation of LNA.B

Linearity simulations with two tone signals with 10MHz space from 0.5 to 6GHz are also implemented, as shown in Figure 5.7 and Figure 5.4. As all

the transistor dimensions and biases are optimized for 2.4GHz application, the LNA achieves the best IIP2 performance at 2.4GHz; nevertheless, the IIP2 is still above 30dB up to 6GHz.

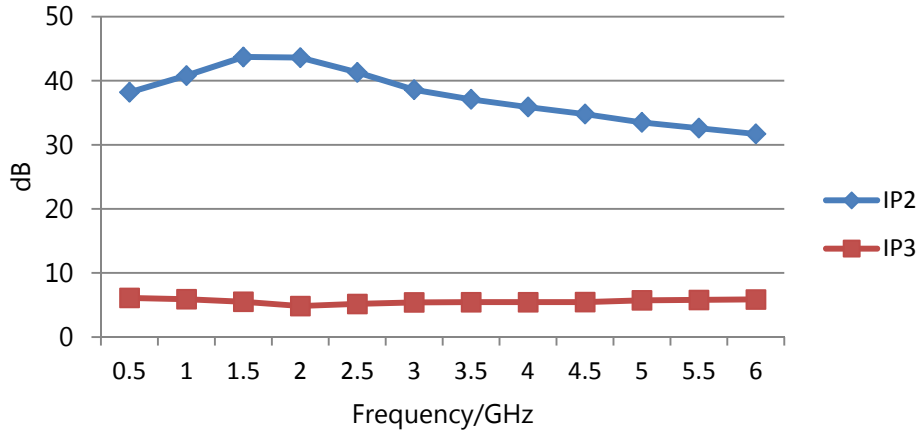

Figure 5.7 IIP2 and IIP3 versus input RF frequency for LNA.B

5.3 IIP2 Analysis

Components mismatches may cause variation of IIP2. In this section, the IIP2 against components mismatches and V_{gs} of the CS transistor are analysed.

Another circuits using topology of LNA.A but with 250µm CS transistor, which achieves the same IIP2 and power consumption as the 90µm one, was simulated to find out the effects on IIP2 due to components mismatches. In order to test this, the circuits are simulated by Monte Carlo analysis. We present, in Figure 5.8, the IIP2 result of a 200-points, mismatch only, Monte Carlo simulation of LNA.A with dimension of 90/0.06µm CS transistor which is biased by a fixed voltage. The average IIP2 of this circuit is 28.3dB; however, only 83.5% of the IIP2 are greater than 25dB, implying the IIP2 is very sensitive to components mismatches. Figure 5.9 shows the stability of IIP2 is improved by replacing the CS transistor by a larger one (250/0.06µm). The IIP2 greater than 25dB

account for 96% of total runs. This is because mismatch is always an absolute value, not a percentage of the parameters' value. So a large transistor is less sensitive to mismatches than a small one. According to the equation

$$I_d = \frac{K}{2} \cdot \frac{W}{L} \cdot {V_{ov}}^2. \quad (5.1)$$

The mismatch on W causes a small change on I_d, and then results in imbalance at outputs, thus deteriorating the linearity. Consequently, the 250μm transistor has less mismatch, leading to stable IIP2.The LNA.B, which benefits from the DCB, provides stable IIP2 even though the dimension of transistors is small, as shown in Figure 5.10. The IIP2 greater than 35dB occupy 92.5% among total runs.

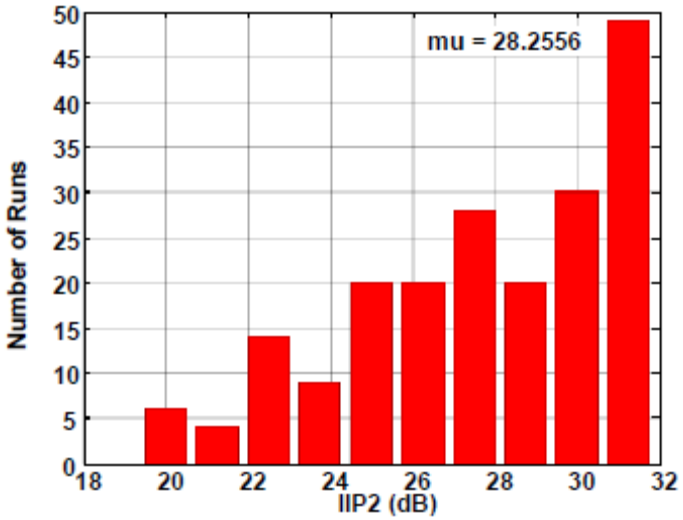

Figure 5.8 Monte Carlo analyse of IIP2, LNA.A, W2=90μm

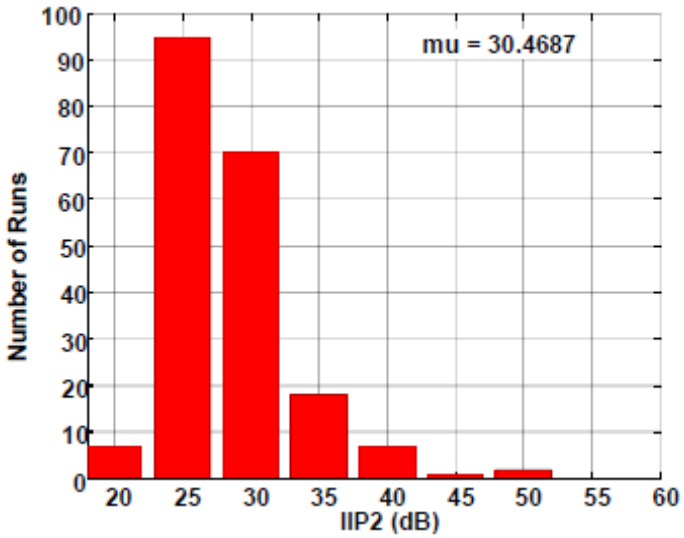

Figure 5.9 Monte Carlo analyse of IIP2, LNA.A, W2=250µm

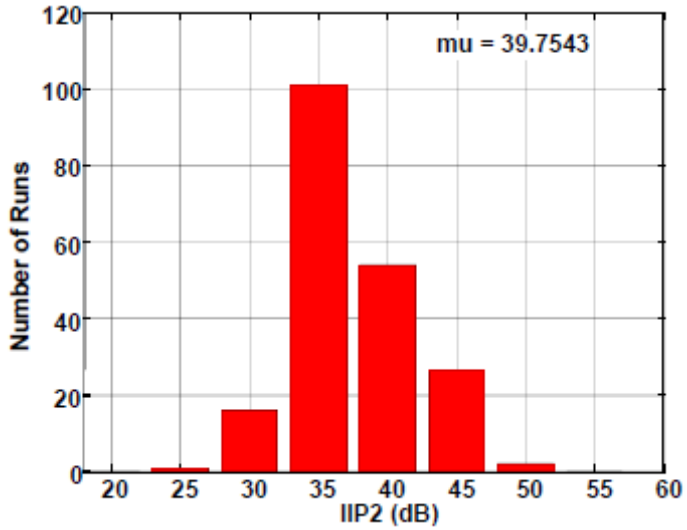

Figure 5.10 Monte Carlo analyse of IIP2, LNA.B

Another way to emulate the effects of matching is to vary the bias voltage of the CS stage since the distortions of the CS stage dominates the output distortion. To tune the bias voltage of the CS transistor is helpful to find an optimized bias point for linearity. Figure 5.11 compares the simulated IIP2

sensitivity with respect to V_{gs} of CS stages. It can be seen that the LNA.B has the widest window of IIP2, verifying that the DCB does help to improve the IIP2 as well as the stability.

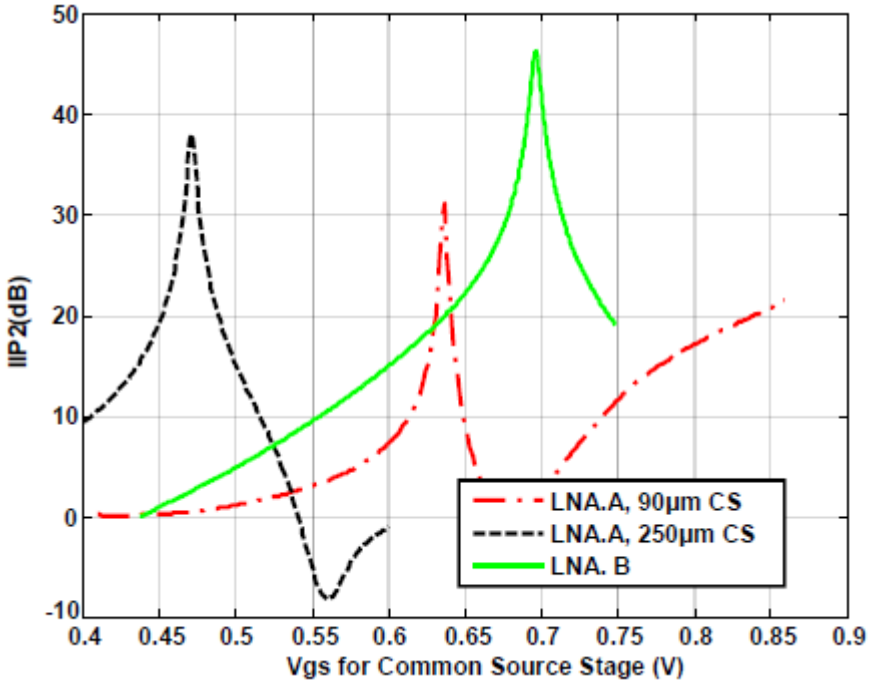

Figure 5.11 Vgs of CS stagesVS IIP2

5.4 Simulation Results for I/Q-BLIXER using LNA.A

5.4.1 Conversion Gain, Input Matching and Noise Figure

The measured voltage conversion gain from RF port to IF port is 20.5dB at IF bandwidth of 500MHz when input frequency is 2.4GHz, as shown in Figure 5.12. The DSB Noise Figure of the I/Q-BLIXER at 2.4GHz LO frequency is 2.7dB and the SSB NF is 5.7dB; see Figure 5.13.

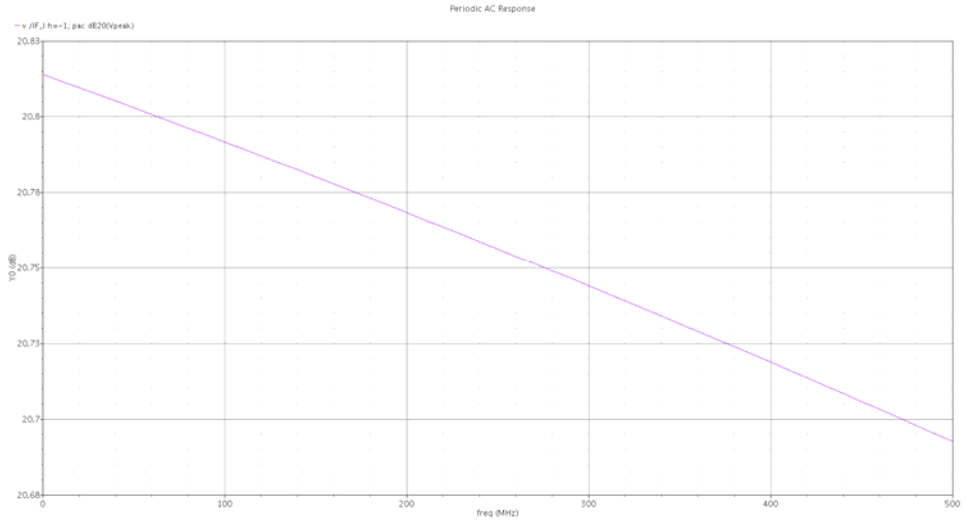

Figure 5.12 Conversion gain of BLIXER using LNA.A for f_{IF}=500MHz

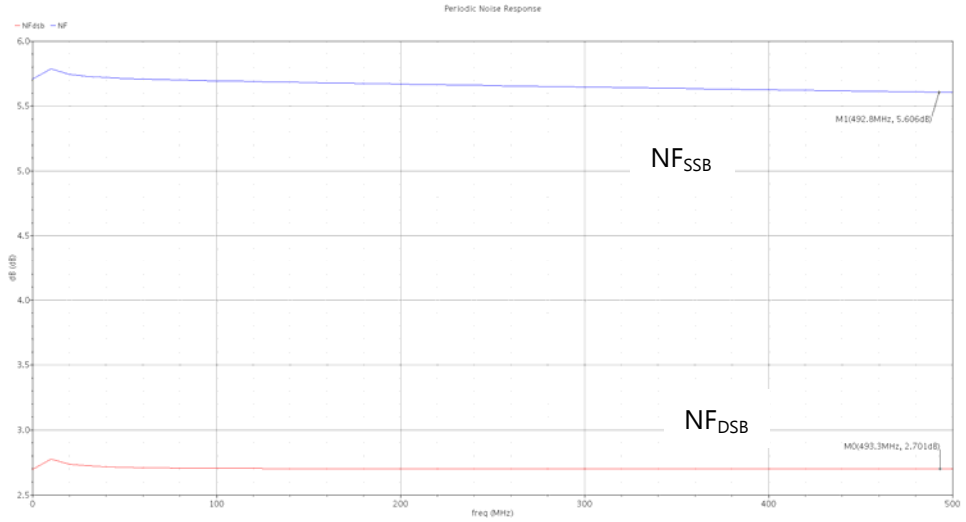

Figure 5.13 Noise Figure of BLIXER using LNA.A for f_{IF}=500MHz

The S11 parameter is below -14dB between 500MHz and 8GHz; see Figure 5.14

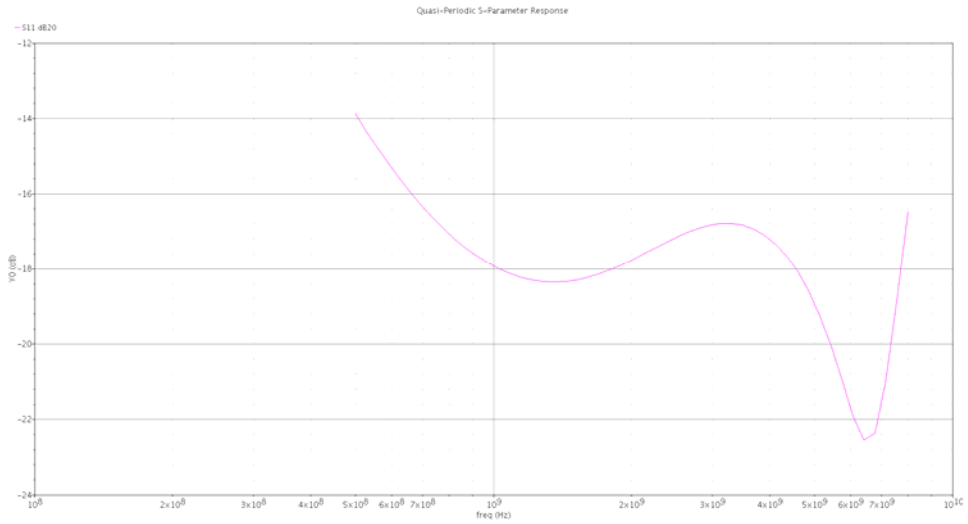

Figure 5.14 S11 parameter simulation for the BLIXER using LNA.A

Figure 5.15 shows the wideband RF performance of the BLIXER. The conversion gain remains flat within 1.5dB up to 8GHz at 50MHz IF frequency. From 0.5-8GHz, the double sideband noise figure and the single sideband noise figure are below 3.23dB and 6.18dB, respectively, using a fixed IF of 50MHz.

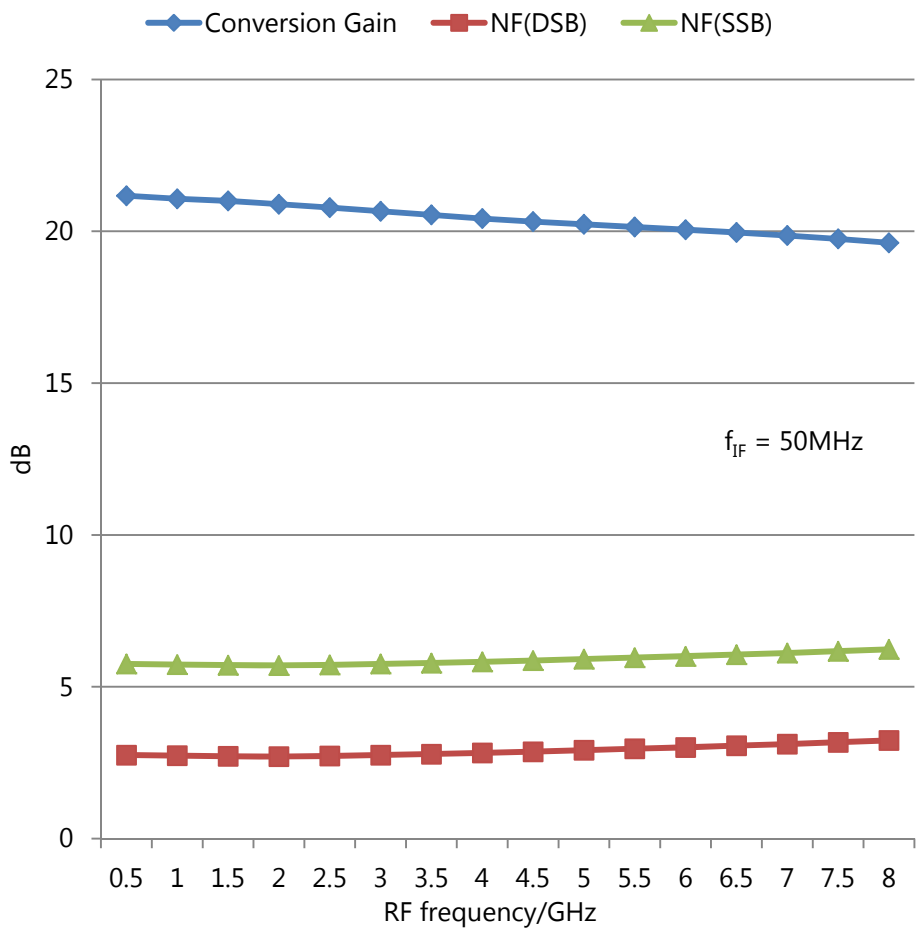

Figure 5.15 Conversion gain (GC), NF_{SSB} and NF_{DSB} of the I/Q-BLIXER using LNA.A

5.4.2 Linearity

Two tones at 5.2GHz and 5.7GHz, which represents two IEEE 802.11a interferers, are used to test the IP3 performance. Using an LO frequency of 4.6GHz, the 3rd –order intermodulation product locates at 100MHz. the simulated IIP3 is -3dB, as shown in Figure 5.16.

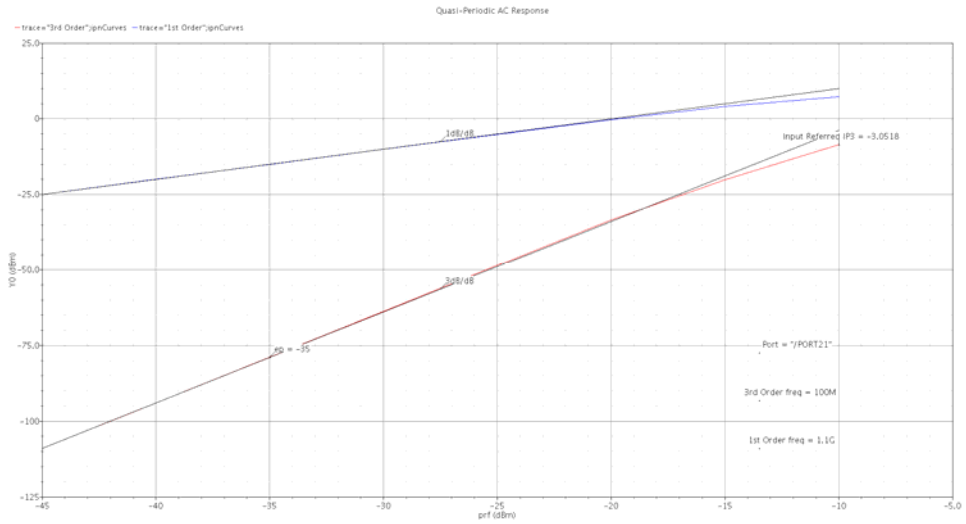

Figure 5.16 IIP3 simulation for BLIXER using LNA.A

The IIP2 equals 18.3dB using 2.4GHz (802.11b/g) and 5.7GHz (802.11a) input tones and LO of 3.2GHz; see Figure 5.17. In addition, 5.7GHz and 5.8GHz signals (two 802.11a interferes) are taken to simulate the intermodulation for tones that leak through the mixer. The intermodulation product at 100MHz shows IIP2s greater than 30dB, regardless of the LO frequency.

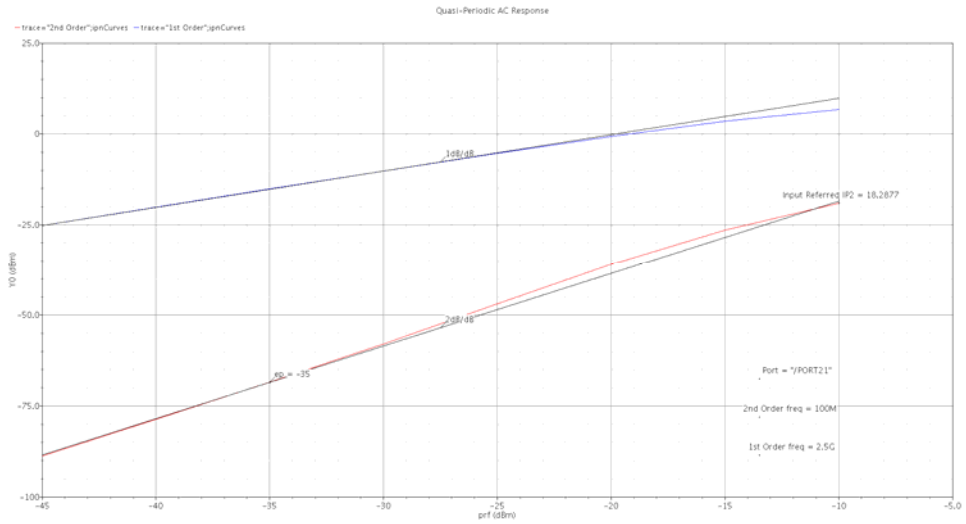

Figure 5.17 IIP2 simulation for BLIXER using LNA.A

5.5 Simulation Results for I/Q BLIXER using LNA.B

5.5.1 Conversion Gain, Input Matching and Noise Figure

The measured voltage conversion gain from RF port to IF port is 20.22dB at IF bandwidth of 500MHz when input frequency is 2.4GHz, as shown in Figure 5.18. The DSB Noise Figure of the I/Q-BLIXER at 2.4GHz LO frequency is 3.4dB and the SSB NF is 6.4dB; see Figure 5.19. The noise is higher than that of the BLIXER using LNA.A. This is due to the noise of the CS stage as stated in section 3.1.3. In addition, Figure 5.20 shows the S11 parameter is below -10dB up to 8GHz.

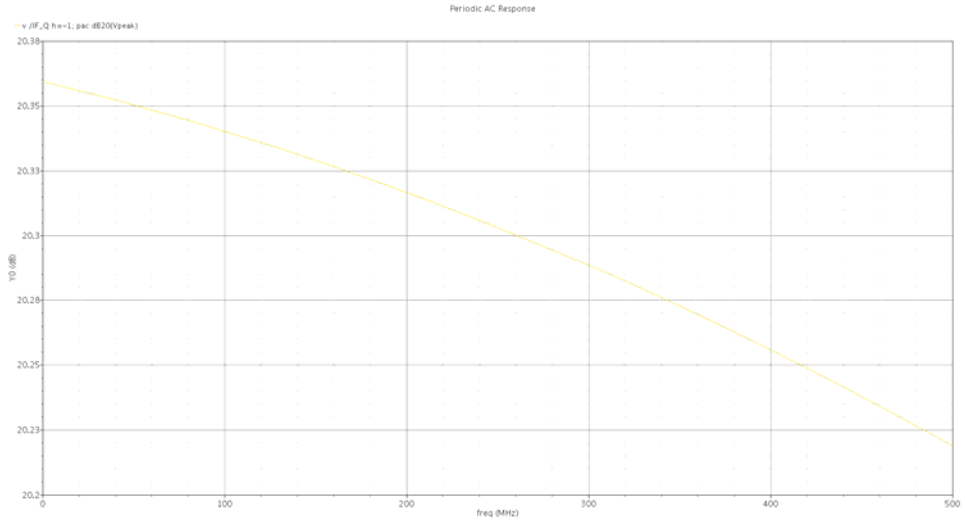

Figure 5.18 Conversion gain of BLIXER using LNA.B for f_{IF}=500MHz

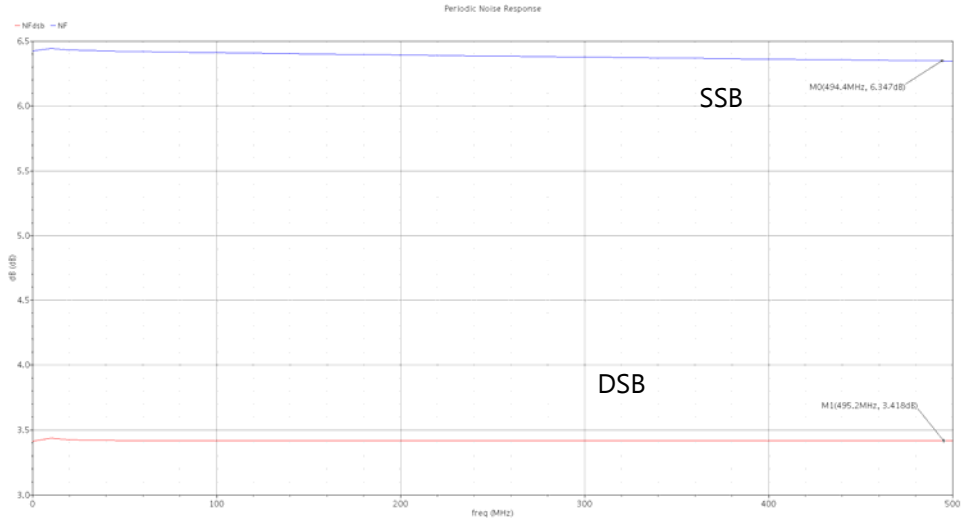

Figure 5.19 Noise Figure of BLIXER using LNA.B for f_{IF}=500MHz

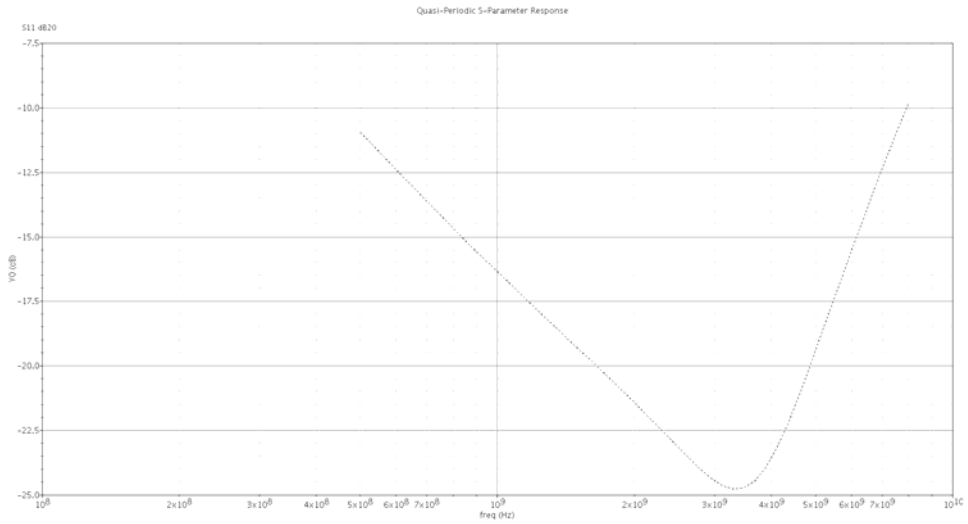

Figure 5.20 S11 parameter simulation for the BLIXER using LNA.B

Figure 5.21 shows the conversion gain, DSB NF and SSB NF against the input RF frequency with a fixed IF frequency of 50MHz. The conversion gain remains flat within 1.5dB up to 8GHz and the NF_{DSB} is below 4.2dB over this bandwidth.

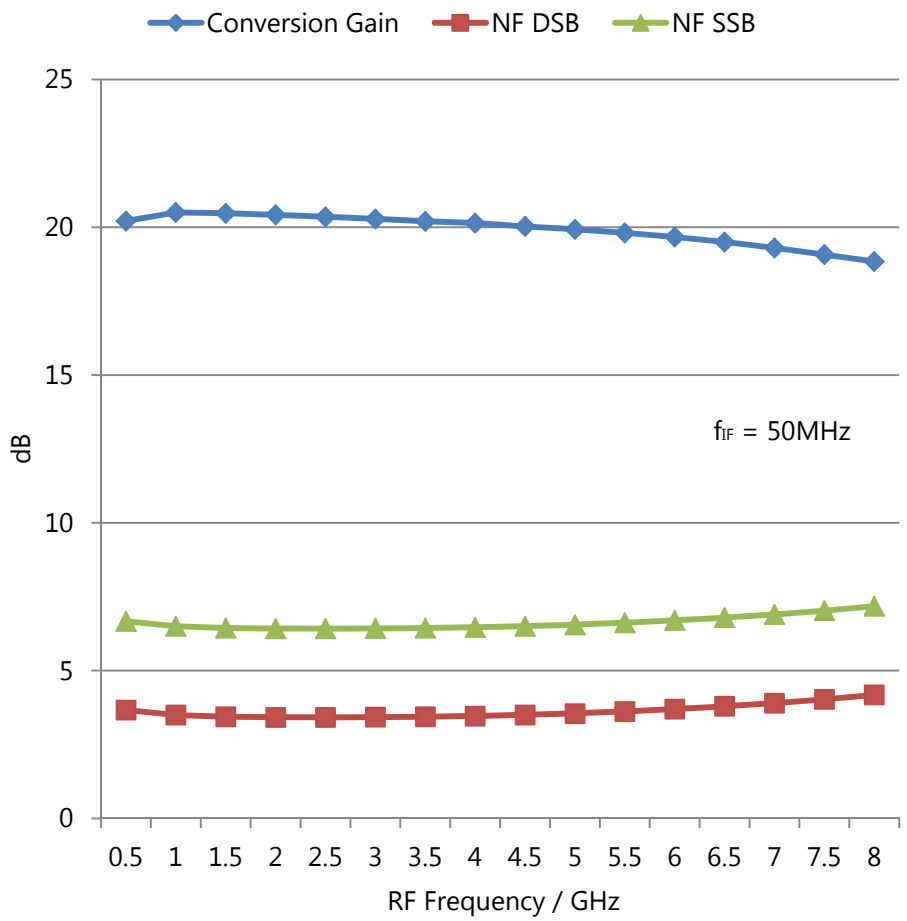

Figure 5.21 Conversion gain (G_C), NF_{SSB} and NF_{DSB} of the I/Q-BLIXER using LNA.B

5.5.2 Linearity

The same tones used to simulate the linearity of the BLIXER using LNA.A are used here to test the IIP2 and IIP3 of the BLIXER using LNA.B. Two tones at 5.2GHz and 5.7GHz with LO frequency of 4.6GHz give the IIP3 of 2.8dB; see Figure 5.22. The IIP2 equals 38dB using 2.4GHz and 5.7GHz input tones and LO of 3.2GHz; see Figure 5.23. Also, 5.7GHz and 5.8GHz signals show IIP2s greater than 40dB, regardless of the LO frequency.

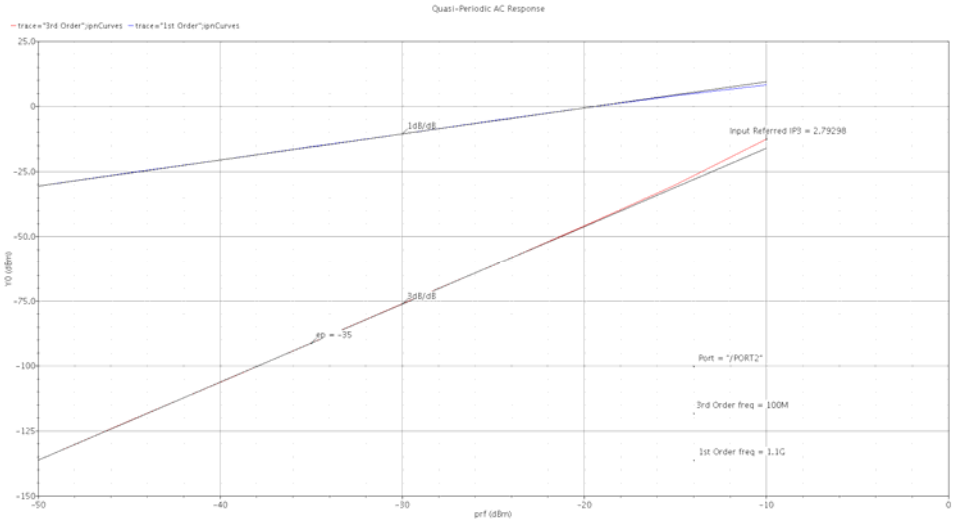

Figure 5.22 IIP3 simulation for BLIXER using LNA.B

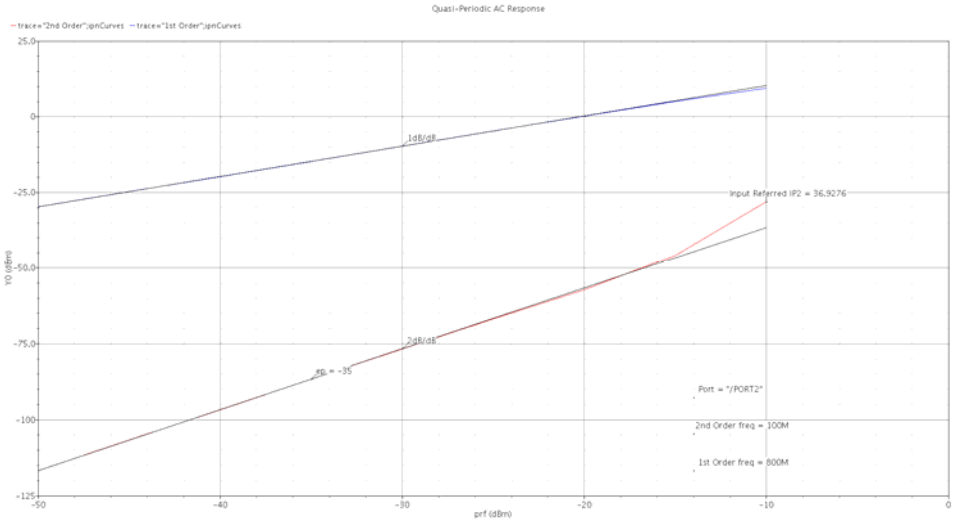

Figure 5.23 IIP2 simulation for BLIXER using LNA.B

5.6 Performances Summary

Table 5.2 lists the obtained performances of the designed BLIXERs using the balun-LNA cores in this work.

	BLIXER using LNA.A	**BLIXER using LNA.B**
Process	STMicroelectronics 65nm CMOS	STMicroelectronics 65nm CMOS
Supply Voltage	2.5V	2.5/1.8V
Bandwidth	0.5-8GHz	0.5-8GHz
Voltage Conversion Gain	>19.6dB	>18.8dB
Noise Figure (DSB)	<3.2dB	<4.2dB
Noise Figure (SSB)	<6.2dB	<7.2dB
S11	<-12dB	<-9dB
IIP2	18.3dBm	37dBm
IIP3	-3dBm	2.8dBm
DC Power	29mW	15mW

Table 5.2 Performances summary of the BLIXERs

6

CONCLUSIONS

6.1 Conclusions

Two wideband balun-LNAs have been designed in STMicroelectronics 65nm COMS technology. Both of them employ a single-end-to-differential conversion topology composed of a common gate (CG) amplifying stage and a common source (CS) stage, providing output balancing and noise and distortion cancelling. One uses transconductance-scaling technique and the other one exploits gain-boosting current-balancing topology. With 2.5V and

2.5V/1.8V supplies the LNAs achieve voltage gains of 24.5dB and 22.8dB, noise figures of below or close to 3dB, IIP2 of 31dB and 41.8dB, respectively. The gain-boosting current-balancing Balun-LNA (LNA.B) with equal transconductance and DCB provides better IP2 performance, both the IIP2 and stability, with small transistors, but suffers the problem of noise figure due to the noise from CS stage. The unequal-g_m topology has better noise performance but unstable IIP2 if the CS transistor is not wide enough. To get stable IIP2, large transistors are required but that calls for more area. In addition, it consumes more power than the equal-g_m LNA.

Balun-LNA I/Q-mixers, which combine the balun-LNA cores and double-balanced mixers, are also designed in the same CMOS technology to resolve the bandwidth limitation in traditional direct-conversion receivers. With 2.5V supply, around 20dB conversion gain, 3dB DSB noise figure, 18.3dB IIP2 and -3dB IIP3 are obtained by the BLIXER using LNA.A over the bandwidth of 0.5 to 8GHz, while consuming 29mW DC power. The counterpart, the BLIXER using LNA.B, achieves around 20dB conversion gain, 4dB DSB noise figure, 38dB IIP2 and 2.8dB IIP3 over the same bandwidth while dissipating 15mW from 2.5/1.8V supplies.

6.2 Future work

The BLIXER topology greatly improves the operating bandwidth of receivers, however, the conversion gain is limited as the current reused double-balanced mixer does not provide any gain. Future work can be done by connecting an active mixer to the any of the balun-LNAs and try to enhance the voltage conversion gain and minimize the noise figure as much as possible for applications which do not require very high bandwidth.

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ACRONYMS

CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
GSM	Global System for Mobile Communications
UWB	Ultra Wideband
SDR	Software Defined Radio
CG	Common Gate
CS	Common Source
S-to-D	Single-end-to-Differential
IMD	Intermodulation Distortions
RF	Radio Frequency
IF	Intermediate Frequency
SNR	Signal-to-Noise Ratio
NF	Noise Figure
NR	Noise Ratio
SSB	Signal-Side Band
DSB	Double-Side Band

APPENDIX 1

L. Zhu and M. Liliebladh, “Comparison and IIP2 analysis of two Wideband Balun-LNAs Designed in 65nm CMOS,” Norchip, November 2011.

Comparison and IIP2 Analysis of Two Wideband Balun-LNA Designed in 65nm COMS

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***Abstract*—Two wideband Balun-LNA configurations have been designed in 65nm COMS technology. Both of them employ a single-to-differential (S-to-D) conversion topology composed of a common gate (CG) and a common source (CS) amplifying stages, providing output balancing and noise cancelling. One is inductorless and the other one exploits gain-boosting current-balancing topology. With 2.5V and 2.5V/1.8V supply the LNAs achieve voltage gains of 24.5dB and 22.8dB, noise factors of below or close to 3dB, input second-order intercept points (IIP2) of 31dB and 41.8dB, respectively. In addition, the sensitivity of IIP2 is deeply investigated.**

Keywords-low noise amplifiers (LNA), Balun-LNA, common gate, common source, self-biasing, single-to-differential (S-to-D), second-order input-referred intercept point (IIP2), noise-cancelling, gain-boosting current-balancing, Monte Carlo.

I. INTRODUCTION

Recent works on wideband low noise amplifiers (LNAs) based on single-to-differential (S-to-D) topology [1] [2] have shown reliable RF performances such as output balancing, moderate noise figure (NF), high linearity and broadband input matching. This topology serves as a useful single-ended to differential converter, which takes input from the antenna and drives the differential inputs of the mixer. This topology combines a common gate (CG) and a common source (CS) amplifying stages, as shown in Figure 1. The CG stage provides wideband input matching and in-phase gain ($g_{m,CG} \cdot R_{CG}$), while the CS stage provides an anti-phase gain ($-g_{m,CS} \cdot R_{CS}$). When the gains of the two stages are equal the functionality of a Balun is realized.

However, it is well known that the CG amplifier presents a high noise factor, which is usually greater than 3dB. This topology addresses the problem by using a properly designed CS stage to cancel the noise of the CG transistor, which dominates in the CG stage [3]. The noise current due to the CG transistor generates an in-phase noise voltage on the source resistor ($v_{n,in}$) and an amplified anti-phase noise voltage across R_{CG} ($v_{n,CG}$). The CS stage also amplifies the noise voltage ($v_{n,in}$) leading to an in-phase noise voltage ($v_{n,CS}$), which is fully correlated with $v_{n,CG}$, across R_{CS}. For equal CS and CG gain, the noise due to CG transistor is fully cancelled by differential sensing.

Two wideband Balun-LNAs using the S-to-D topology were designed in 65nm CMOS technology to investigate IIP2 property. In the inductorless LNA the g_m of CS stage is scaled up n times and the load resistor is scaled down n times ($g_{m,CS}=n \cdot g_{m,CG}$, $R_{CG}=n \cdot R_{CS}$), while still keeping balanced gain

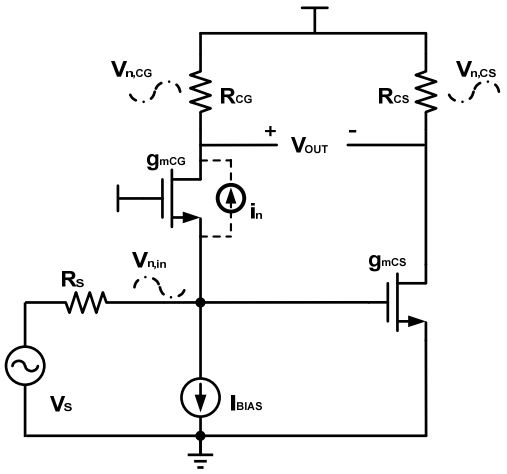

Figure 1. The basic common-gate-common-source single-to-differential topology

for the two stages ($g_{m,CS} \cdot R_{CS} = g_{m,CG} \cdot R_{CG}$). In the gain-boosting current-balancing Balun-LNA [4], the transistors are of equal size and biased same (equal g_m). Normal equal-g_m scheme suffers the problem of noise. The noise from CS stage becomes significant due to its low g_m ($\approx 1/R_s$) and is magnified by the voltage division of ½ by R_s and Z_{in}, leading to degradation of noise performance. But the topology presented in section II. B addresses this by adopting an extra amplifier between the CS and CG stages to improve the gain, thus suppressing the noise.

Not only the noise, but also the distortion of CG transistor is cancelled, as shown in [3], providing remarkably enhanced IIP2 and IIP3. The stability of the IIP2, however, becomes a problem since high linearity is only available in a very small range of V_{gs} of the CS transistor. In practical implementation, the IIP2 of this topology is also relatively sensitive to components mismatches.

One way to improve the stability of IIP2 is to adopt a differential current balancer (DCB) [5], consisting of cascaded amplifiers and cross-coupled capacitors, as the DCB shown in Figure 3. It can be treated as a current controlled current source with unity gain, offering the desired differential balancing inherently. Using the double cascaded amplifiers (M_5-M_8) with cross-coupled capacitors (C_1-C_4), the DCB significantly increases the precision of

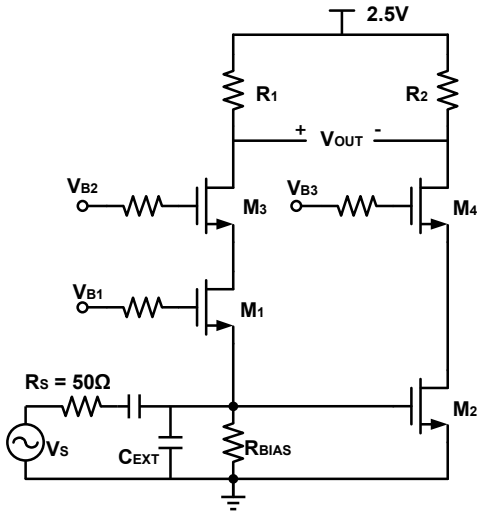

Figure 2. Schematic of inductorless noise-cancelling Balun-LNA

outputs balancing. The final differential imbalance should be just the residual of the original error so that distortions can be minimized.

However, the current balancer cannot be employed on scaled circuits as discussed before. The DCB requires equal output resistance of the cascaded transistors to cancel imbalances. But this is not possible for a scaled circuit.

The paper is structured as follows. Section II presents two topologies of Balun-LNAs. Simulated results for both LNA designs are given in Section III followed by discussion about IIP2 performance. The conclusions are drawn in Section IV.

II. Inductorless Noise-Canceling Balun-LNA (LNA.A) and Gain-boosting Current-balancing Balun-LNA (LNA.B) Topologies

A. Inductorless Noise-Canceling Balun-LNA (LNA.A)

Figure 2 depicts the schematic of the inductorless noise-canceling Balun. It employs the S-to-D conversion described in the previous section. Both of the CG and CS stages are cascaded to achieve a high voltage gain. The CG stage is biased using a resistor to avoid internal or external inductors. And the resistor can also provide a bias voltage to M_2. So the input impedance becomes

$$Z_{in} \approx \frac{1}{g_{m,CG}} \,//\, \mathrm{R}_{BIAS} \tag{1}$$

An external capacitor (C_{EXT}) is adopted to form a π-network, which gives a broad input match, together with the input bondwire inductance and the input capacitance. Depending on the application or requirement the C_{EXT} can be removed and the input matching would only be degraded by a few dB.

When the input impedance is matched to R_s, the NF with respect to R_s is

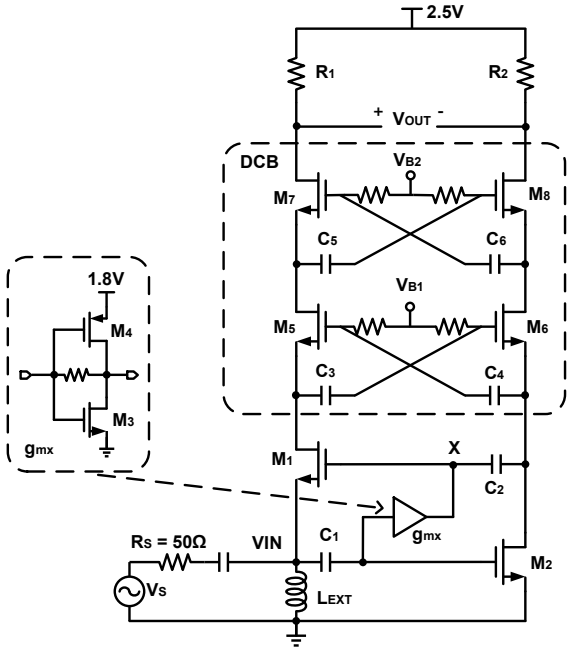

Figure 3. Schematic of Gain-boosting Current-balancing Balun-LNA

$$NF = 1 + \frac{\gamma(g_{m1}R_1 - g_{m2}R_2)^2}{{A_V}^2} + \frac{4\gamma {g_{m2}}^2 {R_2}^2}{{A_V}^2 R_S} + \frac{4\gamma(R_1+R_2)}{{A_V}^2 R_S} \tag{2}$$

$$A_V = g_{m1}R_1 + g_{m2}R_2 \tag{3}$$

where the second, third and fourth term of NF account for noise of M_1, M_2 and load resistors , respectively.

B. Gain-boosting Current-balancing Balun-LNA (LNA.B)

Figure 3 shows the schematic of the gain-boosting current-balancing Balun-LNA. It consists of an S-to-D amplifier, an inverter based gain-boosting amplifier (gmx), and a differential current balancer (DCB).

The S-to-D amplifier achieves output balancing while realizing wideband input impedance matching. Unlike the S-to-D topology of LNA.A, this amplifier applies equal biased and sized transistors (equal g_m) for both common gate and common source stages, leading to better linearity. Moreover, the DCB, which corrects the errors of the two branches, can be applied on this topology. The extra gmx can be seen as an amplifier with transconductance of g_{mx}. It enhances the gain of the circuit, helps to achieve good input matching and self-biases M_1 and M_2 simultaneously.

The circuit works as follows. The common source stage composed of gmx and M_2 generates an anti-phase output signal at point X. Assuming that the signal at X is $-Av_{in}$, v_{out+} is given by

$$\begin{aligned} v_{out+} &= A_{v1} \cdot v_{in} = G_{m1} \cdot R_1 \cdot v_{in} \\ &= g_{m1} \cdot (1 + A) \cdot R_1 \cdot v_{in} \end{aligned} \tag{4}$$

The gain is boosted by this scheme and the noise and input resistance are reduced. Moreover, the negative output is given by

$$v_{out-} = A_{v2} \cdot v_{in} = -G_{m2} \cdot R_2 \cdot v_{in} = -(g_{m2} + g_{mx}) \cdot R_2 \cdot v_{in} = -(g_{m2} + g_{m3} + g_{m4}) \cdot R_2 \cdot v_{in} \quad (5)$$

So in order to balance the outputs,

$$A = \frac{g_{mx}}{g_{m1}} = \frac{g_{m3} + g_{m4}}{g_{m1}} \quad (6)$$

should be satisfied.

An external inductor is used to achieve a wideband impedance matching. The input resistance is

$$Z_{in} \approx \frac{1}{g_{m,CG}(1+A)} \quad (7)$$

When assuming $G_{m1} \cdot R_s = 1$, the noise factor with respect to R_s becomes

$$NF = 1 + \frac{\gamma(G_{m1}R_1 - G_{m2}R_2)^2}{(A_{V1} + A_{V2})^2} + \frac{4\gamma {G_{m2}}^2 {R_2}^2}{(A_{V1} + A_{V2})^2 R_S} + \frac{4\gamma(R_1 + R_2)}{(A_{V1} + A_{V2})^2 R_S} \quad (8)$$

where the second, third and fourth term account for M_1, M_2 and load resistors noise.

III. Simualtion Results and Disccusion

The circuits designed in 65nm COMS technology have been simulated with 50fF capacitive loads in the frequency range between 600MHz and 5GHz. Parameters of the circuits are shown in Table I. the LNA.A was simulated with transistors of 90µm or 250µm width to find out the effects of components mismatches. Since all the other parameters in the circuit were equal the power consumption, gain, NF and S11 reported in this section are valid for both 90 and 250µm width amplifiers.

TABLE I. Parameters of the Circuits

	LNA.A	LNA.B		LNA.A	LNA.B
W_1(µm)	66	26	**g_{m1}(mS)**	21	17
W_2(µm)	90/250	26	**g_{m2}(mS)**	76	17
W_3(µm)		10	**g_{m3}(mS)**		8.3
W_4(µm)		5	**g_{m4}(mS)**		3.2

Length of all transistors is 0.06 µm

LNA.A consumes 25mW from a 2.5V supply and LNA.B dissipates 17mW from 2.5V/1.8V supplies. Figure 4 shows the gain, noise factor and the S11 parameter of the two LNAs. The two circuits achieve almost same NF, close or less than 3dB, however, the gain of LNA.B is higher. That implies that LNA.B requires higher gain to suppress the noise as discussed in Section I. In addition, good input matching (<11dB) is obtained by both the LNA topologies. Table II compares the overall performance of the Balun-LNAs in this paper with the state-of-art in 65nm CMOS, showing feasibility of the configurations.

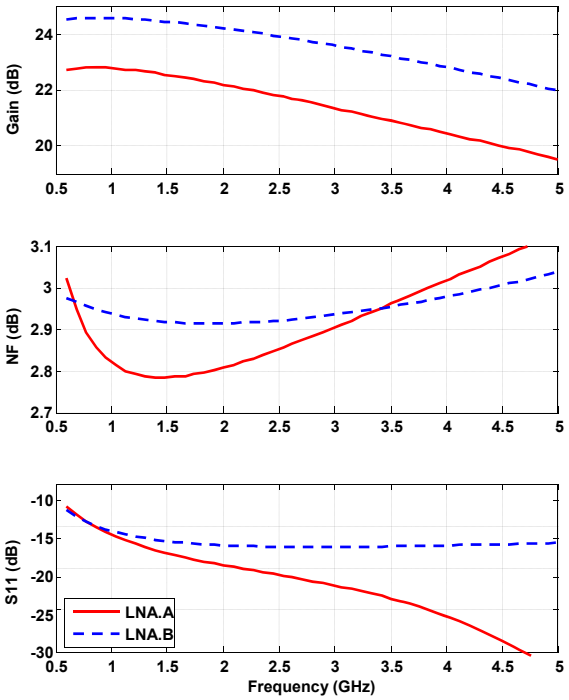

Figure 4. Simulation Results of two LNAs

TABLE II. Comparison of Balun-LNAs in 65nm CMOS

	LNA,A*	LNA.B	[3]	[4] (sim)	[6]
Band (GHz)	0.6-5	0.6-5	0.2-5.2	0.17-1.7	0.05-10
Gain (dB)	24.5	22.8	13-16	25.6	24-25
NF (dB)	<3.1	<3.1	<3.5	2.5	2.7-3.6
Input Matching	Matched	Matched	Matched	Matched	Matched
IIP2 (dB)	31	41.8	>20	44.8	32.4 (max)
IIP3 (dB)	-2.1	5.1	>0	5.6	-2 (max)
Power (mW)	25	17	14	11.6	21.7

*For both 90µm and 250µm width transistor configurations

Two sinusoidal tones located at 2.4 / 2.41GHz are taken to simulate the linearity of the circuits. LNA.A achieves 31dB for IIP2 and -2.1dB for IIP3. And its counterpart, which benefits from the equal sized and biased transistors as well as the current-balancing scheme, shows 41.84dB and 5.1dB for IIP2 and IIP3, respectively.

In order to test the IIP2 sensitivity against components mismatches, the circuits are simulated by Monte Carlo analysis. We present in Figure 5 the IIP2 result of a 200 points of mismatch only Monte Carlo simulation of LNA.A with dimension of 90/0.06µm CS transistor which is biased by a fixed voltage. The average IIP2 of this circuit is 28.3dB, however, Only 83.5% of the IIP2 are greater than 25dB, implying the IIP2 is very sensitive to components mismatches. Figure 6 shows the stability of IIP2 is improved

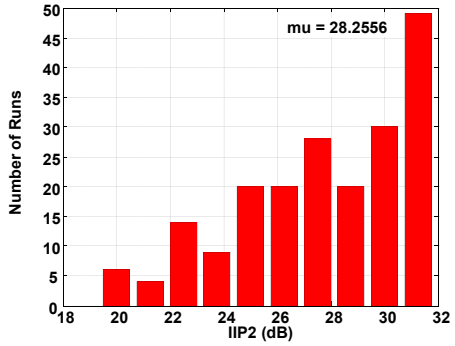

Figure 5. Monte Carlo Simulation of IIP2, LNA.A, W2=90µm

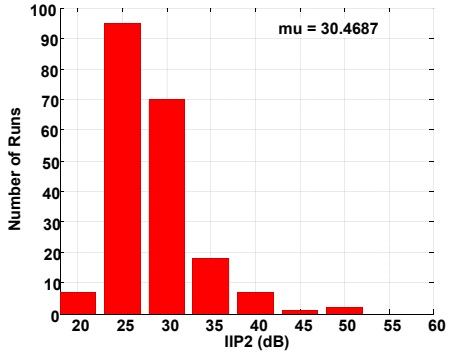

Figure 6. Monte Carlo Simulation of IIP2, LNA.A, W2=250µm

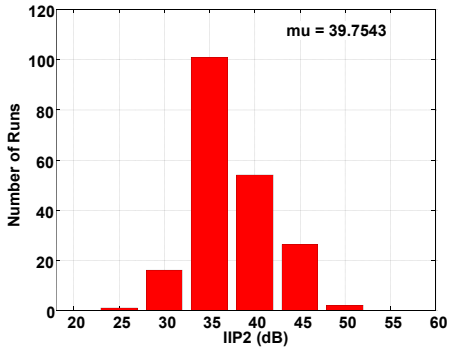

Figure 7. Monte Carlo Simulation of IIP2, LNA.B

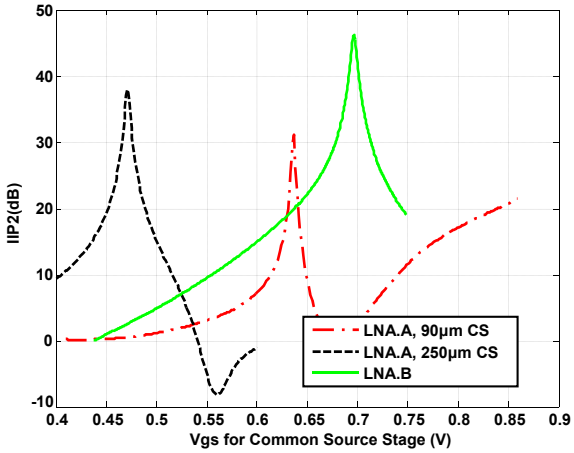

Figure 8. V_{gs} VS IIP2

by replacing the CS transistor by a larger one (250/0.06µm). The IIP2 greater than 25dB account for 96% of total runs. This is because mismatch is always an absolute value, not a percentage of parameters of components. So a large transistor is less sensitive to mismatches than a small one. According to the equation

$$I_d = \frac{K}{2} \cdot \frac{W}{L} \cdot {V_{ov}}^2 \tag{9}$$

, the mismatch on W causes a small change on I_d, and then results in imbalance at outputs, thus deteriorating the linearity. Consequently, the 250µm transistor has less mismatch, leading to stable IIP2.The LNA.B, which benefits from the DCB, provides stable IIP2 even though the dimension of transistors is small, as shown in Figure 7. The IIP2 greater than 35dB occupy 92.5% among total runs.

Another way to emulate the effects of matching is to vary the bias voltage of the CS stage. Figure 8 compares the simulated IIP2 sensitivity with respect to Vgs of CS stages. It can be seen that the LNA.B has the widest window of IIP2, verifying that the DCB does help to improve the IIP2 as well as the stability.

IV. Conclusion

The gain-boosting current-balancing Balun-LNA with equal g_m and DCB provides better IP2 performance, both IIP2 and stability, with small transistors, but suffers the problem of noise factor due to the noise from CS stage. The unequal g_m topology has better noise performance but with very unstable IIP2 if CS transistor is not big enough. To get stable IIP2, large transistors are required but that calls for more area. In addition, it consumes more power than the equal- g_m LNA.

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