Digital Design Flow Techniques and Circuit Design for Thin-Film Transistors

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Digital Design Flow Techniques and Circuit Design for Thin-Film Transistors

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Abstract

Thin-Film Transistor (TFT) technology refers to process and manufacture transistors, circuits, Integrated circuits (ICs) using thin-film organic or metal-oxide semiconductors on different substrates, such as flexible plastic foils and rigid glass substrates.

TFT technology is attractive and used for applications requiring flexible, ultra-thin ICs to enable seamless integration into devices. TFT technology shows great potential to be an enabling technology for Internet of Things (IoT) applications. TFT is currently used and a dominant technology for switching circuits in flat-panel displays and are the main candidates for IoT applications in the near future because of its flexible structure, low cost. It is possible to design different kinds of Application-specific integrated circuits (ASIC) with flexible TFTs.

Logic gates are considered as the basic building blocks of a digital circuit. An Integrated circuit (IC) is built from a standard cell library that consists of simple and complex logic gates. In this thesis, using TFTs, a variety of standard cell libraries are built using different logic styles. The designed standard cell libraries are compared with respect to parameters like performance, power and area. A digital ASIC design flow is a crucial and important for any System on Chip (SoC) implementation. The designed libraries are prepared for digital design flow such as synthesis, place and route and sign-off analysis to utilize the benefits of existing automated Electronic design automation (EDA) tools. This research was carried out at Imec. TFT technology transistors were used to design the circuits, standard cells and ICs presented in the thesis.

Popular Science Summary

TFT is currently the dominant technology used for switching circuits or switches in an active matrix of flat-panel displays. The key advantages of TFT technologies compared to traditional silicon Complementary Metal-Oxide Semiconductor (CMOS) transistors are that they can be manufactured at low-cost on and low processing temperatures, which allows it to be integrated onto a flexible substrate. Metal-oxide TFT are available only as N-type transistors, since they do not have P-type transistors, the cost of manufacturing goes down.

There is an increase in demand to manufacture ICs; the three critical factors which influence the IC industry are power consumption, speed of operation and how small is the IC. Due to this high demand in the competitive market, there is a rise to another parameter known as schedule, which is time to manufacture an IC is very short. The quicker the design is completed helps the companies to seize the market with more opportunities. Designing an IC takes considerable time, the design flow of an IC needs to be accelerated. The increased advancements in the IC industry has increased the complexity of designing an IC. The design flow plays a crucial role in the design process. However, if the design flow is not optimum, the design cycle might take a huge time. Besides, during the design of an IC, it needs to be optimized several times before manufacturing. Therefore long and non-optimum design flow would increase the design lifetime and impacts the schedule parameter.

Anybody who wants to design integrated circuits needs a methodology to navigate the complex design process. This methodology is usually called Design Flow. Hence this thesis uses TFT technology to not only to design digital circuits in transistor level but also to characterize and to have an entire digital design flow to design a larger IC.

Acknowledgements

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List of Abbreviations

a-Si Amorphous silicon

a-IGZO Amorphous Indium-Gallium-Zinc-Oxide

ALU Arithmetic-logic unit

ASIC Application-specific integrated circuits

CCS Composite Current Source

CMOS Complementary Metal-Oxide Semiconductor

DFL-1 Differential-1

DFL-2 Differential-2

DLL Diode-Load Logic

DRC Design Rule Check

DUGA Dual-Gate Self-Aligned

ECSM Effective Current Source Model

EDA Electronic design automation

GDS II Graphic Data System II

HDL Hardware description language

IC Integrated circuit

ICs Integrated circuits

IGZO Indium-Gallium-Zinc-Oxide

IoT Internet of Things

LEF Library Exchange Format

LIB Liberty Timing File

LTPS Low-temperature polycrystalline silicon

LVS Layout vs schematics

NFC Near Field Communication

NLDM Non-Linear Delay Model

PNR Place and Route

PSC Pseudo-CMOS

QOR Quality of results

RTL Register-transfer level

SDC Synopsys Design Constraints

SDF Standard delay format

SoC System on Chip

SPEF Standard Parasitic Exchange Format

TFT Thin-Film Transistor

VLSI Very large scale integration

ZVGS Zero-VGS

Chapter 1
Introduction

Thin-Film electronics is a technology that is used to make transistors and circuits using thin-film organic or metal-oxide semiconductors on flexible plastic foil substrates. The electronic properties and functionality in flexible ICs are retained even if they are folded and rolled.

1.1 Thesis Motivation

TFT technologies have considerable potential for fabrication on ultrathin stretchable substrates [4] that can be made porous to create breathable devices for contact with skin. With these features, thin-film ICs could be used in wearable electronics.

TFT technologies are extremely cost-effective, owing to the simple process flow (less number of lithographical steps compared with silicon CMOS) and material choices. Implementing a complementary technology flow is more complex than fabricating a unipolar transistor technology. Unipolar logic gates are the main candidates for realizing flexible ICs in TFT technologies that do not have a complementary counterpart (P-Type). Currently, thin-film ICs are area-inefficient due to non-optimized design flows, the transistor architectures and standard cell architectures have not been optimized for ICs.

TFT technologies are expected to improve parameters such as charge carrier mobility, variability and bias instability. Higher mobilities will enable logic gate optimization in terms of speed, area or a combination of both. Power density will have immense importance in the future, as circuits tend to evolve into more complex chips, yielding more functionality and transistors in a similar area. On a system level, low power is a concern to enhance battery life. Topologies for low power need to address this and find a way to reduce the static power consumption, which is one of the main challenges of unipolar logic gates.

1.2 Aim and Challenges Of Thesis

The basic building blocks of complex digital circuits are logic gates and require specific optimization depending on the process technology. A complex digital integrated chip is built from a standard cell library containing a multitude of simple and complex logic gates. The development and optimization of transistor technologies are driven by the critical figures of merit such as power, performance and area [5]. The most optimal configuration is CMOS, which profits from not only the co-existence of P-Type and N-Type transistors but also, all the circuit techniques developed for conventional silicon CMOS. In this thesis, the TFT library is uni-polar, which means the library has only N-type transistors. A fundamental problem of uni-polar (N-Type only transistor) logic gates is their static power consumption and reduced robustness.

The common practice in the field of flexible electronics is to use a transistor level approach to design circuits. It is necessary to simulate the schematic entry with an analog circuit-level simulator. Analog circuit simulators are not adapted to deal with a high level of complex design due to a large number of switching gates and input/output signals. Transistor level simulation (analog simulations) delivers the highest simulation accuracy. However, it also is the slowest circuit simulation method, not a very effective method for complex digital circuits. It is, therefore, only viable for smaller designs. The best architecture for designing a library of thin-film transistor cells is chosen by performing DC and transient analysis [6] using simulation tools. The parameters such as performance (noise margins, delay, rise and fall time, sensitivity to threshold voltage), power (static, dynamic) and the area will be the main characteristics we use to determine best performing architectures.

As there are only N-type transistors, the static power consumption of the circuits becomes one of the main concerns. Therefore one of the main challenges is to come up with standard cell topologies with low power consumption and reduce the power [7] at the circuit level. The second challenge can be considered as creating a digital design flow environment (library files, synthesis, place and route tools) taking thin-film transistor design rules and parameters into account. To design integrated circuits, a methodology is needed to navigate the complex design process. This methodology is usually called Design Flow. Design flow is a set of rules and guidelines on how to proceed from a specification towards the final IC implementation. The aim is to have a digital ASIC flow for the TFT libraries similar to that we have in the silicon CMOS libraries is implemented.

This thesis focuses on building a library using novel logic styles based on unipolar technologies that actively compensate for the shortcomings of regular unipolar logic gates, without needing to add the complementary transistor type and consequently, avoiding a more complicated process flow. Another focus of the thesis is to have a digital design flow (synthesis, place and route) for thin-film technology to exploit all the benefits of existing automated EDA tools.

1.3 Thesis Outline

The rest of the thesis is organized as follows:

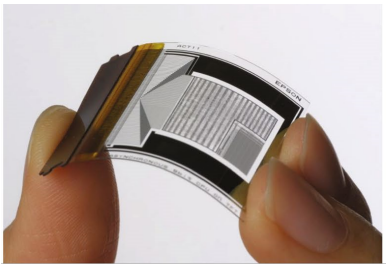
- **Chapter 2: Thin-Film Transistor Technology**: This Chapter introduces the TFT technology and some basic simulations related to it.
- **Chapter 3: Circuits Using Thin-Film Transistor Technology**: In this Chapter, different standard cell topology architectures and all the relevant simulations are discussed.
- **Chapter 4: Digital Design Flow**: A digital design flow for IC implementation using TFTs is discussed in this Chapter.
- **Chapter 5: Design Cases, Simulations and Analysis**: In this Chapter a system is designed and IC is implemented using the digital design flow and all relevant implementation results are discussed.
- **Chapter 6: Conclusion and Future work**: A conclusion is drawn and discusses the future work of this thesis.

Chapter 2

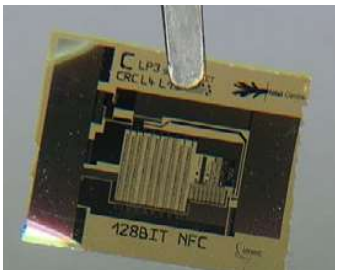
Thin-Film Transistor Technology

In this chapter, thin-film semiconductors that are used to implement thin-film transistors are discussed. The reasons for using thin-film technologies are discussed. Device architecture of TFTs used in this thesis is discussed in detail and some essential simulations related to TFT are discussed.

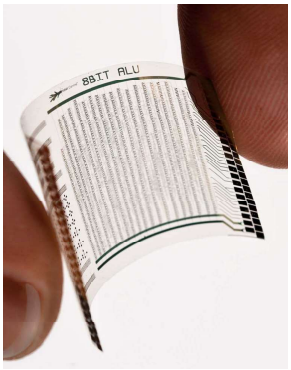
TFT is implemented as a backplane technology for displays and is currently the dominant technology for switching circuits in flat-panel displays and are the main candidates for IoT applications in the near future because of its flexible structure, low cost and high uniformity.



(a) TFT-based microprocessor [8]



(b) TFT-based NFC tag [8]



(c) TFT-based ALU [9]

Figure 2.1: Implemented designs using TFT

It is possible to design many kinds of ASIC with flexible TFTs. As shown in Figure 2.1, a flexible TFT-based microprocessor [8], Arithmetic-logic unit (ALU) [8] and Near Field Communication (NFC) tag [8], are some examples of such state-of-the-art work which are published. This technology can also be used in logic under a flexible display [10]. TFT technology is attractive for IoT applications requiring ultra-thin, flexible integrated circuits.

Using thin-film transistors have some advantages compared to single-crystalline silicon CMOS transistors, such as manufacturing on large substrates at a low cost per unit area, at low processing temperatures [3] and being able to integrated onto a variety of flexible substrates. In TFT technology field, there are two routes to improve maturity (technology) and circuit complexity (design) [11]: Scaling, new process techniques, higher mobility materials and others can be categorized as technological improvements [11]. Correspondingly, new design techniques [12] and tools are used to design integrated circuits with high performance, robustness and power efficiency.

2.1 Thin-film Semiconductors

TFT technology use substrates such as flexible plastic foils and semiconductor materials such as Amorphous silicon (a-Si), Low-temperature polycrystalline silicon (LTPS) and amorphous metal-oxide semiconductors.

At present, the TFT technologies available are a-Si, LTPS and amorphous metal-oxide semiconductors [3], mainly Indium-Gallium-Zinc-Oxide (IGZO). A comparison of the three most common TFT technologies is shown in Figure 2.2 (left part shows the availability of N-Type and P-type transistors and the right part compares parameters such as temperature budget for fabrication, mask steps required, stability for manufacturing of the available technologies).

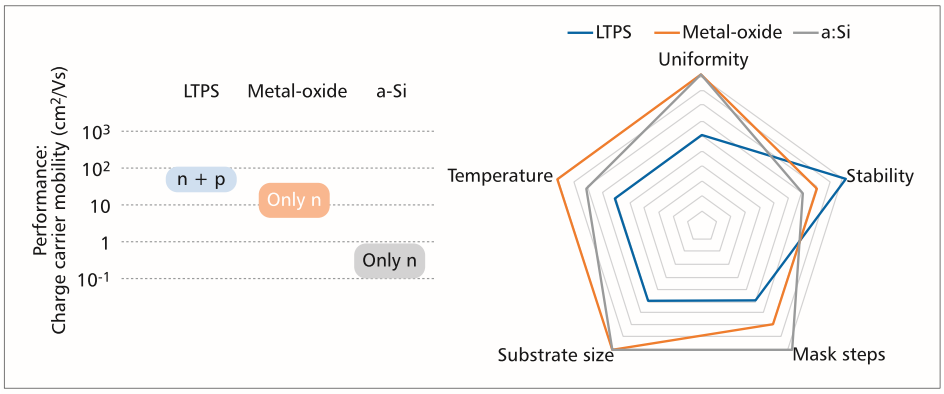


Figure 2.2: Comparison of the three most common TFT technologies [1]

Metal-oxide TFT is an N-Type only technology for flexible ICs. It can be manufactured at process temperatures within the thermal budget of flexible substrates [13].

P-Type and N-type TFT can be realized in LTPS, but they require larger processing temperatures and a more complex fabrication process flow.

In amorphous metal-oxide semiconductors, mainly IGZO only N-Type TFT can be realized. Also, the amorphous nature of IGZO as a semiconductor [13] provides a TFT scaling roadmap in which shorter gate length (channel) TFTs retain excellent performance characteristics, which is beneficial for flexible ICs applications. Amorphous metal-oxide semiconductor TFT, mailnly Amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) are widely used as a potential candidate for flexible ICs to implement N-Type metal-oxide TFTs, because P-Type metal-oxides matching the performance of amorphous metal-oxide semiconductor (IGZO) have not yet been discovered.

The comparison of process complexity and manufacturing cost of the available TFT technology is shown in Table 2.1. LTPS has higher manufacturing cost than a-Si and amorphous metal-oxide semiconductors because in this technology, there are both P-Type and N-type transistors available hence requiring more fabrication steps, masks and higher process temperatures. Therefore the process complexity also increases. The threshold voltage of the transistors built using a-Si, LTPS and amorphous metal-oxide semiconductors can be different or varied because of either intrinsic device properties such as doping, channel length, active material or because of the presence of a back-gate to control the channel properties. This thesis uses a-IGZO transistors.

Table 2.1: Table showing comparison of the three most common TFT technologies [3]

Parameter	LTPS	Metal-oxide	a-Si
Process complexity	High	Low	Moderate
Manufacturing cost	High	Low	Moderate
Mobility	High	Moderate/High	poor
Transistor Type	P-Type and N-Type	N-Type	N-Type

2.2 Thin-Film Transistor Device Architecture

After the selection of the semiconductor material, a device structure that consists of a stack of semiconductor layers, insulators and metal layers needs to be designed. The device structure used in this thesis is DUGA TFT. The name DUGA because it has dual (two) gates, which are gate and back-gate.

The layout view of a DUGA TFT is shown in Figure 2.3. The layout view shows the source and drain regions of the TFT. It also shows the area of the gate and back-gate terminals in the TFT.

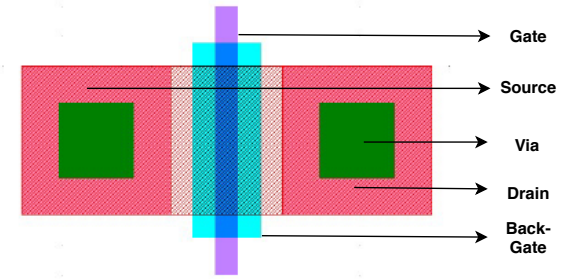


Figure 2.3: Layout and top View of a DUGA TFT

The side view and structure of a DUGA TFT is shown in Figure 2.4. In this structure, the back-gate metal and back-gate dielectric are deposited and patterned before the active material a-IGZO is deposited. Then the gate oxide, gate metal, dielectric, source and drain metals are patterned and deposited.

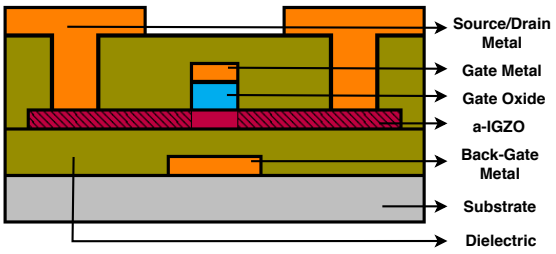
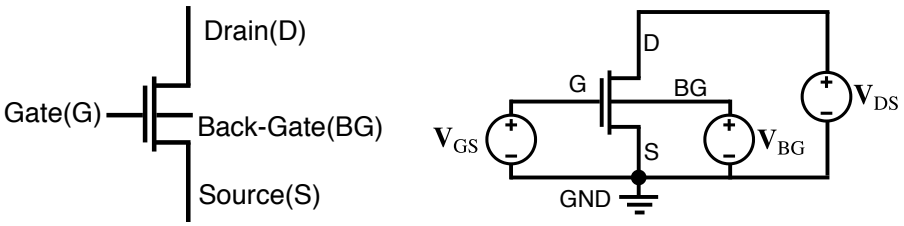


Figure 2.4: Structure and side view of a DUGA TFT [2]

2.3 N-Type TFT and Simulations

The circuit symbol of N-type DUGA TFT is shown in Figure 2.5a. It consists of four terminals: drain (D), source (S), gate (G) and back gate (BG). The source and drain terminals are interchangeable. The terminals are similar to that of traditional CMOS transistor.

The schematic setup of a DUGA TFT for simulation is shown in Figure 2.5b. There are three voltage sources V_{GS}, V_{DS} and V_{BG} which control the flow of current (electrons) in the TFT.

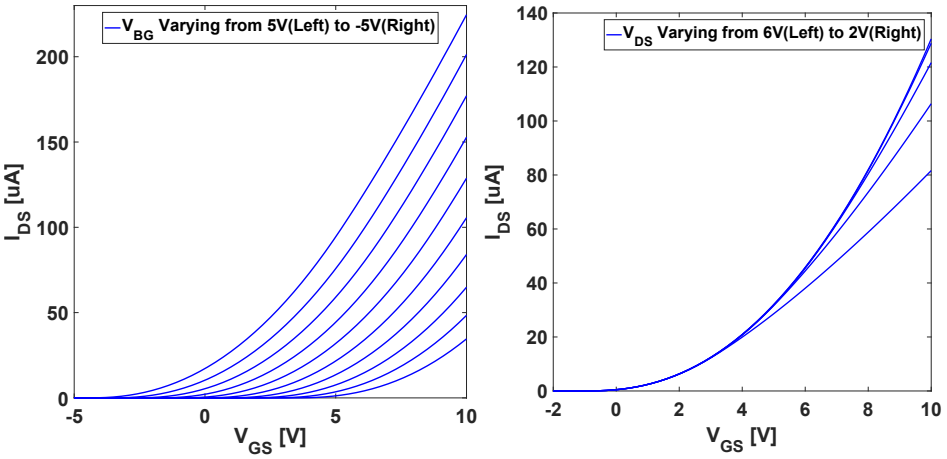


(a) N-Type DUGA TFT **(b)** Schematic of a DUGA TFT

Figure 2.5: Terminals and simulation configuration of a DUGA TFT

The transistor size for the simulations is W/L = 10 μm/1.5 μm, this is the minimum size of the TFT. The N-type TFT threshold voltage is -0.933V, which means it is a depletion mode transistor. So, to turn off a transistor a negative gate-source voltage is needed or a negative back-gate voltage should be applied. The I_{DS} - V_{GS} characteristics of a N-type TFT is shown in Figure 2.6.

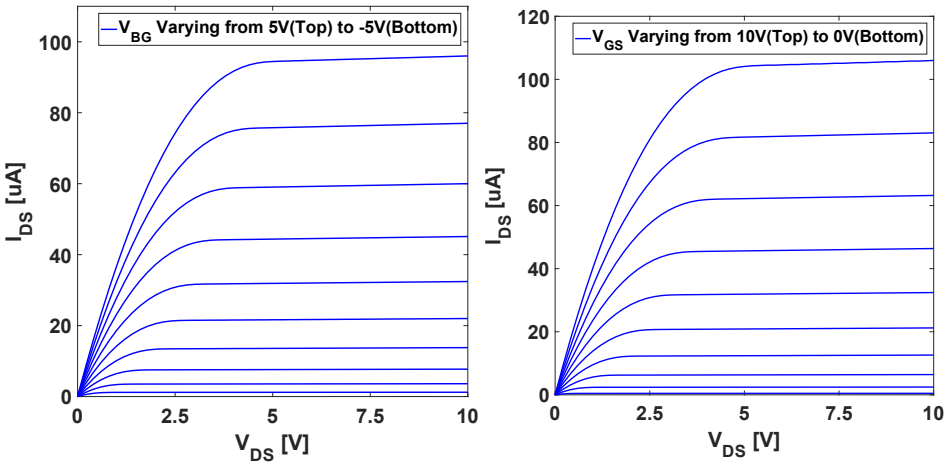
Figure 2.6a shows I_{DS} - V_{GS} characteristics of an N-type TFT at 5V V_{DS} which is the supply voltage. We see as the back-gate voltage decreases from 5V to -5V, the performance of TFT in terms of switching response decreases due to decreased current values. Figure 2.6b shows I_{DS} - V_{GS} characteristics of an N-type TFT for varying V_{DS} voltages and fixed back-gate voltage at 0V. We see a higher current values for higher V_{DS} voltages.



(a) I_{DS} - V_{GS} characteristics V_{DS} at 5V **(b)** I_{DS} - V_{GS} characteristics V_{BG} at 0V

Figure 2.6: I_{DS} - V_{GS} characteristics of a TFT

The I_{DS} - V_{DS} characteristics of an N-Type TFT is shown in Figure 2.7. Figure 2.7a shows I_{DS} - V_{DS} characteristics of an N-type TFT at 5V V_{GS}. We see the values of current are higher for more positive back-gate voltage and the current value decreases as the back-gate voltage is decreased. Figure 2.7b shows I_{DS} - V_{DS} characteristics of a N-type TFT for varying V_{GS} voltages and fixed back-gate voltage at 0V. The value of current is higher at higher V_{GS} voltages.



(a) I_{DS} - V_{DS} characteristics V_{GS} at 5V **(b)** I_{DS} - V_{DS} characteristics V_{BG} at 0V

Figure 2.7: I_{DS} - V_{DS} characteristics of a TFT

The effect of back-gate voltage on threshold voltage (Vt or Von) is shown in Figure 2.8. A negative voltage on back-gate increases the threshold voltage and a positive voltage on back-gate decreases the threshold voltage of a N-Type TFT. As threshold voltage decreases, the performance increases and power consumption also increases. As the threshold voltage increases, the performance decreases and power consumption also decreases. Hence the back-gate voltage is used to tune the performance and power consumption of a transistor. Figure 2.9 shows the impact of back-gate voltage on leakage current, as the back-gate voltage becomes more positive, it decreases the threshold voltage and hence a higher leakage current.

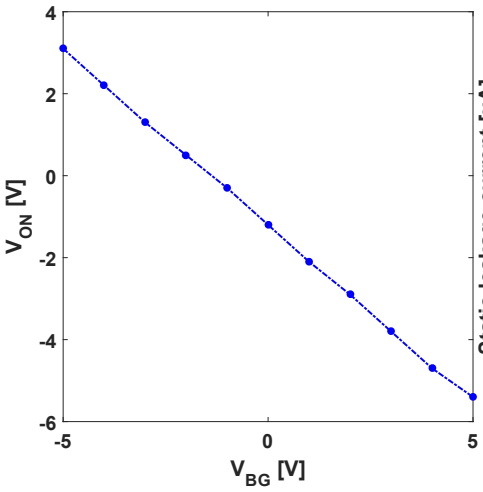


Figure 2.8: V_{ON} - V_{BG} characteristics of a TFT

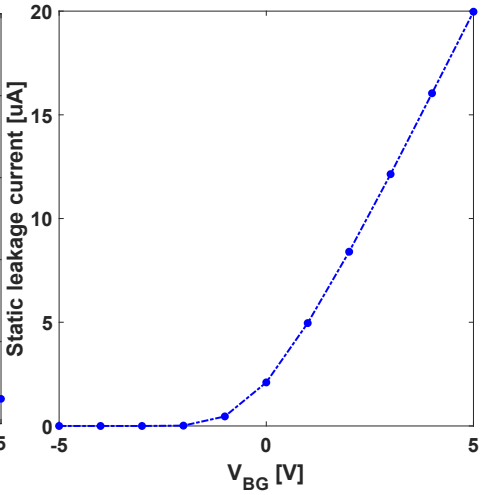


Figure 2.9: Leakage current - V_{BG} characteristics of a TFT

Chapter 3

Circuits Using Thin-Film Transistor Technology

In this chapter, using the TFT discussed in Chapter 2, standard cell schematics are designed based on different topologies and the trade-off between each topology is discussed using the simulation results. Once the schematics of standard cells are completed layouts of these standard cells is drawn. These standard cells are compared based on power consumption, performance and area using transient and DC analysis.

3.1 General Digital Circuit Architecture

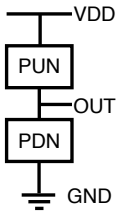


Figure 3.1: A generic configuration of circuit architecture

A general digital circuit architecture is shown in Figure 3.1. The circuit consists of a pull-up network that is responsible for pulling the output to logic high (VDD) and pull down network, which is responsible for pulling the output to logic low (GND). The pull up and pull down networks are complementary to each other. Which means when pull up network is enabled pull-down network is disabled and vice-versa.

The main issue with respect to TFT circuit design is large static power consumption due to negative threshold voltage of transistors and availability of only N-Type TFT. The challenge is to design circuits that consume low power to enhance battery life. The high power consumption is due to lack of P-Type TFT (complementary TFT), since metal-oxide semiconductor used to realize TFTs uses only N-Type TFTs. So all digital circuits must be designed using only N-type TFT.

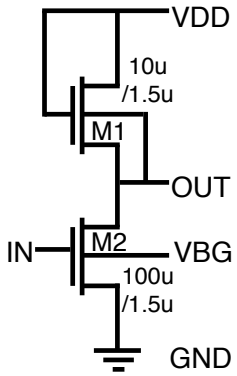
3.2 Digital Circuit Topologies

Different circuit topologies, architectures and working principle of circuits are discussed in this Section and all the corresponding simulations and transistor sizing are discussed in Section 3.3.

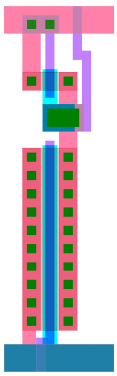
3.2.1 Diode-load logic topology

A Diode-Load Logic (DLL) inverter is shown in Figure 3.2a. M1 and M2 are N-Type TFT. Transistor M1 is always-on transistor since the gate is connected to VDD and hence the name diode-load logic. When the input is low, transistor M2 is off and output is pulled to VDD by transistor M1. When the input is high, both transistors are switched on and the output is pulled to GND depending on the strength of transistor M2. The corresponding layout is shown in Figure 3.2b.

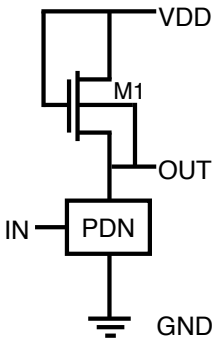
A generic DLL architecture is shown in Figure 3.2c. The pull-up network consists of an always-on transistor and a pull-down network consists of the logic function that needs to be implemented; the output of the circuit depends on the pull-down logic. This topology consumes much leakage power due to always on M1 transistor. It uses less number of transistors at the cost of lower performance.



(a) Sized Diode-Load logic inverter



(b) Layout of Diode-Load logic inverter



(c) A generic Diode-Load logic architecture

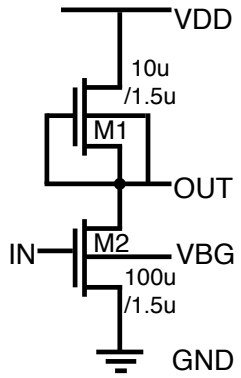
Figure 3.2: A Diode-Load logic topology

3.2.2 Zero-Vgs topology

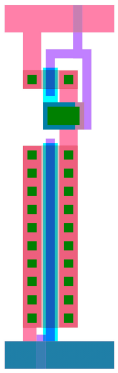
A Zero-VGS (ZVGS) inverter is shown in Figure 3.3a. M1 and M2 are N-Type TFT. Transistor M1 is always-on transistor since the gate and source are shorted together and hence the name Zero-Vgs.

When the input is low, transistor M2 is off and output is pulled to VDD by transistor M1. When the input is high, both transistors are switched on and the output is pulled to GND depending on the strength of transistor M2. The corresponding layout is shown in Figure 3.3b.

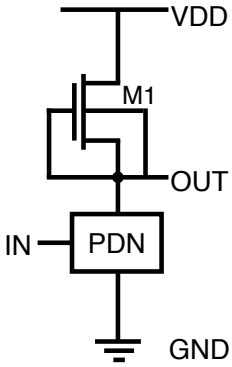
A generic ZVGS architecture is shown in Figure 3.3c. The pull-up network consists of an always-on transistor and a pull-down network consists of the logic function that needs to be implemented; the output of the circuit depends on the pull-down logic. This topology makes use of less number of transistors at the cost of lower performance and high power consumption due to always on transistor M1. This topology works only for negative threshold voltage transistors since gate and source are shorted ($V_{gs} > V_t$ i.e $0 > -V_t$).



(a) Sized Zero-Vgs inverter



(b) Layout of Zero-Vgs inverter



(c) A generic Zero-Vgs architecture

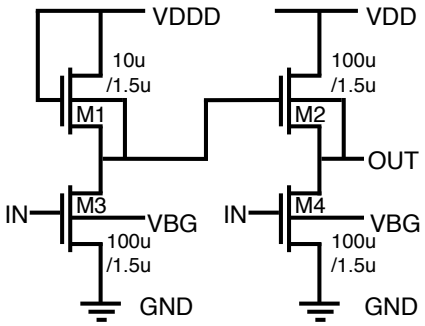
Figure 3.3: A Zero-Vgs topology

3.2.3 Pseudo-CMOS topology

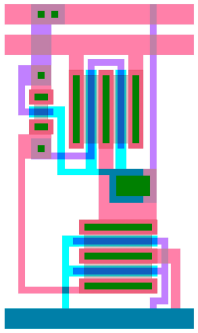
A Pseudo-CMOS (PSC) inverter is shown in Figure 3.4a. M1, M2, M3, M4 are N-Type TFT. Transistor M1 is always-on transistor since the gate is connected to VDD. The first stage is similar to that of DLL; the output of this stage drives the transistor M2. So the signals driving transistors M2 and M4 are complementary signals. When the input is low, M3 and M4 transistors are off and output is pulled to VDD by transistor M2 and with the help of transistor M1. When the input is high, M1 and M3 transistors are switched on and the output is pulled to GND depending on the strength of transistor M3 and with the help of transistor M4. The corresponding layout is shown in Figure 3.4b.

A generic PSC architecture is shown in Figure 3.4c. The first stage is similar to that of DLL. The pull-up network of the first stage consists of an always-on M1 transistor and the second stage consists of M2 transistor whose gate is driven by the output of the first stage. The pull-down network consists of the logic function that needs to be implemented; the output of the circuit depends on the pull-down logic.

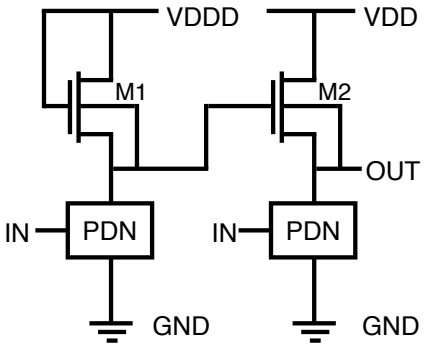
This topology has high robustness and speed but at the cost of higher area due to an increase in the number of transistors and higher power consumption.



(a) Sized Pseudo-CMOS inverter



(b) Layout of Pseudo-CMOS inverter

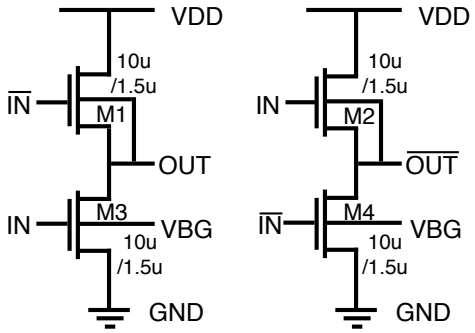


(c) A generic Pseudo-CMOS architecture

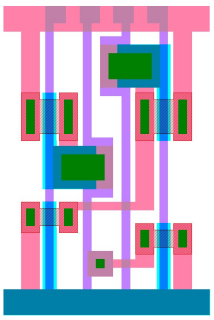
Figure 3.4: A Pseudo-CMOS topology

3.2.4 Differential-1 topology

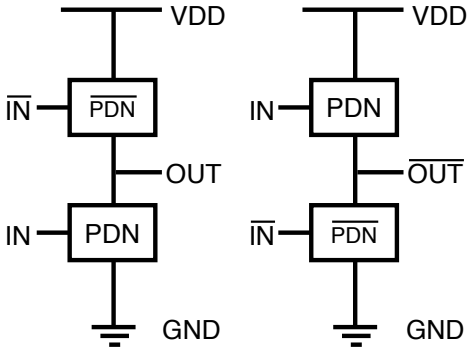
A Differential-1 (DFL-1) inverter is shown in Figure 3.5a. M1, M2, M3, M4 are N-Type TFT. The input signals driving transistors M1, M3 and M2, M4 are complementary signals. The circuit generates output and its complementary. When the input is low, M3 and M2 transistors are off and output is pulled to VDD by transistor M1 and complementary output is pulled to GND by transistor M4. When the input is high, M1 and M4 transistors are off and output is pulled to GND by transistor M3 and complementary output is pulled to VDD by transistor M2. The corresponding layout is shown in Figure 3.5b.



(a) Sized Differential-1 inverter



(b) Layout of Differential-1 inverter



(c) A generic Differential-1 architecture

Figure 3.5: A Differential-1 topology

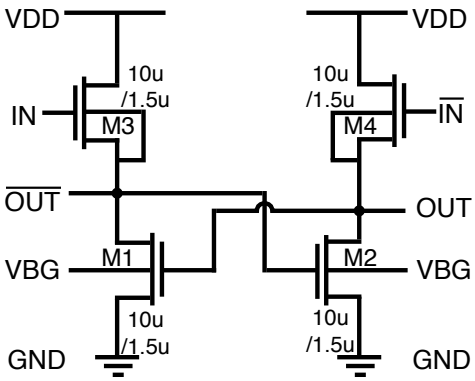
A generic DFL-1 architecture is shown in Figure 3.5c. The circuit is divided into two parts to generate the output and complementary output. In one part of the circuit, the pull-down network consists of the logic function that needs to be implemented; the pull-up network is complementary of pull-down network and the inputs to pull-up network are also complementary to that of pull-down network, which generates the output. In the other part of the circuit, the pull-up network consists of the logic function that needs to be implemented; the pull-down network is the complementary of pull-up network and the inputs to pull-down network are also complementary to that of pull-up network, which generates complementary

output. The output of the circuit depends on both pull-up and pull-down logic.

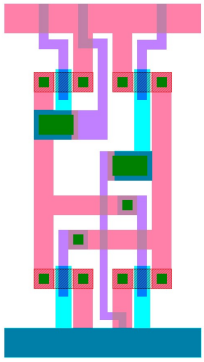
This topology has high robustness and speed but at the cost of higher area due to an increase in the number of transistors and routing. It consumes lower power since there is no direct path for the current to flow from VDD to GND.

3.2.5 Differential-2 topology

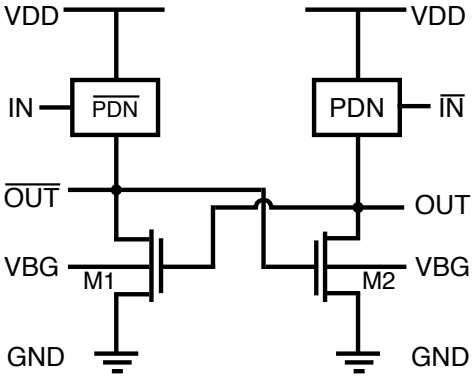
A Differential-2 (DFL-2) inverter is shown in Figure 3.6a. M1, M2, M3, M4 are N-Type TFT. In this topology, a feedback mechanism is used to switch on and off one part of the circuit. The input signals driving transistors M3 and M4 are complementary signals. The circuit generates output and its complementary.



(a) Sized Differential-2 inverter



(b) Layout of Differential-2 inverter



(c) A generic Differential-2 architecture

Figure 3.6: A Differential-2 topology

When the input is low, the complementary of input is high, transistor M4 is switched on and output is pulled high, which switches on transistor M1 so that the complementary output is discharged to GND, which in turn switches off transistor M2. During the whole process, transistor M3 is off. When the input is high, transistor M3 is switched on and complementary output is pulled high, which

switches on transistor M2 so that the output is discharged to GND, which in turn switches off transistor M1. During the whole process, transistor M4 is off. The corresponding layout is shown in Figure 3.6b.

A generic DFL-2 architecture is shown in Figure 3.6c. The circuit generates output and complementary output; this acts as a feedback to switch on and off one part of the circuit. Gate terminals of transistors M1 and M2 are driven by output and complementary output correspondingly. The pull-down logic whose input is driven by complementary inputs and complementary of pull-down logic whose inputs are driven by regular inputs. When output is logic high, which turns on transistor M1 and discharges complementary output to logic low, which in turn switches off transistor M2. When the complementary output is logic high, which turns on transistor M2 and discharges output to logic low, which in turn switches off transistor M2. The output of the circuit depends on the pull-down logic and its complementary logic used in the pull-up network.

This topology has high robustness and speed but at the cost of higher area due to an increase in the number of transistors and routing. It consumes lower static power since there is no direct path for the current to flow from VDD to GND.

A comparison of the layout area consumed in different topologies is shown in Table 3.1

Table 3.1: Table showing layout size of inverter in different topologies

Circuit Architecture/ configuration	**Area (Width x Height) (Size of Inverter)**	
Diode Load Logic (DLL)	60 x 200 μm^2	12000 μm^2
Pseudo-CMOS (PSC)	140 x 240 μm^2	33600 μm^2
Zero-Vgs (ZVGS)	60 x 200 μm^2	12000 μm^2
Differential-1 (DFL1)	120 x 180 μm^2	21600 μm^2
Differential-2 (DFL2)	100 x 180 μm^2	18000 μm^2

3.3 Simulations and Comparisons

To show the effectiveness of the circuits, detailed simulations and results of various circuit topologies are discussed in this Section.

3.3.1 Analyses

Before going into the detailed simulation results of different topologies, the summary of analyses which was carried out and the parameters related to the analyses are explained below and some of the parameters are shown in Figure 3.7.

1. DC analysis: The input for the circuit is swept from 0 to VDD and corresponding output is captured. Various parameters are extracted which are discussed as follows:

(a) Switching Threshold (V_m): Is the voltage at which the value of the input is equal to the value of output.

(b) Noise Margin High (N_{MH}) and Noise Margin Low (N_{ML}): For output to be valid logic high, the voltage should be between output high voltage (V_{OH}) and input high voltage (V_{IH}) which is measured in terms of Noise margin high ($N_{MH} = V_{OH} - V_{IH}$). For output to be valid logic low, the voltage should be between input low voltage (V_{IL}) and output low voltage(V_{OL}) which is measured in terms of Noise margin low ($N_{ML} = V_{IL} - V_{OL}$).

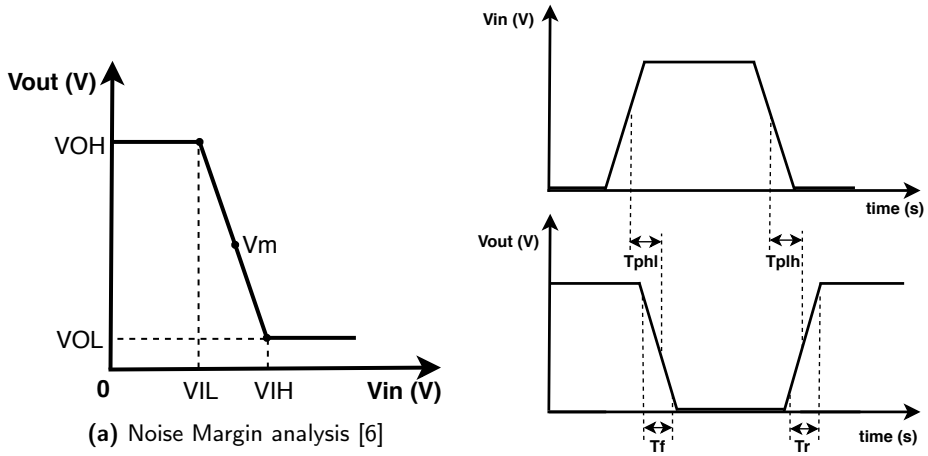
2. Transient analysis: A transient input is given to a circuit for a particular time period and the corresponding output is captured and various parameters are extracted which are discussed as follows:

(a) Rise Time (T_r) and Fall Time (T_f): Rise time is the time taken by output to rise from 10% to 90% of VDD. Fall time is the time taken by output to fall from 90% to 10% of VDD

(b) Propagation Delay (T_{pd}): It defines how quickly the output of circuit changes with respect to its inputs. T_{phl} defines the response time of a circuit for high to low output transition. Similarly, T_{plh} refers to a low to high transition. ($T_{pd} = (T_{phl} + T_{plh})/2$)

(c) Power: Total power consumed by the circuit is a combination of static (power consumed when outputs are stable and not switching) and dynamic power (power consumed during switching).
($P_{total} = P_{static} + P_{dynamic}$)

(d) Power Delay Product (PDP) and Energy Delay Product (EDP): PDP is the product of power and propagation delay. EDP is the product of PDP and time.



(a) Noise Margin analysis [6]

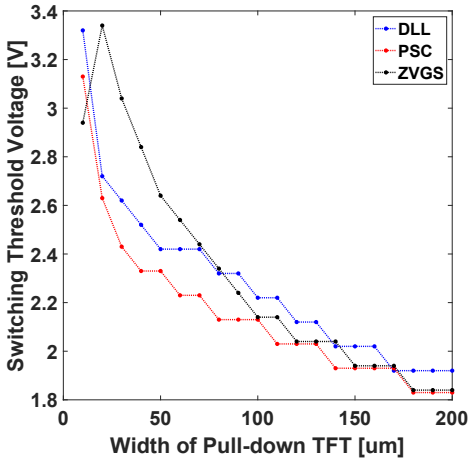
(b) Delay analysis [6]

Figure 3.7: Various parameter analysis and calculation

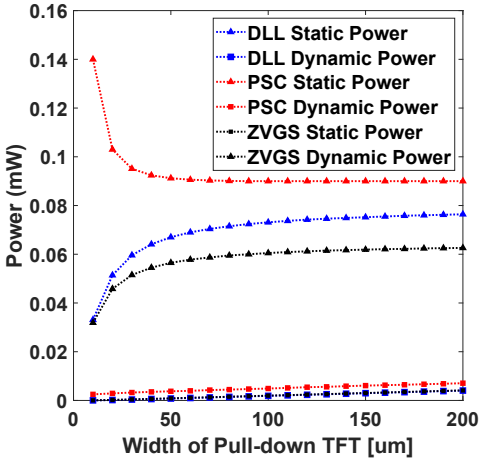
3.3.2 Simulation Results Of Topologies By Varying Width Of The TFT

Topologies explained in Section 3.2 such as DLL, PSC, ZVGS inverters have an always switched on transistor in their pull-up networks.

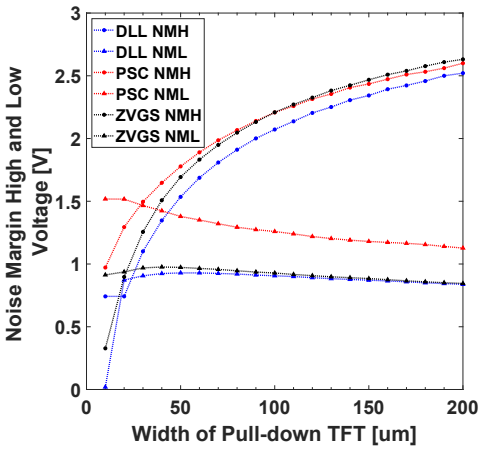
When a logic low input is given to these circuits, the pull-down network is switched off and the output is logic high because of the always-on pull-up transistor. When a logic high input is given to these circuits, both pull-down and pull-up network is active, which does not let the output functionality to depend on the pull-down logic implementation. Hence pull-down transistors should have higher strength than that of the pull-up network, which makes sure that the pull-down network overpowers the always-on pull-up transistor.



(a) Switching threshold (V_m)



(b) Total, static and dynamic power



(c) Noise margin low (N_{ML}) and Noise margin high (N_{MH})

Figure 3.8: Simulation analysis of DLL, PSC, ZVGS topologies by varying width of pull down TFT (VDD=5V)

The simulations of various DC parameters by varying the width of pull-down TFT from 10um (minimum size of transistor in the library) to 200um for topologies such as DLL, PSC, ZVGS is shown in Figure 3.8. The supply voltage (VDD) for these simulations is 5V.

The noise margin analysis by varying width of the pull-down transistor is shown in Figure 3.8c. It is observed that at a lower width, both N_{MH} and N_{ML} overlap, which is not good for circuit performance because a small spike or glitch could produce wrong logic value. As the width increases, the range between N_{MH} and N_{ML} increases, which is good for circuit performance in terms of robustness and noise propagation. The N_{MH} curves shift a lot because there is a huge difference in V_{OL} when the width increases which in turn effects V_{IH} .
In terms of equations:

$$VOH = VDD$$

$$VOL = \frac{R2 * VDD}{(R1 + R2)}$$

Where V_{OH} and V_{OL} are output high and output low voltage respectively.
V_{IH} and V_{IL} are input high and input low voltage respectively.
R2 and R1 are the resistance of pull-down and pull-up TFT respectively.

The switching threshold voltage values by varying width of the pull-down transistor are shown in Figure 3.8a. As the width of the pull-down transistor increases, the switching threshold value decreases due to noise margins and the values approximately approaches to VDD/2 = 2.5V, which are ideal values for circuits. The static and dynamic power by varying width of pull-down transistor is shown in Figure 3.8b. Due to the always-on transistor, the static power in the circuits is larger than that of dynamic power.

After analyzing the obtained results, it is evident that the sizes of pull-up and pull-down TFT in these circuits cannot be similar. The pull-down transistor size needs to be larger than that of the pull-up transistor. So a pull-up transistor of size 10um (minimum size) is chosen and from the results of noise margins and switching threshold, a pull-down transistor size of 100μm is chosen and circuits are designed. This is not the case in DFL-1 and DFL-2 topologies since they do not have always switched on transistor.

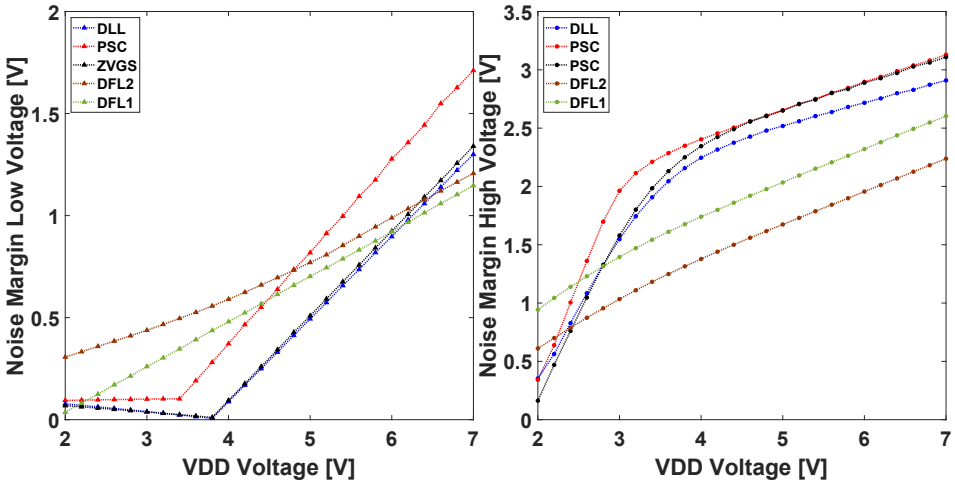
3.3.3 Simulation Results Of Topologies By Varying Supply Voltage

After the transistor sizes for each topology is decided and designed, now we can vary the supply voltage (VDD) and essential properties of different topologies are captured. The IGZO TFT can handle supply voltages varying from 2V to 7V, while 5V being a typical supply voltage value.

One of the critical parameters in digital circuits is robustness. The circuits should be robust to process variations or from noise interference. In uni-polar logic, robustness is an important parameter that should be considered. The robustness is measured in terms of noise margins and switching threshold.

The noise margin low and noise margin high values are shown in Figure 3.9a and 3.9b respectively by varying supply voltage. The switching threshold voltage values are shown in Figure 3.10, ideally the switching voltage values should be approximate and close to VDD/2. We observe that only DFL-1 and DFL-2

topologies are more stable or robust for all supply voltages ranging from 2V to 7V, mainly due to the absence of always-on transistor. Whereas topologies like DLL, PSC and ZVGS are robust for higher supply voltages greater than 4V at supply voltage values below this, these circuits cannot perform efficiently in terms of robustness because of always-on transistor.



(a) Noise margin low (N_{ML}) **(b)** Noise margin high (N_{MH})

Figure 3.9: Noise margin of different topologies at various VDD voltages

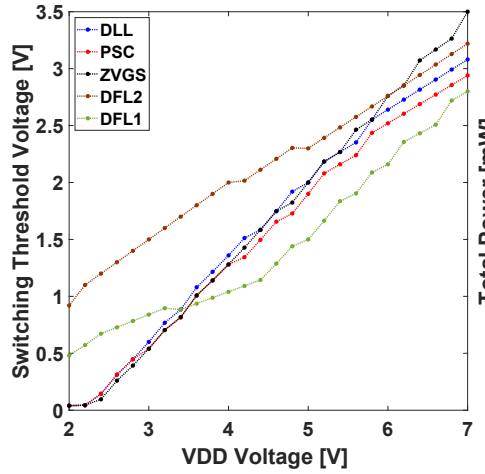


Figure 3.10: Switching threshold (V_m) of different topologies at various VDD voltages

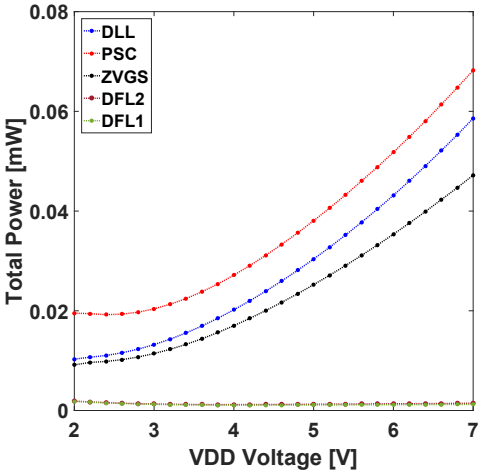
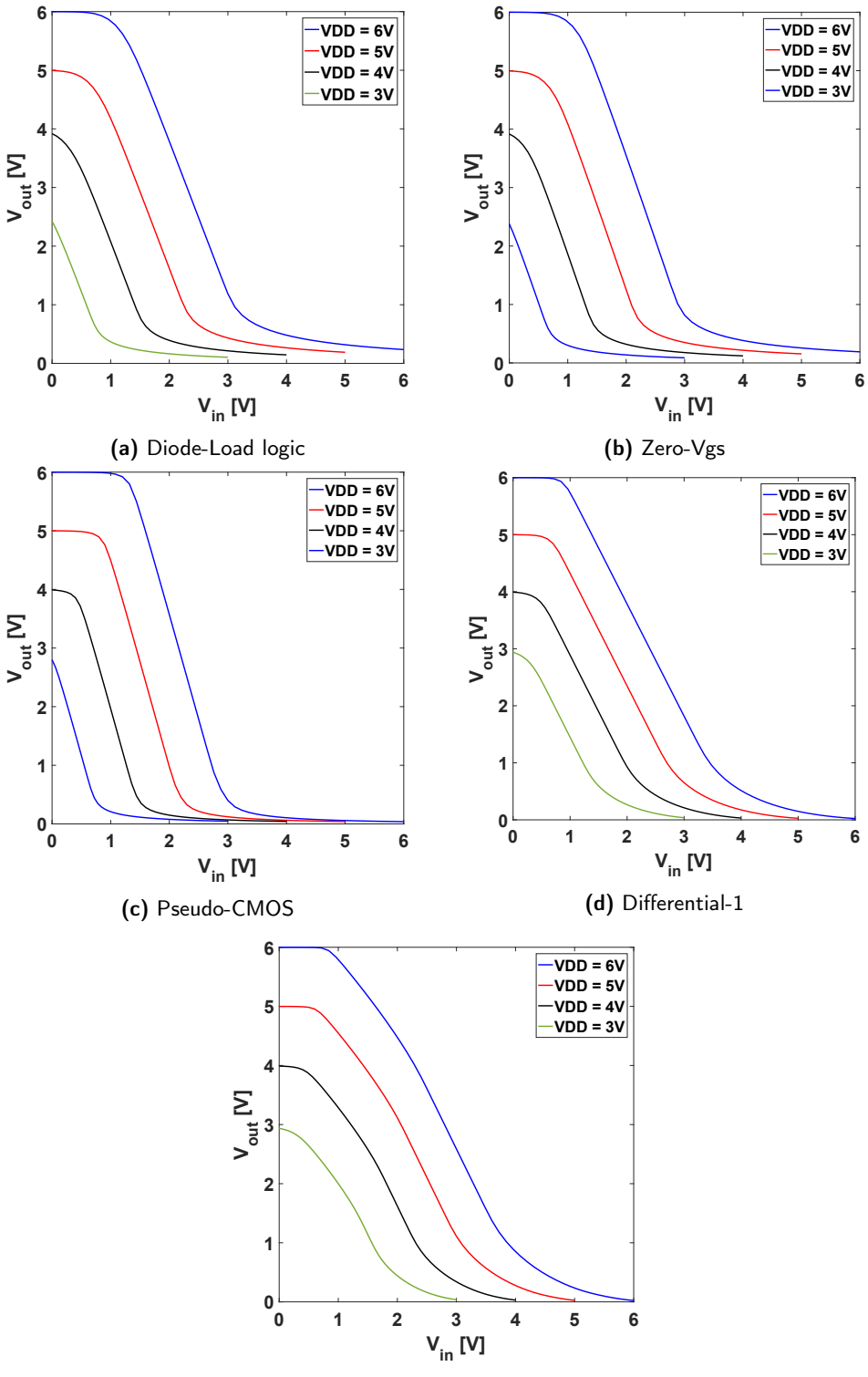


Figure 3.11: Total power of different topologies at various VDD voltages



(a) Diode-Load logic

(b) Zero-Vgs

(c) Pseudo-CMOS

(d) Differential-1

(e) Differential-2

Figure 3.12: Transfer Characteristics (Vin - Vout) of different topologies at various VDD voltages

Power consumption is another vital comparison parameter. The power component is divided into static power and dynamic. In uni-polar logic, static power is higher than dynamic power consumption. The total power values are shown in Figure 3.11. We see DFL-1 and DFL-2 topologies consumes much less power because they do not have a always on transistor as in ZVGS, DLL and PSC topologies. DFL-1 and DFL-2 operation is similar to that of traditional CMOS technology where only either pull-up or pull-down logic network is switched on at a given instant depending on the inputs.

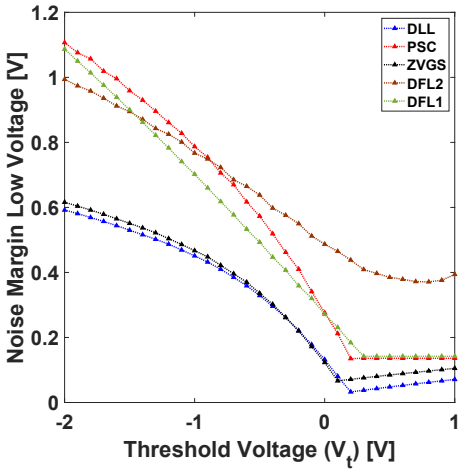
The transfer characteristics that is a plot of input voltage and output voltage of all the designed topologies are shown in Figure 3.12. All the DC parameters were extracted from these plots. It can be observed from the plots of DLL (Figure 3.12a) and ZVGS (Figure 3.12b) topologies that the output voltages can never reach to zero (0) volts because of the always-on transistor no matter how large the pull-down transistor is sized as compared to pull-up transistor. DLL, ZVGS and PSC (Figure 3.12c) do not perform well at low supply voltages especially below 4V. From the graph it is evident that at 3V supply voltage the output high voltage never reaches 3V. DFL-1 (Figure 3.12d) and DFL-2 (Figure 3.12e) perform well at lower supply voltages and still achieves a complete logic high and low voltages.

3.3.4 Variation: Sensitivity to the Threshold Voltage (V_t)

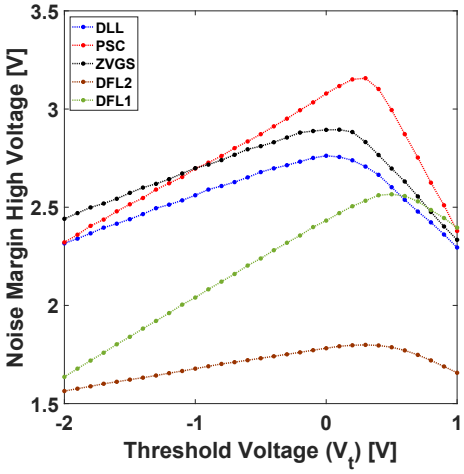
The sensitivity to variation in threshold voltage for different topologies is simulated and discussed here. This sensitivity analysis can only be performed in simulations by changing the threshold voltage of the transistor. The threshold voltage of the transistor can slightly vary during the fabrication process. TFT suffer from an unstable threshold voltage; the effect of variation can be studied and evaluated doing the simulations. The supply voltage (VDD) for these simulations is 5V.

All topologies are sensitive due to variation in threshold voltage as shown in Figure 3.13. The change in noise margin low and noise margin high due to variation in threshold voltage of all topologies is shown in Figure 3.13a and Figure 3.13b. The noise margin low values decrease as we increase threshold voltage and noise margin high values increases as we increase threshold voltage mainly due to the change in values of output high and low voltage (V_{OH} and V_{OL}). Which means the undefined region increases between noise margin high and low. So circuits become less robust when the threshold voltage increases. The change in switching threshold value due to variation in threshold voltage of all topologies is shown in Figure 3.13e. The ideal value of the switching threshold is around VDD/2 = 2.5V. As we increase threshold voltage, all topologies become less robust, which impacts the performance of circuits.

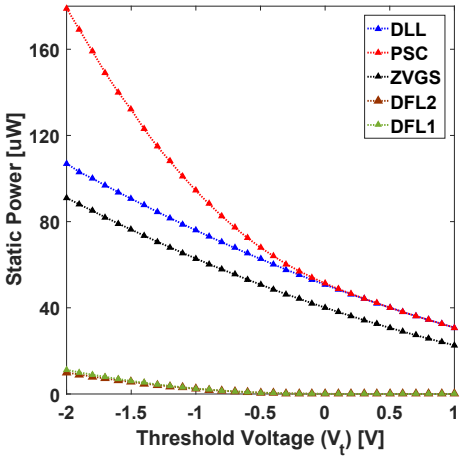
The change in static and dynamic power due to variation in threshold voltage of all topologies is shown in Figure 3.13c and Figure 3.13d. As the threshold voltage increases, the static power of all topologies decreases because the transistor requires a higher voltage to turn on a transistor and leakage current in these transistors is decreased due to high threshold voltage similar to that of CMOS technology. All topologies except PSC are insensitive to variation in threshold voltage because short circuit is dynamic and depends on the value of threshold voltage.



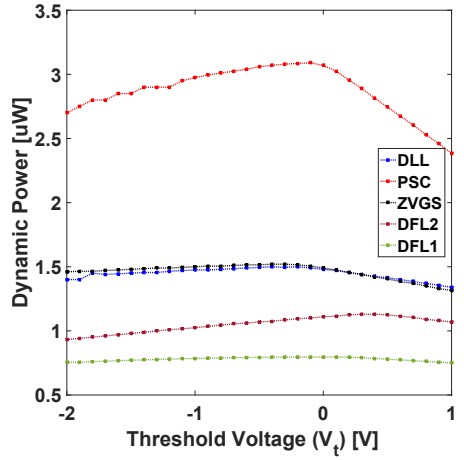
(a) Noise margin low (N_{ML})



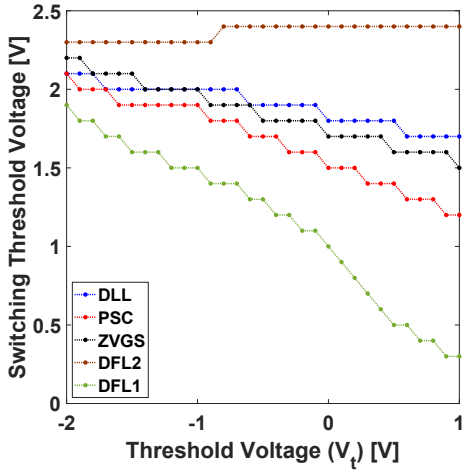
(b) Noise margin high (N_{MH})



(c) Static Power



(d) Dynamic power



(e) Switching threshold (V_m)

Figure 3.13: Sensitivity analysis due to variation of threshold voltage in different topologies (VDD=5V)

Transient simulations were performed on inverters of all topologies to extract parameters such as propagation delay, rise time, fall time, power delay product and energy-delay product. The propagation delay, rise time and fall time of different inverter topologies are shown in Figure 3.14. DFL-1 and DFL-2 have lower propagation delay, rise time, fall time than other topologies because the operation of these two circuits is similar to that of regular CMOS circuit where either pull-up or pull-down logic is enabled. In contrast, other topologies have an always-on transistor, which increases the propagation delay, rise time and fall time.

The power delay product and energy-delay product of different inverter topologies are shown in Figure 3.15. Due to the absence of always-on transistor in DFL-1 and DFL-2 topologies, their performance are better than other topologies in terms of propagation delay and power consumption. Therefore they have lower power-delay product and energy-delay product values.

Gain is another specification which contributes to robustness. The gain of different inverter topologies are shown in Figure 3.16. The gain value gives the steepness of the meta-stable point and also gives a measure of how easy an inverter can get out of meta-stable state [6].

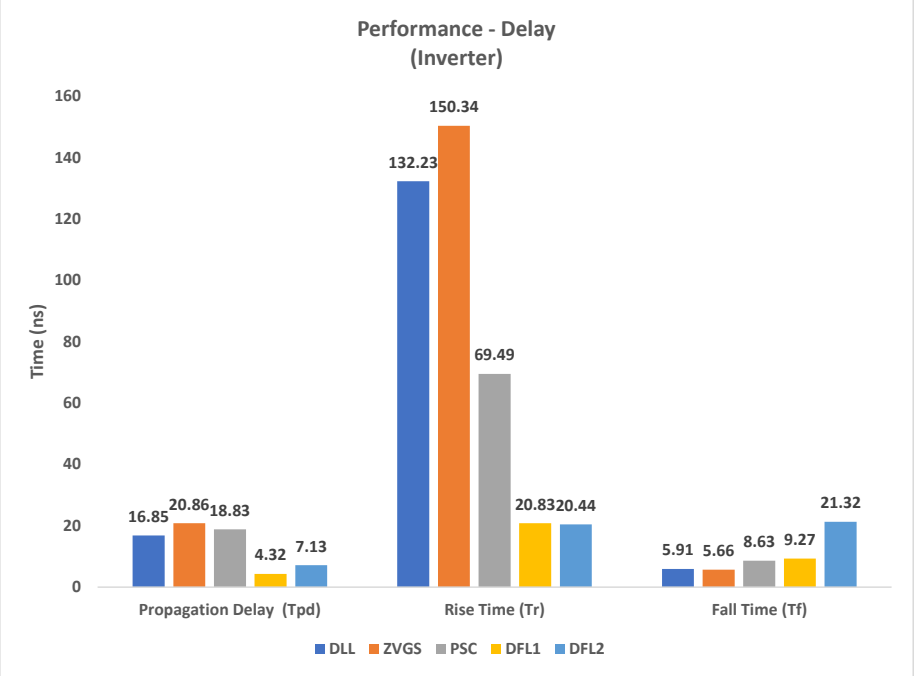


Figure 3.14: Propogation delay,rise and fall time of an inverter using different topologies at VDD=5V

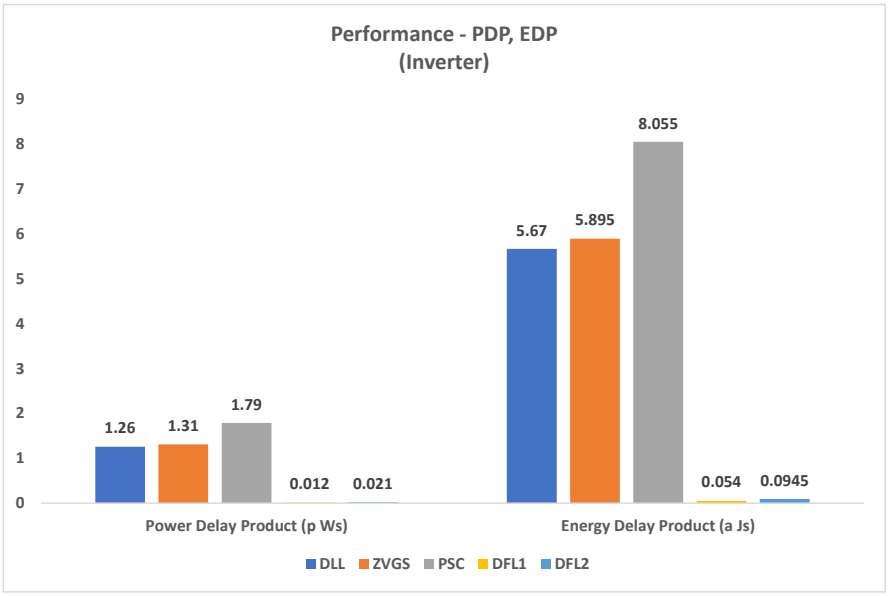


Figure 3.15: Power delay and energy delay product of an inverter using different topologies at VDD=5V

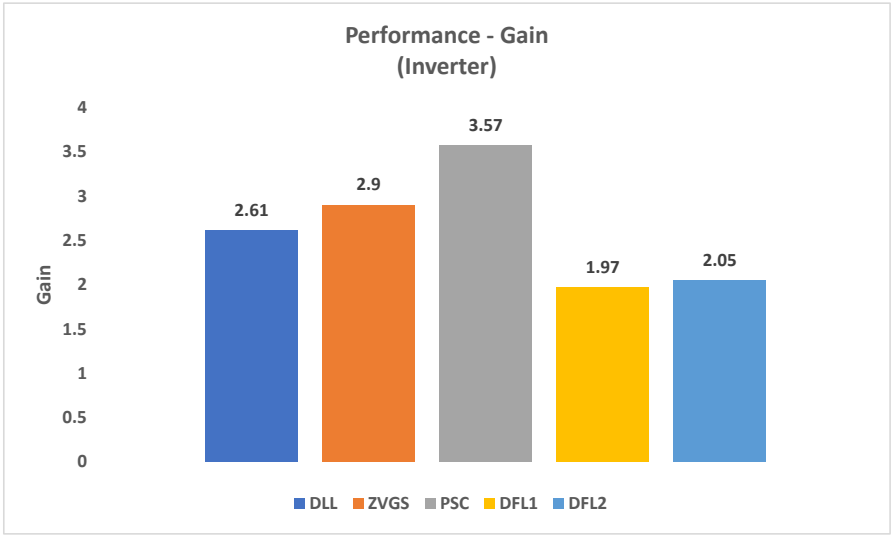


Figure 3.16: Gain of an inverter using different topologies at VDD=5V

The generalized number of transistors required for a logic circuit implementation for different topologies is shown in Table 3.2.

Table 3.2: Table showing required number of transistors in different topologies (Where N is the number of inputs)

Circuit Architecture/ configuration	Number of Transistors (General circuit)	Number of Transistors (Inverter)
Diode Load (DLL)	N+1	2
Pseudo-CMOS (PSC)	2N+2	4
Zero-Vgs (ZVGS)	N+1	2
Differential-1 (DFL1)	4N	4
Differential-2 (DFL2)	2N+2	4

After performing extensive simulations and studying various parameters, a circuit topology selection scheme in terms of parameters such as power consumption, performance and area requirements is shown with the help of Venn diagram in Figure 3.17.

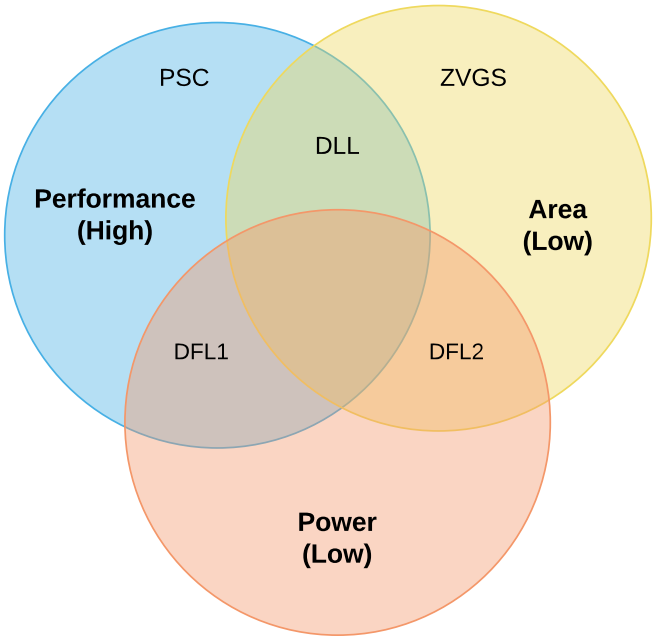


Figure 3.17: Topology selection venn-diagram for a unipolar TFT technology

Chapter 4
Digital Design Flow

In this chapter, a digital IC design flow that was developed during the course of the project is presented. The logic cells that were designed in Chapter 3 are taken through a standard cell design flow by characterizing it to create a library; all the views that are required for the digital backend design such as synthesis, PNR are designed and discussed. Finally, a discussion is presented on a list of standard cells in each designed library.

4.1 VLSI Digital Design Overview

The advancements in IC industry has increased the complexity of designing an IC. By using the technique of divide and conquer the IC industry overcame the complexity issue, this holds true for digital design flow, Hierarchical design and system partitioning which are essential in digital IC design flow.

There are multiple levels of abstraction in the Very large scale integration (VLSI) design flow. The different levels of abstraction is shown in Figure 4.1 [14]. The idea of this chart is to show examples of partitioning and hierarchical design. The chart has three domains: Behavioural, structural and physical. Each domain has different levels from high to low level. The behavioral domain describes the operation of the system at different levels; the structural domain describes the interconnects to achieve a certain operation and the physical domain describes the physical elements and construction of each level from transistor to a package level. The chart describes the tasks and tools that are used in different loops.

A diagram showing a top-down digital IC design flow is shown in Figure 4.2. The system-level defines the description of functionality the system should perform; it is also called a high level description. The architecture level models the system-level description and verifies if the functionality is the same as defined in the system level. The system-level and architecture level is the starting point of any digital system design. High-level synthesis can be performed on an architecture level design to convert it to Register-transfer level (RTL). A RTL describes the system in terms of registers and combinational logic using Hardware description language (HDL). The RTL is converted to a gate-level netlist/description using synthesis, which consists of logic gates and flip-flops. The final step in the design flow maps the logic cells to circuit level description containing transistors, interconnects using PNR to have an IC/chip-implementation.

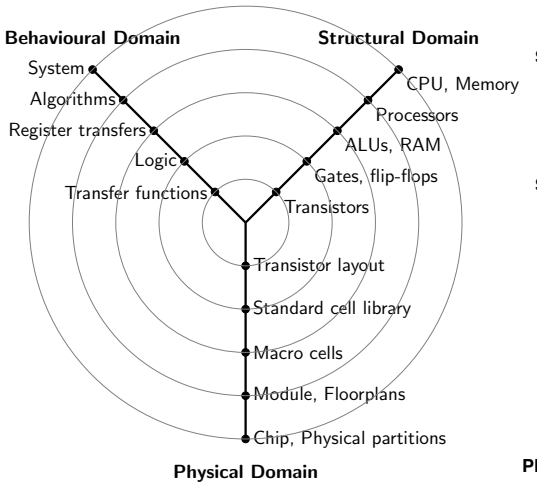


Figure 4.1: Chart showing Digital IC design methodologies [14]

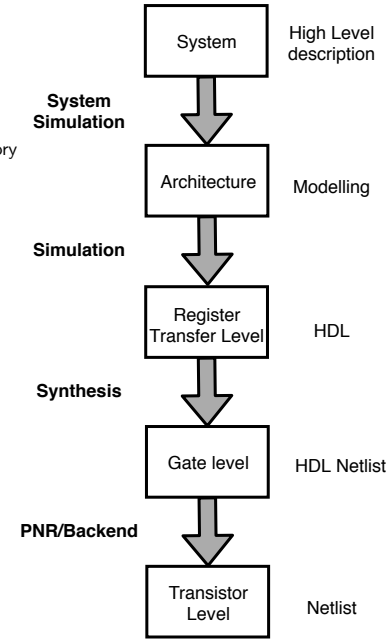


Figure 4.2: Overview of Digital IC design top-down design flow

4.2 Standard Cell Library

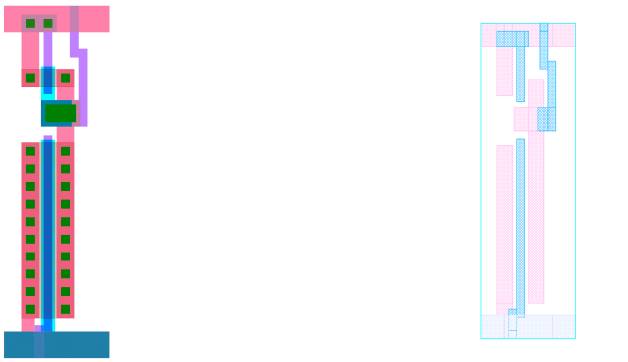
Logic gates are considered as the basic building blocks of a digital circuit. An IC is typically built from a standard cell library that consists of simple and complex logic gates. The reason for building the standard cell library is re-usability. Once the standard cell library is created, it can be considered as black boxes in VLSI.

4.2.1 Standard cell

A standard cell can be represented in various views, Figure 4.3a shows a layout view, Figure 4.3b shows an abstract view, Figure 4.4 shows logic view and netlist of an inverter. The Inverter can also be represented in terms of their timing and power views explained in Section 4.2.2. These representations complete a standard cell and can be used to build an IC.

- Layout view describes detailed geometries of transistors and metals connections. This view is very detailed for digital design flow, so we extract the abstract view of the layout and use it in a digital design flow. The layout view is only used in Graphic Data System II (GDS II) and sign-off. Standard cells have a fixed height and variable width, which allows them to be placed in a row. Input, output, power, ground and backgate pins are placed on a grid at top and bottom of a standard cell.

- Abstract view is created from a layout to show a simple representation. It has details of metals used, pin locations and metal blockages.
- Netlist view provides netlist description of a circuit in transistor level including transistor types and their dimensions, the parasitics of the cell is also provided to have accurate models.
- Logic view provides the logic functionality of a cell, which is useful for synthesis, PNR and optimization.
- Timing view provides the propagation delay, rise and fall time of a standard cell with respect to input slew rates and output load capacitances (Non-Linear Delay Model (NLDM)). Values that are not present inside and outside the table are interpolated and extrapolated. Registers such as flip-flops also have hold time, setup time, minimum pulse widths described in the view.
- Power view provides leakage and dynamic power details of the standard cells; the tables/events are the same as in timing view.



(a) Layout view of an inverter **(b)** Abstract view of an inverter

Figure 4.3: Different views of an inverter

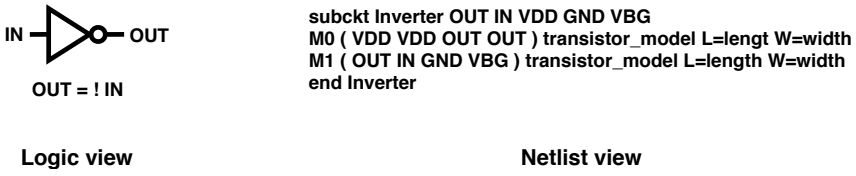


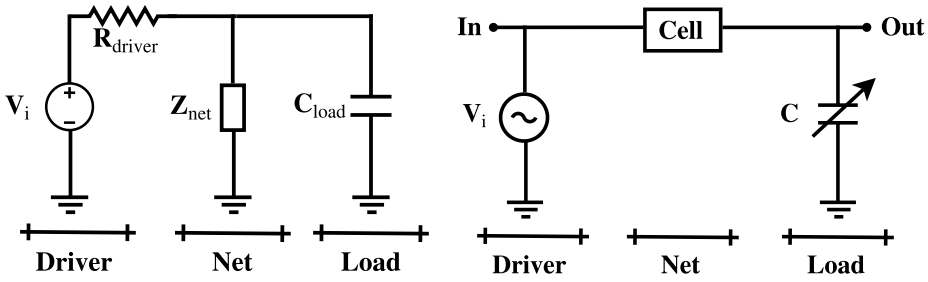
Figure 4.4: logic view and netlist view of an inverter

4.2.2 Library Characterization

Library characterization is a process of modeling the functionality of a standard cell along with its timing, power and area information. A proper modeling method

is required to characterize a standard cell. The characterized library can be reused to design other ICs; hence characterization is important and takes much effort.

The characterization approach used here is NLDM shown in Figure 4.5a, which uses a driver, net and load modelling technique. The standard cell modelling technique is shown in Figure 4.5b, where the input slew and output load is varied and values of propagation delay ($T_{pl\text{-}h}$, $T_{ph\text{-}l}$), rise time (T_r), fall time (T_f), static (leakage) power and dynamic (switching) power values are recorded in a form of table.



(a) Characterization approach in NLDM model **(b)** Standard cell Characterization

Figure 4.5: Library Characterization Methodology

The TFT standard cell circuits follow a full custom design; it needs to be characterized. The block diagram of characterization is shown in Figure 4.6. Cadence Liberate [15] is used as a characterization tool. The inputs to the tool are standard cell spice netlist along with technology dependant model files and setup scripts are used to simulate the standard cell under various conditions and all possible combinations of the input signal to capture the behaviour. The outputs of the process are timing and power data compiled in a library (Liberty Timing File (LIB)) file and functionality is captured in a verilog file.

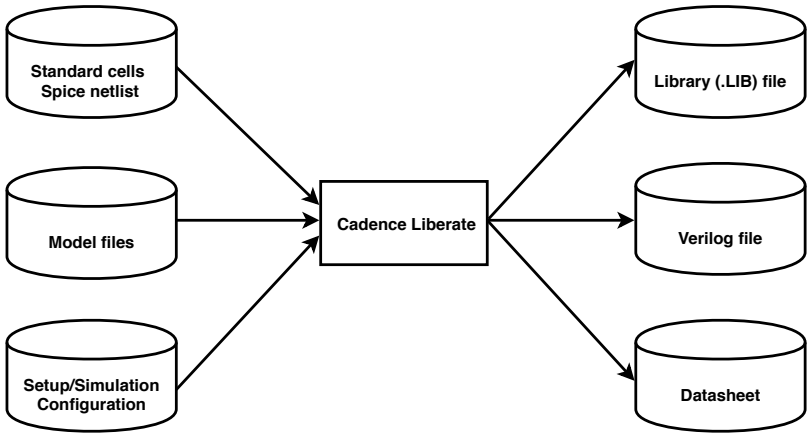


Figure 4.6: Overview of Library characterization flow

4.3 Synthesis

Synthesis is one of the critical steps in the digital design flow since it is the first step in physical backend design. It maps the RTL written in a HDL to a gate-level netlist, which is technology dependent. The synthesis tool takes into account timing, power, area and design constraints during the mapping and optimization. After the functionality of an IC has been described on a high level of abstraction, the circuits can be synthesized.

The block diagram of synthesis is shown in Figure 4.7. Cadence Genus [16] is used as the synthesis tool. The inputs that are required for synthesis are RTL, LIB and Synopsys Design Constraints (SDC) files. RTL describe the functionality of an IC. Library (LIB) files containing details of timing, power and area of standard cells in the library. Clock constraints (SDC) file which contain details of clock used in the IC. The outputs of this process are netlist and Standard delay format (SDF) files. A synthesized gate-level netlist consists of standard cells used from the library. SDF file consists of the timing details of the gate-level netlist and reports of the synthesis.

The main reports generated from synthesis are area, Power, Timing and Quality of results (QOR) reports. The area report gives details of the standard cells used and the area of standard cells. Power report which mentions the total, static and dynamic power of the design. The timing report gives details of the critical path of the design. The acqor report gives details such as combinational instance count, sequential instance count, total cell area, maximum and minimum fanout, memory usage and time elapsed for the synthesis process.

The main steps in synthesis are elaboration, mapping and optimization. In the elaboration step, the combinational logic and registers are inserted into the design. This process uses generic logic gates and registers. This generic circuit must then be mapped and optimized to the available registers and logic gates from the designed library (LIB) file; this step is called mapping and optimization.

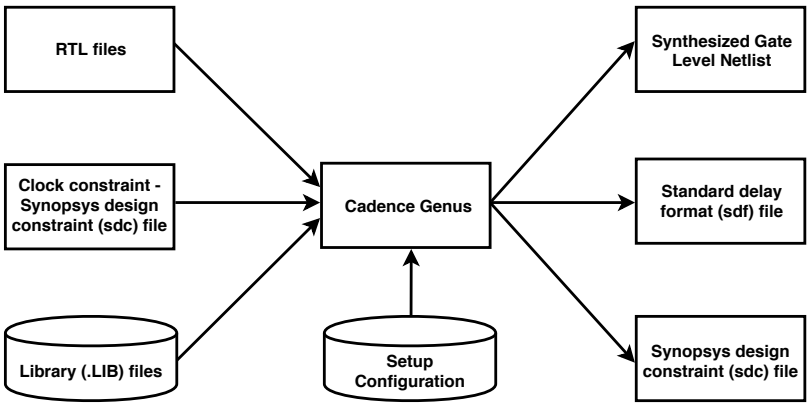


Figure 4.7: Overview of a Synthesis flow

4.4 Place and Route

The PNR step is where the actual IC is implemented and realized in the digital design flow. If this step is not done correctly, it can have a massive impact on the final IC design in terms of performance, power and area. It is the final step in the physical backend design.

For physical IC design implementation, three representations are required: netlist, (Library Exchange Format (LEF)) and (LIB). The gate-level netlist obtained from synthesis provides the standard cell used and their connectivity in an IC. The physical (LEF) representation provides abstract views of the cell for PNR. Timing and power (LIB) representation contain the timing and power values for different input slew rate and output capacitance. The above representations are needed to engineer a reliable IC.

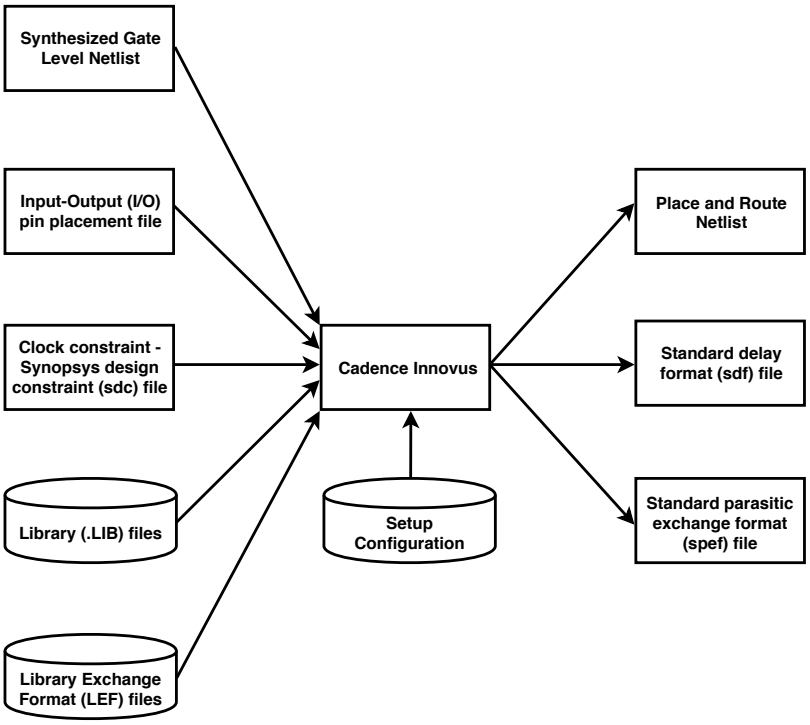


Figure 4.8: Overview of PNR flow

The main steps in PNR are floor-planning, power-planning, placement, clock-tree synthesis and routing. The input-output pin locations, macro placement, the aspect ratio of the IC, the utilization factor of the core are decided in the floor-planning. A power delivery network is designed in a power plan. In the placement step, the standard cells are placed. Clock tree synthesis defines how the clock signal is routed and delivered in the design. Routing routes the interconnects in

the design. The optimization step optimizes the design for timing and power. A Design Rule Check (DRC) is conducted on the final PNR layout or GDS II using the design rule deck available for TFT technology. A Layout vs schematics (LVS) check is conducted on the extracted netlist after PNR and layout of PNR.

The block diagram of PNR is shown in Figure 4.8. Cadence Innovus [17] is used as the PNR tool. The input files that are required for PNR are netlist, LIB, LEF, SDC and input-output pin files. The gate-level netlist file is obtained from synthesis. A library (LIB) files containing details of timing, power and area of standard cells in the library. A LEF file contains the physical details of the standard cell library, such as cell sizes and pin locations. Input-output pin file that contains the placement details of the pins. Clock constraints (SDC) file which contain details of clock used in the IC. The outputs of this process are a PNR netlist,Standard Parasitic Exchange Format (SPEF) and SDF files. The PNR netlist consists of standard cells used from the library. A SPEF file contains information of the interconnect parasitics. A SDF file contain information of the timing details of the PNR netlist. A GDS II file is extracted from the final PNR layout.

The main reports generated from PNR are area, power and timing reports. Area reports give detail of the dimensions of an IC chip, placed standard cells used and the area of standard cells. Power reports which mention the total, static and dynamic power of the design. Timing reports give details of the timing paths and critical path of the design.

4.5 Digital Design Flow Approach

An efficient digital design flow methodology is crucial to design a larger IC. A full custom digital design flow is required when using TFTs similar to that of a ASIC design flow for CMOS transistors. A digital design flow approach that was used for TFT is shown in Figure 4.9. This flow chart describes the steps to implement a TFT IC. The flow could be split into three levels:

1. Library level sets up the standard cell library. Initially the custom circuit is designed in Cadence Virtuoso [18] [19]. The layout of the custom circuit is designed using the Cadence Layout tool [20], keeping the standard cell rule of fixed height and variable width. The abstract or LEF view of the layout is created using Cadence Abstract [21], which gives the physical views of standard cell. A library (LIB) file is created using Cadence Liberate [15] which gives the logical elements of the standard cells such as timing, power and functionality

2. In Logic level, a RTL is used to describe the functionality of an IC. once the standard cell library is characterized by describing their timing, power and logic details. Synthesis [22] can map the RTL to gate-level netlist.

3. In Physical level, the gate-level netlist along with the characterized library can be used for the physical implementation of an IC, which is timing and power aware. PNR [17] provides a layout that can be manufactured in a fab.

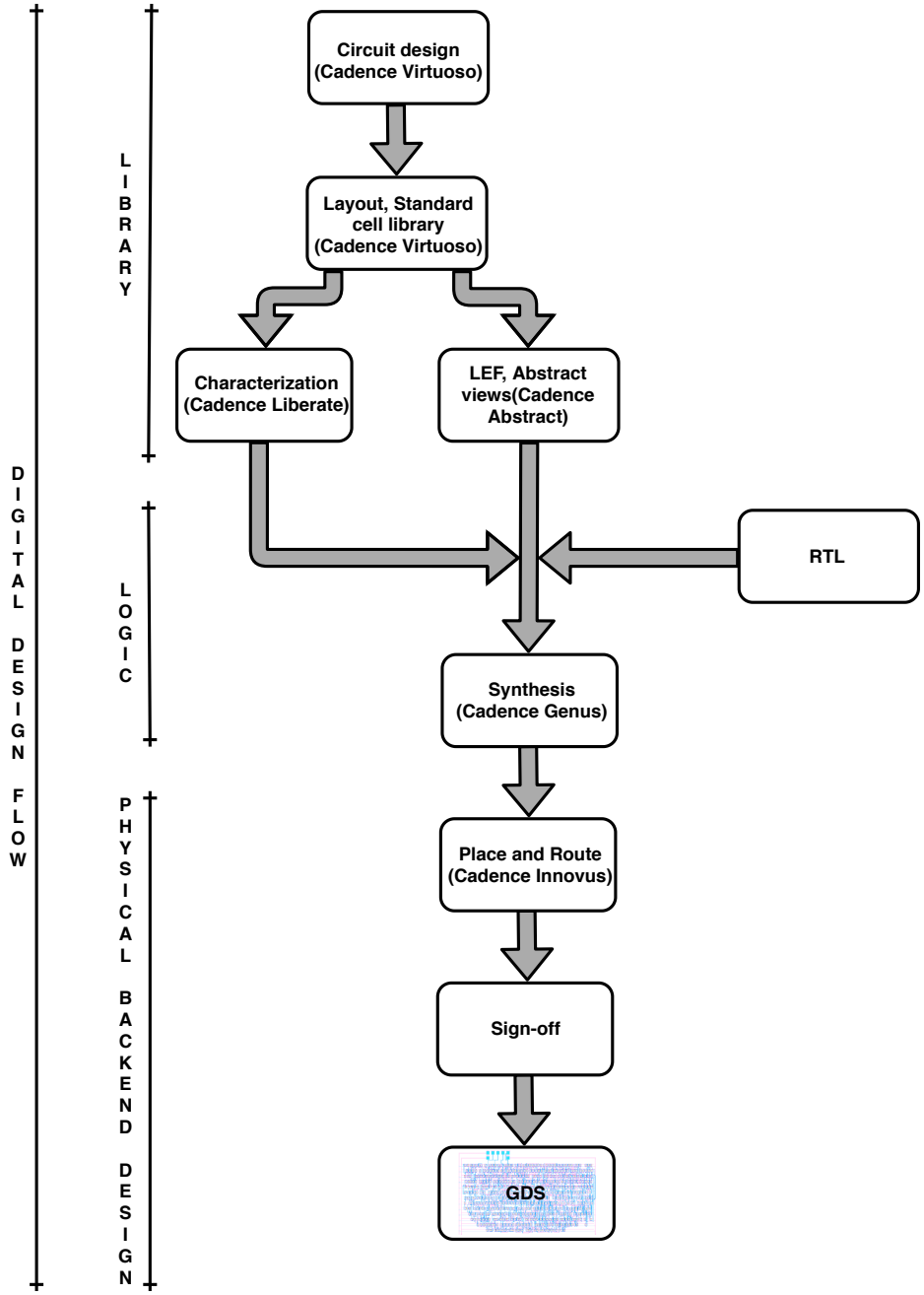


Figure 4.9: Digital design flow methodology for TFT technology

The digital design flow explained is largely EDA tool-driven. Cadence, Mentor Graphics and Synopsys are the main drivers of these tools and they work with IC manufacturing fabs to tune the tools according to the technology used. In this thesis, Cadence tools are used for full custom flow from circuit design to designing an IC.

A list of standard cell libraries built using different topologies is shown in Table 4.1.
Where, INV is Inverter.
BUF is Buffer.
NOR is NOR gate.
AOI is AND-OR-INVERT gate.
NAND is NAND gate.
DFF is D-FLIP FLOP.
OAI is OR-AND-INVERT gate.
HA is Half-Adder.

Table 4.1: Table showing a list of standard cells in different library topologies

Diode Load Architecture			**Pseudo-CMOS Architecture**		**Differential Architecture**
Small Library	**Large Library**	**Largest Library**	**Small Library**	**Large Library**	**Small Library**
INV	INV	INV	INV	INV	INV
BUF	BUF	BUF	BUF	BUF	BUF
NOR2	NOR2	NOR2	NOR2	NOR2	NOR2
AOI3	NOR3	NOR3	AOI3	NOR3	AOI3
DFF	NOR4	NOR4	DFF	NOR4	DFF
	NAND2	NAND2		NAND2	
	AOI3	HA		OAI3	
	DFF	AOI3		OAI4	
		AOI4		DFF	
		AOI5			
		OAI3			
		OAI4			
		OAI5			
		OAI6			
		DFF			

The DLL architecture is shown in Figure 3.2c and PSC architecture is shown in Figure 3.4c. The reason to have different number of libraries in each topology by increasing the number of standard cells is to study how the constraints of timing, power and area would vary when designing an IC.

The reason for not having a library of ZVGS architecture, as shown in Figure 3.3c because, for this topology of circuits to work, the threshold voltage (V_t) of the transistor should always be negative. The libraries of DFL-1 and DFL-2 architectures as shown in Figures 3.5c and 3.6c were characterized, but the operation of synthesis was not possible in these libraries because there are no industry standard EDA tools that perform synthesis using the differential input and output architectures. So for a DFL-2 topology, the differential inputs were replaced by DLL inverters to form a modified differential library (Differential Architecture).

Chapter 5

Design Cases, Simulations and Analysis

In this chapter, a digital system is designed and presented. It makes use of the standard cells and the digital design flow that were discussed in Chapters 3 and 4. The digital design flow test plan will be discussed. A four-bit adder and a four-bit multiplier designs are presented and results such as performance, power, area are discussed.

5.1 Digital Design Flow Test Plan

The complete digital design flow for TFT was discussed in the previous chapter. But there should be a methodology to verify the results extracted from the digital design flow are correct and accurate. To ensure whether the results are correct, the extracted results from digital design flow (Digital simulations) are compared with analog simulations (SPICE simulations). In this way, we are sure and confident about the digital design flow methodology and the extracted digital simulation results.

A methodology of digital design flow test plan is shown in Figure 5.1.

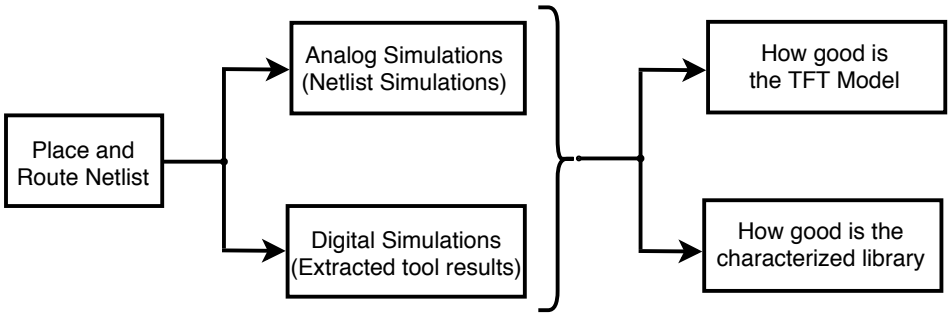


Figure 5.1: Block diagram of Digital design flow test plan

The netlist that is extracted after place and route is used as an input to the analog simulator (Spectre) for extracting timing and power information, which are compared with the results that are extracted from the digital design flow tools.

These results are compared to see how good the characterized library and the TFT model. Once the results of this methodology are verified for correctness in terms of timing and power, in the future for designing a digital system, we could only use the digital design flow techniques and eliminate the analog simulations.

5.1.1 Analog/SPICE simulation

To have more accurate results on the timing and power, the place and route netlist are fed to a SPICE (Spectre) simulator along with standard cell library and TFT model for simulation, the flow is shown in Figure 5.2. Spectre [23] simulator performs simulations in the transistor level; it provides high accuracy in the results but needs high time and high memory for larger designs. So this method is only used at the end to validate the results and library.

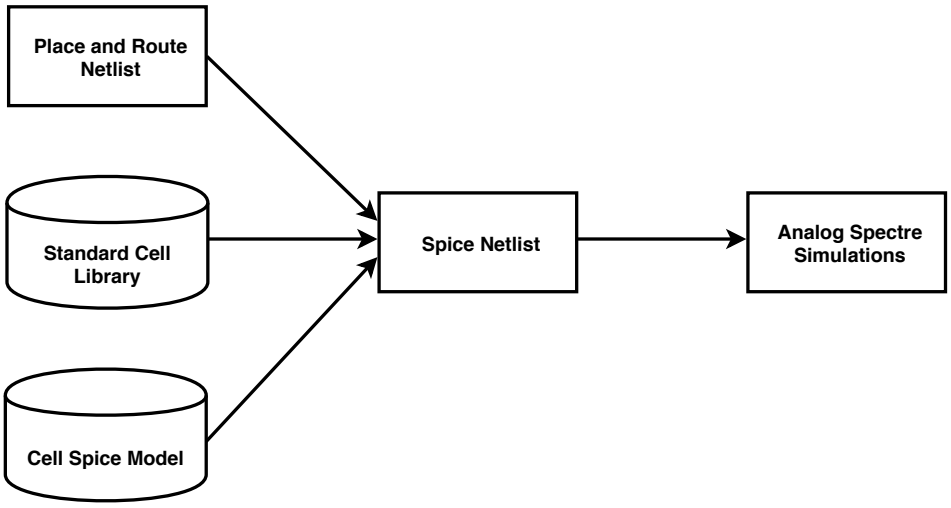


Figure 5.2: Block Diagram of Analog/SPICE simulation flow

5.2 Four-Bit Adder

In order to verify the digital design flow, a general purpose four-bit adder was designed. To have read-out and read-in of data, a scan chain circuit/configuration is used to clock the data in and clock the result data out [6]. At the input, we have 2 sets of 4-bit data and a carry-in bit constituting 9 bits and at the output, we have 4-bit result and a carry-out bit constituting 5 bits, the schematic diagram is shown in Figure 5.3.

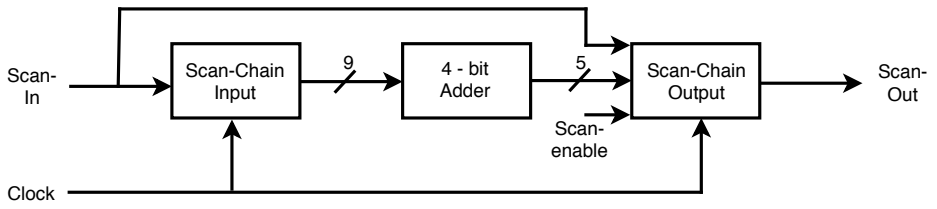


Figure 5.3: Block diagram of a 4-bit Adder with scan-chain

5.2.1 Four-Bit Adder Simulations and Analysis

Once the digital system (4-bit adder) design is complete by using the standard cell libraries that were designed (Table 4.1), the RTL is synthesized as explained in section 4.3 and taken through PNR steps as explained in section 4.4. The reports of power, performance and area are extracted and the netlist of PNR is used as an input to SPICE simulation as in section 5.1.1. In this way, we have results from Digital reports and analog simulations for comparison.

The performance in terms of maximum frequency (critical path of the design), is compared by using the different libraries, as shown in Figure 5.4. The power consumption of the design using different libraries is shown in Figure 5.5. All circuits operate at 5V (VDD=5V), the constraints for synthesis and PNR is common for all the designs. The PSC library has higher performance than DLL and differential library; meanwhile, the power consumption of PSC library is higher than differential and DLL library this is mainly due to higher number of transistor per standard cell in PSC. We observe that as we use libraries containing higher standard cells, the maximum frequency drops by a small amount, but we observe huge power savings as we use less number of standard cells. The reason for the difference between digital reports and analog simulation is that in the characterized digital libraries, the values of timing and power are not available continuously at every instant. Only specific values are available in the library; remaining values are mathematically interpolated and extrapolated.

Comparison of libraries in terms of standard cell area and final PNR area is shown in Figure 5.6. The PSC library occupies a higher area than differential and DLL library due to a high number of transistors per standard cell. As we use libraries containing higher standard cells, the area decreases, this is mainly because higher functional expressions can be easily implemented using a larger library. There is an increase in the total area of standard cells and area of PNR because in the TFT technology, there are only 2 metal layers available for routing, hence horizontally there are empty standard cell rows alternatively after every other standard cell row. Within a cell row, vertically the standard cells are not stacked. There must be room for routing since no routing can be done over a standard cell.

The layout after PNR of a four-bit adder with scan-chain using a diode-load library is shown in Figure 5.7.

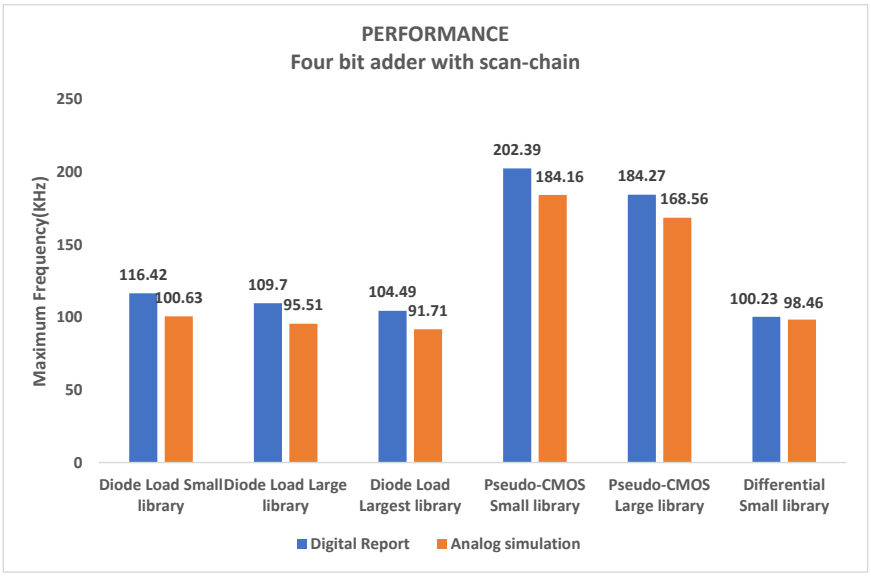


Figure 5.4: Maximum Frequency/Performance of a 4-bit adder using different libraries

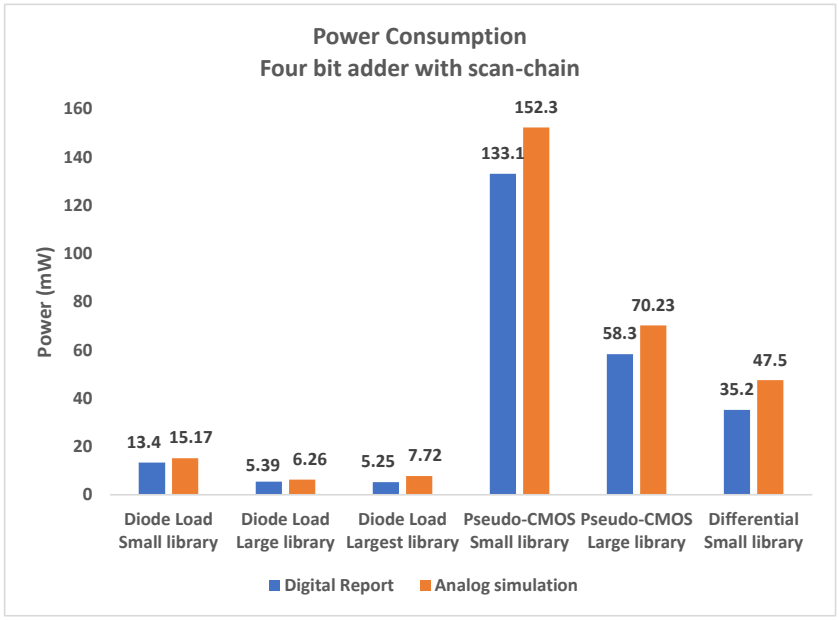


Figure 5.5: Power consumption of a 4-bit adder using different libraries

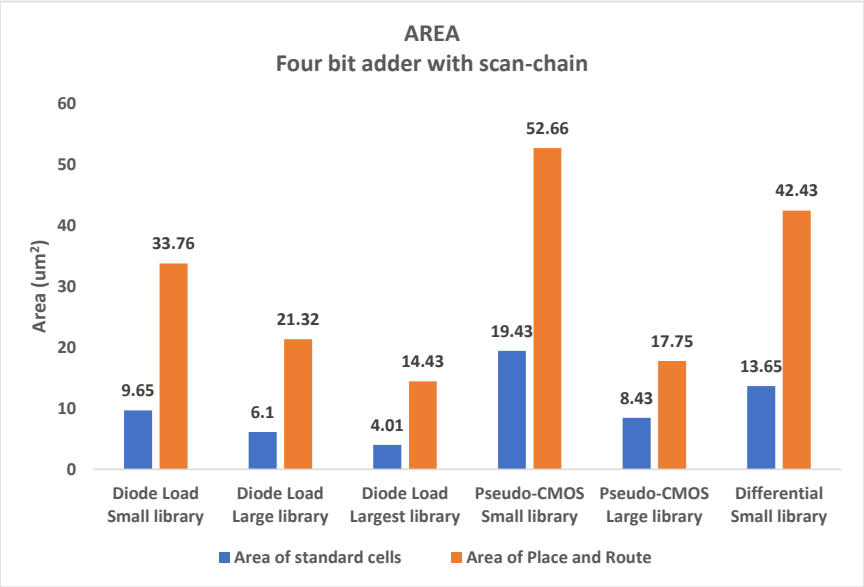


Figure 5.6: Area of PNR and area of standard cells of a 4-bit adder using different libraries

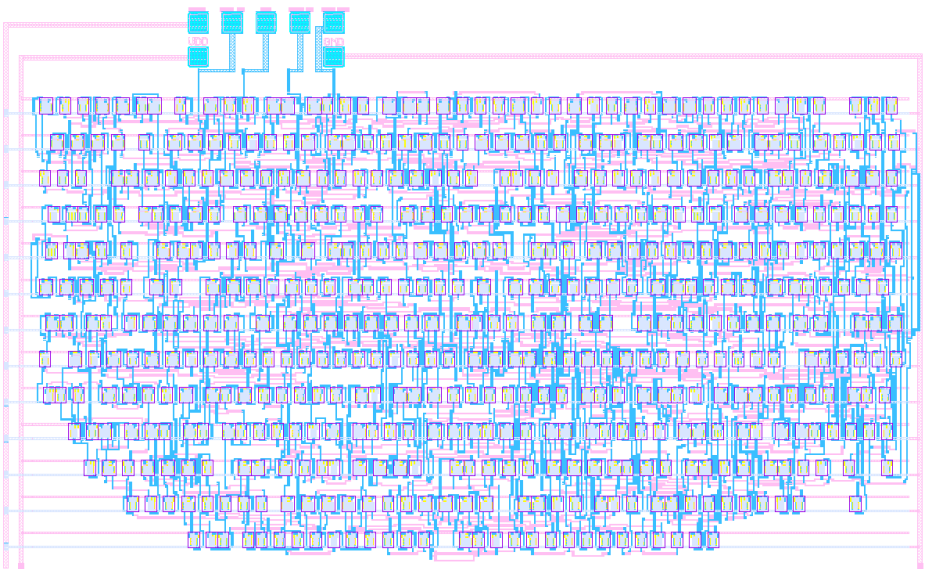


Figure 5.7: PNR snapshot of a 4-bit Adder using diode-load logic library

5.3 Four-Bit Multiplier

A general four-bit multiplier was designed, which has a similar read-in and read-out functionality as in the four-bit adder. At the input, we have 2 sets of 4-bit data constituting 8 bits and at the output, we have 8-bit result, the block diagram is shown in Figure 5.8.

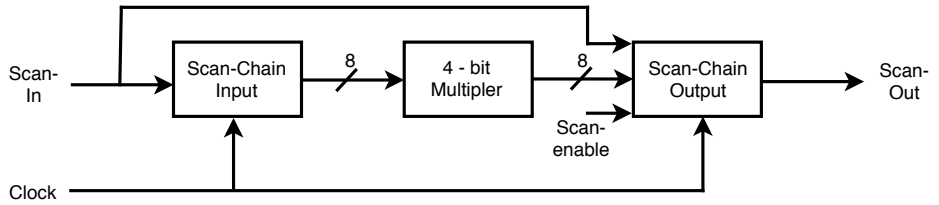


Figure 5.8: Block diagram of a 4-bit Multiplier with scan-chain

5.3.1 Four-Bit Multiplier Simulations and Analysis

The performance in terms of maximum frequency (critical path) of the design is compared using the different libraries, as shown in Figure 5.9. The power consumption of the designs is shown in Figure 5.10. All circuits operate at 5V, the constraints for synthesis and PNR is common for all the designs. The PSC library has higher performance than DLL and differential library; meanwhile, the power consumption of PSC library is higher than differential and DLL library this is mainly due to higher number of transistor per standard cell in PSC. The difference in digital reports and analog simulation is discussed in Section 5.2.1.

Comparison of libraries in terms of standard cell area and final PNR area is shown in Figure 5.11. The PSC library occupies a higher area than differential and DLL library due to a high number of transistors per standard cell. The increase in the total area of standard cells and the area of PNR is discussed in Section 5.2.1 The layout after PNR of a four-bit multiplier with scan-chain using a diode-load library is shown in Figure 5.12.

We have compared the digital design flow with analog/SPICE simulations for two designs and the results obtained between the two are comparable and close. In this way, the digital design flow methodology is validated and verified. The methodology could be used for projects to design digital systems using TFT.

The Importance of Digital design flow compared to analog flow:

- Digital flow is robust and reduces non-recurring engineering costs. Digital design flow is quicker; Analog flow consumes huge computation memory.
- Digital design flow is automated in almost every step in the design flow, whereas analog flow is not automated.
- With Digital design flow, it is easier to have a quick sign-off flow before the actual tape-out.
- A centralized database for the flow such as LIB files, LEF files, standard cell libraries, flow scripts are available, which can be used for all projects.

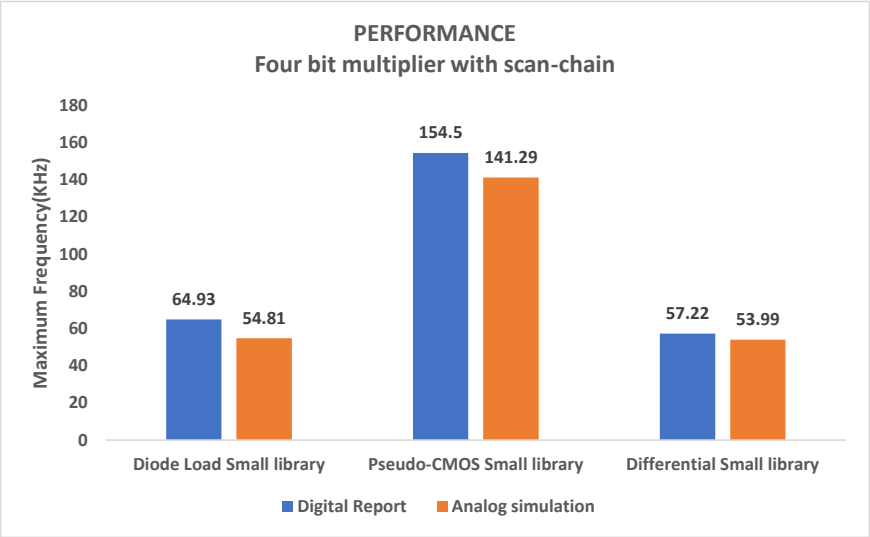


Figure 5.9: Maximum Frequency/Performance of a 4-bit multiplier using different libraries

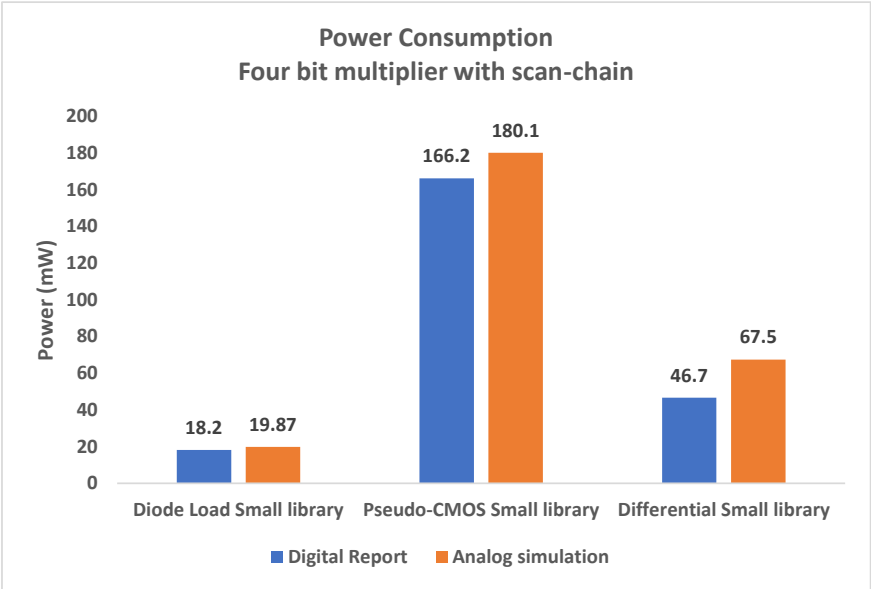


Figure 5.10: Power consumption of a 4-bit multiplier using different libraries

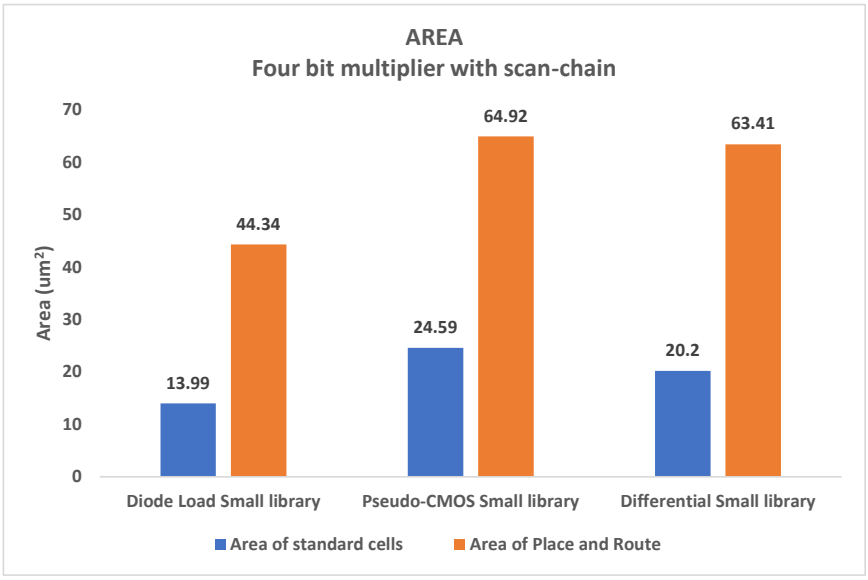


Figure 5.11: Area of PNR and area of standard cells of a 4-bit multiplier using different libraries

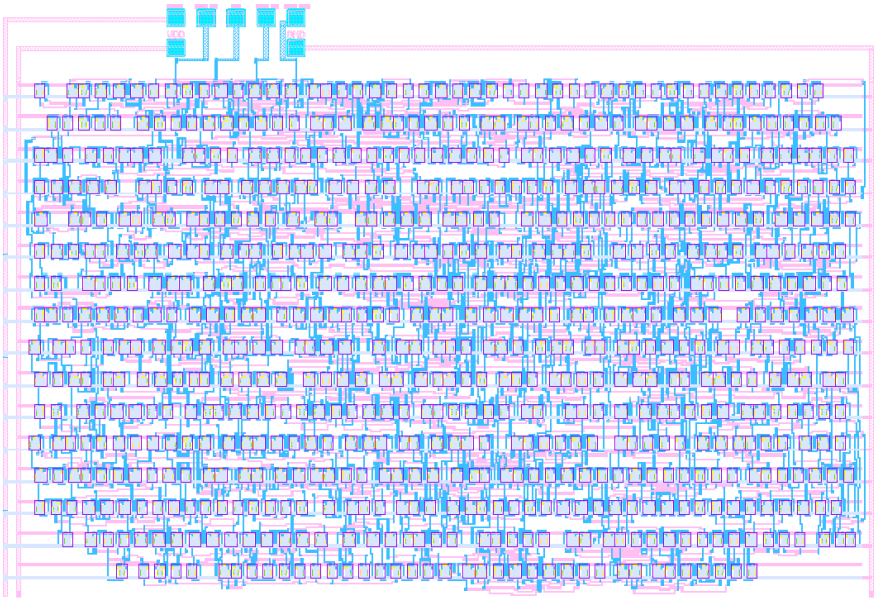


Figure 5.12: PNR snapshot of a 4-bit Multiplier using diode-load logic library

Chapter 6

Conclusion and Future work

6.1 Conclusion

In this thesis project, the goal was to improve the circuit design and to develop a digital design flow using unipolar TFT technology. The thin-film technology used is a unipolar IGZO, which can be fabricated on foils to make the ICs flexible.

Circuit architectures of different topologies comparing the trade-off between them in terms of power, performance and area were discussed in Chapter 3. Design flow is a set of rules and guidelines on how to proceed from a specification to the final hardware implementation. This digital design flow approach which includes creation of standard cell library (LIB) files, abstract (LEF) files, synthesis flow, place and route flow was discussed in Chapter 4 taking TFT design rules and parameters into account.

Some complex designs such as 4-bit adders and 4-bit multipliers were implemented and validated with the digital design flow. To verify this flow, a digital design flow test plan methodology was discussed in Chapter 5. The trade-off using different standard cell library in terms of power, performance and area were discussed.

We have a digital design flow for TFT technology, which is used to exploit all the benefits of existing automated EDA tools.

6.2 Future Work

It is essential to explore how a digital system design implementation would vary in terms of power, performance and area by increasing the number of standard cells in a standard cell library for TFTs. A basic standard cell library contains gates such as inverter, buffer, NOR, NAND, flip-flop. Future work may include extending this standard cell library, also containing more complex gates with different fanout (drive) strength. These cells should be characterized and included in the library database. The library can be characterized using more efficient models such as Composite Current Source (CCS) or Effective Current Source Model (ECSM) models instead of NLDM model.

Different topologies of circuits which are explained in Chapter 3 presents trade-off between power, performance and area constraints. To optimize all of parameters, a digital circuit should combine and have a mix of different topologies and use them whenever required. This is done to have a speed specification while maintaining the power and the area as low as possible. It is also vital to explore newer low-power and high-speed topologies for a unipolar TFT, as the large power consumption and speed are limiting factors for TFT used in digital systems.
The area limiting factor is due to the availability of only two metal layers for routing, which increases the area of a IC design in PNR. It is necessary to explore technology advancements in TFT to increase the number of metals and routing resource.

The differential-1 and differential-2 topologies discussed in Chapter 3 have differential inputs and differential outputs; there is no industry standard EDA tools that performs synthesis using the differential input and output architecture library. It's therefore important to investigate how to tackle the issue in the future to have a differential library.

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