2014 SoS Workshop
Mixed-Signal IC Design

Presented by Pietro Andreani

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Lund University
Work performed in 2013-2014

- Filtering CT ΔΣ ACSs for LTE
  - Mattias Andersson
- An ultra-low-power CT ΔΣ ADC with SAR quantizer
  - Dejan Radjen (simulations)
- CT ΔΣ ADC for LTE
  - Xiaodong Liu (not shown)
- A digital PLL
  - Ping Lu (simulations)
- Two class-D VCOs
  - Luca Fanori
- A reconfigurable wideband VCO
  - Ahmed Mahmoud (not shown)
Merging LPF and ADC

LNA

X

Mixer

LPF  ADC

DFE  DBB

VCO/PLL

Mattias Andersson
Channel-Select Filter + CT ΔΣ ADC

Tow-Thomas 2\textsuperscript{nd}-order CSF

Noise from DSM is 2\textsuperscript{nd}-order shaped by global feedback

ESSCIRC ’13
SoS workshop ’13
Improved Version: Filtering CT $\Delta \Sigma$ ADC Supporting LTE 2x20MHz

3$^{rd}$-order CSF
2$^{nd}$-order DSM

Noise from DSM shaped by three zeroes in CSF
Simulation with white noise at DSM input

Conventional CSF and DSM cascade
SNR=54dB

Filtering ADC
SNR=73.8dB

BW = 18.5 MHz

DSM noise suppressed by three zeroes → 19dB gained!
Filtering ADC

- 3rd-order Chebychev CSF, 9.0/18.5 MHz BW
- 2nd-order DSM, 3-bit DACs, $f_s=288/576$ MHz
Filtering ADC vs plain ΔΣ ADC

Topologically identical! – However:

- **5\textsuperscript{th}-order DSM**
  - 5 poles at high frequencies to maximize SQNR

- **Filtering ADC:**
  - 2 poles at low frequencies for filtering
  - 3 poles at high frequencies for SQNR
Chip photograph

- ST 65nm CMOS
- $V_{dd}=1.2V$, $I_{dd}=9.4mA$ (11.3mW)
- $f_s=288MHz$, $BW=9MHz$
- Core area $0.5\times0.22mm^2$
Signal Transfer Function in 2xLTE20

![Graph of Signal Transfer Function](image)

- **Input Frequency [MHz]**
- **STF [dB]**

- **Markers**:
  - Chip1
  - Chip2
  - Chip3

- **Anti-aliasing**

- **Frequencies**:
  - 557.5
  - 576
  - 594.5

- **Signal Levels**:
  - -48
  - -43

- **Graph Details**:
  - Vertical lines indicating signal levels
  - Circular highlight on the right side
SNR and SNDR in 2xLTE20

Input Referred Noise
IRN = 5.1 nV/√Hz
Tolerance to blockers, 2xLTE20

5MHz SC-FDMA blockers

- Chip1
- Chip2
- Chip3
- Blockers

- IBB2
- IMD
- ACS1

- P$_{1dB}$

CW blockers

- Chip1
- Chip2
- Chip3
- Blockers

- OBB3
- OBB2
- OBB1
- IMD
- NBB

- P$_{1dB}$

- Frequency [Hz]

- Input RMS power [dBVrms]

- 10$^7$ - 10$^8$

- $-50$ - $-10$

- $-40$ - $-20$

- $-30$

- $-40$

- $-50$

- $10^7$ - 10$^8$

- $-50$ - $-10$

- $-40$ - $-20$

- $-30$

- $-20$

• P$_{1dB}$ vs. blockers (P$_{1dB}$ = blocker power for which in-band noise increases by 1dB)

• Assuming 10mS front-end and -54dB TX-to-RX in duplexer
Tolerance to blockers, LTE20

5MHz SC-FDMA blockers

- \( P_{1\text{dB}} \) vs. blockers
- Assuming 10mS front-end and -54dB TX-to-RX in duplexer
# State-of-the-art in filtering ADCs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Paper V</th>
<th>Paper IV</th>
<th>Philips ISSCC’04</th>
<th>Sosio ESSCIRC’11</th>
<th>Rajan ISSCC’14</th>
</tr>
</thead>
<tbody>
<tr>
<td>fs (MHz)</td>
<td>576</td>
<td>288</td>
<td>64</td>
<td>405</td>
<td>256</td>
</tr>
<tr>
<td>BW (MHz)</td>
<td>18.5</td>
<td>9</td>
<td>1</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>56.4</td>
<td>68.4</td>
<td>59</td>
<td>74.6</td>
<td>74.4</td>
</tr>
<tr>
<td>Filter order</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Avg. IRN in BW (nV/√Hz)</td>
<td>5.1</td>
<td>8.1</td>
<td>280</td>
<td>–</td>
<td>40</td>
</tr>
<tr>
<td>Gain setting (dB)</td>
<td>26</td>
<td>12</td>
<td>0</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>In-band IIP3 (dBV$_{rms}$)</td>
<td>-8.5</td>
<td>11.5</td>
<td>19</td>
<td>–</td>
<td>24</td>
</tr>
<tr>
<td>Out-of-band IIP3 (dBV$_{rms}$)</td>
<td>20</td>
<td>27</td>
<td>–</td>
<td>–</td>
<td>34</td>
</tr>
<tr>
<td>f$_{-3dB}$ (MHz)</td>
<td>25.0</td>
<td>16.9</td>
<td>3</td>
<td>–</td>
<td>4</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>7.9</td>
<td>11.3</td>
<td>2</td>
<td>54</td>
<td>5</td>
</tr>
<tr>
<td>Tech. (nm)</td>
<td>65</td>
<td>65</td>
<td>180</td>
<td>90</td>
<td>130</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
<td>1.2-1.8</td>
<td>1.4</td>
</tr>
<tr>
<td>DR at BW×4 (dB)</td>
<td>82</td>
<td>80</td>
<td>65</td>
<td>90</td>
<td>90.5</td>
</tr>
<tr>
<td>FOM1 at BW×4 (fJ/c.)</td>
<td>21</td>
<td>77</td>
<td>700</td>
<td>180</td>
<td>45</td>
</tr>
<tr>
<td>FOM2, OOB IIP3 (aJ)</td>
<td>4</td>
<td>7</td>
<td>–</td>
<td>–</td>
<td>15</td>
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</table>
A 2nd-order CT ΔΣ modulator with an SAR quantizer

Part of a large SSF project, "Wireless Communication for Ultra Portable Devices (UPD)", lead by Prof. Henrik Sjöland
Architecture of ΔΣ modulator

- ΔΣ modulator with a 4-bit SAR quantizer
- SAR more power efficient than standard flash quantizers
- Generation of clock at $5f_s$ avoided with asynchronous control
Details of $\Delta \Sigma$ modulator

- 2$^{nd}$-order loop filter with single opamp to save power
- Resistive feedback DACs with NRZ pulses
Simulation results

- Unfortunately, unstable in real life due to impact of layout parasitics
- Redesign ongoing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated performance</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>800 mV</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Maximum input amplitude</td>
<td>200 mV differential</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>16 MHz</td>
</tr>
<tr>
<td>SNDR</td>
<td>65 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>69 μW</td>
</tr>
<tr>
<td>Figure of merit</td>
<td>47 fJ/conv</td>
</tr>
</tbody>
</table>
Digital PLL
Time-to-digital converter (TDC)

2-D gated-ring-oscillator (GRO) Vernier TDC

- GRO $\rightarrow$ shaping of quantization noise
- 2-D $\rightarrow$ large detection range, low latency
Class-D DCO
Noise cancellation

Cancellation off

Cancellation on

REF
25MHz

GVTDC

MASH-3
ΔΣ
Modulator

DCO

Tuning Bank
Controller

DLF

Bi-Ther
Decoder

fine
medium
coarse

Divider

ckv

kz
z − 1

Full scale is $2^7$
Phase noise simulations

- **With ΔΣ noise cancellation**

- **BW=1.1MHz**

- Noise cancellation strongly reduces quantization noise

- Waiting for IC to return from fab
VCOs

Luca Fanori & Thomas Mattsson (Ericsson)
Prior art: class-D oscillator

- Amplitude $A \approx 3V_{dd}$, efficiency $> 90\%$
- Excellent switches available in nm CMOS
- Suitable for very low $V_{dd}$

ISSCC 2013, JSSC Dec. 2013
1\textsuperscript{st} VCO: dual-core VCO with TR > 1 octave

- Orthogonal 8-shaped inductor $\rightarrow$ no magnetic field between coils
- Very wide tuning range with small inductor area
- Class-D $\rightarrow$ low voltage supply, high performance
Chip photograph

- 65nm CMOS process without thick metal
- Inductors: 1nH and 0.6nH
- Overall tuning range: 2.4-5.3GHz (75%)
- 0.33mm$^2$ active area
- Voltage supply: 0.4-0.5V
Tuning range

- HB VCO (3.36 - 5.30GHz)
- LB VCO (2.40 - 3.61GHz)

Approximately 200MHz overlap

$V_{dd} = 0.4V$
Q vs. frequency

(1) Actual design
(2) Other inductor removed (difference < 10%)
(3) Inductor optimized for standalone VCO
Phase noise at $V_{dd} = 0.5V$

- FoM $\approx 188/189$ dBc/Hz across the tuning range
- $1/f^3$ noise corner frequency between 0.7MHz and 1.5MHz
2\textsuperscript{nd} VCO: class-D VCO with on-chip LDO

- \( P_{\text{top}} \) gate follows \( P_{\text{top}} \) source above \( f_{LP} \) → spurs and noise from \( V_{dd,\text{ext}} \) are rejected

- Narrow-band op-amp → negligible op-amp impact on phase noise
Chip photograph

- 65nm CMOS with thick top metal
- 0.9nH inductor
- $Q_{\text{ind}} = 14$, $Q_{\text{tank}} = 11$ @ 4GHz
- Tuning range: 3.0 – 4.3GHz
- Area: 850$\mu$m $\times$ 410$\mu$m
- $V_{\text{dd}} = 0.4$-0.5V
- $V_{\text{dd,ext}} = V_{\text{dd}} + 200$ mV
Phase noise at $V_{dd} = 0.5V$

- $V_{dd} = 0.5V$, FoM 190/191dBc/Hz

- 1/f$^3$ corner frequency

- -146.5dBc/Hz

- -144dBc/Hz

- -149.5dBc/Hz

- PN @ 3.0GHz, $I_{dc} = 13mA$

- PN @ 3.6GHz, $I_{dc} = 11mA$

- PN @ 4.3GHz, $I_{dc} = 8mA$
SCANDINAVIAN EXCELLENCE DEFINED IN LUND