Reconfigurable UMTS-filter

The task is to implement the UMTS-filter that has been used as a case study in the DSP Design course in silicon. A modification to the existing design will be to modify the control unit to run at the lowest sampling rate, i.e. 3.84MHz instead of 15.36MHz. Further, optimization of coefficients multiplications might also be performed. The original filter architecture is shown below.

Figure 1.

The signal power for the in-band, out-of-band and desired signal from the de-spreader are measured and the control unit decide the number of taps required in the FIR-filter to perform the necessary filtering. One disadvantage of the above architecture is that the filtering is performed at the input sample rate of 122.88MHz with a following decimation of the coefficients. An alternative architecture was developed which performs the decimation before the filtering and thus the filter is divided into four sub-filters. By this the filter is instead clocked at 15.35MHz and the power consumption is reduced by a factor 4. Furthermore coefficients are optimized to achieve the filtering with the lowest number of bits and the simplest arithmetic operations.
References


