Accessing On-chip Instruments Through the Life-time of Systems

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***Abstract*—The electronic systems we find in almost every product today are implemented using integrated circuits (ICs) mounted on printed circuit boards (PCBs). Developing electronic systems is a challenging task due to complexity and miniaturization. A single IC can contain billions of transistors, which are smaller than ever. As a result more Design-for-Test (DfT) features, so called instruments, are embedded on-chip in modern ICs to handle and monitor various activities. Many defects are handled at IC manufacturing; however, there are many problems occurring after ICs are being mounted on PCBs. In many cases, it is unfortunately not possible to reproduce the problem when the electronic system is taken to a repair shop. These problems are known as No Trouble Found (NTF). One obstacle is the limited access to the on-chip DfT instruments that exist in most ICs. We will discuss access to on-chip DfT instruments through the life-time of electronic systems. We will focus on electronic systems using the IEEE 1687 standard.**

***Index Terms*—IEEE Std. 1687, DfT instrument, access time, security**

I. Introduction

The increasing transistor count of integrated circuits (ICs) enables the implementation of more functionality in each IC. However, high transistor count increases design complexity making it an difficult task to get everything as intended. Typically, a significant amount of effort is spent on post-silicon validation, debugging, wafer sort, package test, burn-in, printed circuit board bring-up, and printed circuit board assembly. Even if great effort is spent on these activities during manufacturing, there is a growing need of power-on self-test and in-field test. To ease all these activities, Design-for-Test (DfT) features, so called instruments are embedded in ICs. These instruments are accessed at manufacturing test and in-field testing; hence, the embedded instruments are accessed through the life-time of the IC.

The process for instrument design, integration and usage can be described as follows. An *instrument designer* develops an instrument, for example a temperature sensor. An *instrument integrator* selects and integrates a number of instruments, for example temperature sensors onto the IC, and ensures the instruments can be accessed from the chip boundary (pins). An *instrument user* can access the instruments. Note that there are a number of different instrument users. Some instrument users access instruments at the manufacturing phase when performing post-silicon validation, debugging, wafer sort, package test, burn-in, later other instrument users access instruments to perform printed circuit board bring-up, printed circuit board assembly manufacturing test, and finally there are instrument users that access instruments at power-on self-test and in-field test. In cases, when a system malfunction during operation, there is a need to take the system, or parts of it, to a repair-shop to identify the problem. In these situation, it is desirable to be able to access embedded features.

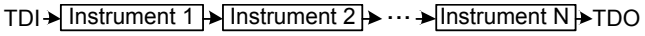


Fig. 1. Chaining instrument shift-registers into a regular scan-chain

In this paper we introduce IEEE 1687 and detail works using IEEE 1687.

II. Introduction to IEEE 1687

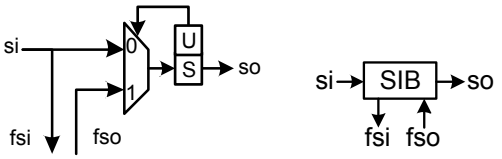
A straight-forward scheme to enable access to instruments is to make use of scan-chains, see Fig. 1. The instrument integrator simply connects all instruments into a long shift-register (scan-chain). For instrument access, the instrument users simply shifts data through the scan-chain to access desirable instruments. The drawback is that all instruments are *always* accessed even when a single instrument is to be accessed. For a large IC with many instruments the access time becomes very high.

IEEE 1687 (IJTAG) [1] enables flexible access, mainly through the JTAG test access port (TAP) [2], to the on-chip instruments. IEEE 1687 makes it possible to include only those instruments on the scan-path that are desired at the moment. IEEE 1687 introduces two new languages, Instrument Connectivity Language (ICL) and Procedural Description Language (PDL), to standardize the access and control of on-chip instruments.

ICL describes the instruments port functions and logical connection to other instruments and to the JTAG TAP, and PDL describes how an instrument should be operated. The idea in introducing ICL and PDL is to provide an adequate and standardized description of the IEEE 1687 network, instruments, and instrument access procedures, and to enable ICL and PDL interpreter tools to automate the retargeting of access procedures.

To enable variable-length (flexible) scan-path, IEEE 1687 introduces two components:

1) a Segment Insertion Bit (SIB), which is used to include in, or exclude a scan-chain from the active scan-path. Fig. 2 shows a simplified schematic of a possible implementation of a SIB, as well as a symbol which we will use through the rest of this paper. Fig. 2(a) shows



(a) Simplified schematic (b) Symbol

Fig. 2. Segment Insertion Bit (SIB)

only as few components and terminals as are needed to explain the operation of a SIB: a one-bit shift-update register, and a mux. However, a realistic schematic would contain more components (such as logic gates for gating control signals, keeper muxes for the registers, and delay elements to avoid race condition) and terminals (such as selection and control signals used to enable shift and update operations).

2) a *ScanMux* control bit, which is a shift-update register that can be placed anywhere on the scan-path to configure one or more scan multiplexers (ScanMux components). Fig. 3 shows a two-bit ScanMux control register used to configure a network of two instruments. In this work, we consider one-bit ScanMux control bits, to control two-input muxes which bypass instrument shift registers in, e.g., daisy-chained architectures.

Both SIBs and ScanMux control bits must be configured to have the correct value every time the scan-path they are on is accessed.

The flexibility in an 1149.1-2013 [3] TDR is achieved by defining segments of that TDR as *selectable*. A selectable segment mux with a one-bit wide control, is similar to the SIB component specified by 1687. Moreover, 1149.1-2013 also allows for controlling a selectable segment mux from another part of the scan-path or from other TDRs. The selectable segments can be nested to create a hierarchical network for accessing instruments, similar to what is achievable by a hierarchical IEEE 1687 network.

Although there are differences between 1149.1-2013 and 1687 in implementation details, the corresponding reconfigurable networks described under each of the two standards show the same behavior regarding instrument access time.

1149.1-2013 and 1687 use a similar Procedural Description Language (PDL) for describing the operation of embedded instruments. For example, assuming that the DFT feature in Fig. 4 is a BIST instrument, to operate on this BIST instrument there is a need of PDL commands (read/write) to configure the SIBs such that the BIST instrument is placed on the scan-path. While the BIST instrument is running, there is no need to access the network for this particular instrument. Hence, the PDL commands can be divided as commands that configure and access the network, such as read/write, and as commands that utilize a given network configuration without requiring any accesses, such as a command used for waiting for a number of clock cycles. The idea is that the retargeting tool generates network configuration vectors/commands. The user needs only to specify what should be written to the registers of the BIST engine (for example algorithm selection and start command).

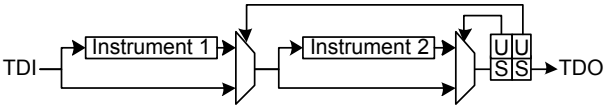


Fig. 3. A network configured by a two-bit ScanMux control register

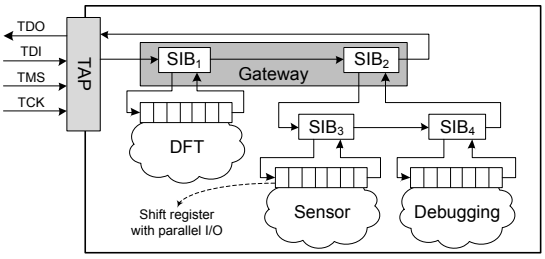


Fig. 4. A 1687 network with three instruments inside a chip

III. Previous works

In this section, we present previous works on IEEE 1687 in respect to standards, access optimization, in-field usage, security aspects, and case studies.

The boundary scan (IEEE 1149.1) [2] and the standard for embedded core test (SECT) [4] suffers from drawbacks when used for accessing on-chip instruments. The boundary scan (IEEE 1149.1) does not allow flexible access to any instrument [2] and the standard for embedded core test (SECT) [4] has no test controller and there is no description of the test infrastructure. IEEE 1687 [1] and the updated IEEE 1149.1 [3] both allows flexible access to any instrument at any time. IEEE 1687 makes use of ICL and PDL, discussed above, to meet these goals.

In the progress to IEEE 1687, several works outlined ideas and requirements [5], [6], [7], [8], [9], [10]. Designing the IEEE 1687 network and optimizing the access has gained much interest [11], [12], [13], [14], [15], [16], [17] [18] [19], [18], [19], [20], [21], [22]. For in-field use there are works [23], [24], [25], [26]. An important aspect in allowing access to embedded instruments is the ability to be able to only allow the instrument user to access the instruments the instrument integrator wants to disclose [27], [28], [29], [30], [31]. There are reports on cases studies using IEEE 1687 [32], [33].

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