Paper: 

M. Yiu, C. Winstead, et al.
Design for Testability of CMOS Analog Sum-Product Error-Control Decoders.

Presented by:
Reza Meraji
Outline

• A brief review of analog iterative decoders
• Testability of analog iterative decoders: a major challenge
• Digital built-in self test (BIST) for analog decoders
  – BIST for computational core
  – BIST for I/O interface
• Test IC and measurements
  – Self test
  – BER test
• Summary
Analog Iterative Decoding
Complete Decoder Architecture

\[ V_{in} \quad SEL1 \quad PIPE \quad V_{in1} \quad C_{S1} \quad C_{H1} \quad \ldots \quad SEL8 \quad PIPE \quad V_{in8} \quad \ldots \quad C_{S8} \quad C_{H8} \]

\[ V_{ref} \quad SEL1 \quad PIPE \quad V_{ref1} \quad C_{S1} \quad C_{H1} \quad \ldots \quad SEL8 \quad PIPE \quad V_{ref8} \quad \ldots \quad C_{S8} \quad C_{H8} \]

Decoder Core

LLR to Probability Conversion

\[ D_{out1} \quad D_{out2} \quad D_{out3} \quad D_{out4} \]
Overall Structure of Decoder:
With core and I/O BIST controllers
BIST for the Computational Core

Original Gilbert multiplier-based check node circuit

Modified mode-switching check node circuit

\[ V_{out1} = X_0Y_1 + X_1Y_0 \]
Die microphotograph:
(8,4) Hamming decoder with BIST IN 180-nm technology
## Performance Characteristics of the Test Chip

<table>
<thead>
<tr>
<th>Technology</th>
<th>180-nm 1P6M CMOS, 1.8V Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decoder Area incl I/O</td>
<td>0.072 mm²</td>
</tr>
<tr>
<td>Core BIST Area</td>
<td>0.036 mm²</td>
</tr>
<tr>
<td>I/O BIST Area</td>
<td>0.006 mm²</td>
</tr>
<tr>
<td>Total Core Area</td>
<td>0.138 mm²</td>
</tr>
<tr>
<td>Clock Speed</td>
<td>8.3 MSps</td>
</tr>
<tr>
<td>Throughput</td>
<td>3.7 Mbps</td>
</tr>
<tr>
<td>Self Test Time</td>
<td>5 μs @ 12.5 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>13mW @ $I_U = 5μA$, SNR = 8dB</td>
</tr>
<tr>
<td>Energy/Decoded Bit</td>
<td>3.5 nJ/bit</td>
</tr>
</tbody>
</table>
Core Decoder Architecture:
Node organization and BIST labelling

1 byte read, C8 downto C1: 10101010
1 byte read, C16 downto C9: 10101010
1 byte read, E8 downto E1: 11011011
1 byte read, E16 downto E9: 10110110
1 byte read, E24 downto E17: 01101101
1 byte read, Good_Core, Good_IO, E25: 001
BER curves of Decoder IC with BIST

Varying test speed with $I_u=5uA$

- Uncoded BPSK
- ML
- Digital (8,4) Hamming SP
  (64 iterations, no extra check nodes)
- Test speed = 155 kSps
- Test speed = 1.087 MSps
- Test speed = 8.33 MSps
Summary

• Presenting an all digital built-in self test technique
• Proposed technique was used to test a Hamming decoder chip
• Reasonable area overhead of the BIST circuit
• Negligible effect on the performance of the decoder