

# Contents: III/V Nanowires

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## **Vertical InAs NW transistors:**

**C Thelander et al IEEE Electron Dev. Lett. 29, 2008 p 206 "Vertical Enhancement-Mode ..."**

## **Scaling in quantum capacitance limit:**

**J Knoch et al IEEE Electron Dev. Lett. 29, 2008 p 372 "Outperforming the Conventional..."**



# Nanowire FETs: Why InAs?

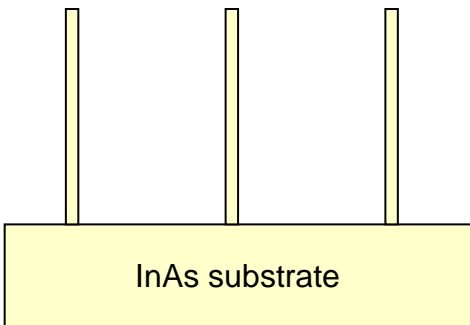
Surface pinning in conduction band and good ohmic contacts!

Material property	Si	GaAs	In <sub>0.53</sub> Ga <sub>0.47</sub> As	InAs	InSb
Electron mobility (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	1500	8500	14000	<b>33000</b>	<b>78000</b>
Saturation velocity (cms <sup>-1</sup> )	1x10 <sup>7</sup>	1.2x10 <sup>7</sup>	8x10 <sup>6</sup>	<b>3.5x10<sup>7</sup></b>	<b>&gt;5x10<sup>7</sup></b>
Band gap (eV)	1.1	1.4	0.75	<b>0.36</b>	<b>0.17</b>
Effective mass	0.19	0.067	0.041	0.023	0.014

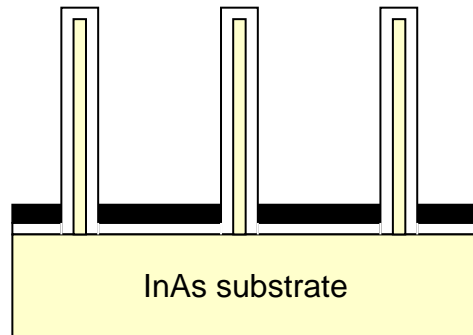


# Processing Flow Short Gate Lengths

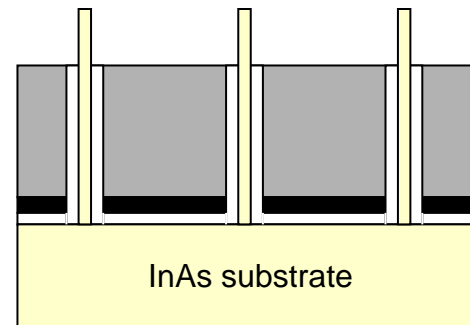
1. Nanowire growth



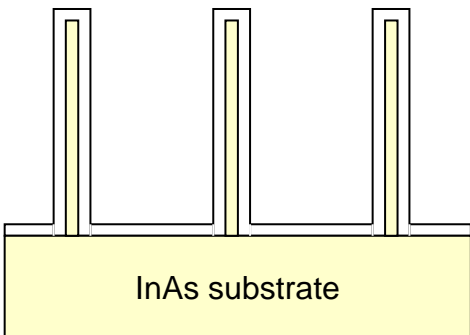
3. Evaporation of gate



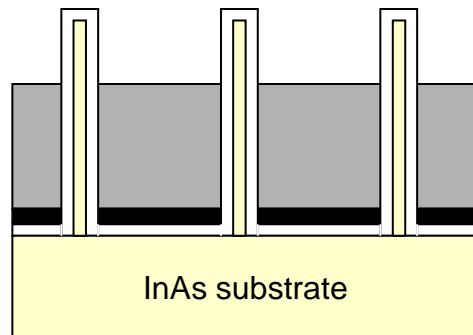
5. Wet etching of drain contacts



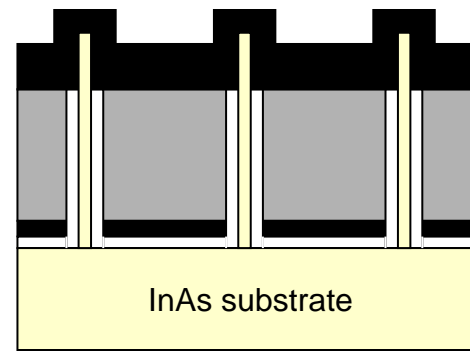
2. Deposition of SiN<sub>x</sub> gate dielectric layer



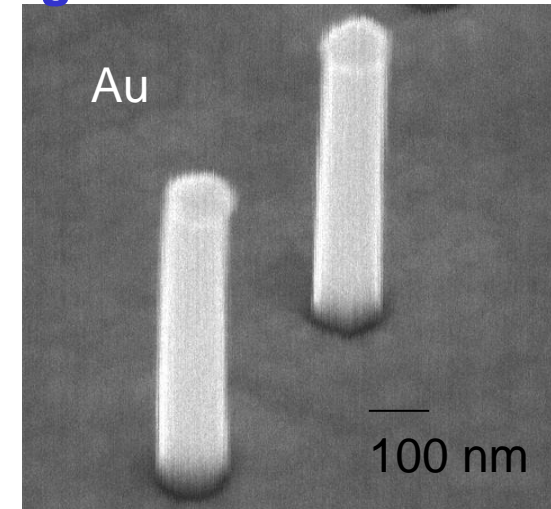
4. Spin-coating with BCB



6. Evaporation of drain contact



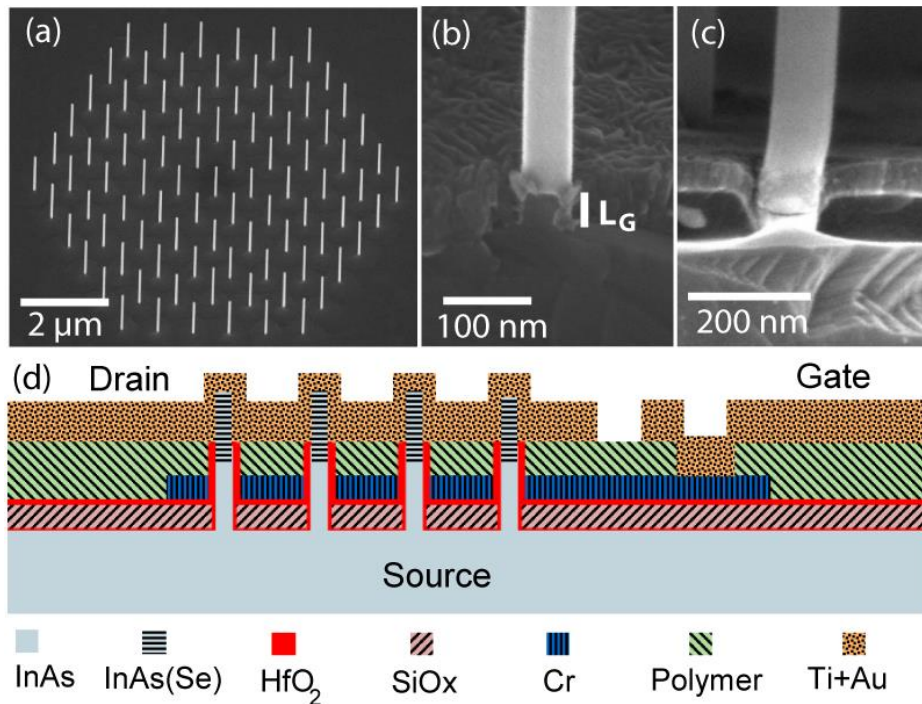
Nanowires after gate formation



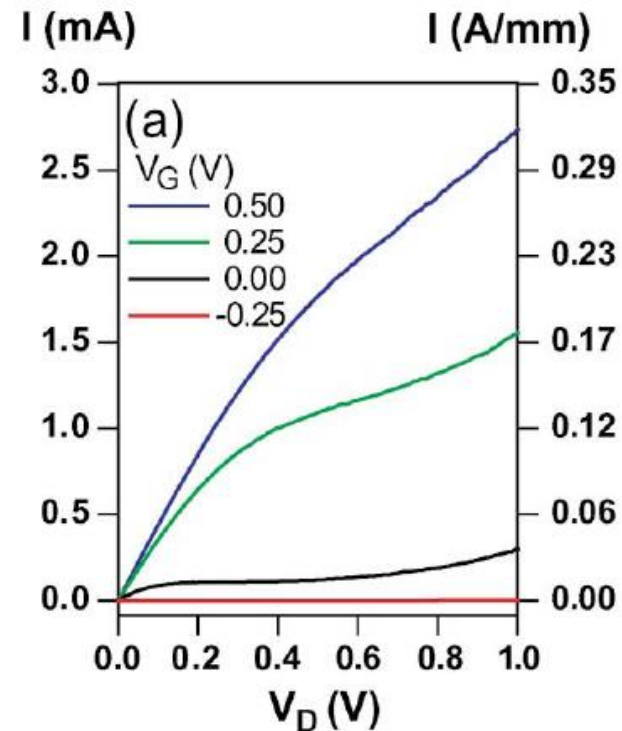
40 nm SiN<sub>x</sub> thickness



# 50 nm $L_g$ Transistors with Elevation Layer



## Good Output Characteristics



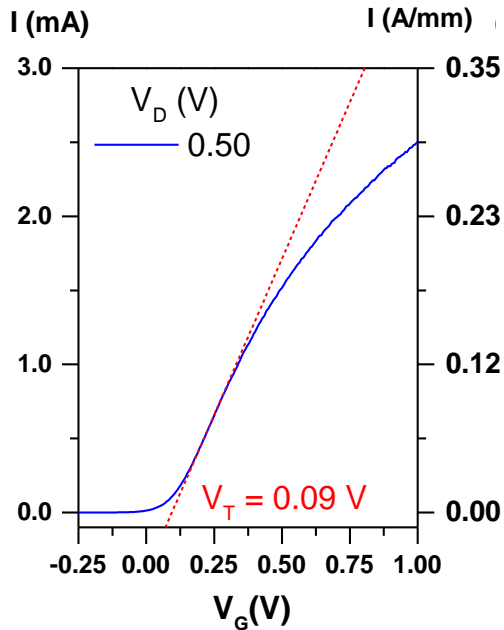
10 nm HfO<sub>2</sub>, 91 Nanowires in matrix  
Processed by QuMat

Thelander et al EDL 2008

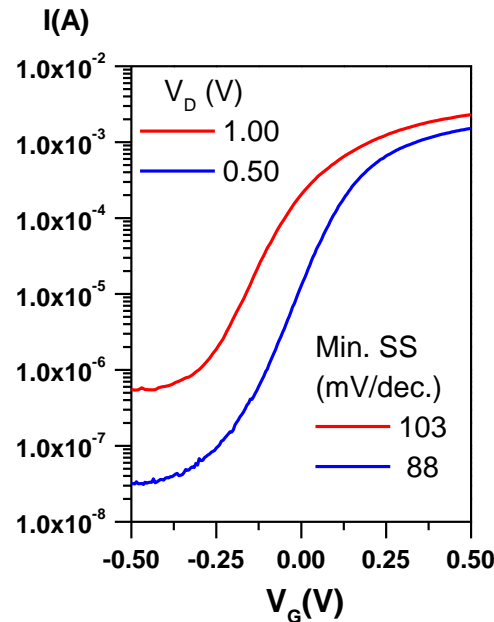


# 50 nm Lg Transistors with Elevation Layer II

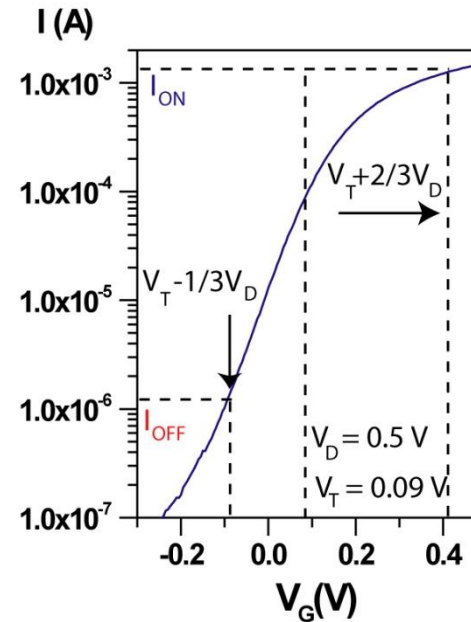
Enhancement mode operation



SS 80mV/dec.  
DIBL 60mV/V  
below 0.7 V



High  $I_{on}/I_{off}$  ratio for  
 $V_d=0.5V$  (>1000)



$V_D$ (V)	Average $V_T$ (V)	Average $g_m$ (S/mm)	Max $g_m$ (S/mm)	Average SS (mV/dec.)	Min. SS (mV/dec.)
0.50	$0.05 \pm 0.05$	$0.44 \pm 0.06$	0.52	$100 \pm 8$	88
1.00	$0.00 \pm 0.04$	$0.58 \pm 0.12$	0.80	$150 \pm 43$	103

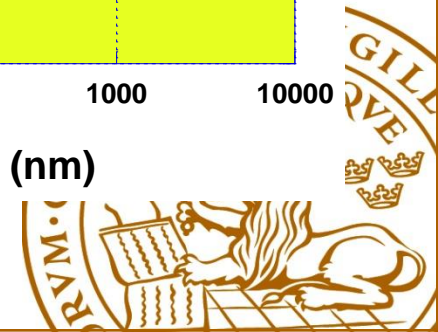
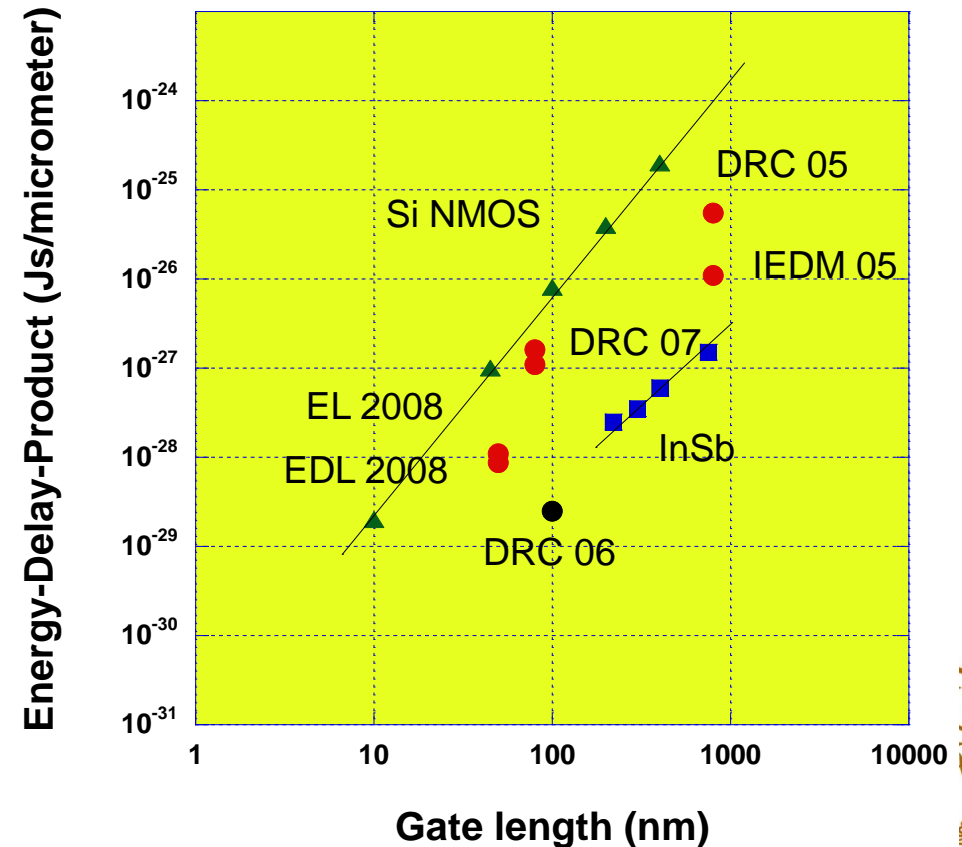
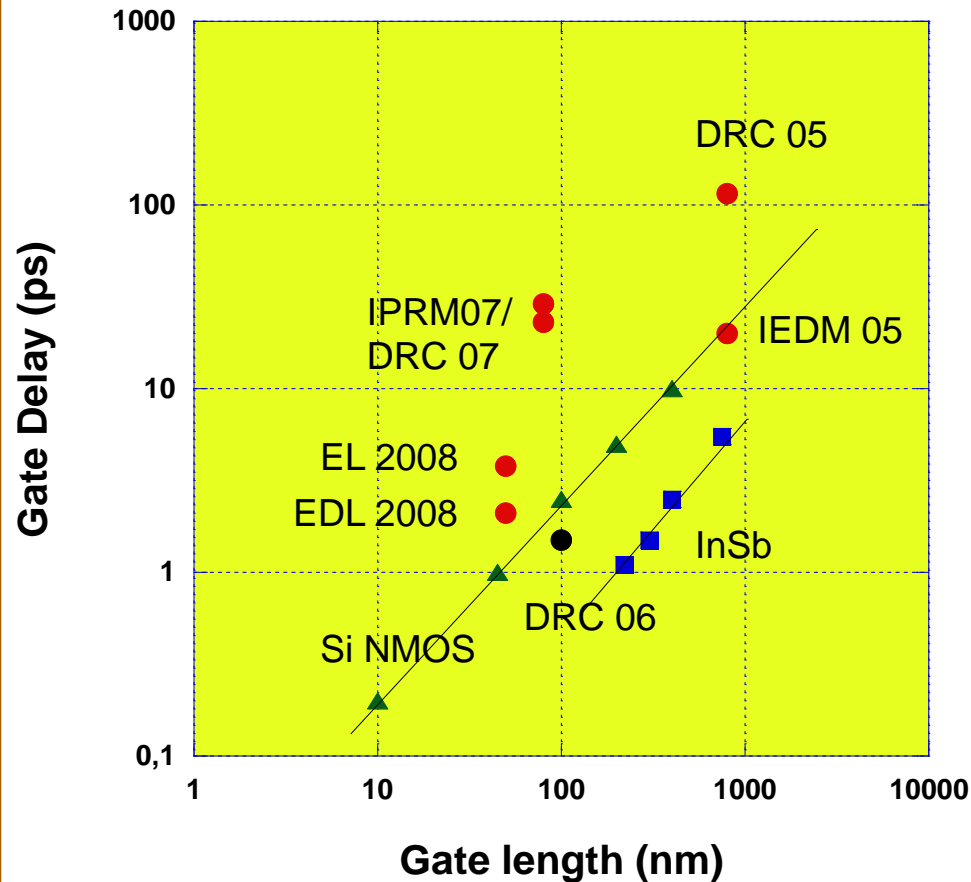
- + High  $g_m$ !
- + Good  $V_t$  control!
- + No gate leakage!
- + Low hysteresis (20mV)!



# Benchmarking: MOS Devices

Gate Delay  $\tau=(CV/I)$

Energy Delay Product  $EDP=\tau*CV^2$



# 20-80nm Channel Length InGaAs Gate-all-around Nanowire MOSFETs with EOT=1.2nm and Lowest SS=63mV/dec

J. J. Gu,<sup>1)</sup> X. W. Wang,<sup>2)</sup> H. Wu,<sup>1)</sup> J. Shao,<sup>3)</sup> A. T. Neal,<sup>1)</sup> M. J. Manfra,<sup>3)</sup> R. G. Gordon,<sup>2)</sup> and P. D. Ye<sup>1)</sup>

<sup>1)</sup> School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47906, U.S.A.

<sup>2)</sup> Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.

<sup>3)</sup> Department of Physics, Purdue University, West Lafayette, IN, 47906, U.S.A.

Tel: 1-765-494-7611, Fax: 1-765-496-7443, Email: [yep@purdue.edu](mailto:yep@purdue.edu), [jjgu@purdue.edu](mailto:jjgu@purdue.edu)

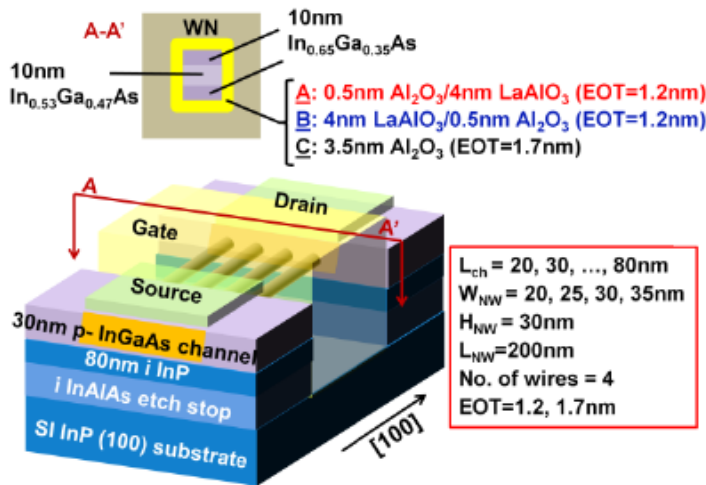


Fig. 1 Device structure, dimension and key parameters of InGaAs GAA MOSFETs.

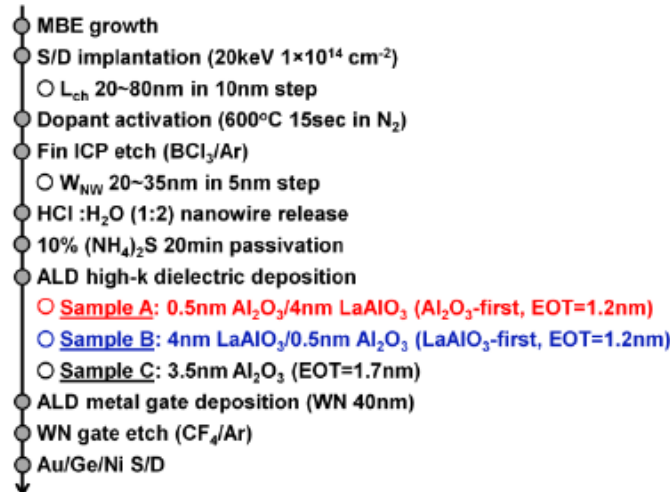


Fig. 2 Fabrication process flow and device splits of InGaAs GAA MOSFETs.

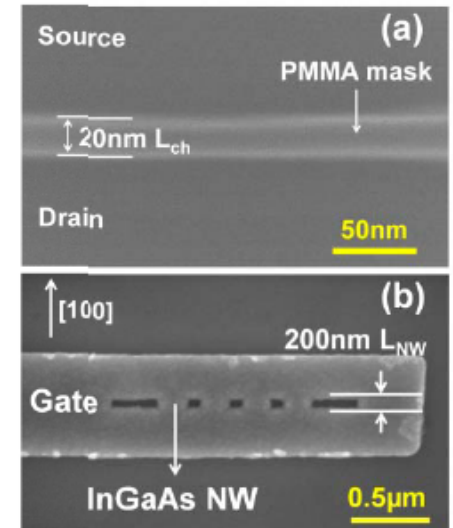


Fig. 3 SEM images of (a) PMMA mask defining 20nm  $L_{ch}$  (b) an InGaAs GAA FET with 4 wires.

Study on scaling of gate length

Gate length 20-80 nm

Nanoelectronics: III-V Nanowires



# Device Performance

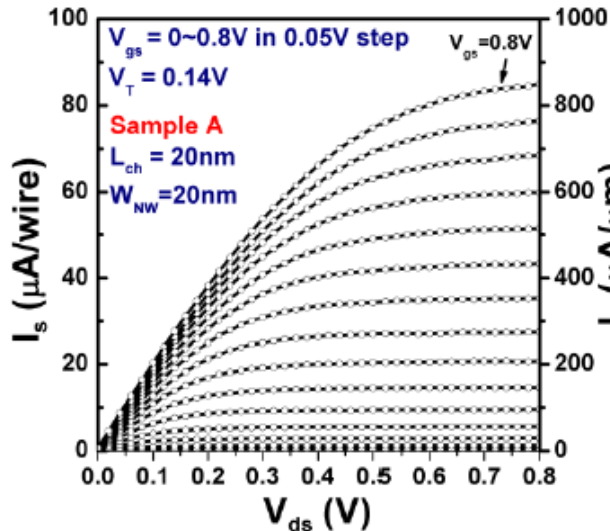


Fig. 4 Output characteristics of a 20nm  $L_{ch}$  InGaAs GAA MOSFET with  $Al_2O_3/LaAlO_3$  gate dielectric (Sample A, EOT=1.2nm) and  $W_{NW}=20nm$ .  $I_s$  is used due to relatively large junction leakage current in  $I_d$ .

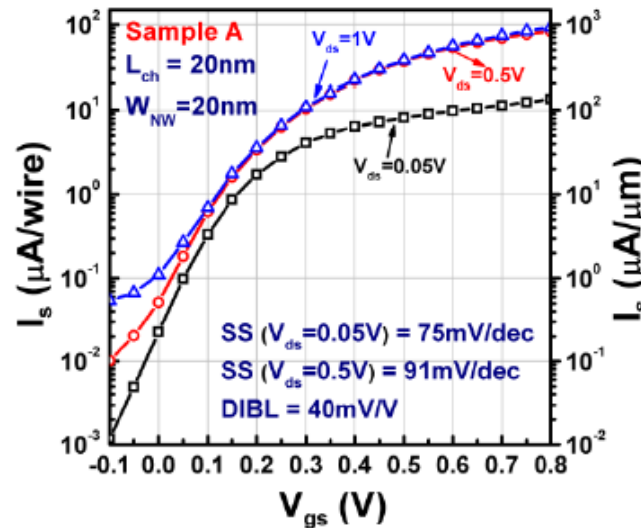


Fig. 5 Transfer characteristics of the same device shown in Fig. 4.  $W_G=100nm$  for  $W_{NW}=20nm$  normalized to perimeter.

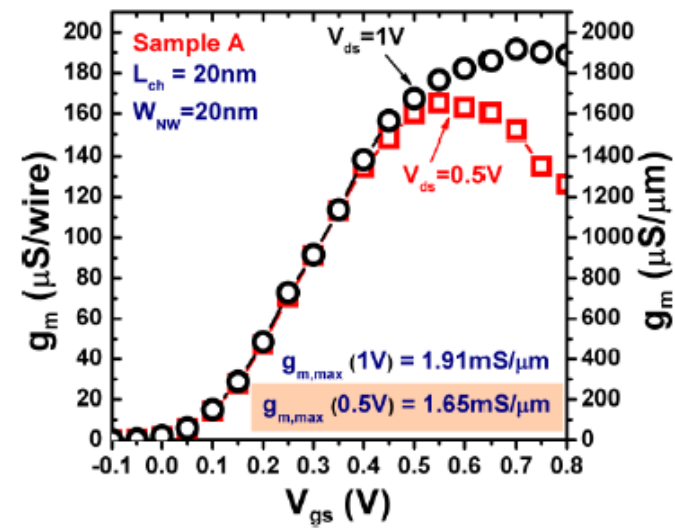


Fig. 6 Transconductance of the same device shown in Fig. 4.

Nanowire diameter 20 nm

Transconductance of 1.7 mS/μm at  $V_d=0.5V$

Drive current of 0.63 mA/μm at  $V_d=0.5V$

SS 75 mV/dec.

Nanoelectronics: III-V Nanowires



# Device Performance II

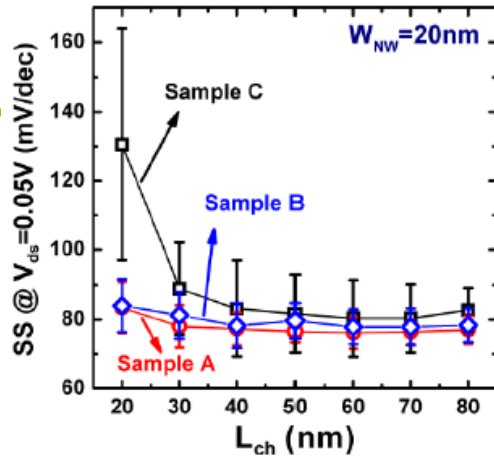


Fig. 19 SS scaling metrics for samples A, B, and C with  $W_{NW}=20\text{nm}$ .

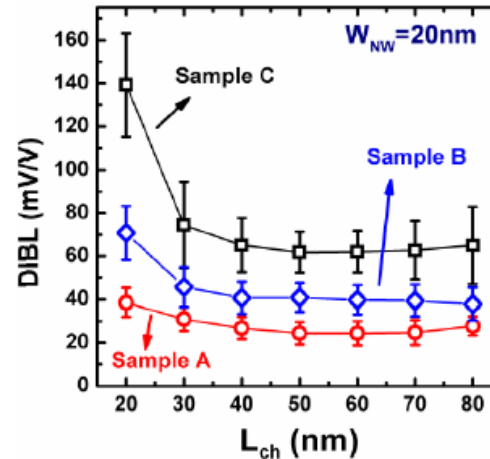


Fig. 20 DIBL scaling metrics for sample A, B, and C with  $W_{NW}=20\text{nm}$ .

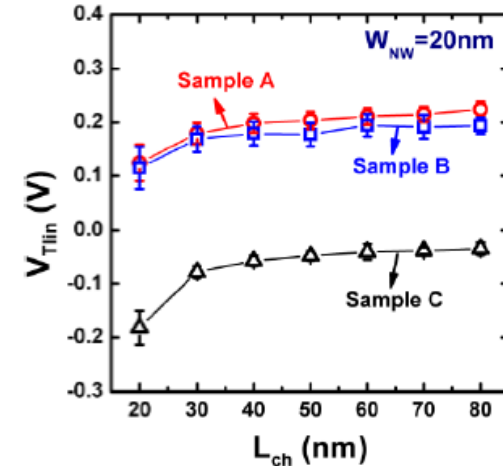


Fig. 21  $V_T$  scaling metrics for sample A, B, and C with  $W_{NW}=20\text{nm}$ .

Excellent scaling  
for SS DIBL, and  $V_t$

Table 1: Performance benchmark of typical non-planar and ETB InGaAs MOSFETs

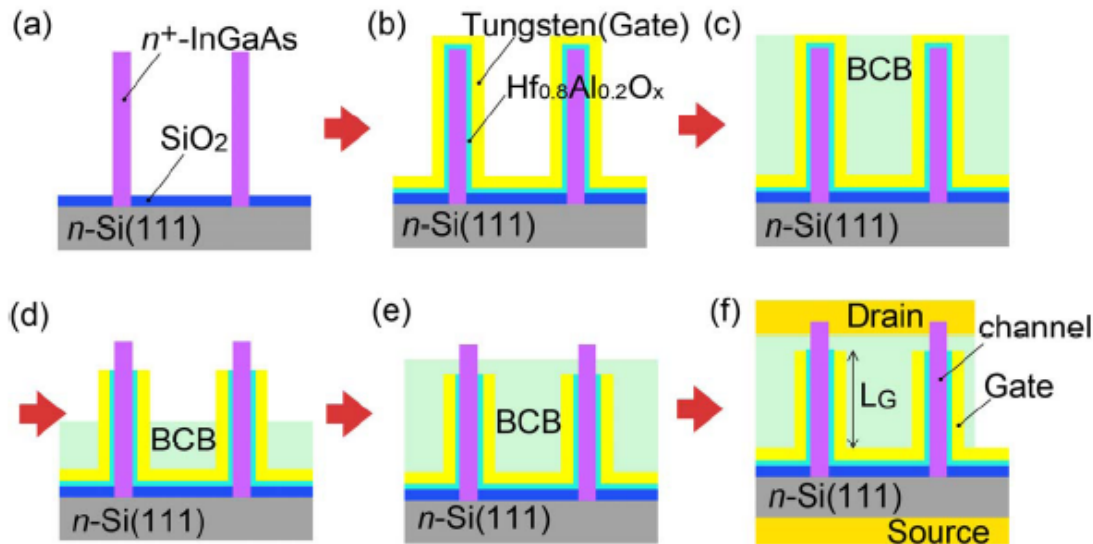
	This work**	Ref. [1]	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [8]
$\text{In}_x\text{Ga}_{1-x}\text{As}$ (x)	0.65	0.53	0.7	0.7	1	0.7	1
Structure	GAA	GAA	Tri-gate	GAA	GAA	FinFET	ETB
Fabrication	Top-down	Top-down	Top-down	Bottom-up	Bottom-up	Top-down	Top-down
$L_{ch,min}$ (nm)	20	50	60	200	100	130	55
$W_{NW(Fin),min}$ (nm)	20	30	30	90	15	220	-
EOT (nm)	1.2	4.5	1.2	1.8*	1.1*	4.5*	3.5
SS [ $V_{ds}=0.5\text{V}$ ] (mV/dec)	88	245	94*	98	140	-	-
SS [ $V_{ds}=0.05\text{V}$ ] (mV/dec)	63	145	66	90*	-	230*	105
DIBL (mV/V)	7	210	60*	170*	60	135	84
$g_{m,max}$ (mS/ $\mu\text{m}$ ) [ $V_{ds}=0.5\text{V}$ ]	1.74	0.45	-	-	1.23	-	-

\*Extracted/estimated from literature

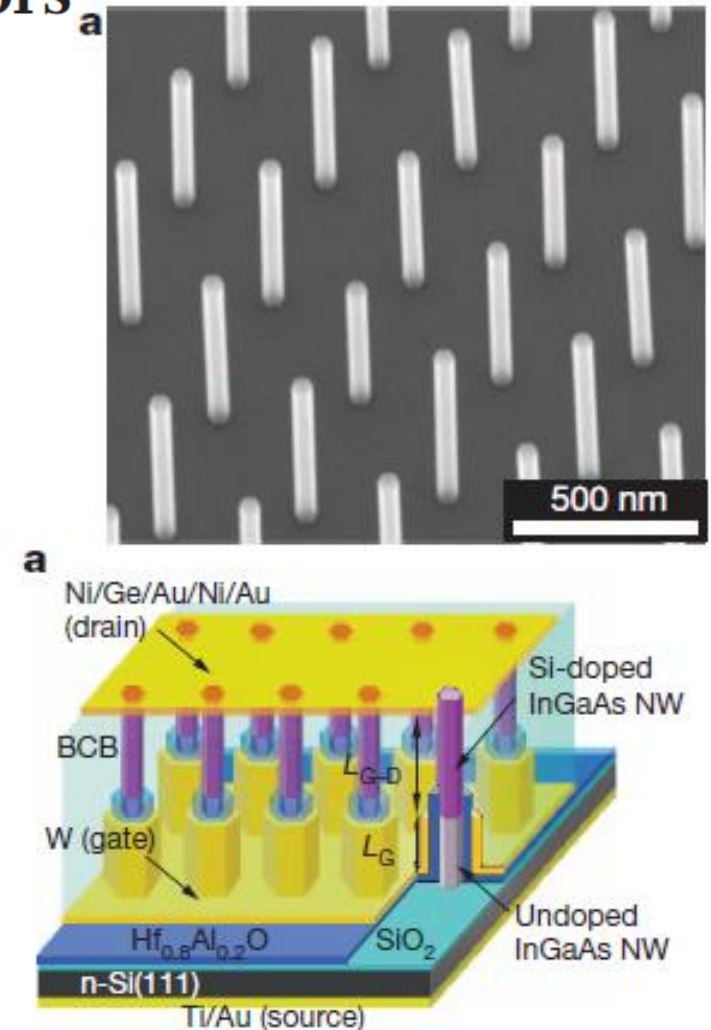
\*\*Reported values are best from all measured devices

## A III–V nanowire channel on silicon for high-performance vertical transistors

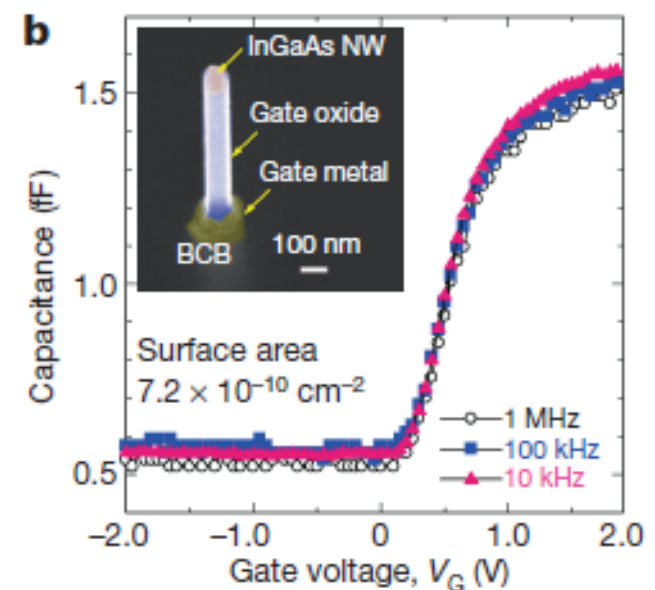
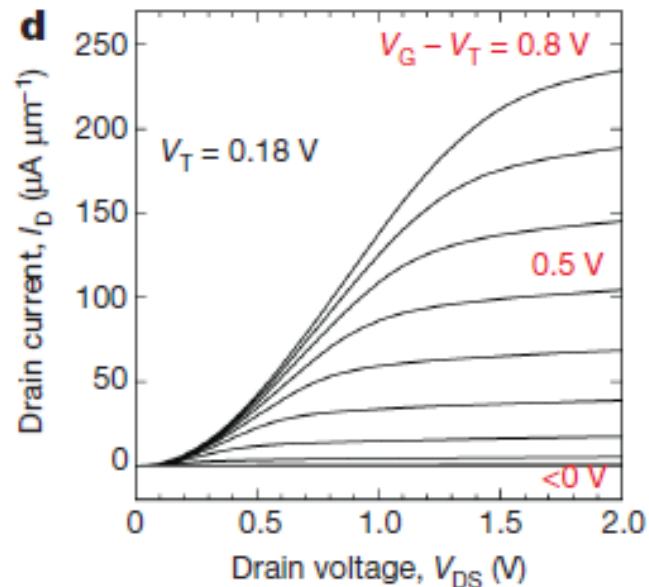
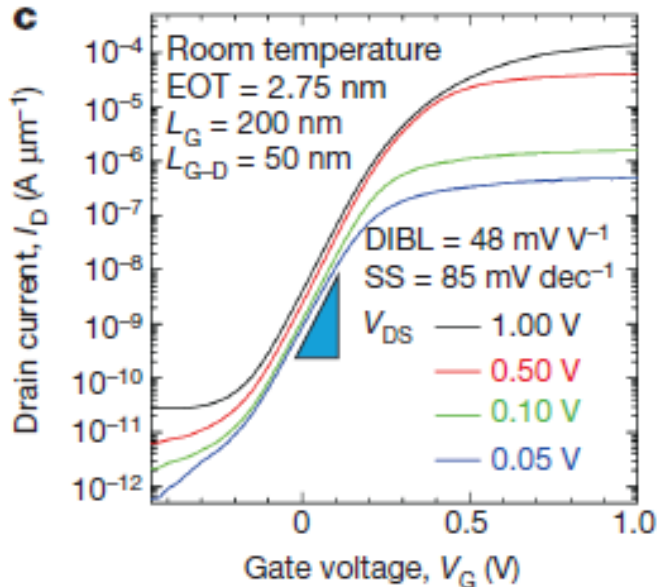
Katsuhiro Tomioka<sup>1,2</sup>, Masatoshi Yoshimura<sup>1</sup> & Takashi Fukui<sup>1</sup>



**Figure 3:** Device fabrication processes: (a) InGaAs NW growth. (b) Atomic layer deposition of  $\text{Hf}_{0.8}\text{Al}_{0.2}\text{O}_x$  and sputtering of W-gate metal. (c) Spin-coating of BCB polymer. (d) RIE of BCB, gate oxide and W metal. (e) Spin-coating of BCB and RIE etch back for electrical separation layer formation. (f) Drain and source metal evaporation.



# Device Performance



Gate length 200 nm

Nanowire diameter 60 nm

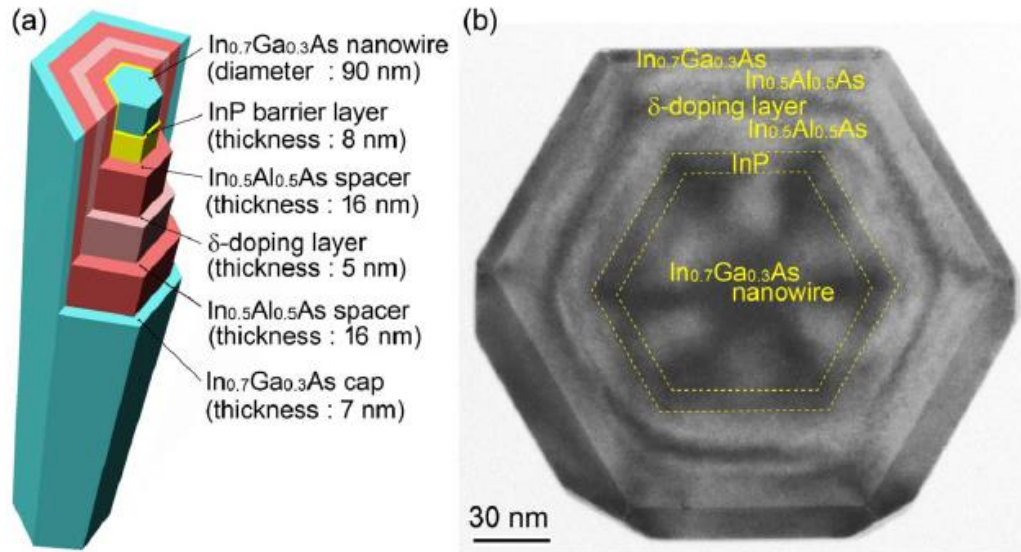
10 nanowires in the array

Transconductance of 280  $\mu\text{S}/\mu\text{m}$  at  $V_d=1\text{V}$

SS 98 mV/dec.

Nanoelectronics: III-V Nanowires

# Device Performance



**Figure 9:** (a) Illustration of InGaAs/InP/InAlAs/ $\delta$ -doped InAlAs/InAlAs/InGaAs core-multishell NW. (b) Cross-section TEM image of the growth results of Fig. 9(a). The InGaAs NW is 90 nm in diameter.

Gate length 200 nm

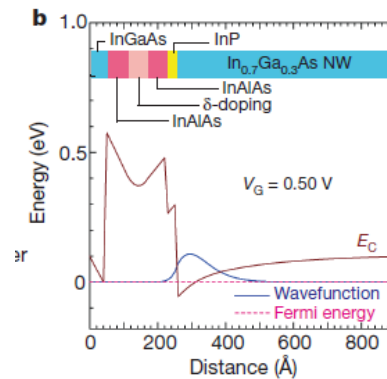
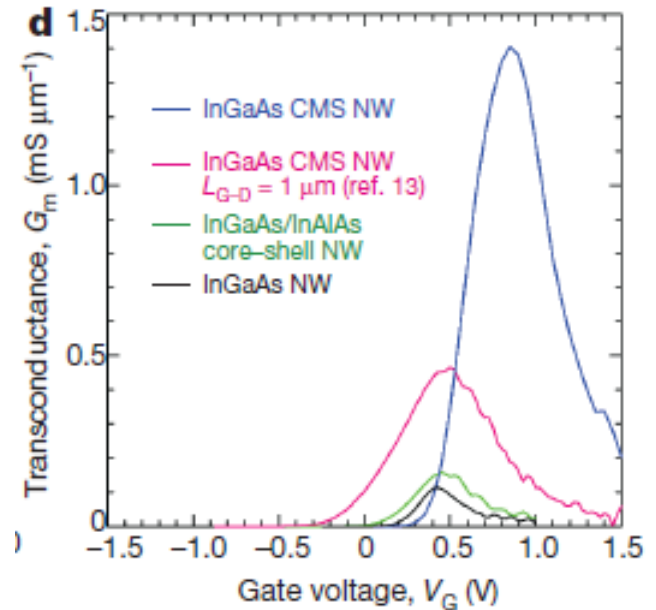
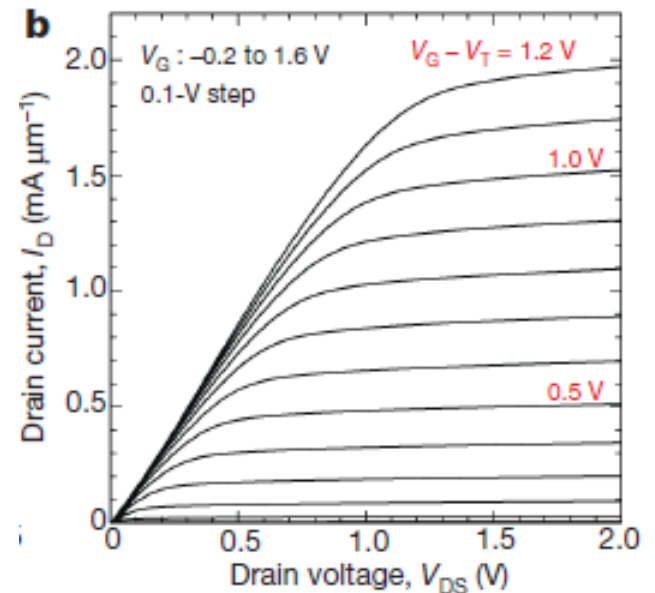
Nanowire diameter 90 nm

10 nanowires in the array

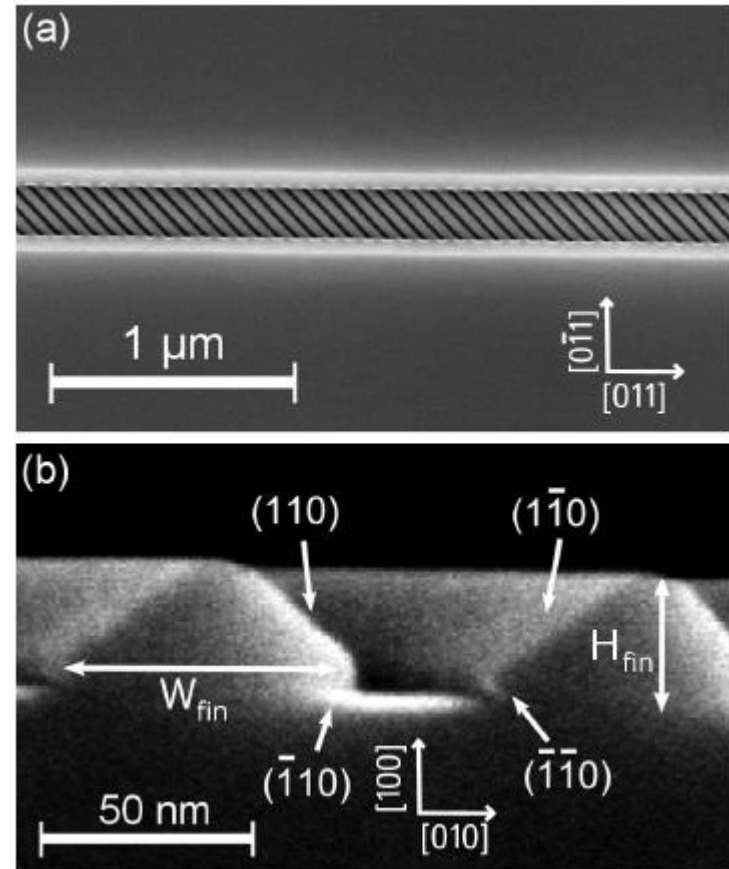
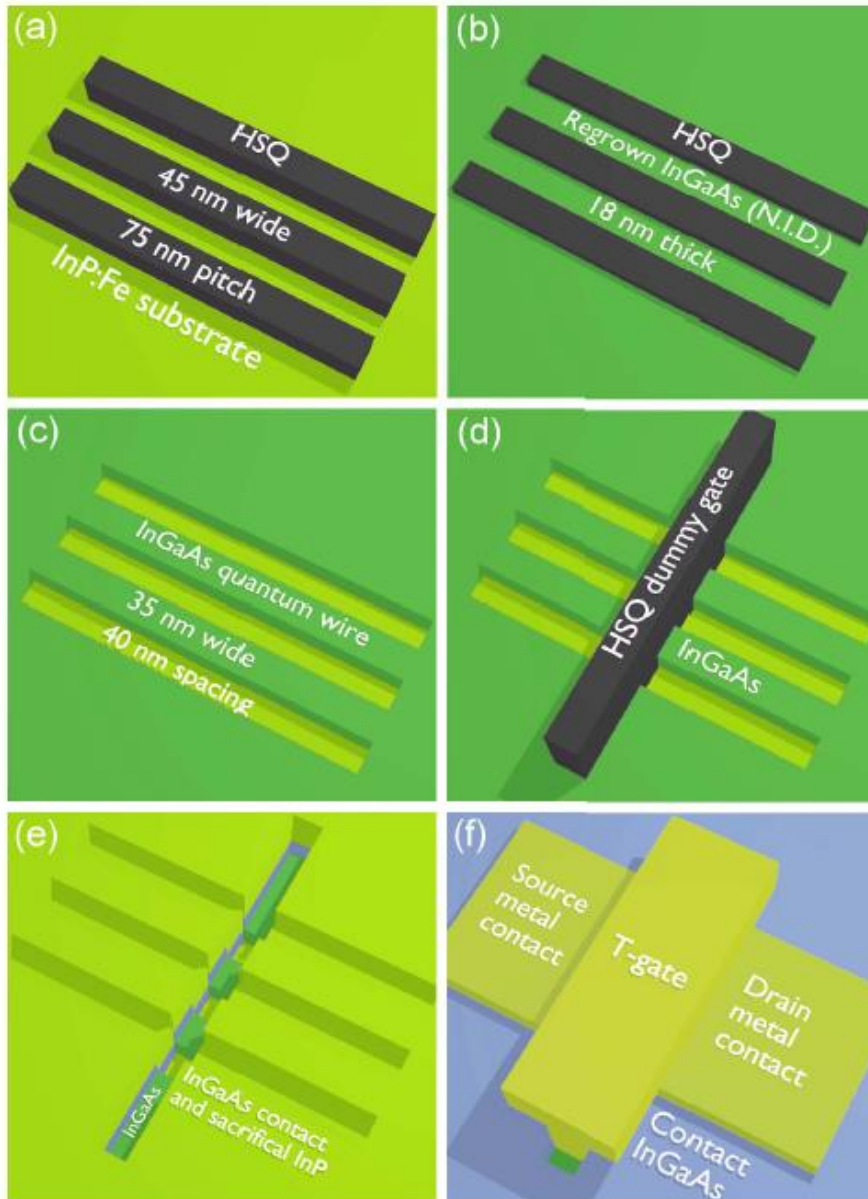
$g_m = 1.42 \text{ mS}/\mu\text{m}$  at  $V_d = 0.5 \text{ V}$

SS 75 mV/dec.

Nanoelectronics: III-V Nanowires

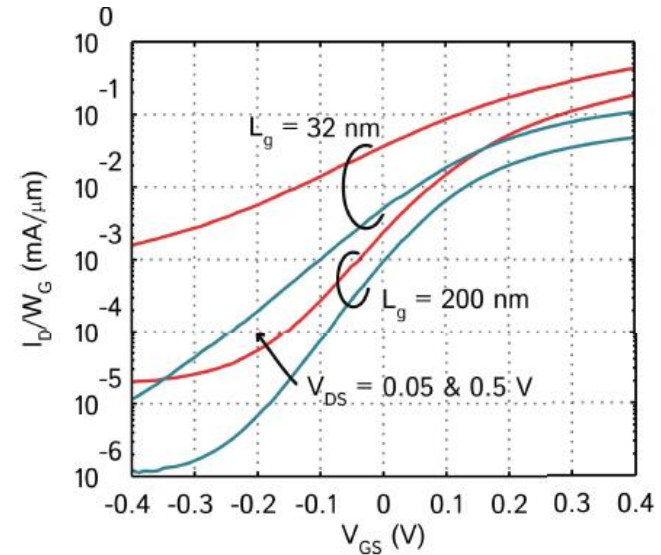
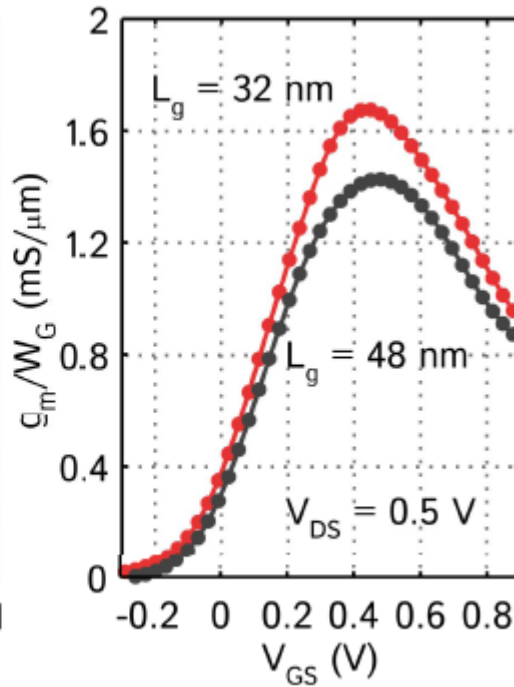
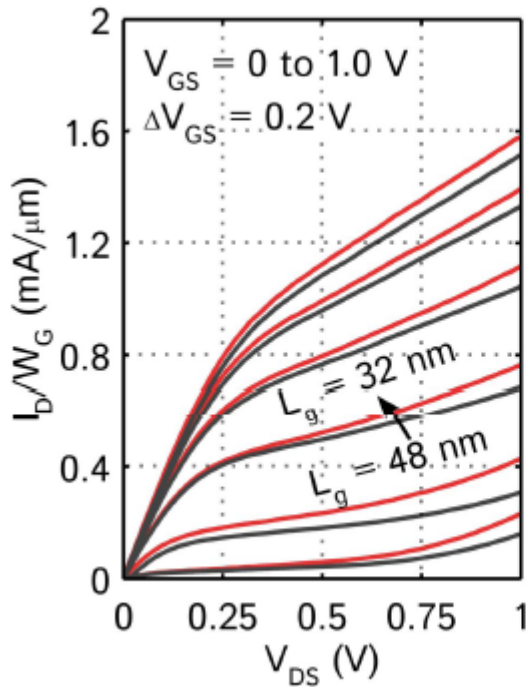


# Lateral Nanowires



MOVPE selective area growth  
 Nanowire dimensions 15x40 nm

# Lateral Nanowires



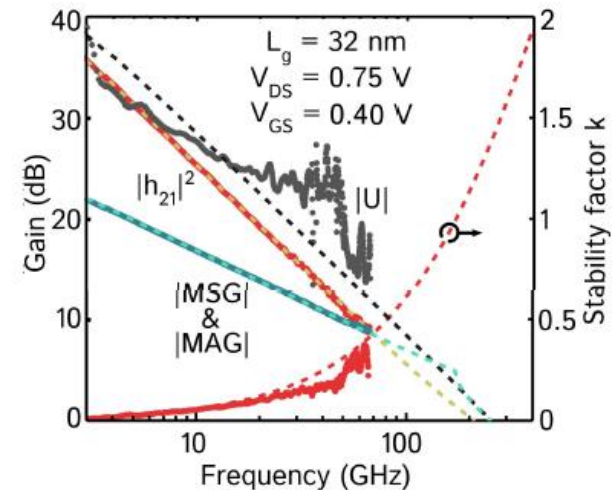
Gate length 32- 200 nm

Transconductance of 1700  $\mu\text{S}/\mu\text{m}$  at  $V_d=0.5\text{V}$

SS 85 mV/dec.

$f_t/f_{max}$  210/250 GHz

Nanoelectronics: III-V Nanowires

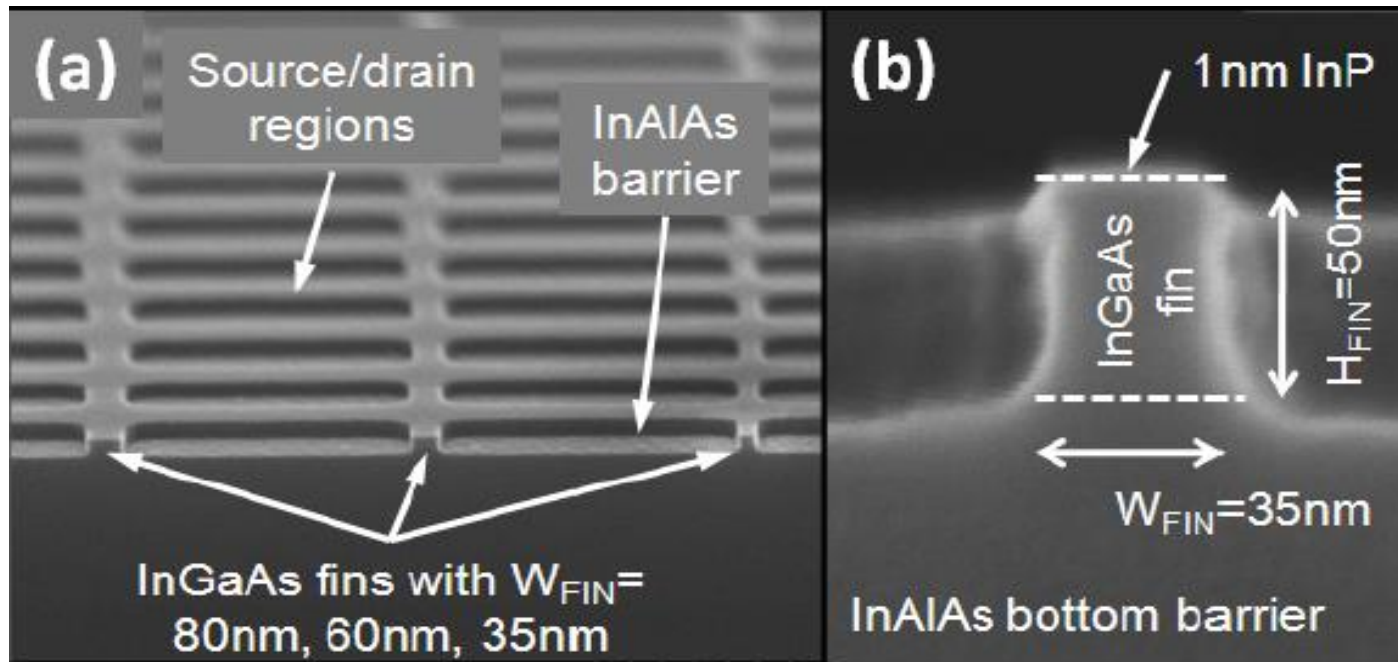


# Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications

M. Radosavljevic, G. Dewey, J. M. Fastenau\*, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu\*, D. Lubyshev\*, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, and Robert Chau

Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

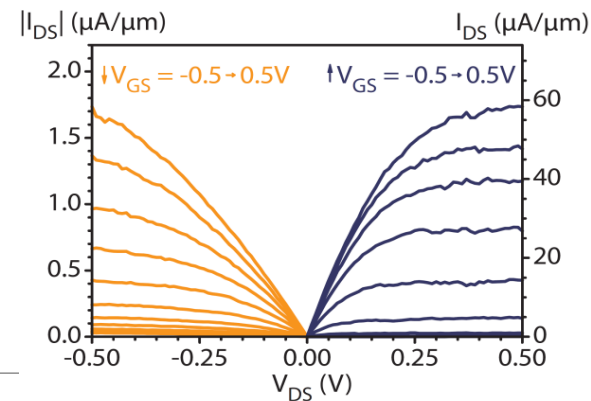
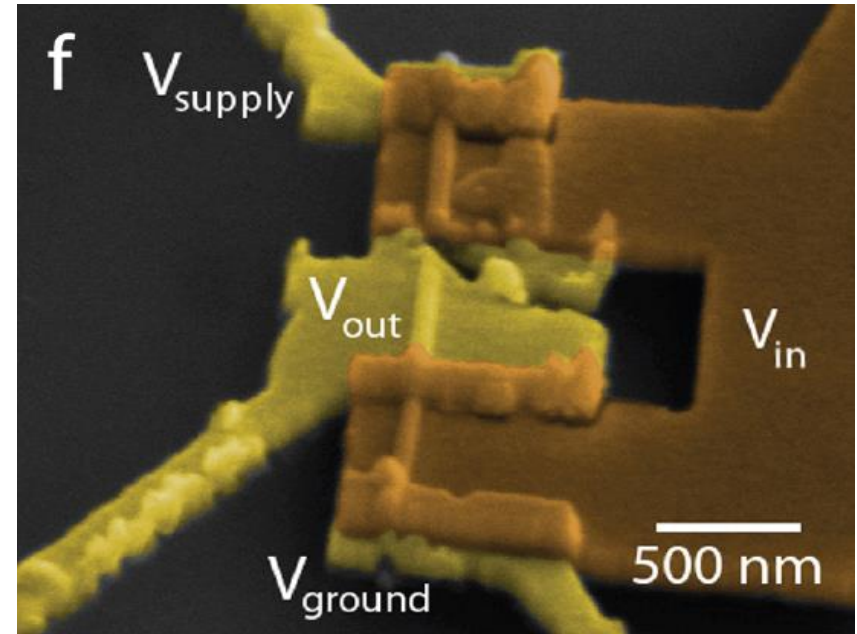
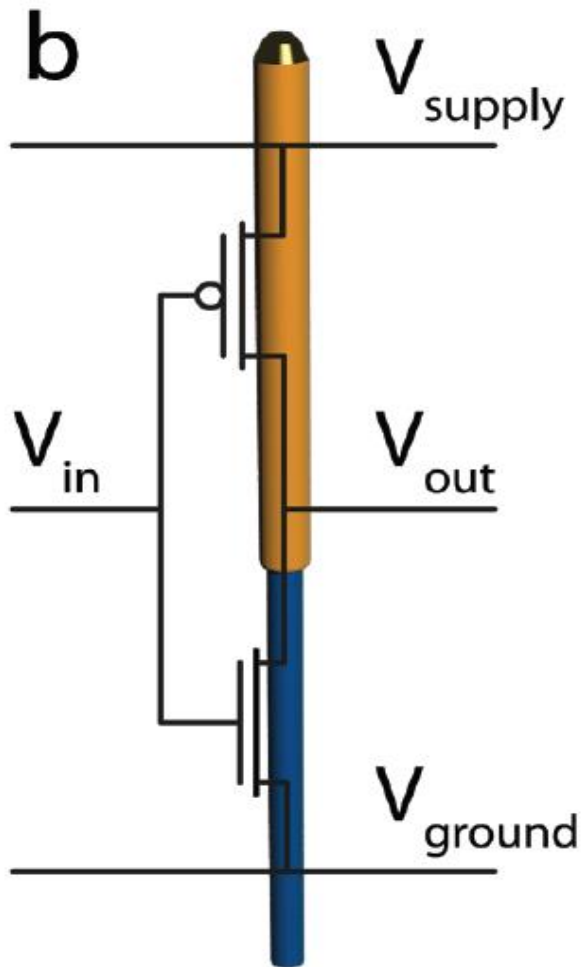
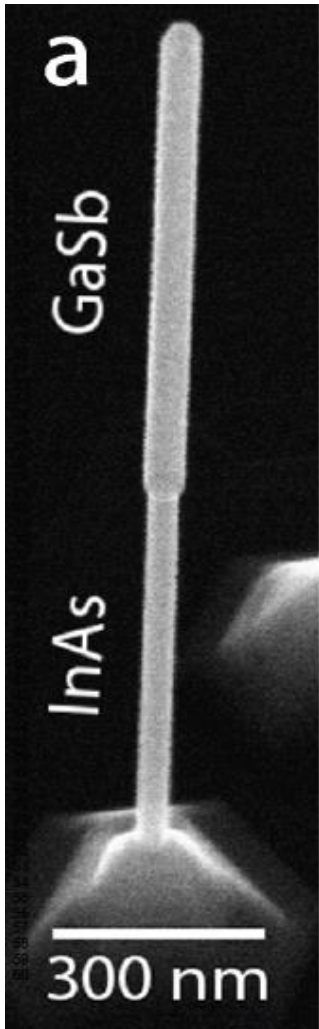
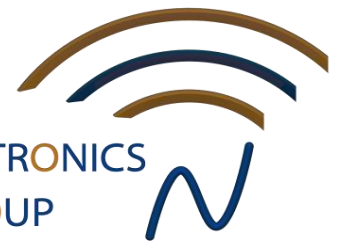
\* IQE Inc, Bethlehem, PA 18015, USA



Intel IEDM 2010:

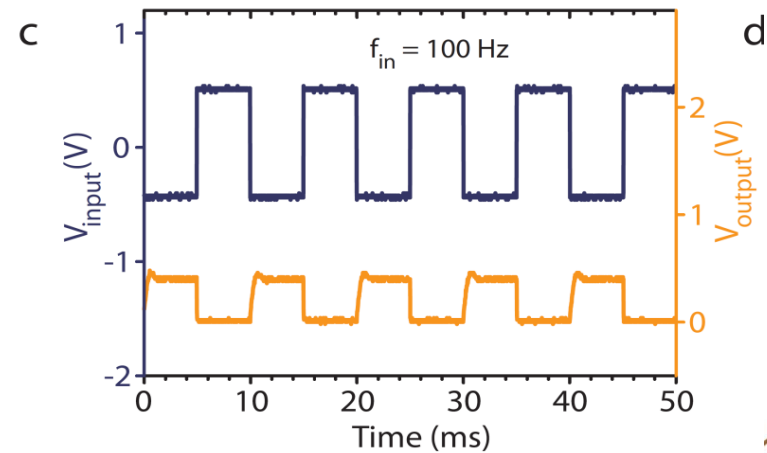
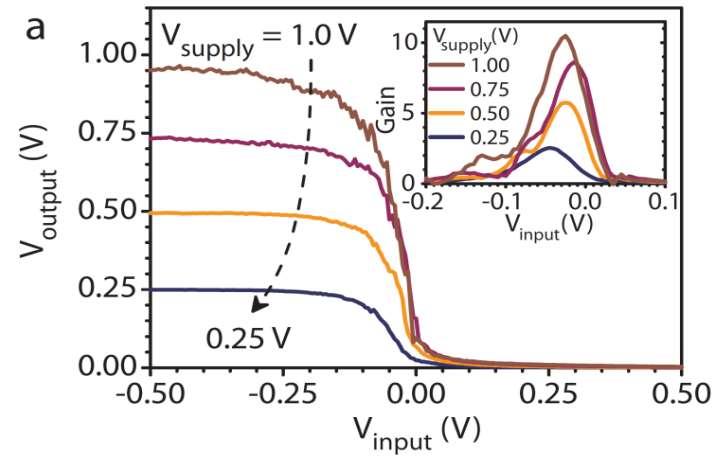
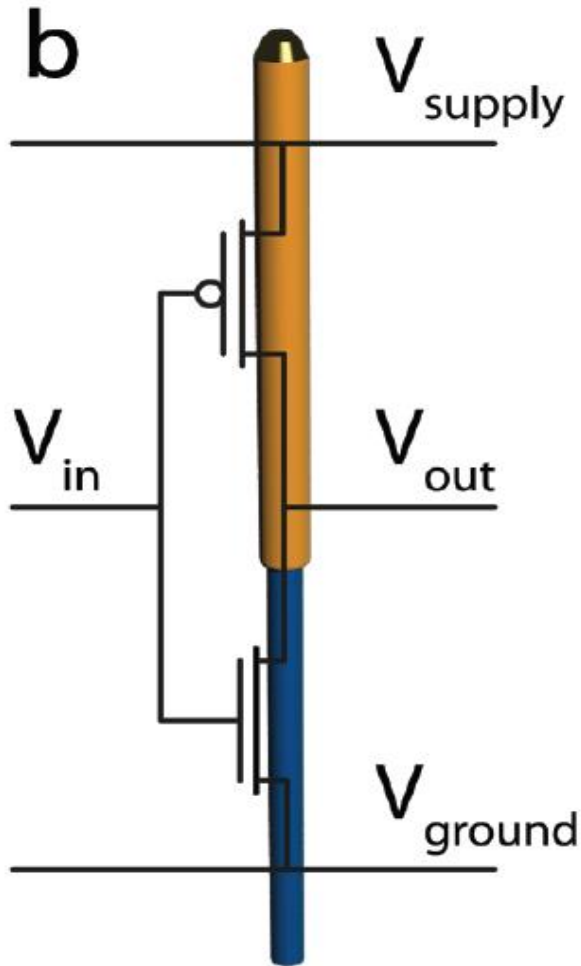
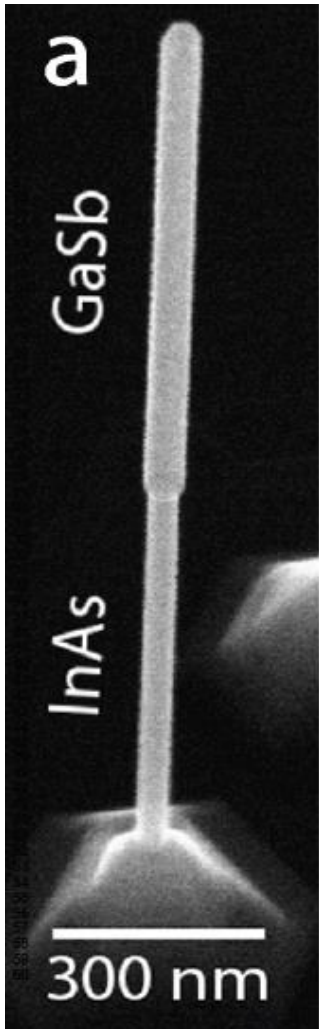
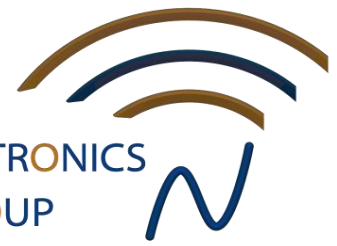


# Nanowire Inverters





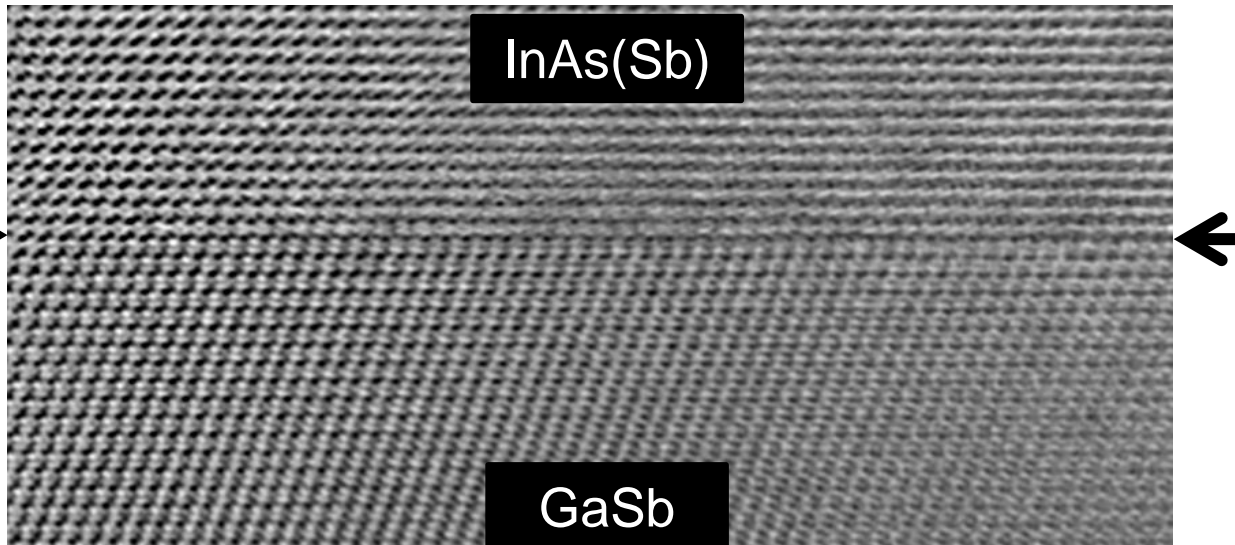
# Nanowire Inverters



# VERY abrupt heterojunction!

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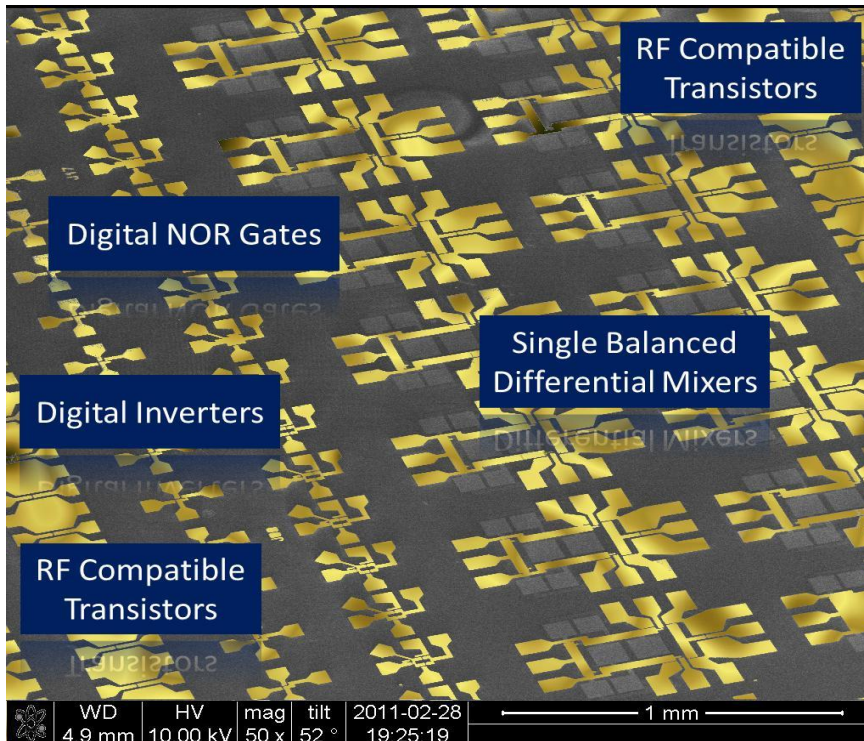
Sudden group-V contrast change indicates abrupt transition



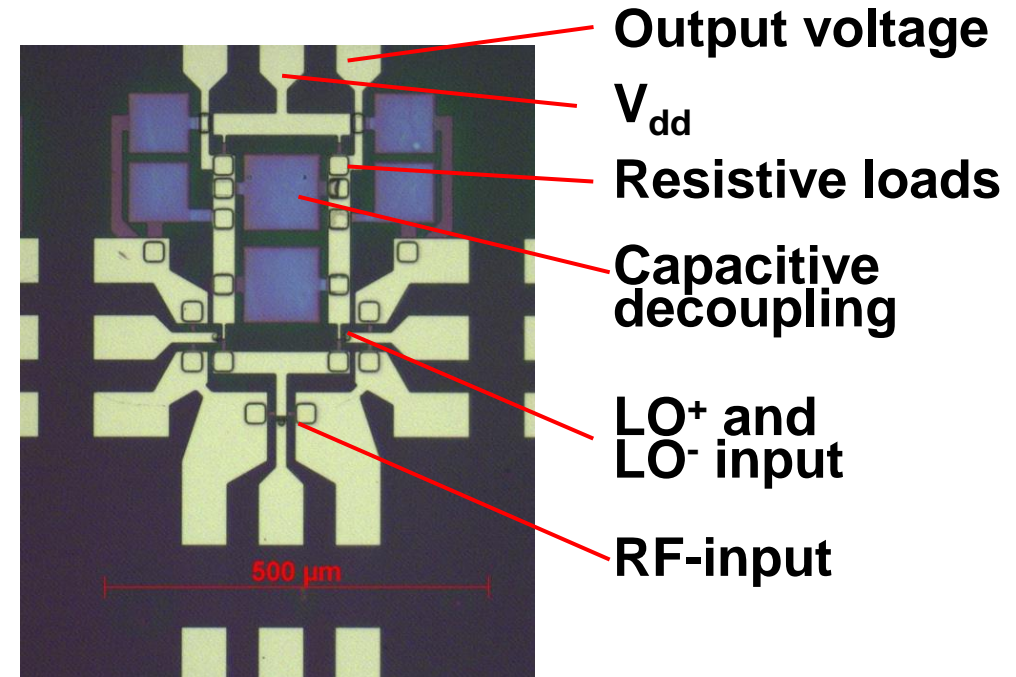
*Courtesy of Martin Ek*

# InAs Circuits on 2" Si

Good wafers: 80% yield  
Area: 2000x6000  $\mu\text{m}^2$



First test circuit:  
Balanced mixer



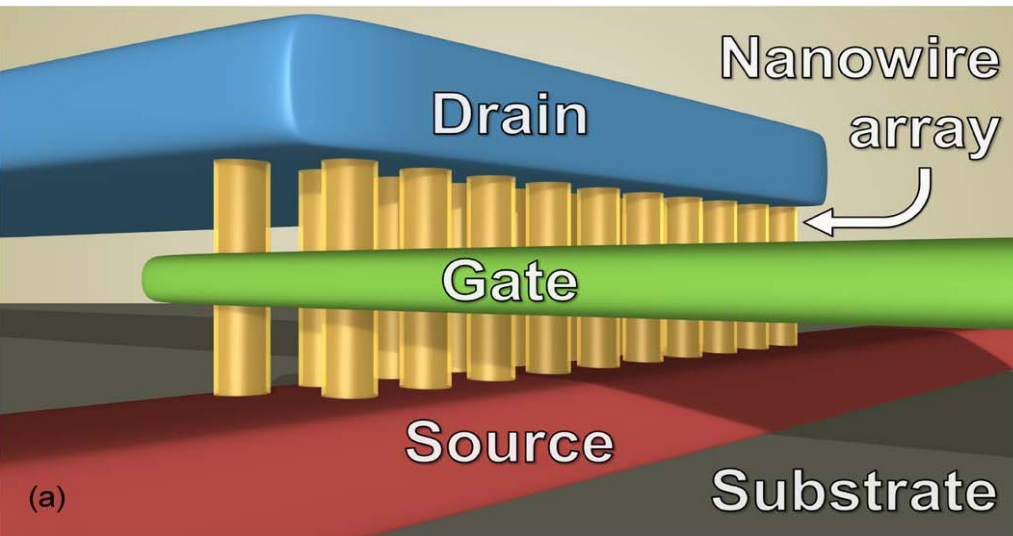
Design with 52 nanowire transistors  
Nanowire resistors  
Designed for 1 GHz input



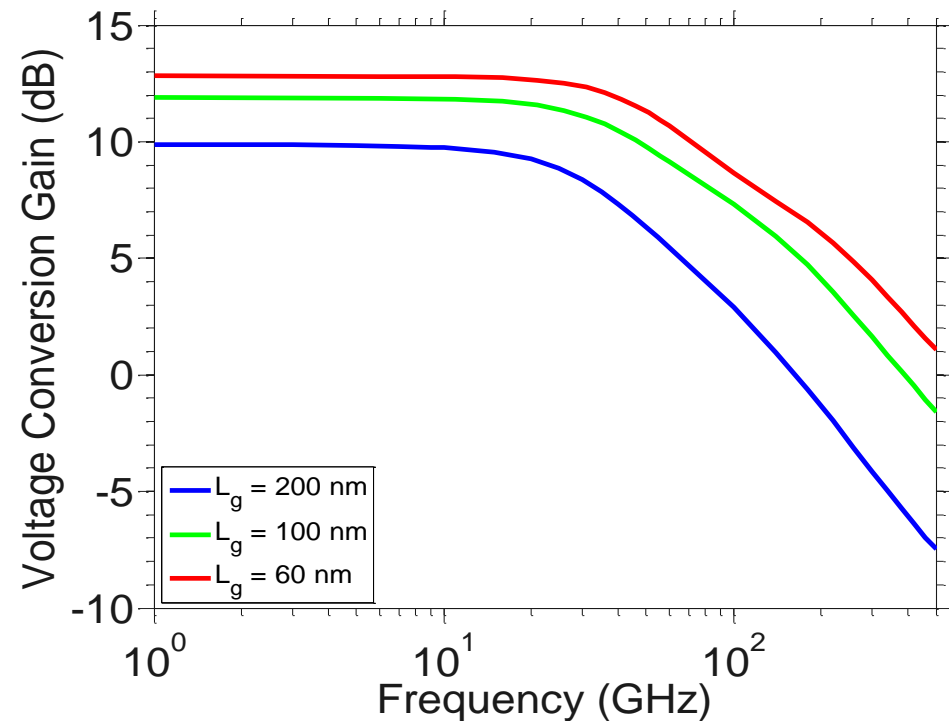
# InAs Circuits on 2" Si



## Device Architecture



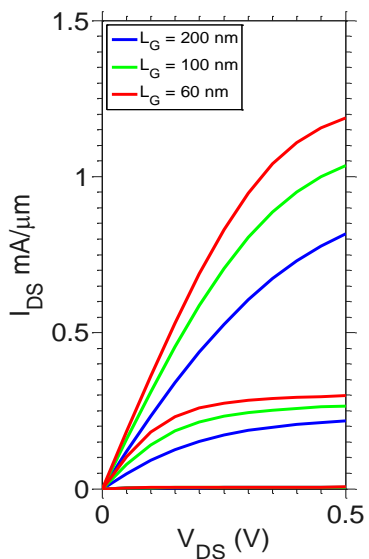
## Mixer Performance



## Transistor Performance

RF FET: 36 NWs (6x6 array)  
LO FET: 72 NWs (12x6 array)  
NW Spacing: 200 nm  
 $L_g$ : 200 nm, 100 nm, 60 nm

$R_L$ : 2.5 k $\Omega$   
 $V_{DD}$  = 1.5 V  
 $P_{DC}$  = 1 mW



# Outperforming the Conventional Scaling Rules in the Quantum-Capacitance Limit

J. Knoch, W. Riess, and J. Appenzeller, *Senior Member*,

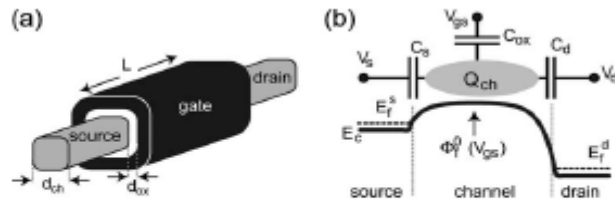


Fig. 1. (a) Schematics of the wrap-gate transistor design under consideration. (b) Surface potential along the direction of current transport. The total charge in the channel is determined by all terminal voltages.

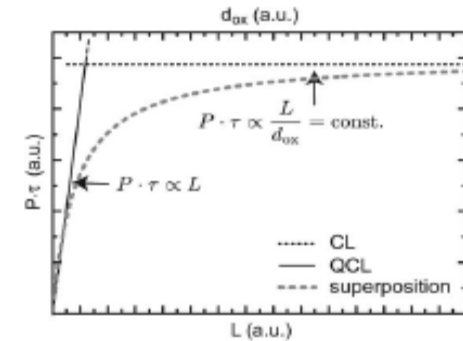


Fig. 2. Power delay product as a function of  $L$  and  $d_{ox}$ . The horizontal black dotted line shows the CL, where  $P \cdot \tau = \text{const.}$ , and the straight black line belongs to the QCL with  $P \cdot \tau \propto L$ . The gray dashed line is the superposition of the two limiting curves showing an increasing scaling benefit in the QCL.

	Gate delay (diffusive) $\tau = C_g V_{dd} / I_d$	Gate delay (ballistic) $\tau = C_g V_{dd} / I_d$	Power –delay product
Classical Limit, CL	$\tau \sim L^2$	$\tau \sim L$	constant
Quantum Capacitance Limit, QCL	$\tau \sim L^2$	$\tau \sim L$	$P^* \tau \sim L$

$$I_d \propto \frac{l_{scat}}{l_{scat} + L} \frac{1}{L} \frac{C_{ox} C_q}{C_{ox} + C_q} (V_{gs} - V_t) v_{inj}$$



# Simulated performance

## Movement of the band with the gate bias

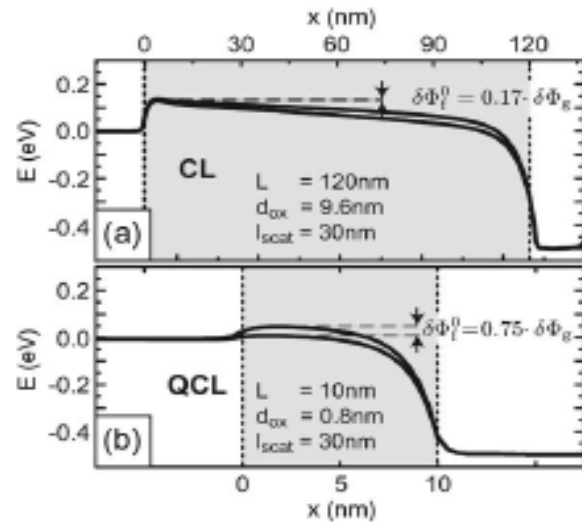
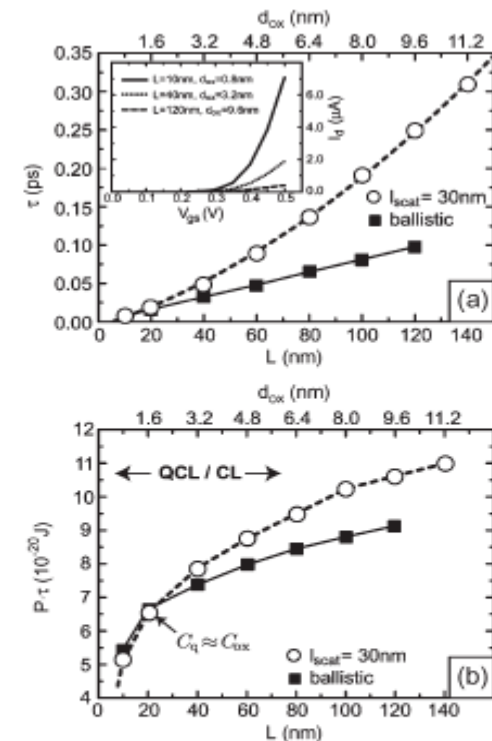


Fig. 3. Conduction band profile for (a) a device with  $L = 120$  nm and  $d_{\text{ox}} = 9.6$  nm and (b) for a FET with  $L = 10$  nm and  $d_{\text{ox}} = 0.8$  nm showing that (a) is rather in the CL, whereas (b) is scaled toward the QCL. Here  $V_{\text{ds}} = 0.5$  V, and  $V_{\text{gs}} = 0.5$  and  $0.55$  V.

Simulations of devices were carried out with the following parameters:  $E_f^{\text{ss,d}} = 0.1$  eV,  $m^* = 0.1m_0$ , and  $d_{\text{ch}} = 3$  nm; a midgap work-function metal was assumed as gate electrode, and  $\Phi_{\text{bi}} = 0.4$  eV. Furthermore,  $\epsilon_{\text{ox}} = 3.9$ , and  $\epsilon_{\text{ch}} = 12$ .

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## QCL vs CL limit



$$\tau = \int Q dV_{\text{gs}} / (V_{\text{dd}} I_d)$$

$$P \cdot \tau = \int Q dV_{\text{gs}}$$

Fig. 4. (a) Gate delay extracted from simulations versus  $L$ ,  $d_{\text{ox}}$  for (hollow circles) scattering and (solid black squares) ballistic transport. The dashed black line is a quadratic fit to the data points. In the case of ballistic transport, the data points lie on a straight line. (b) Simulated  $P \cdot \tau$  as a function of  $L$  and  $d_{\text{ox}}$ . The curves exhibit the same behavior as shown in Fig. 2, implying a significant scaling benefit in the QCL.