High-Speed Circuits and QCAs

Circuit configurations:
- Digital applications
  - CMOS
  - E/D-mode logic
  - Current mode logic
- RF applications
  - nFET drivers
  - Resistive, inductive, or active loads

Emerging technologies:
- QCA
- MEMS
- Molecular electronics
- …

Inverters With Strained Si Nanowire Complementary Tunnel Field-Effect Transistors

Lars Knoll, Qing-Tai Zhao, *Member, IEEE*, Alexander Nichau, Stefan Trellenkamp, Simon Richter, Anna Schäfer, David Esseni, Luca Selmi, Konstantin K. Bourdelle, and Siegfried Mantl, *Member, IEEE*

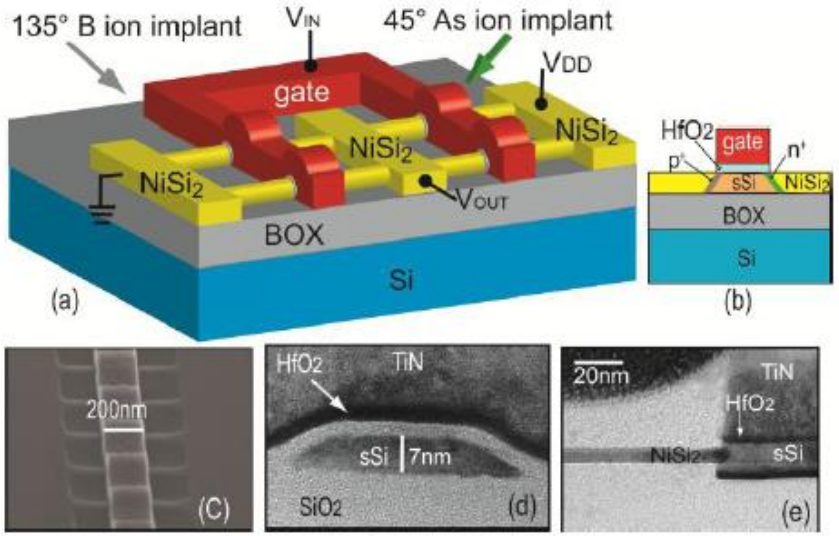

Fig.1 (a) Schematic of sSi NW TFET inverter fabricated using tilted B^+ and As^+ ion implantations into epitaxial $NiSi_2$ S/D contacts. Highly doped n+ and p+ pockets at the silicide edges are created with IIS after a low temperature anneal (b), forming an n-TFET on the left and a p-TFET on the right in Fig.1(a). (c) SEM image of the NW array TFET; (d) XTEM image of single sSi nanowire with gate stack. (e) XTEM cross section along the NW, indicating a perfectly aligned $NiSi_2$ contact to the channel.

Implantation used to form shallow junctions with low temperature annealing (450 C)

$NiSi_2$ leads to reduce resistance (silicidation of thin Ni layer 3 nm)

Inverter configuration

Na

Device Performance

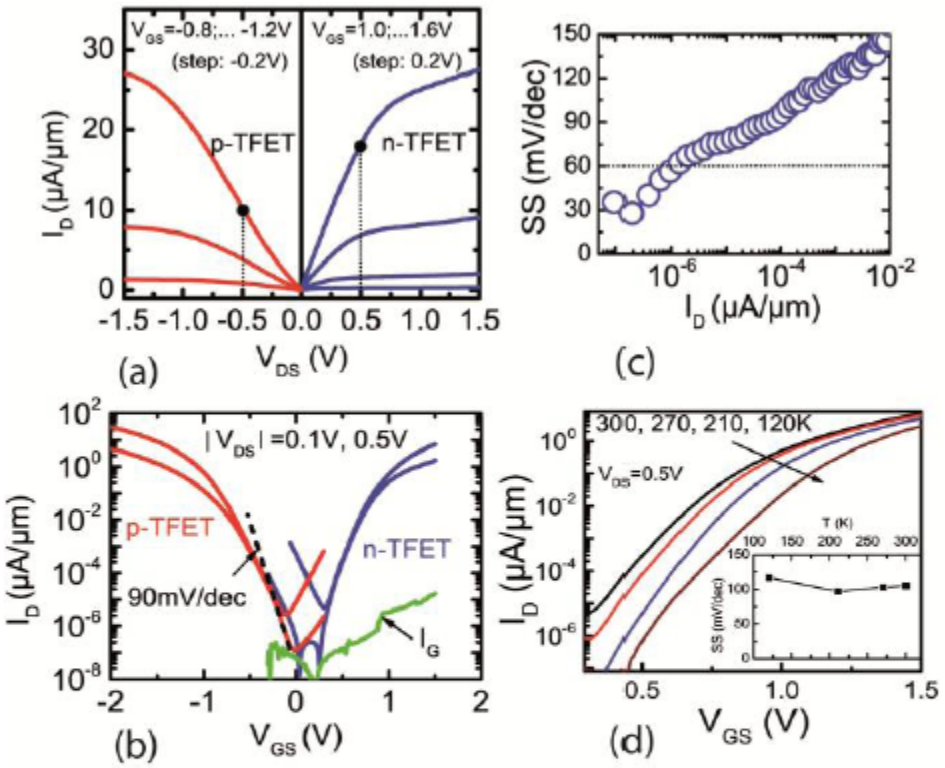

Fig.2. (a) I_D-V_{DS} characteristics of NW array C-TFETs showing high on-currents; (b) The corresponding I_D-V_{GS} characteristics of sSi NW array C-TFETs, providing a minimum SS of 30 mV/dec for the n-FET(c), and of 90 mV/dec for the p-TFETs at 300 K. The I_D-range with SS < 60 mV/dec extends over one order of magnitude of I_D (c). The low temperature (T) measurements demonstrate a BTBT dominated transport mechanism (d) with an almost constant SS in the investigated temperature range.

Balanced on-performance
I_{on} about 10μA/μm

n-FET with low SS at low current levels

p-FET higher SS due to Trap-Assisted-Tunneling (TAT)
Less abrupt doping profile at the junction

Inverter Performance

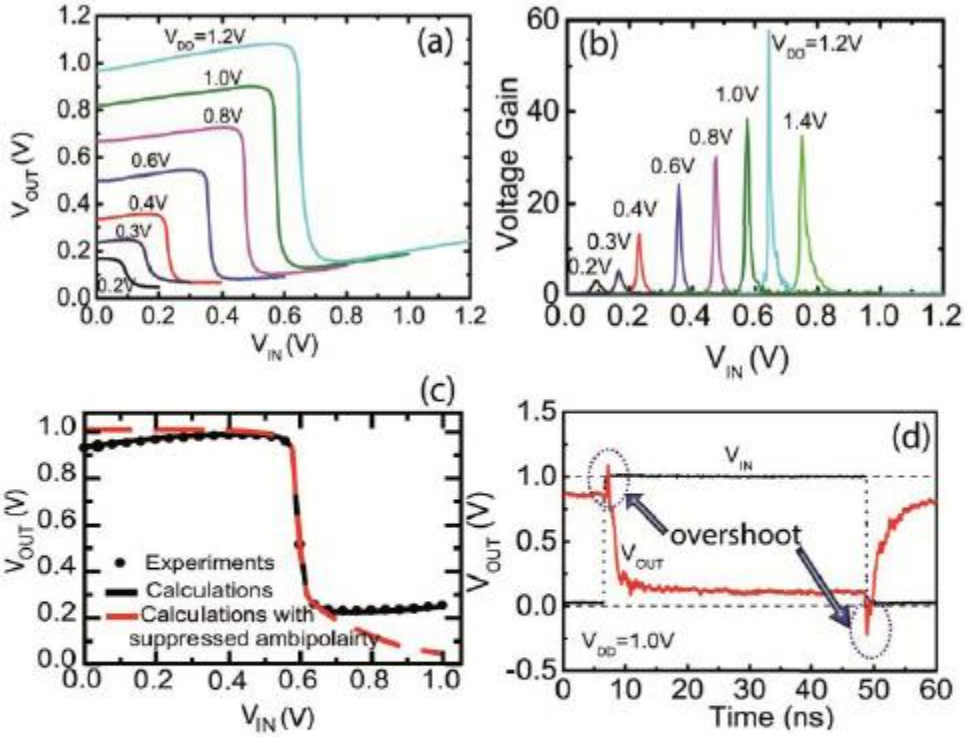

Fig. 3. VTC (a) and voltage gain (b) for NW TFET inverters, functioning at V_{DD}=0.2V. (c) Experimental and calculated VTC for NW TFET at V_{DD}= 1 V. The calculation confirms that the nominal value of the high V_{OUT} recovers to V_{DD}= 1 V and the low V_{OUT} approaches to 0V as the ambipolarities of both the n- and p-type transistors are removed. (d) Transient response of NW C-TFET inverter at V_{DD}= 1.0 V, showing clear voltage overshoots.

Good VTC with high gain and gain also at V_{dd}=0.2 V!

Reduction in voltage swing due to ambipolar conduction (confirmed by modeling)

Inverter rise time ~3 ns
Inverter fall time ~2 ns
(10-90 %)

Propagation delay ~ 1.9 ns

Overshoot due to large Miller capacitance

Fabrication and Characterization of an InAlAs/InGaAs/InP Ring Oscillator Using Integrated Enhancement- and Depletion-Mode High-Electron Mobility Transistors

A. Mahajan, G. Cueva, M. Arafa, P. Fay, and I. Adesida

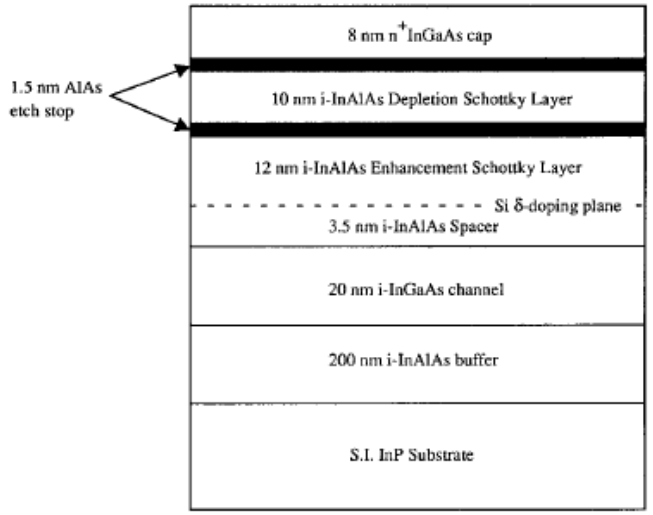

Fig. 1. Cross section diagram of MBE-grown layer structure used in this work.

Use of two etch stop layers to fabricate both E- and D-Mode transistors

Ring Oscillator

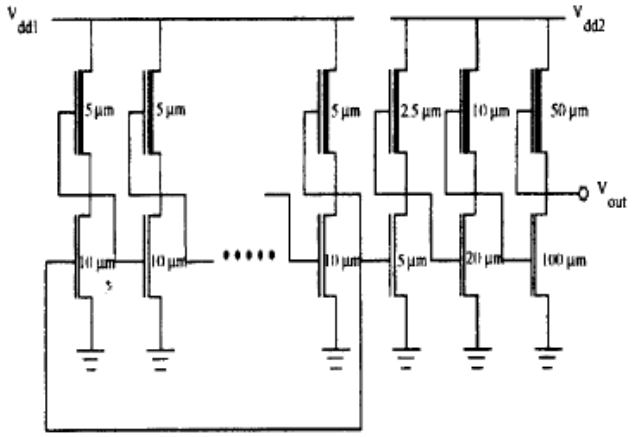

Fig. 6. Schematic for the ring oscillators.

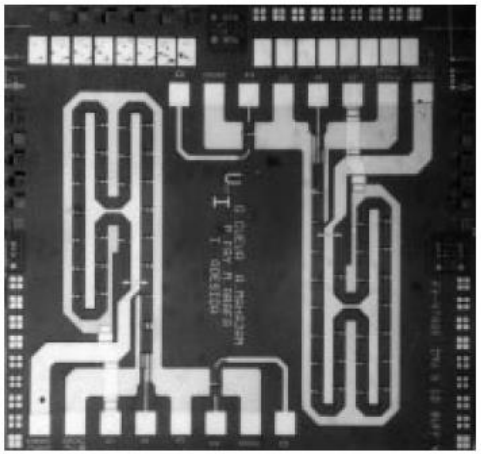

Fig. 7. Die photo of the completed 23 stage ring oscillator.

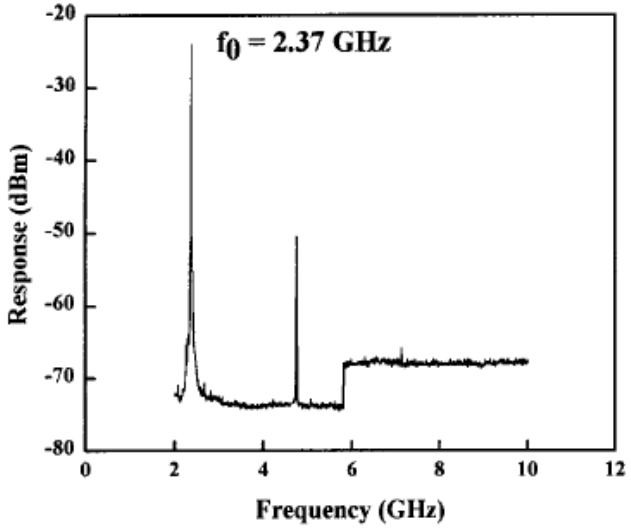

Fig. 8. Spectrum of output of 23 stage 0.25 μm gate-length ring oscillator with $V_{dd} = 0.4$ V.

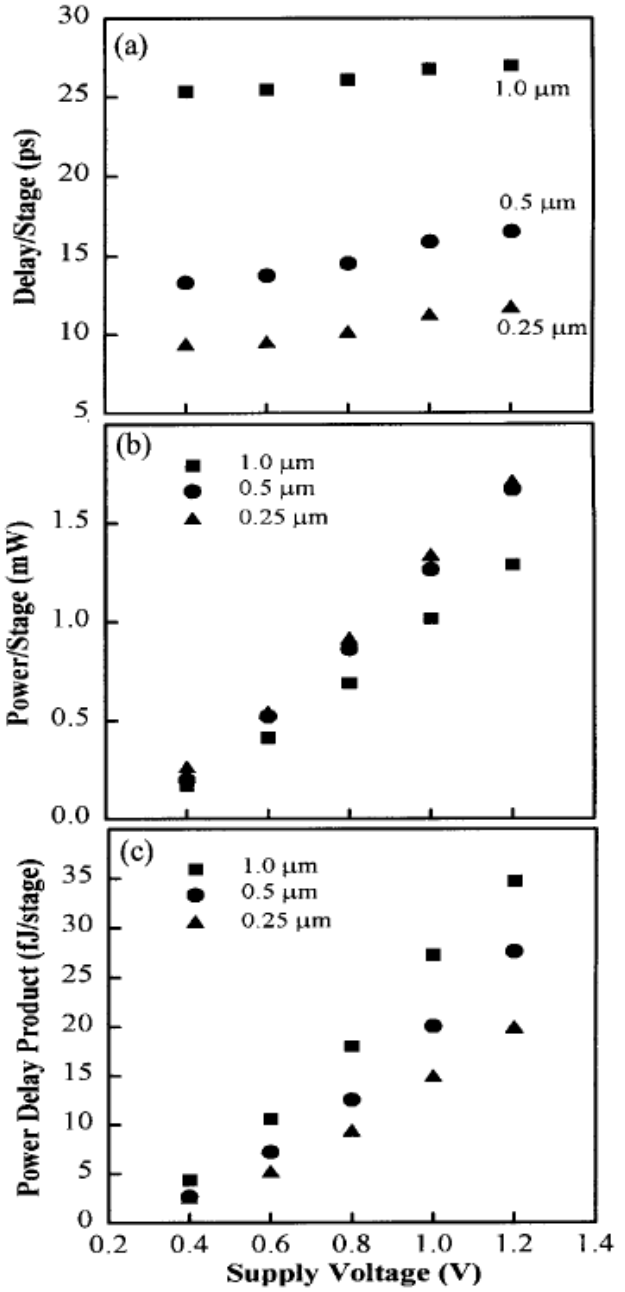

Fig. 9. (a) t_{pd}, (b) P_D and (c) PDP as a function of supply voltage for 1.0, 0.5 and 0.25 μm gate-length inverters.

Ring-oscillator

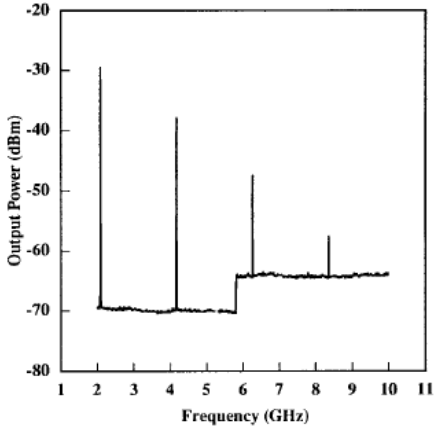

Fig. 4. Spectrum analyzer output of the oscillator circuit for a supply voltage of 0.6 V. The fundamental frequency of oscillation (f_0) is 2.08 GHz.

Spectrum for 11 stage Oscillator

f_0=2.08 GHz

$\tau_{pd}=(2nf_0)^{-1}$

10μm E-HEMT

5 μm D-HEMT

VD=0.6 V

Noise margin of 145 and 205 mV, respectively

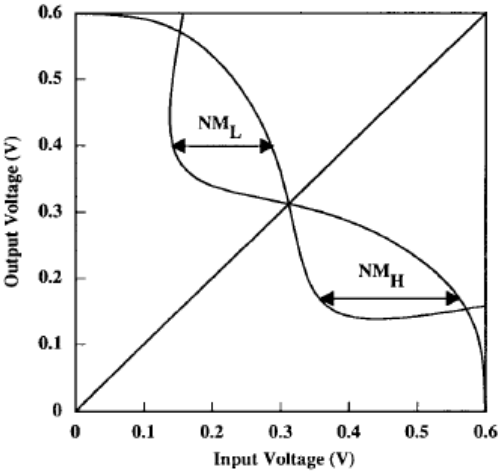

Fig. 3. Voltage transfer curve for a typical E/D HEMT inverter with an E-HEMT width of 10 μm and a D-HEMT width of 5 μm. A logic-low noise margin (NM_L) of 145 mV and a logic-high noise margin (NM_H) of 205 mV are measured using the method of largest width.

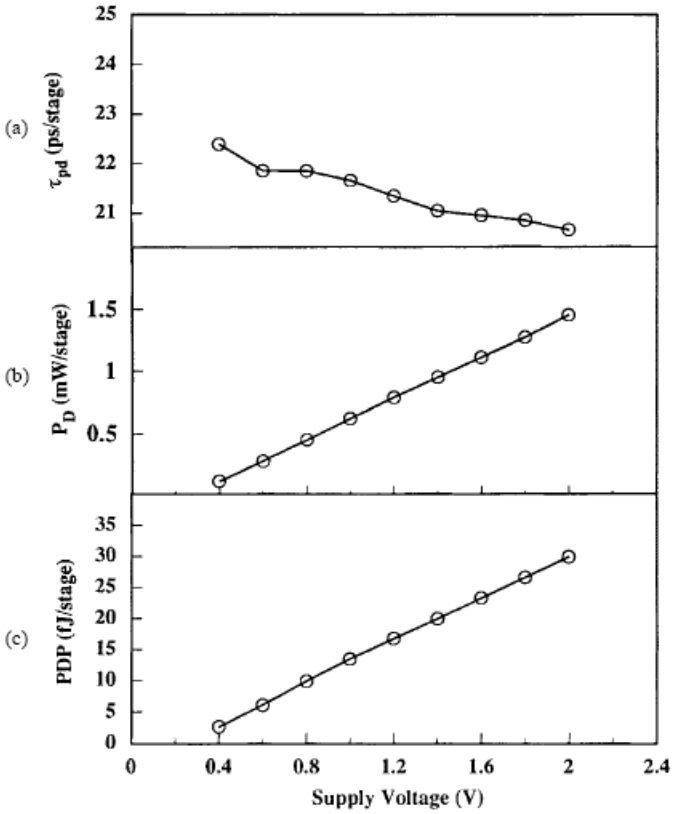

Fig. 5. Measured characteristics of the ring oscillator circuit: (a) propagation delay per stage (τ_{pd}), (b) power dissipation per stage (P_D), and (c) power delay product per stage (PDP) as a function of supply voltage.

High-Performance Self-Aligned Gate AlGaAs/GaAs MODFET Voltage Comparator

P. J. VOLD, STUDENT MEMBER, IEEE, DAVID K. ARCH, MEMBER, IEEE, K. L. TAN, A. I. AKINWANDE, MEMBER, IEEE, AND NICHOLAS C. CIRILLO, JR., MEMBER, IEEE

Low hysteresis
High transconductance
Low input off-sets
(1-6 mV)

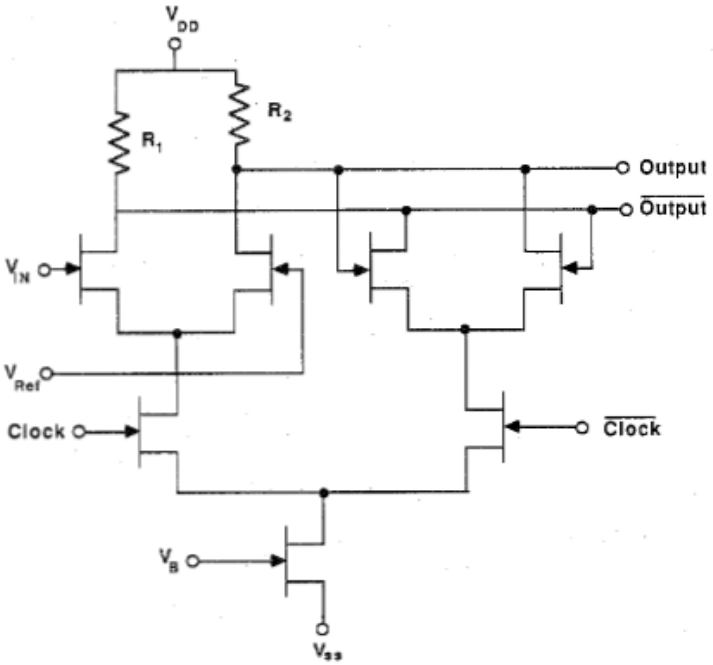

Fig. 1. Circuit schematic of the CML bi-level latch architecture.

TABLE I

Analog Input Resolution	Sampling Rate	ADC Accuracy*
< 1.0 mV	0.5 Gsps	9-10 bits
2.5 mV	1.0 Gsps	8-9 bits
24 mV	1.5 Gsps	5 bits
75 mV	2.0 Gsps	4 bits
105 mV	2.5 Gsps	3 bits

* Based on present MODFET technology

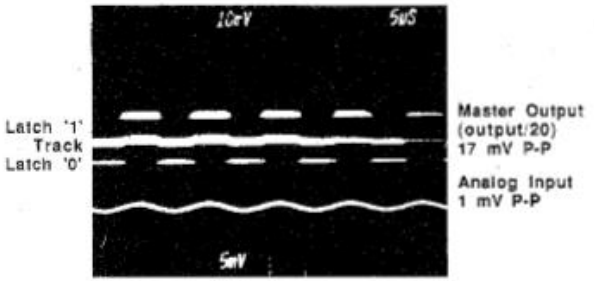

Fig. 2. Oscillograph of comparator output demonstrating correct latch operation with a 1-mV analog input at low input and clock frequencies.

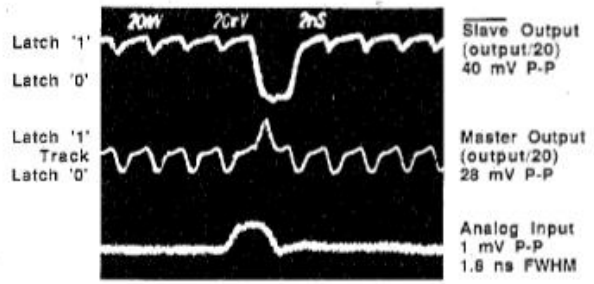

Fig. 3. Oscillograph of high-speed comparator test showing correct operation with a 1-mV analog input pulse at a sampling rate of 0.5 Gsps.

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Quantum cellular automata

Craig S Lent, P Douglas Tougaw, Wolfgang Porod and Gary H Bernstein

Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA

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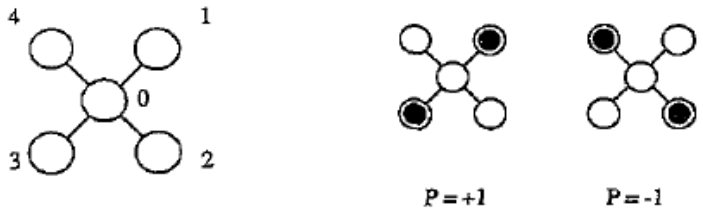

Figure 1. The quantum cell consisting of five quantum dots which are occupied by two electrons. The mutual Coulombic repulsion between the electrons results in bistability between the $P = +1$ and $P = -1$ states.

Pure Quantum Mechanics:

Quantum dots with diameter 10 nm
Nearest neighbor 20 nm

$$H_0^{\text{cell}} = \sum_{i,\sigma} E_{0,i} n_{i,\sigma} + \sum_{i,\sigma} t(a_{i,\sigma}\dagger a_{0,\sigma} + a_{0,\sigma}\dagger a_{i,\sigma}) + \sum_i E_Q n_{i,\uparrow} n_{i,\downarrow} + \sum_{i>j,\sigma,\sigma'} V_Q \frac{n_{i,\sigma} n_{j,\sigma'}}{|\boldsymbol{R}_i - \boldsymbol{R}_j|}. \quad (1)$$

$$(H_0^{\text{cell}} + H_{\text{inter}}^{\text{cell}})|\Psi_n\rangle = E_n|\Psi_n\rangle.$$

Switching behaviour

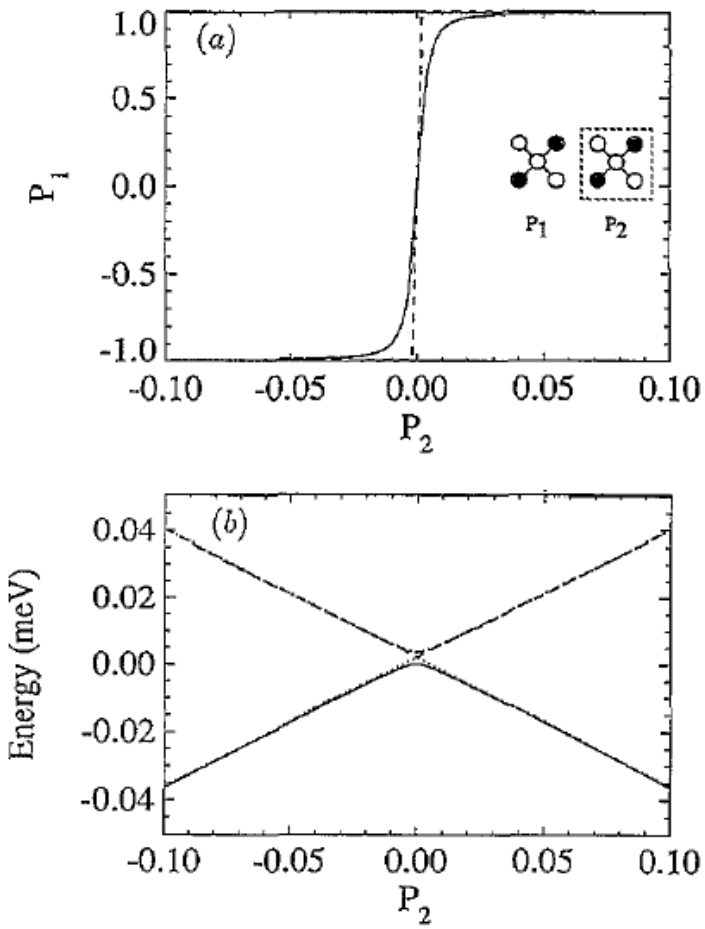

Figure 2. The cell–cell response function. The polarization of the right cell is fixed and the induced polarization in the left cell is calculated. (*a*) The calculated polarization of cell 1 as a function of the polarization of cell 2. Note that the range of P_2 shown is only from -0.1 to $+0.1$. This is because the transition in the induced polarization is so abrupt. (*b*) The first four eigen-energies of cell 1. The polarization of the lowest two are shown in (*a*).

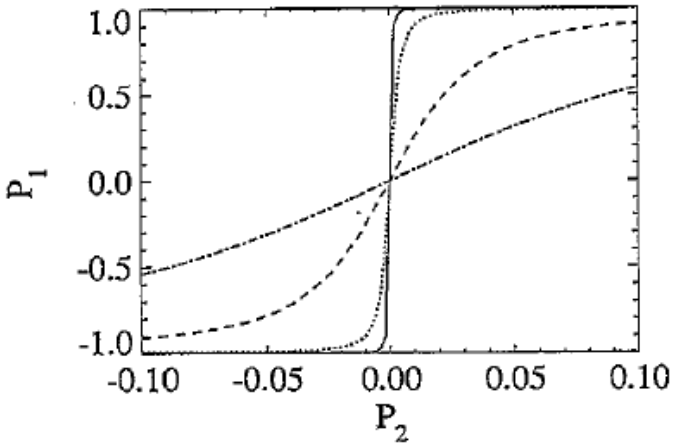

Figure 3. The cell–cell response function for various values of the dot-to-dot coupling energy (t in equation (1)). The induced cell polarization P_1 is plotted as a function of the neighboring cell polarization P_2. The results are shown for values of the coupling energy, $t = -0.2$ (full curve), -0.3 (dotted curve), -0.5 (dashed curve), and -0.7 (dot-dashed curve) meV. Note that the response is shown only for P_2 in the range $[-0.1, +0.1]$.

Edge driven computing

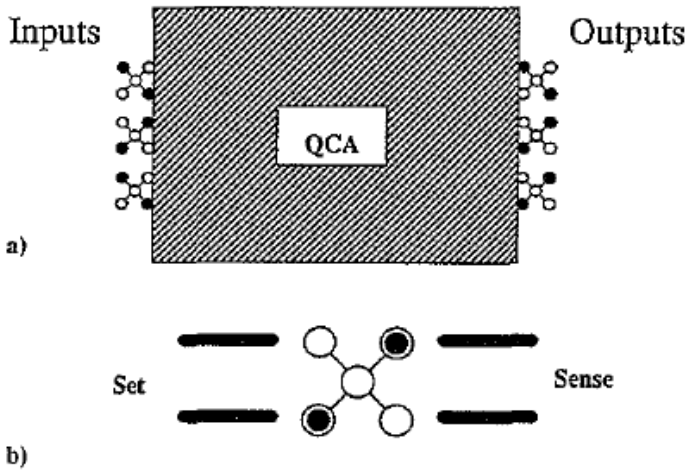

Figure 4. The new paradigm for computing with quantum cellular automata (QCAs). The input to the QCA is provided at an edge by setting the polarization state of the edge cells (*edge-driven computation*). The QCA is allowed to dissipatively move to its new ground-state configuration and the output is sensed at the other edge (*computing with the ground state*). The 'set' and 'sense' lines are shown schematically.

Transmission lines

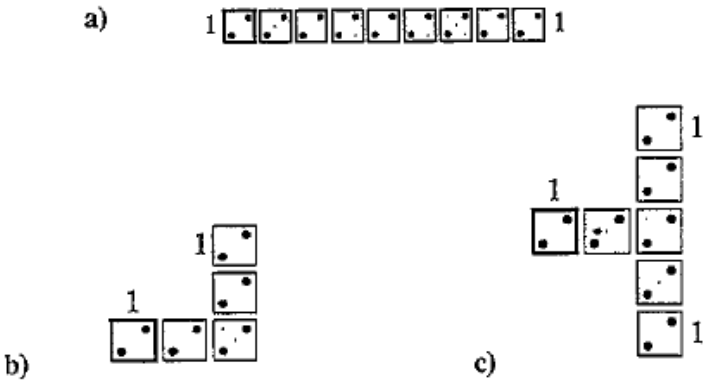

Figure 5. QCA wires: (*a*) the basic wire; (*b*) a corner in a wire; (*c*) fan-out of one signal into two channels. In each case the darker (left-hand) cell has a fixed polarization which constitutes the input. Note that these figures are not simply schematic, but are a plot of the results of a self-consistent many-body calculation of the ground state for the cellular array. The diameter of each circle is proportional to the calculated charge density at each site.

Circuits

Inverter

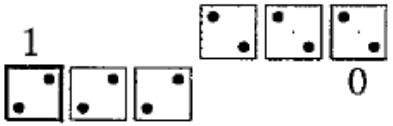

Figure 6. An inverter constructed from a quantum cell automaton.

OR gates

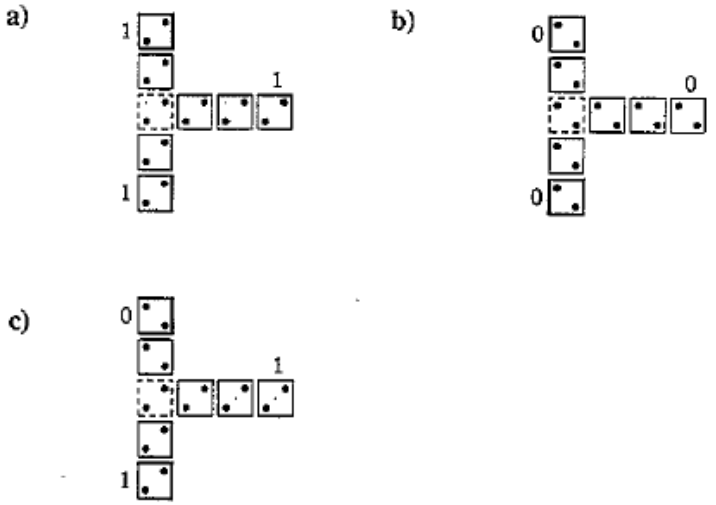

Figure 7. An OR gate. The cells in darker squares are fixed to the input states. The cell in the dashed square is biased slightly toward the '1' state.

AND gates

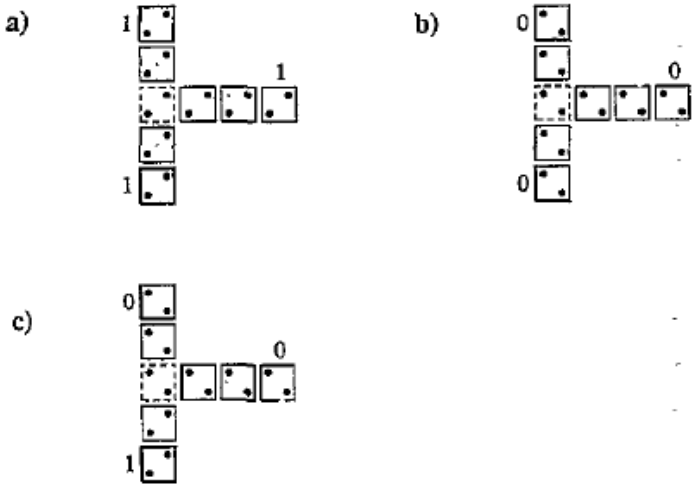

Figure 8. An AND gate. The cells in darker squares are fixed to the input states. The cell in the dashed square is biased slightly toward the '0' state.

Critical Issues and Benefits

Issues:	Benefits:
Uniform cell occupancy	No interconnects
Dot size control	High density
Temperature	Low power
	Ultra-fast computing