



Carbon Nanotube Electronics

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Nanoelectronics FFF160

Outline

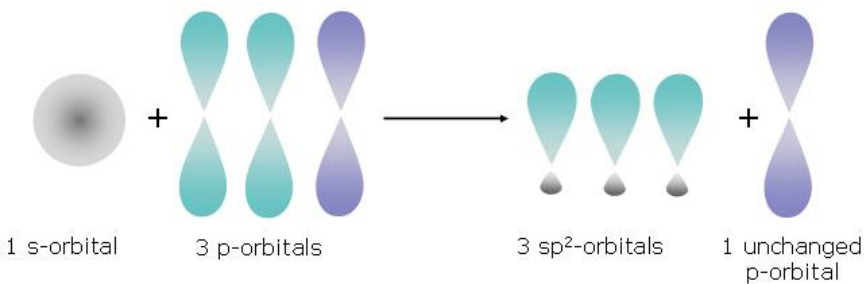
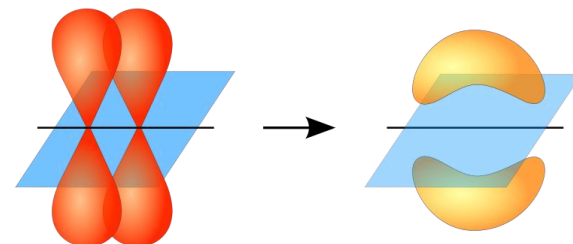
- Basics of graphene and CNTs
 - Structural
 - Electronic
 - Production of CNTs
- Advantages of CNTs for FETs
 - Gate length scaling
 - Coaxial gate
 - High-k compatibility
 - Band-to-band tunneling
- Challenges of CNT integration
 - Contacts
 - Doping
 - Positioning
 - Chirality control
- Towards integration
 - Flexible electronics
 - High frequency performance

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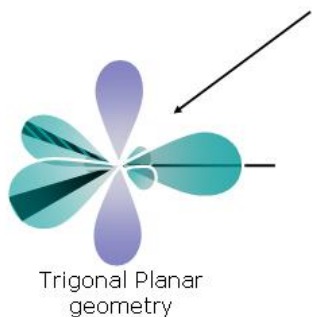
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Hybridisation of carbon orbitals

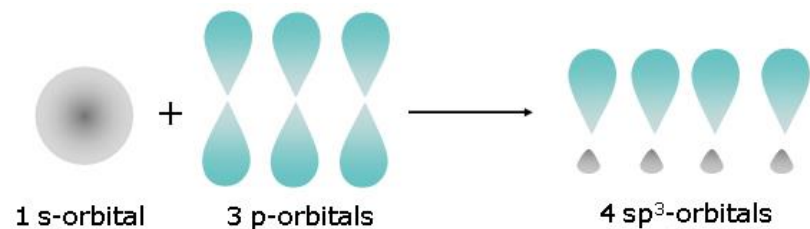
- 4 valence electrons
- 1 s-electron can "mix" with 1-3 p-electrons
- sp^2 have three σ -bonds in a plane + π -bond
- sp^3 have four σ -bonds



sp^2



Trigonal Planar geometry



sp^3



Tetrahedral geometry

Carbon allotropes

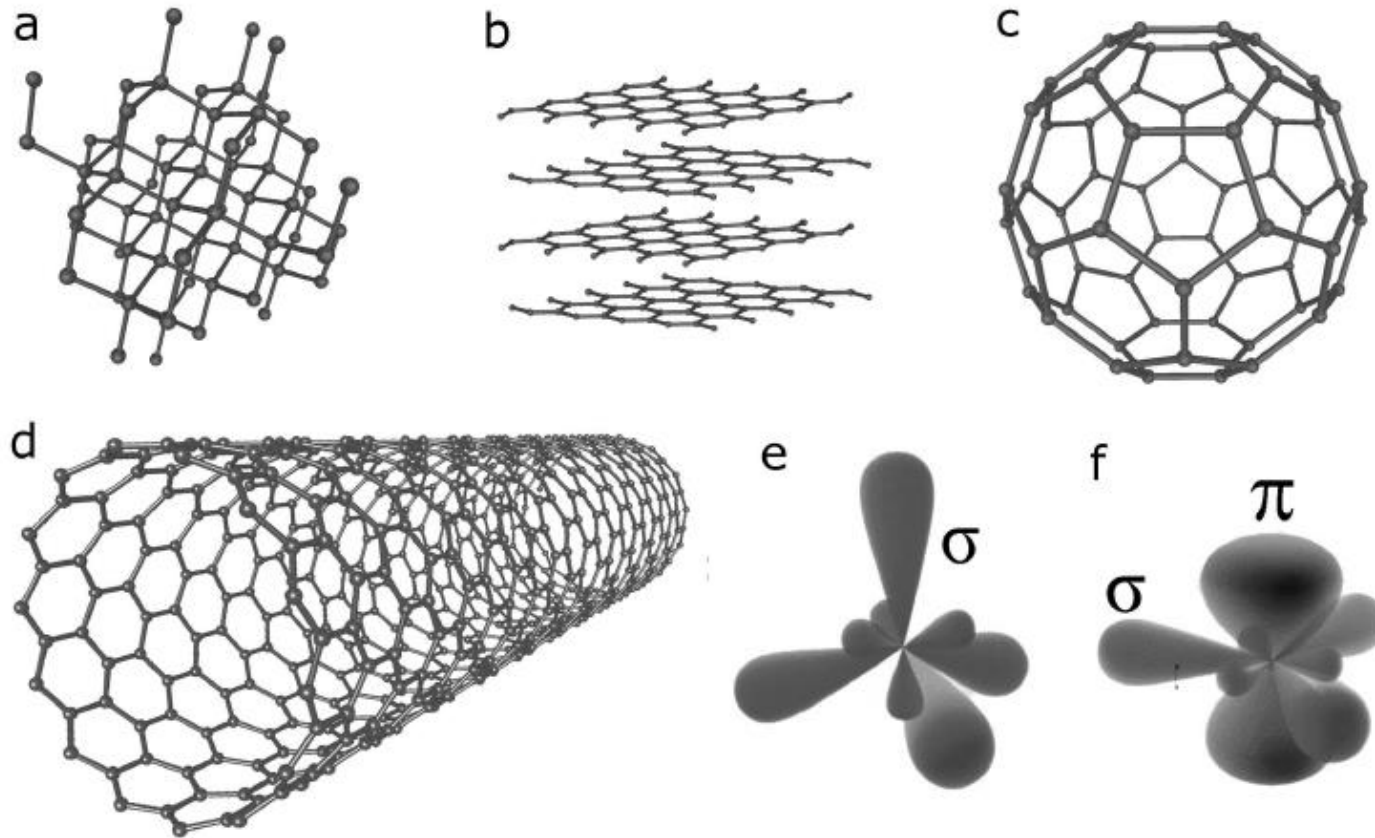
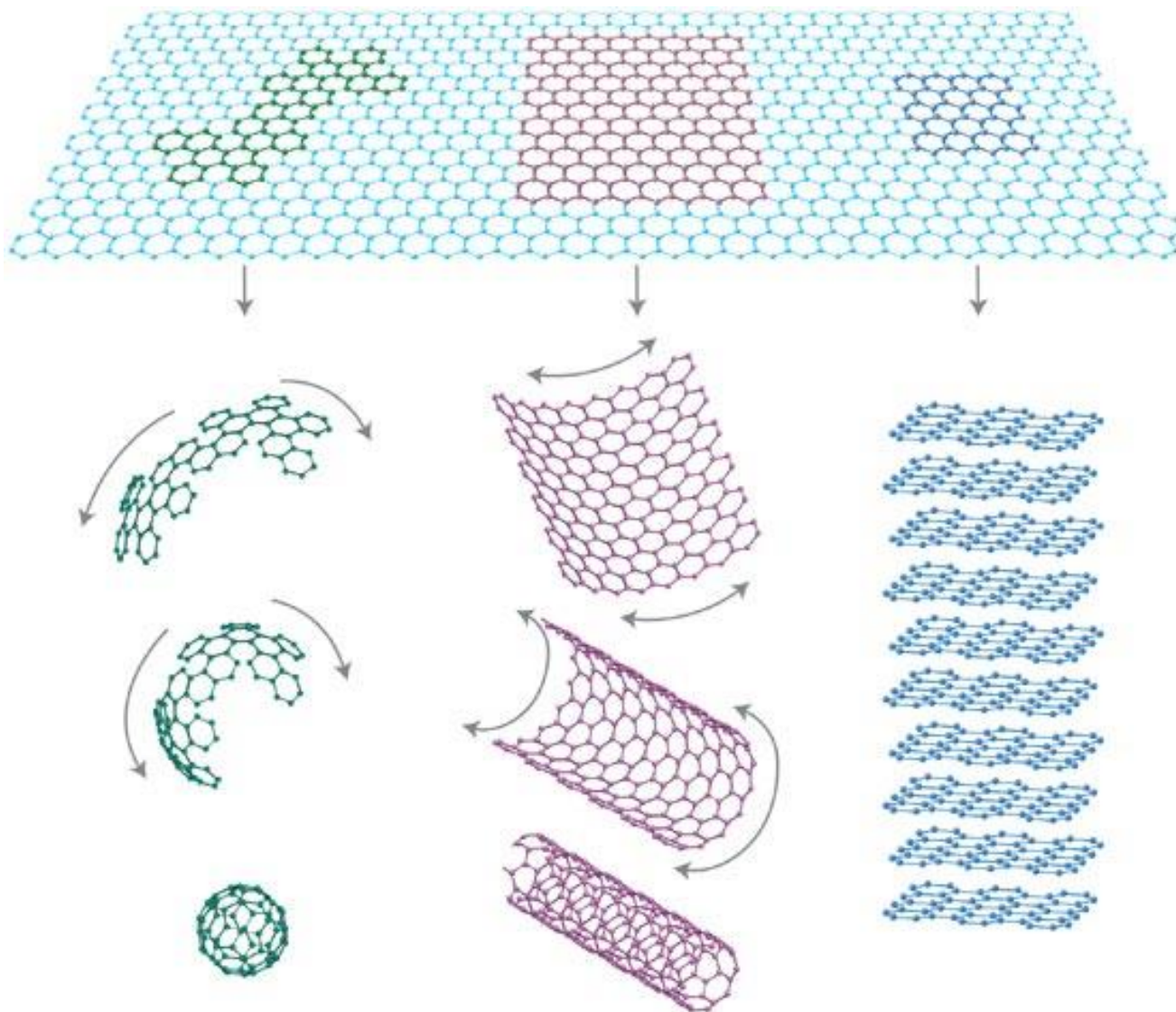


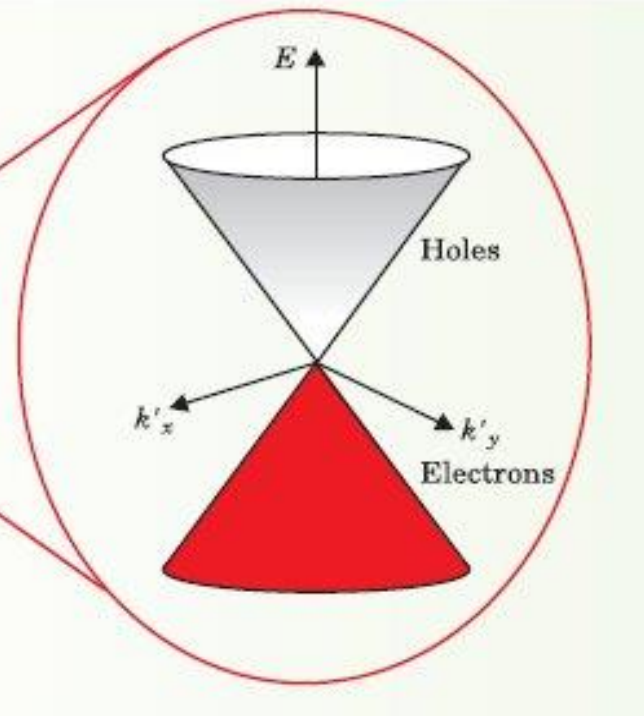
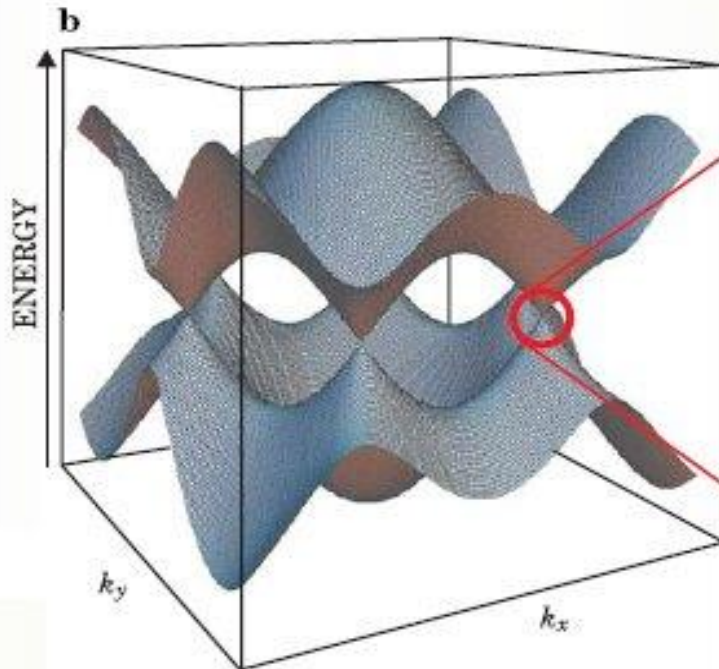
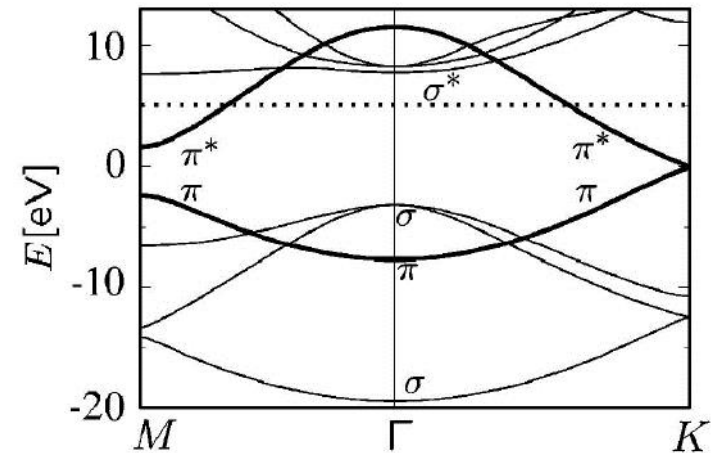
Figure 2.1: *a-d) Crystal structure of a few carbon allotropes a) Diamond b) Graphite c) C₆₀ d) CNT. e) sp³ hybridised orbitals forming σ bonds. f) sp² hybridised orbitals forming σ bonds and the remaining p_z orbital giving rise to π bonds.*

Graphene is mother of all sp^2 -carbon



Graphene band structure

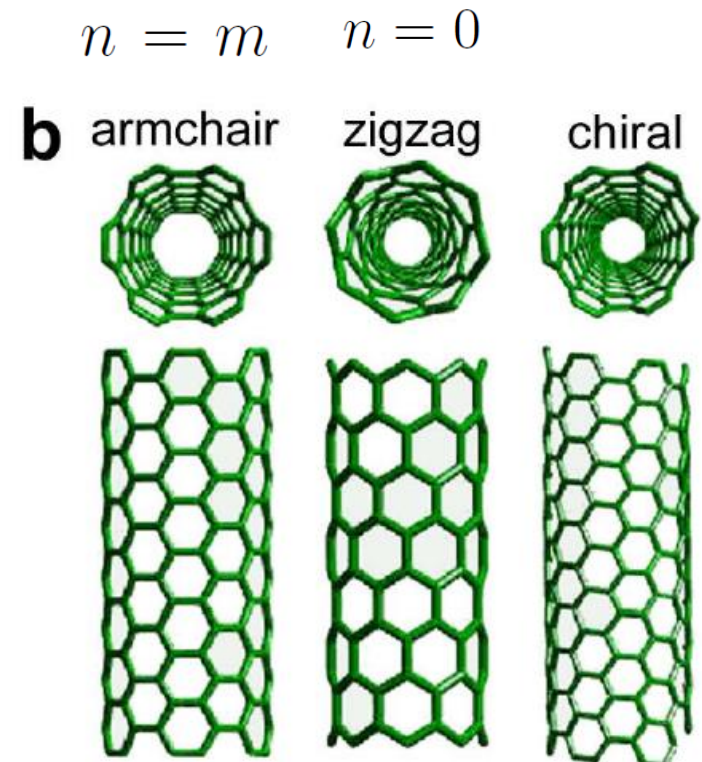
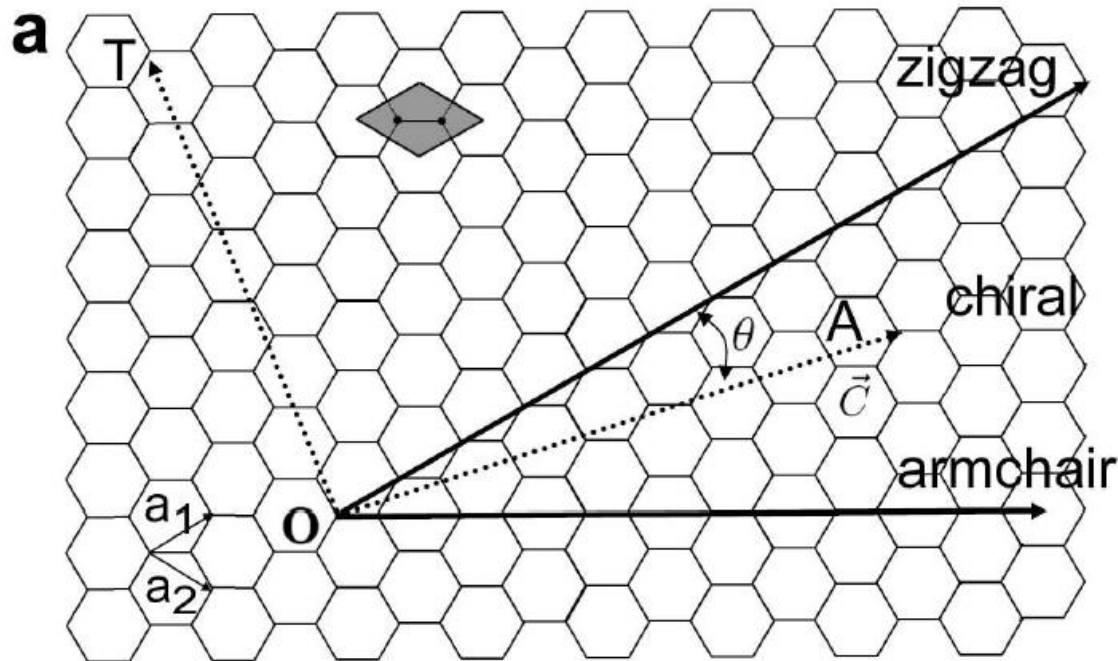
- Semimetal: no gap and zero DOS at E_f
- Only π -bands are interesting
- Linear dispersion near E_f
- Conduction and valence bands meet at the K-points



Rolling graphene

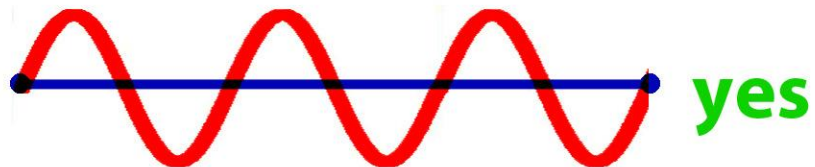
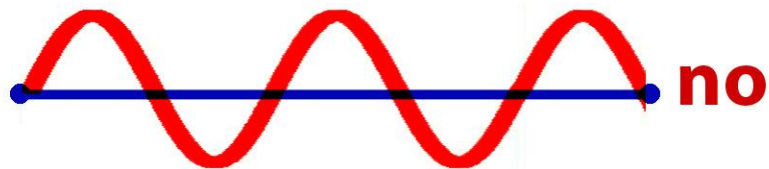
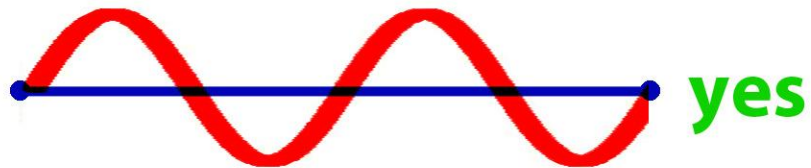
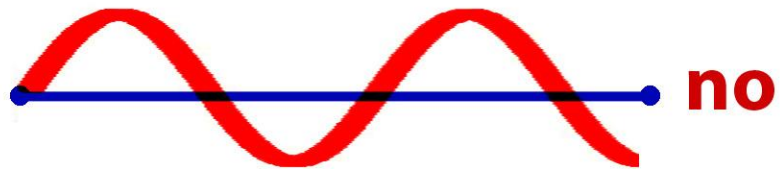
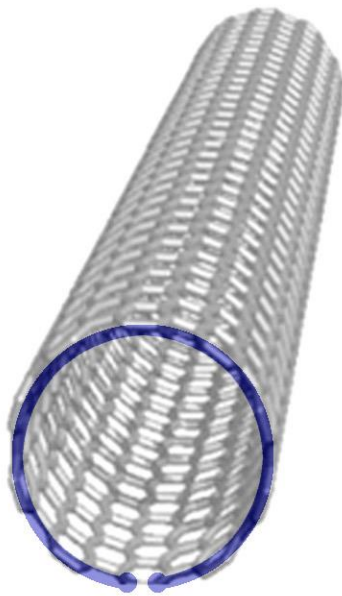
- Cut graphene into narrow strip and roll into tube
- Different structure depending on direction of cut
- Armchair, zigzag, chiral CNTs
- Chirality defined by index (n,m)

$$\vec{C} = n\vec{a}_1 + m\vec{a}_2$$



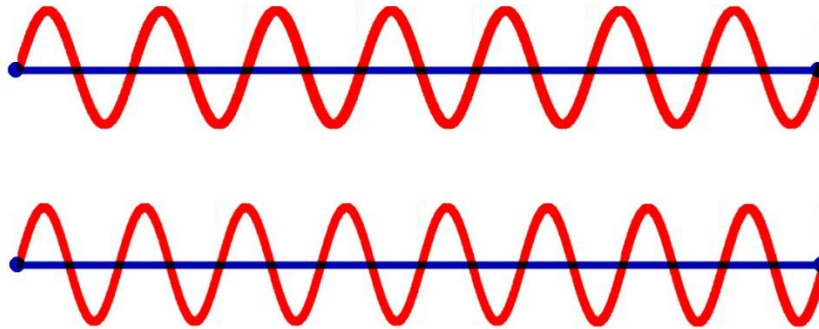
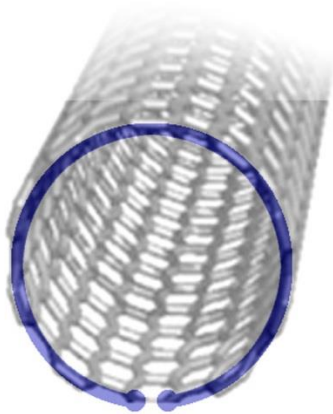
Confinement of electron wavefunctions

- Have to have continuous wavefunction around circumference
- Periodic boundary conditions
- Only some wavevectors $k_{\perp} = 2n\pi/C$ with $n=1,2,3\dots$ allowed

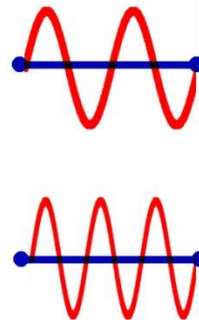
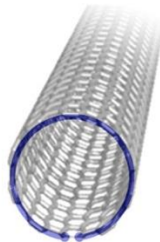


Diameter dependence of confinement

large diameter = small energy difference

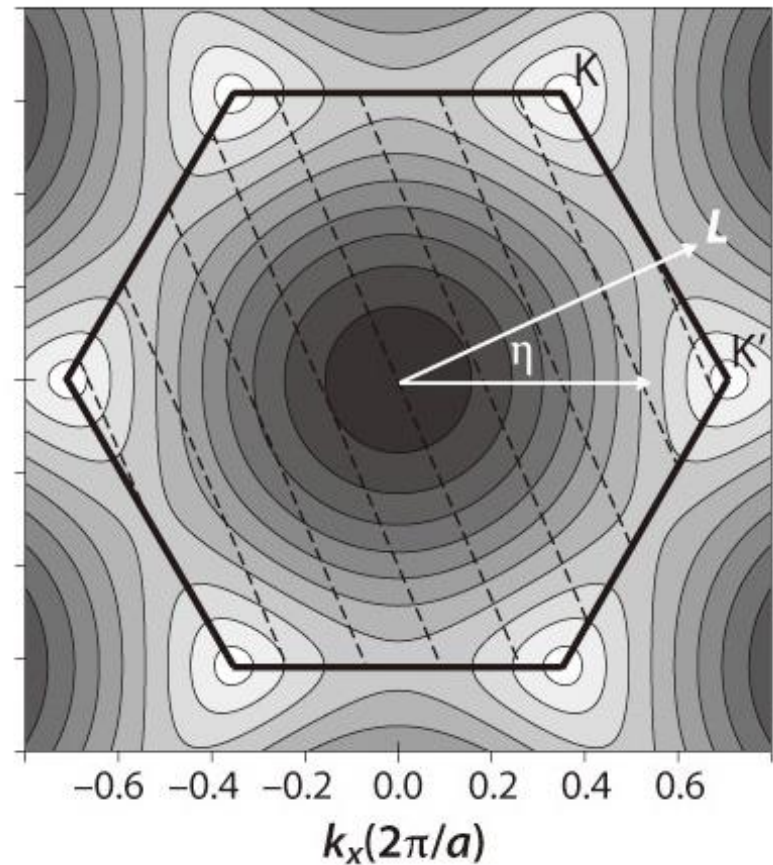
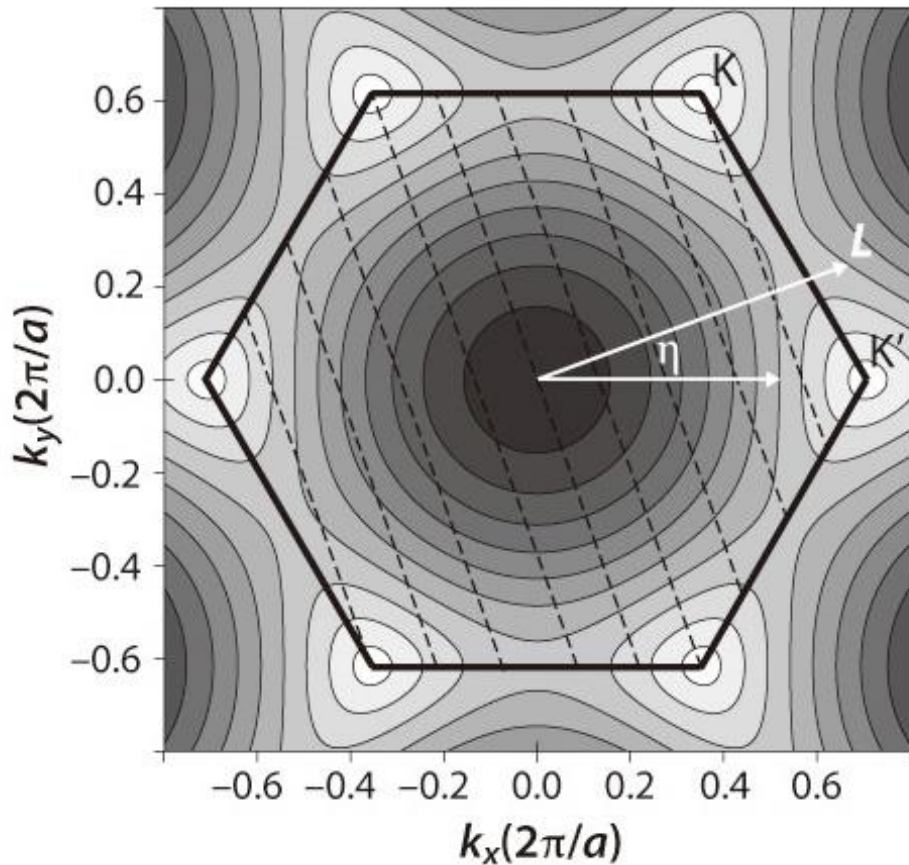


small diameter = large energy difference



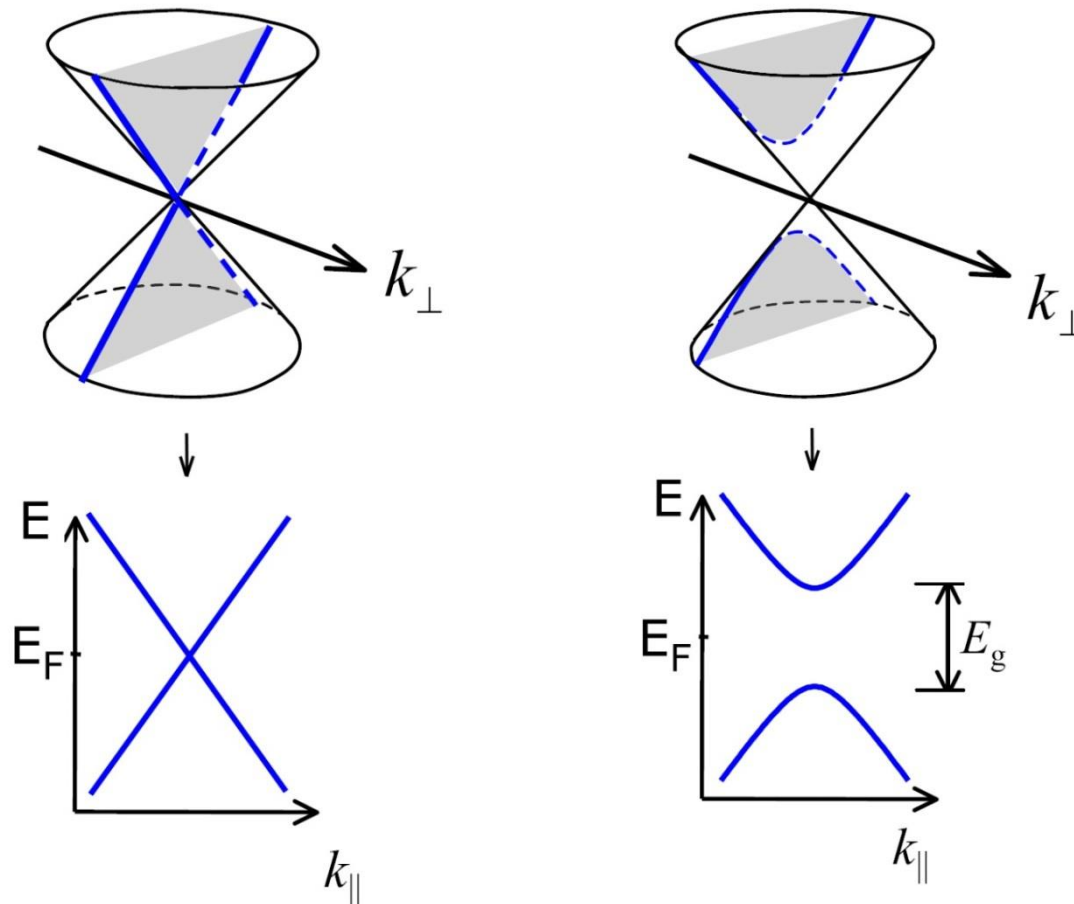
Confinement of electron wavefunctions

- Slices in graphene dispersion relation of allowed wavevectors around circumference
- Position of slices depends on chirality
- Small diameter CNT have larger distance between slices



Allowed wavevectors

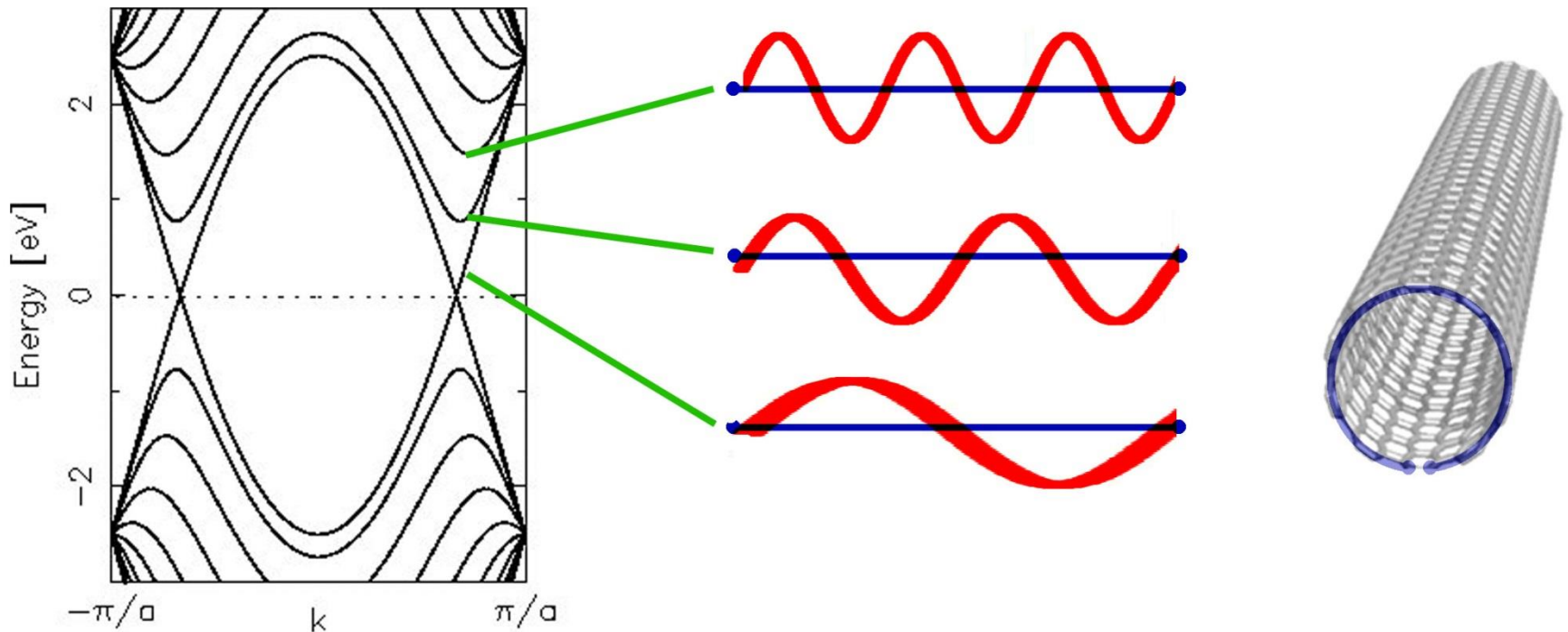
- $n-m = 3i$ with $i=1,2,3\dots$ -> slice goes through K-point -> metallic CNT
- $n-m \neq 3i$ -> slice does not go through K-point -> semiconducting CNT with parabolic bands



$$E(k) = \pm \left((\hbar v_F k)^2 + (E_g/2)^2 \right)^{1/2}$$

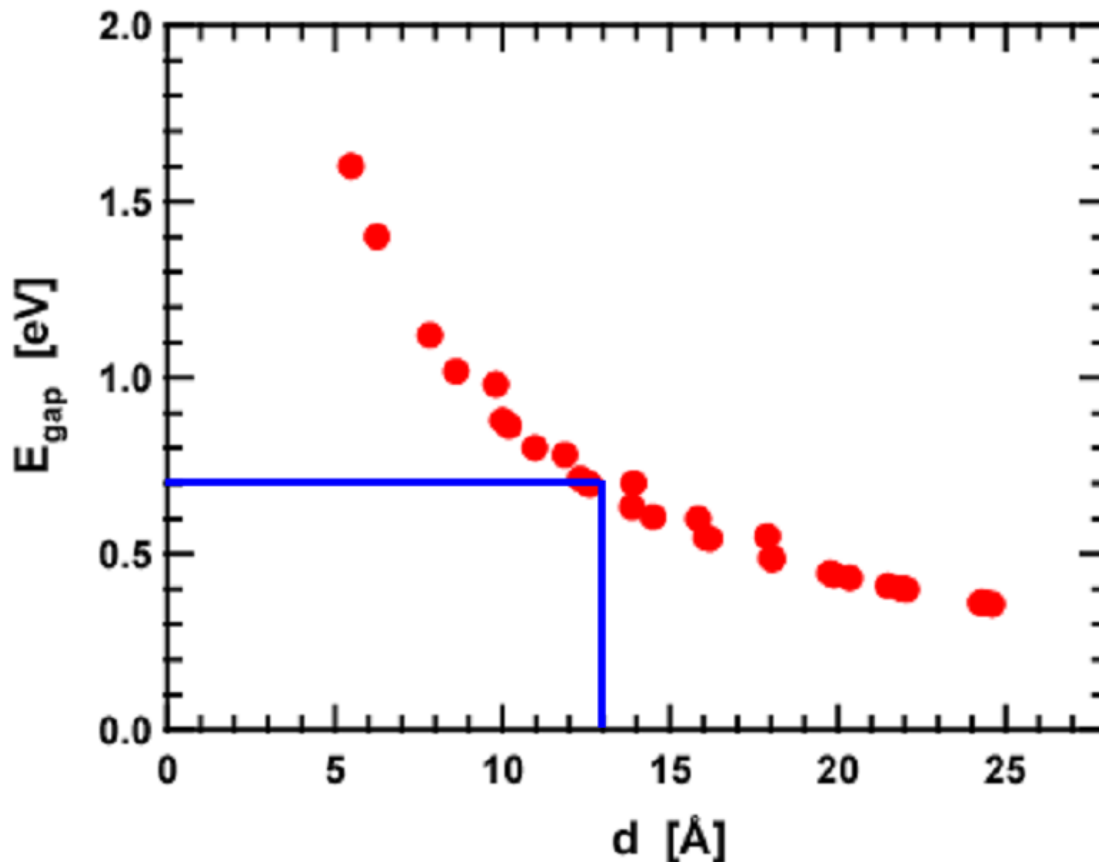
Subbands

- π -bands split into 1D subbands of increasing energy
- Mainly important at high gate voltages or for optical transitions
- Wavefunctions just schematic, need TB calculation



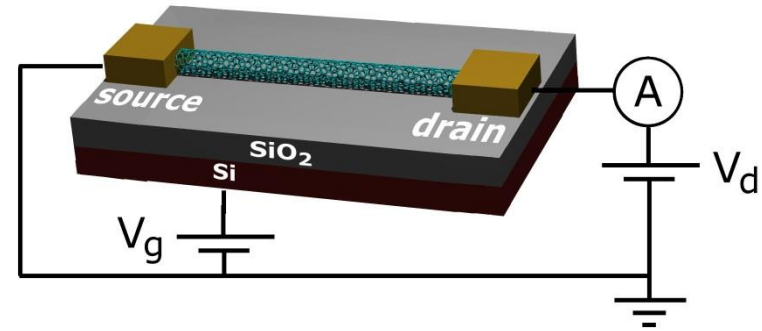
Band gap vs diameter

- Linear dispersion of graphene gives $E_g=0.8/d$ [nm]
- Curvature induced gap of 10's of meV in most of the "metallic" CNTs
- Only armchair CNTs truly metallic

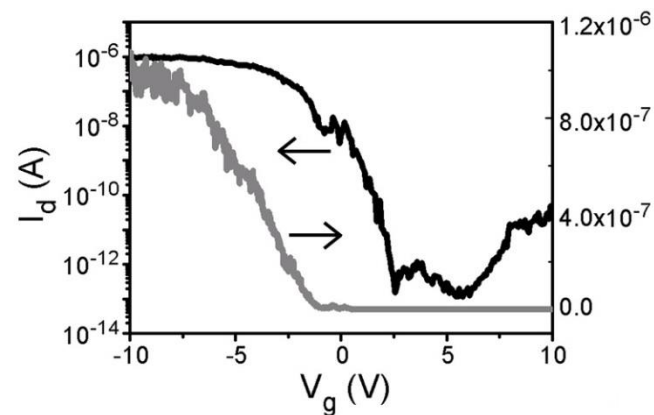


Electrical characteristics

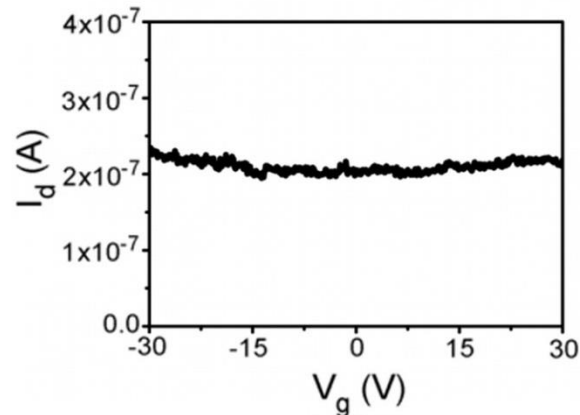
- semiconducting: strong gating effect
- metallic: no gating effect
- small gap semiconducting: some gating effect



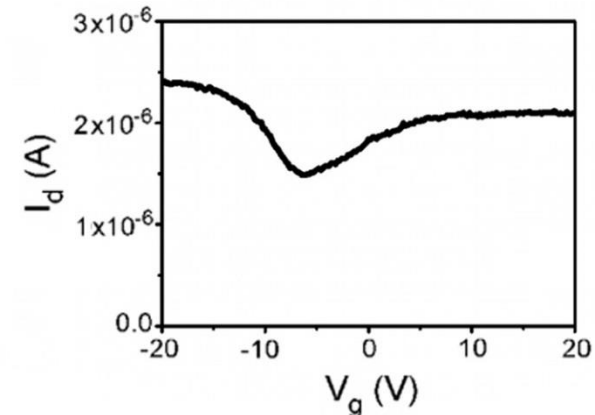
semiconducting



metallic

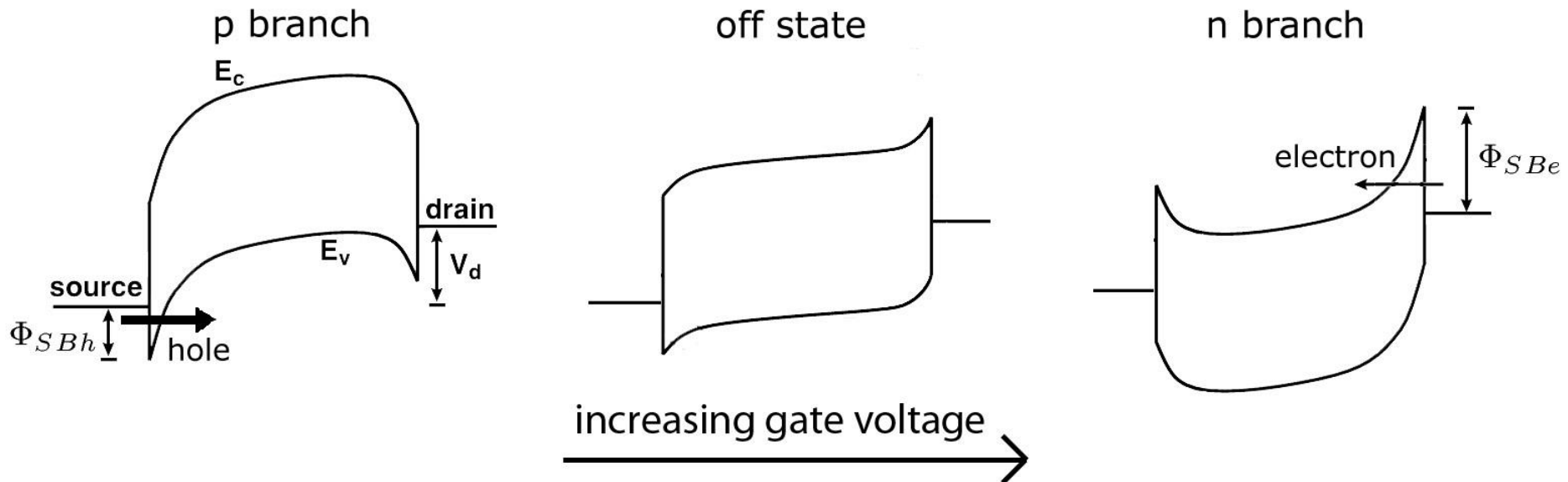


small band gap



Band diagrams

- Schottky barriers at metal contacts
- Tunneling through SB determines transport
- Negative gate voltages -> hole transport
- Positive gate voltages -> electron transport
- Similar SB heights -> ambipolar characteristics

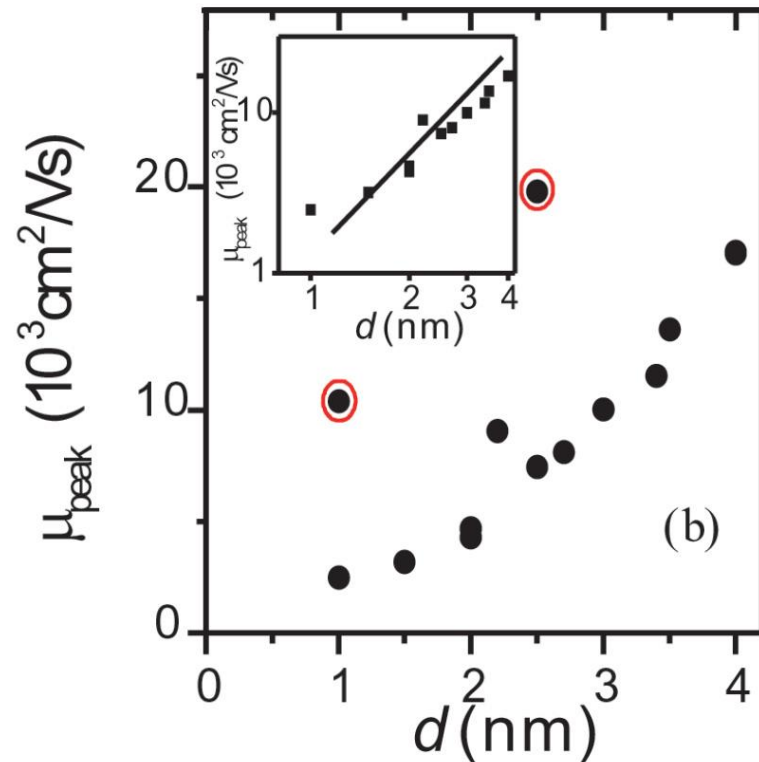
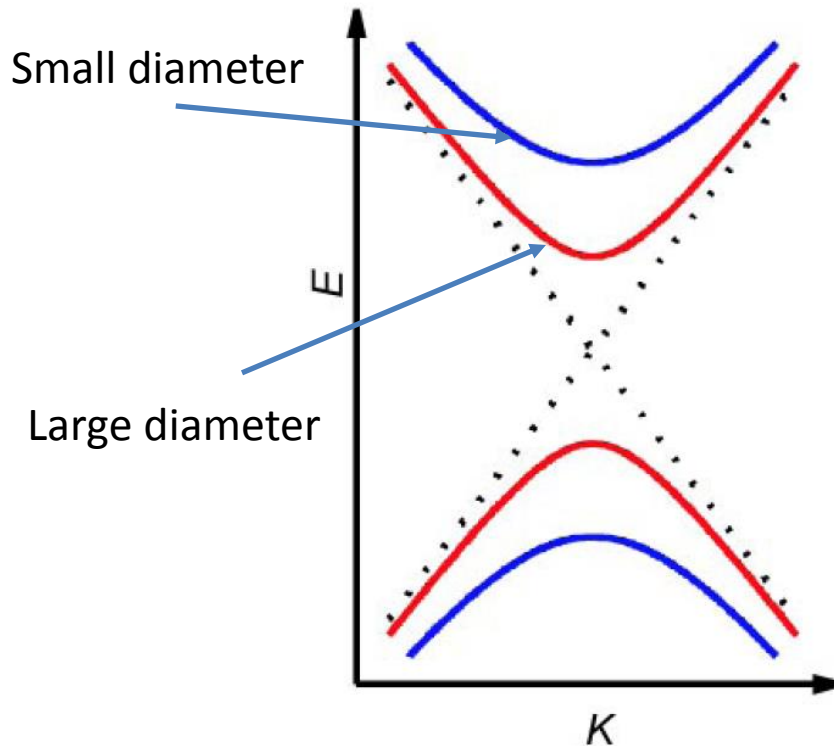


Mobility vs diameter

- Lower curvature of bands for smaller diameter -> mobility proportional to d^2
- $\mu > 100000 \text{ cm}^2/\text{Vs}$ at 50 K

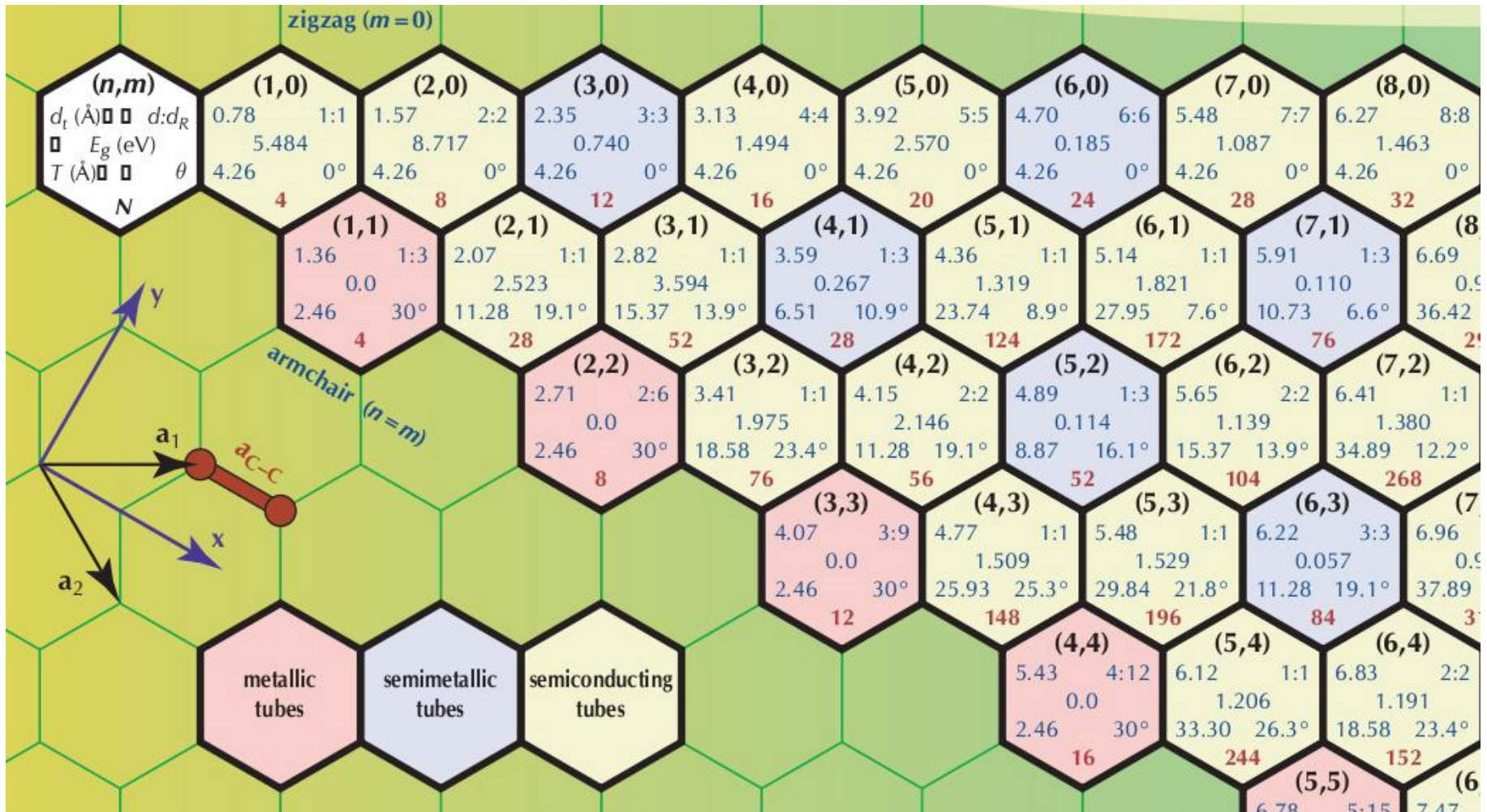
$$m^* = \hbar^2 \cdot \left[\frac{d^2 \epsilon}{dk^2} \right]^{-1}$$

$$\mu_{FE} = \frac{L^2}{C_g} \frac{\partial G}{\partial V_g}$$



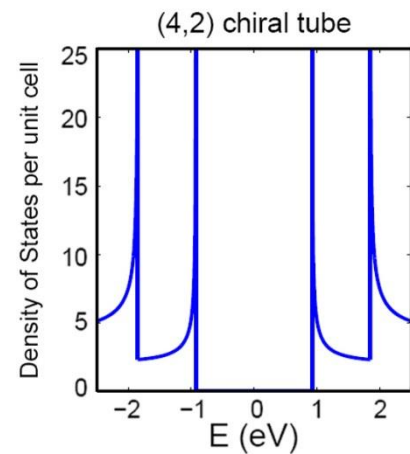
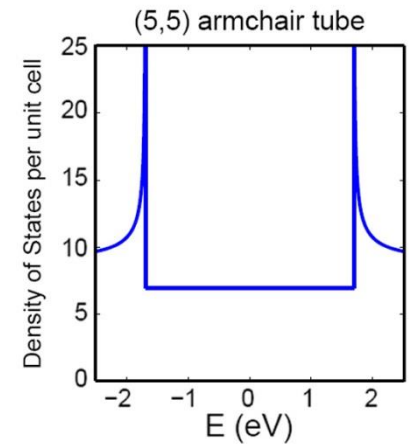
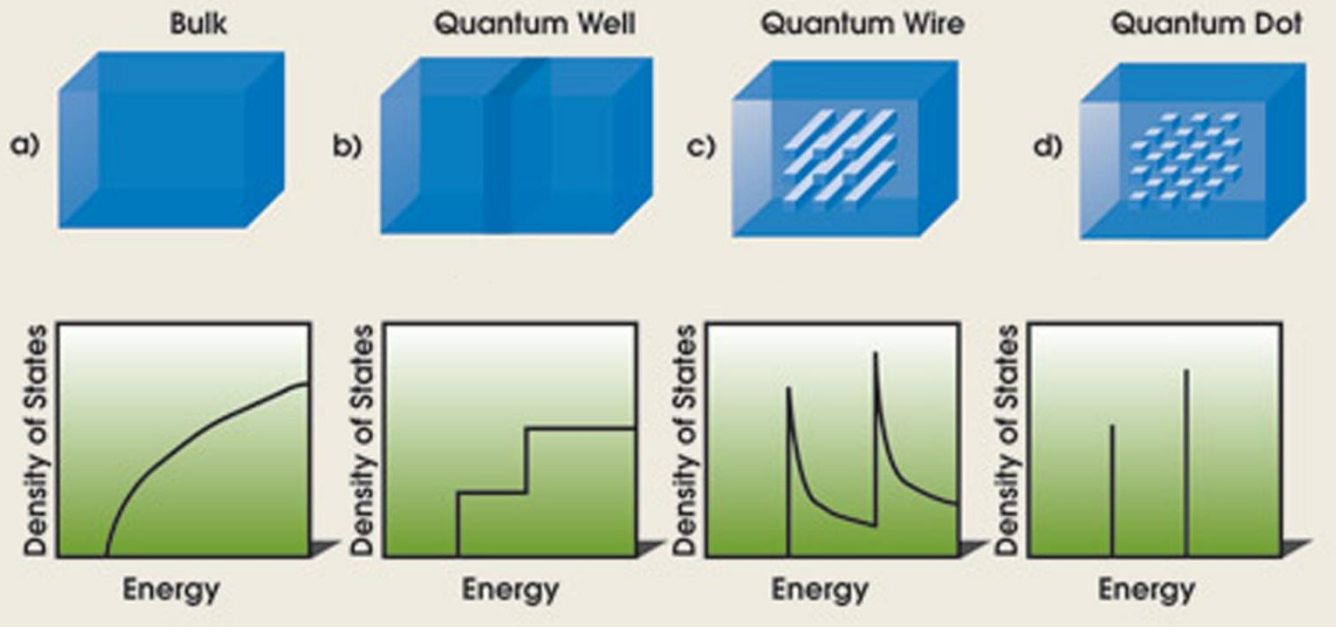
All CNTs are different

- 1/3 metallic or small gap
- 2/3 semiconducting with different gap



Density of states

- Van Hove singularities with high DOS at band edges
- Can be seen in STM or capacitance measurements
- Strong influence on optical properties



Scattering

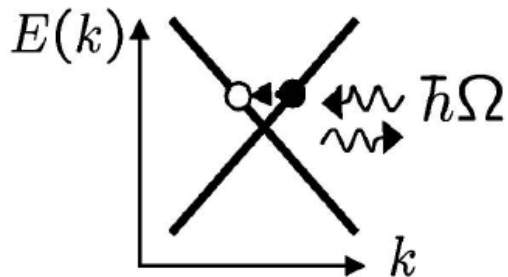
- Elastic scattering have to reverse direction of electron



- Acoustic phonon scattering dominates at low bias and low temperatures and gives $\text{mfp} > 300 \text{ nm}$ \rightarrow ballistic transport possible
- Optical phonons scattering dominates at high bias and gives $\text{mfp} = 15 \text{ nm}$
- Potential variations or phonons in substrate under CNT can also scatter electrons

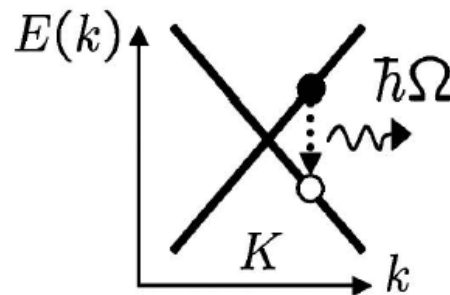
Acoustic phonon

$$q \sim 0, \hbar\Omega \ll k_B T$$



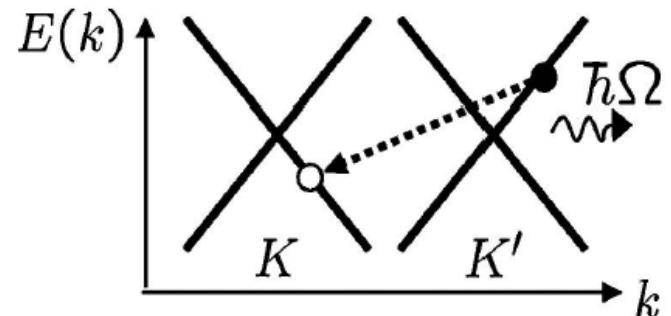
Optical phonon

$$q \sim 0, \hbar\Omega > k_B T$$



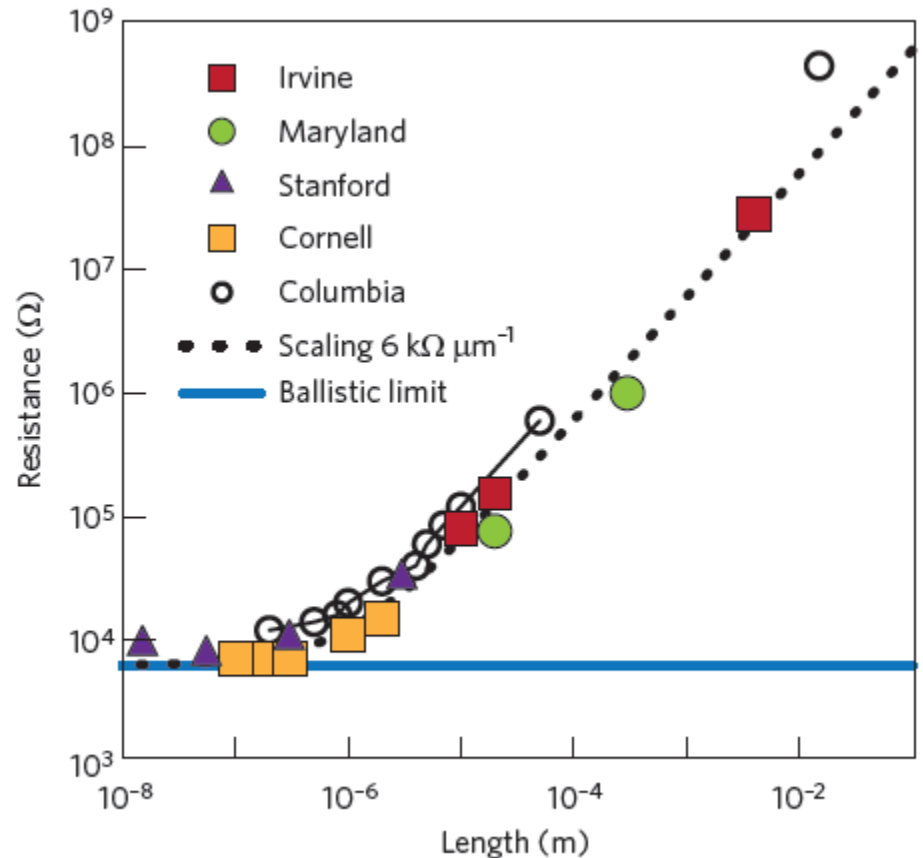
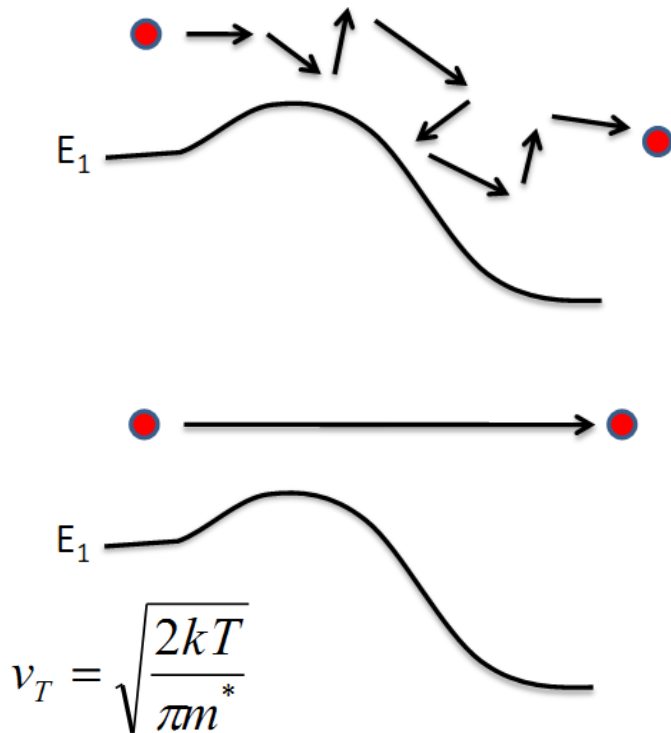
Zone boundary phonon

$$q > 0, \hbar\Omega > k_B T$$



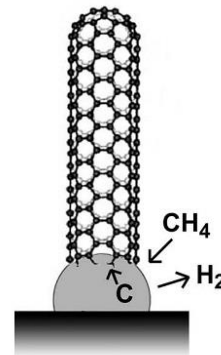
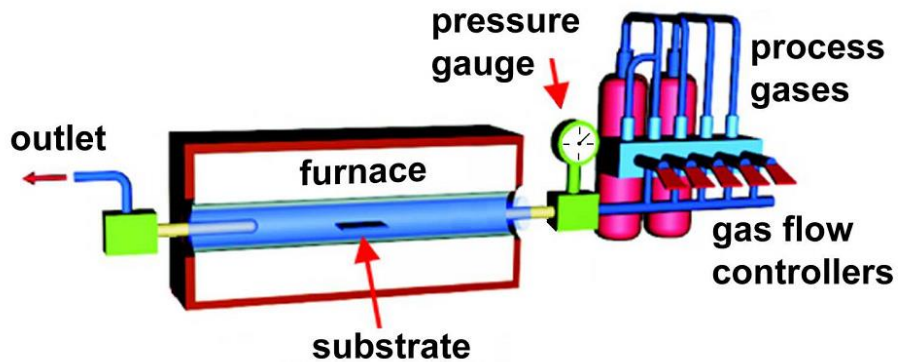
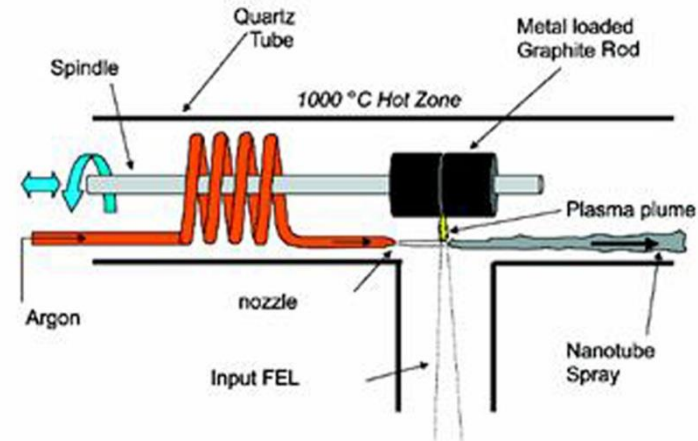
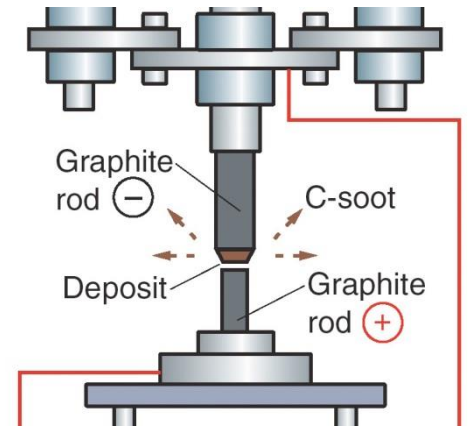
Ballistic transport

- Channel length \ll mfp \rightarrow no scattering in channel
- Mobility not important but injection velocity is
- $R_{\min} = 6.5 \text{ k}\Omega$ in 1D system with 4 modes \rightarrow Ballistic transport



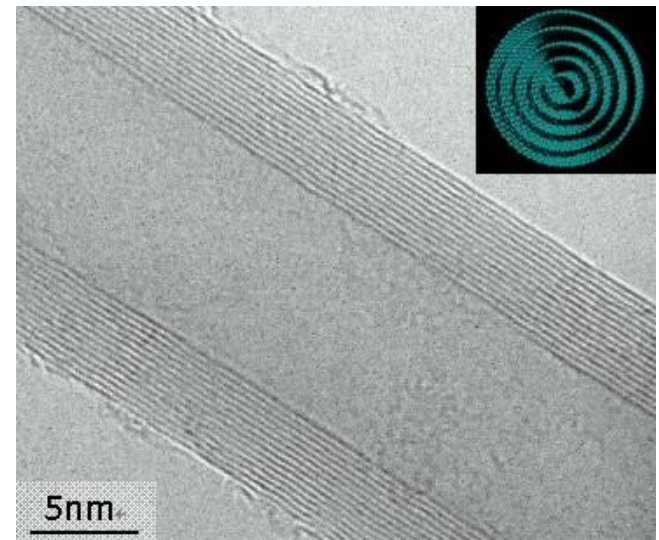
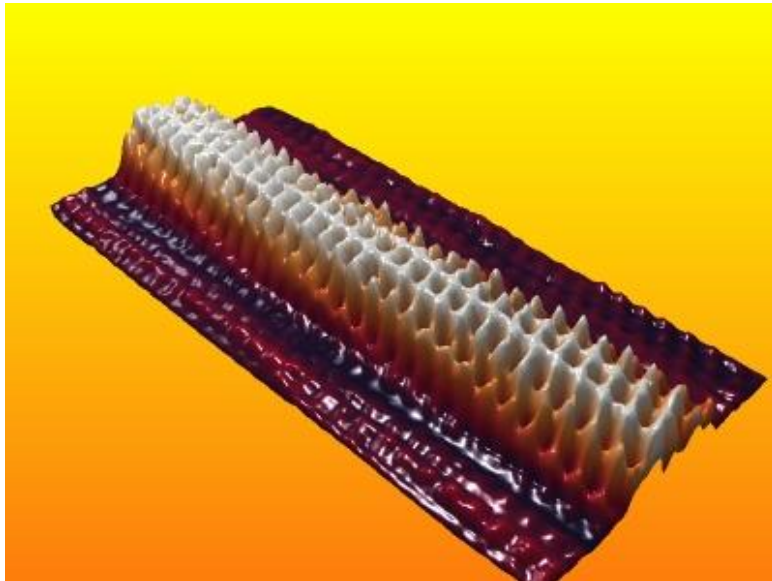
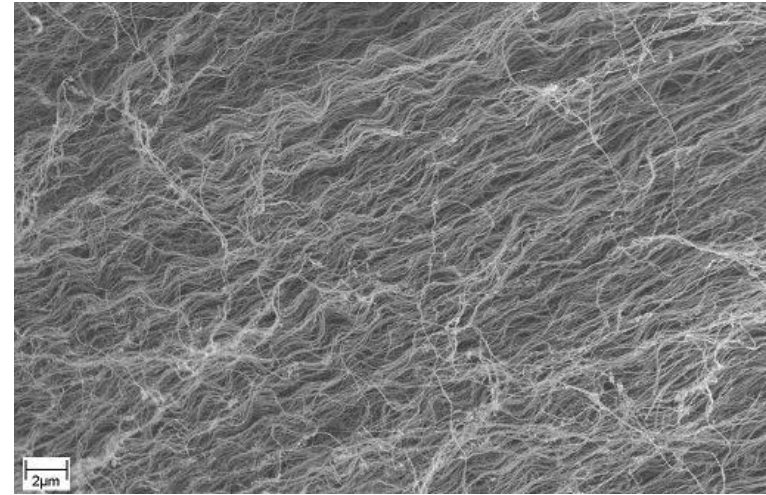
Production of CNTs

- Arc discharge: high voltage creates spark between graphite rods
- Laser ablation: laser vaporises graphite target
- Chemical vapor deposition: metal catalyst particles decompose hydrocarbon gas



Grown CNTs

- $d=1-4$ nm, $L>10$ cm
- Tangled web of CNTs
- Can be imaged using SEM, TEM, AFM, STM
- Deposit from suspension or grow on device substrate



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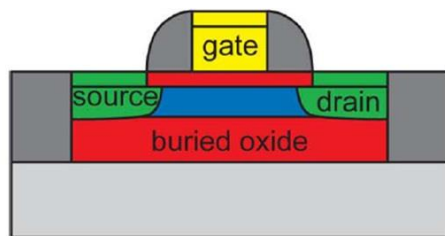
Gate length scaling

- + Increased speed -> lower gate delay (CV/I), higher g_m and f_T
- + Reduced power consumption -> energy delay product ($CV/I \cdot CV^2$)
- + Enables higher packing density
- Short channel effects when source and drain influence potential in the channel

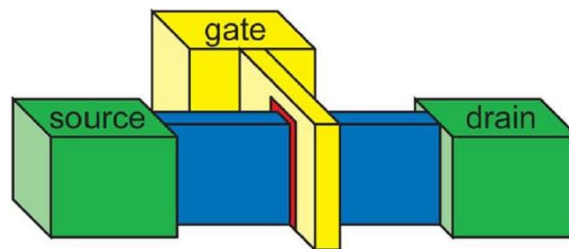
Need to reduce gate dielectric thickness, increase dielectric constant or change design.

Different gating geometries

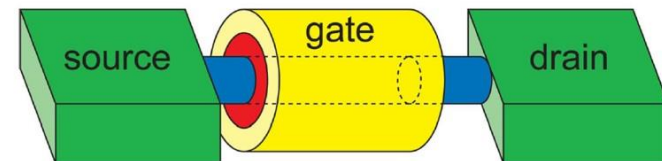
- $L_g > 5\lambda$ to avoid short channel effects
- λ is reduced by higher gate dielectric constant or thinner channel
- More wrapping of the channel gives lower λ
- CNTs and graphene allows for ultimate gate length scaling



$$\lambda_1 \approx \sqrt{\frac{\epsilon_{ch}}{\epsilon_{ox}} t_{ox} t_{ch}}$$



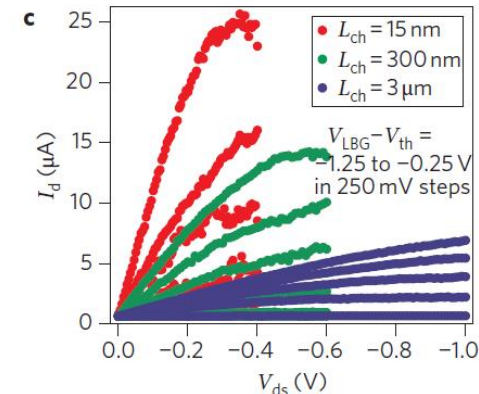
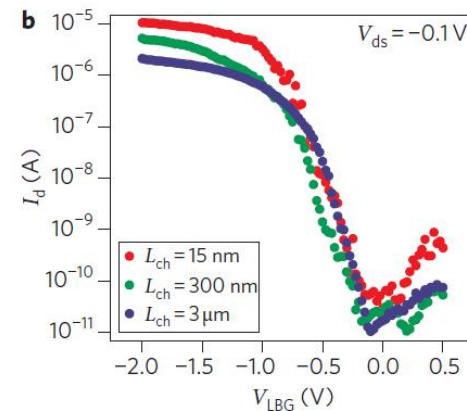
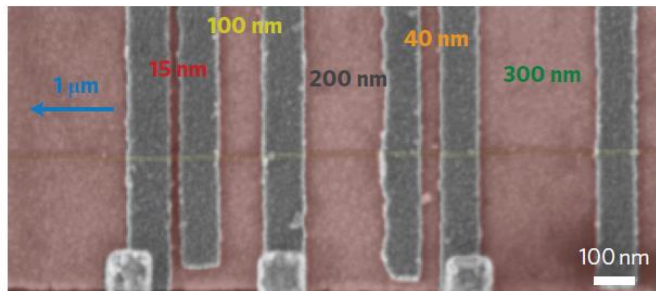
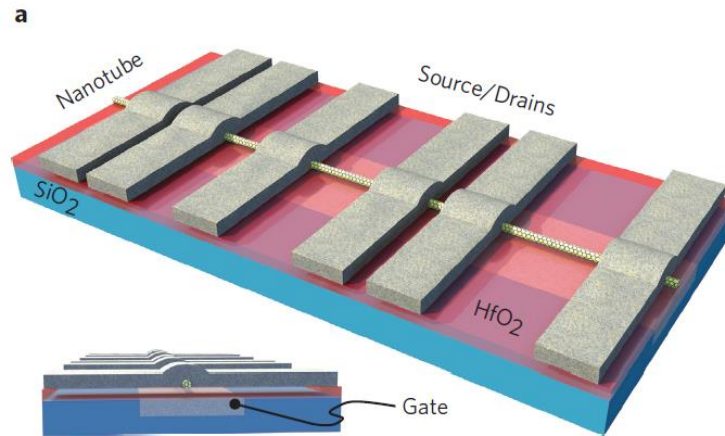
$$\lambda \approx \sqrt{\frac{\epsilon_{ch}}{2\epsilon_{ox}} t_{ch} t_{ox} \left(1 + \frac{\epsilon_{ox}}{4\epsilon_{ch}} \frac{t_{ch}}{t_{ox}} \right)}$$



$$\lambda \approx \sqrt{\frac{\epsilon_{ch}}{4\epsilon_{ox}} t_{ch} t_{ox} \left(1 + \frac{\epsilon_{ox}}{4\epsilon_{ch}} \frac{t_{ch}}{t_{ox}} \right)}$$

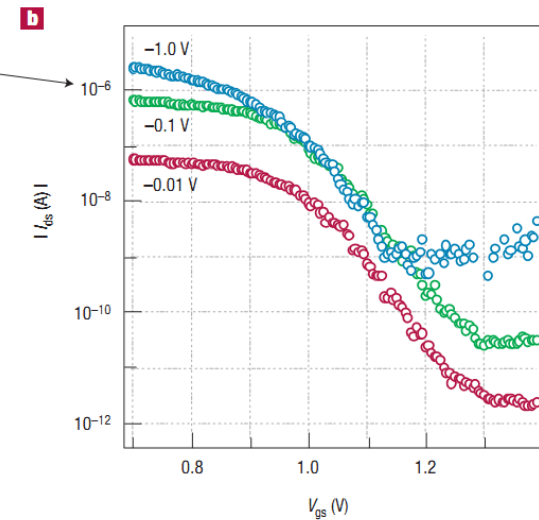
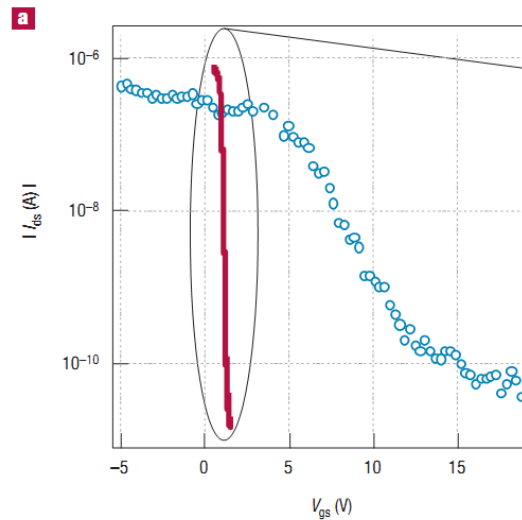
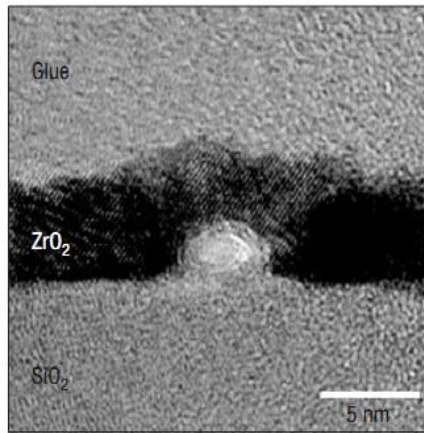
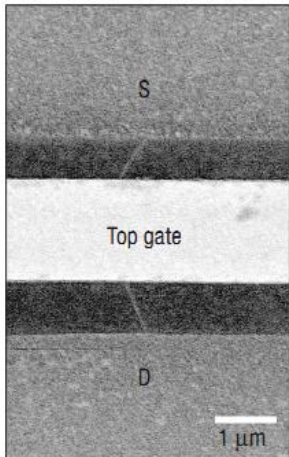
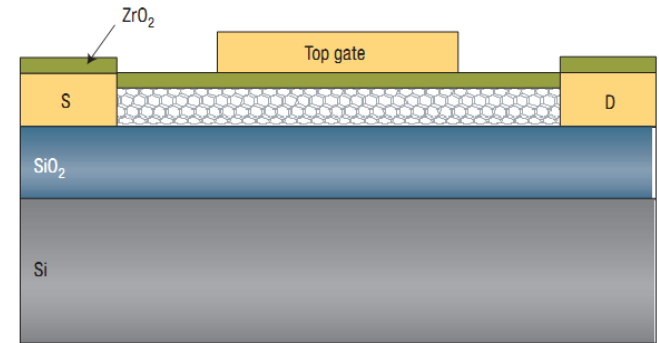
Gate length scaling

- No short channel effects down to $L_g=15$ nm
- $I_{on}=10 \mu A$
- on/off ratio = 10^5
- $S=90$ mV/dec also for short devices



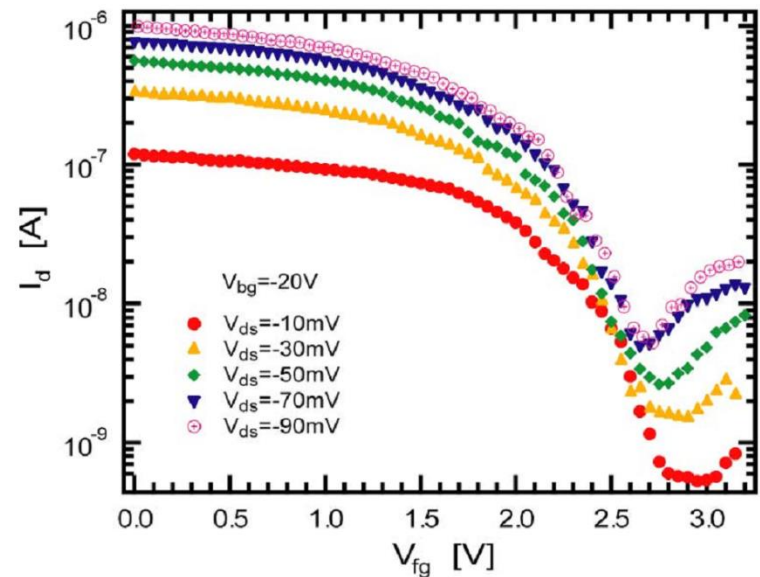
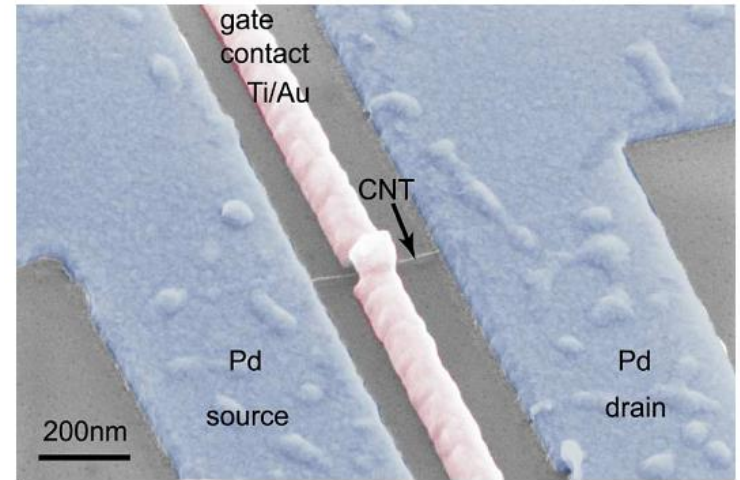
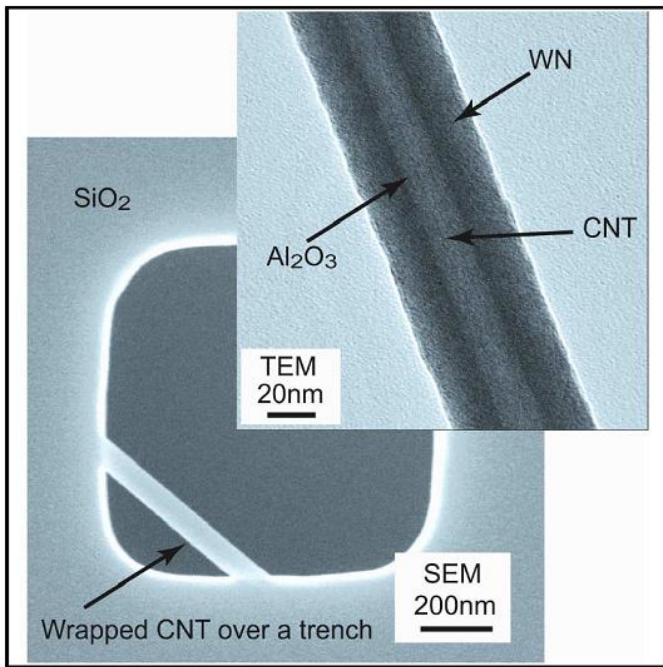
High k gate dielectrics

- No dangling bonds give nice interface
- Difficult to use ALD directly, dielectric grows only on substrate surface



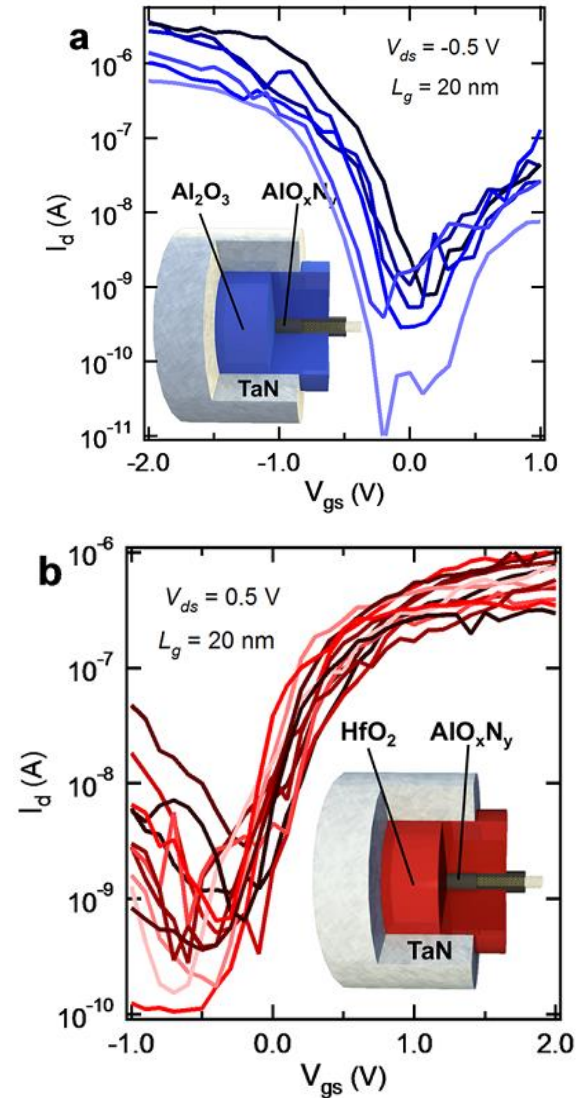
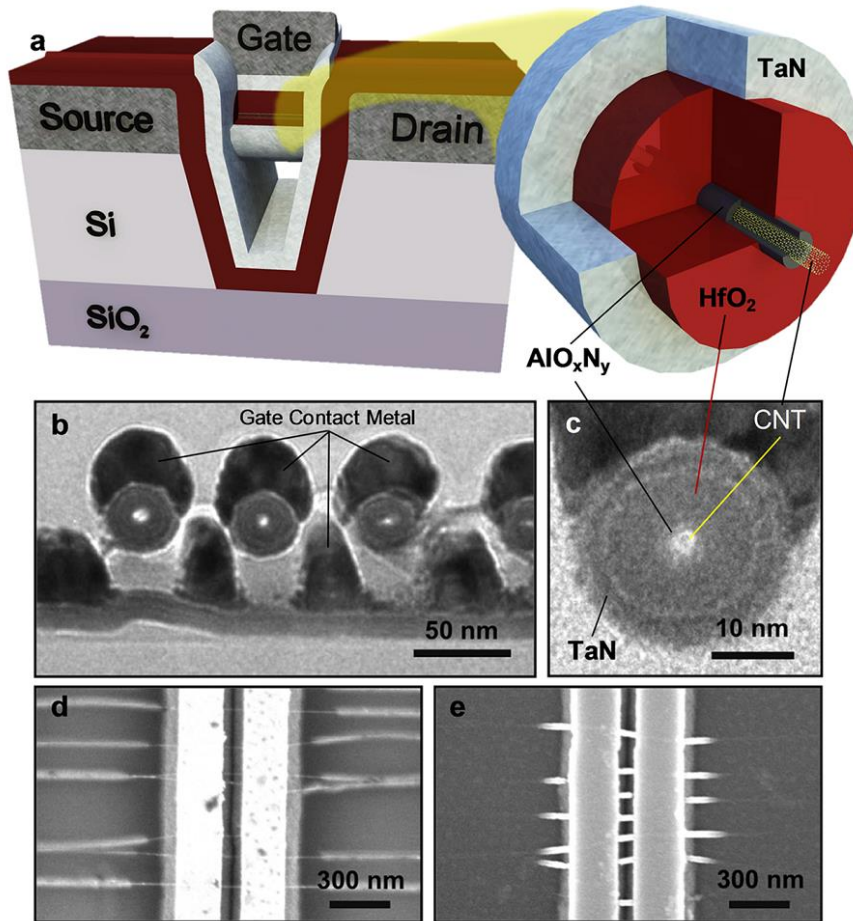
Coaxially gated CNTFET

- Wrap CNT in Al₂O₃ and WN using ALD
- Poor subthreshold swing due to interface charge and short channel effects



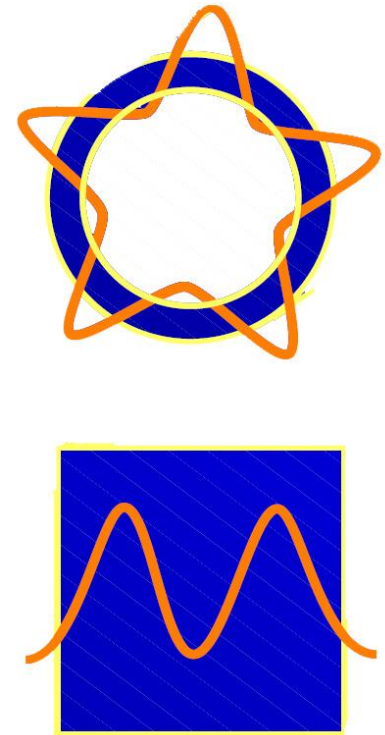
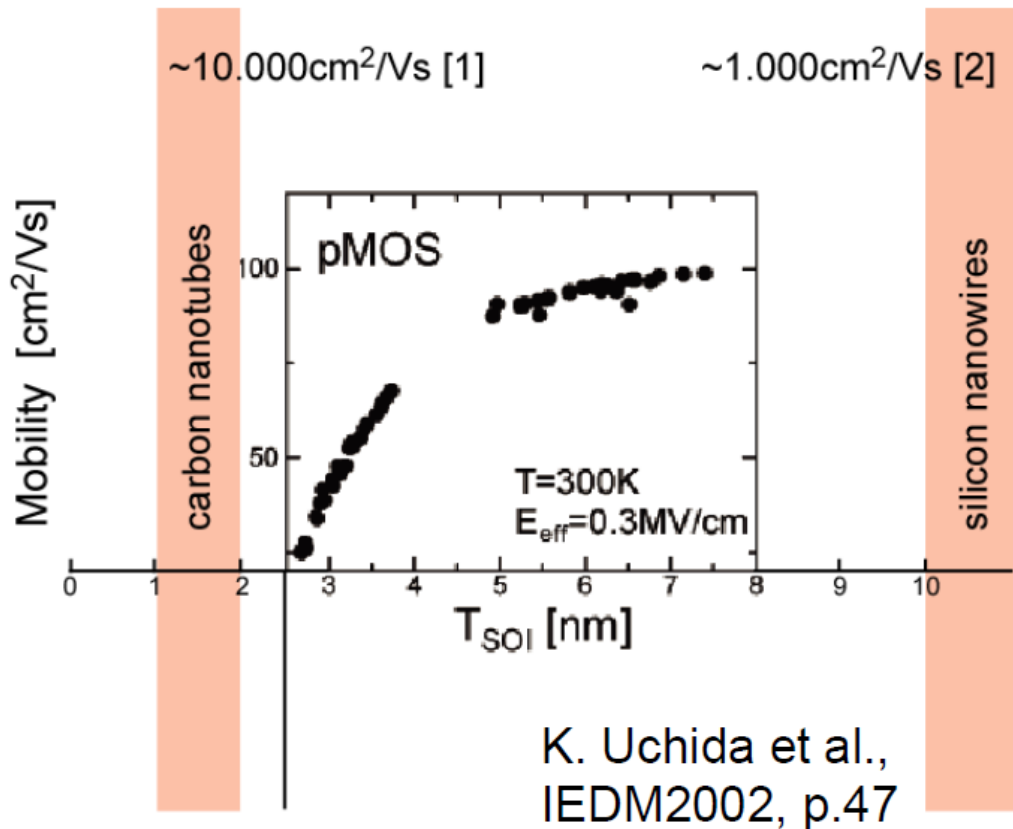
Coaxially gated CNTFET

- Control p or n-type by different high-k



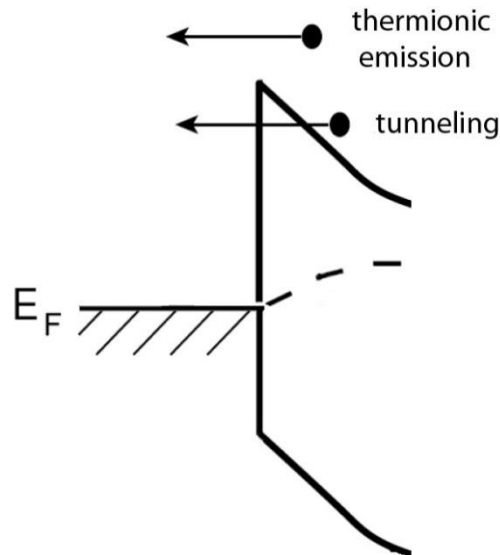
Surface scattering

- Need to reduce channel thickness to be able to reduce L_g
- Mobility of SOI MOSFETs is lowered with t_{SOI} due to surface scattering
- Not a problem for CNTs

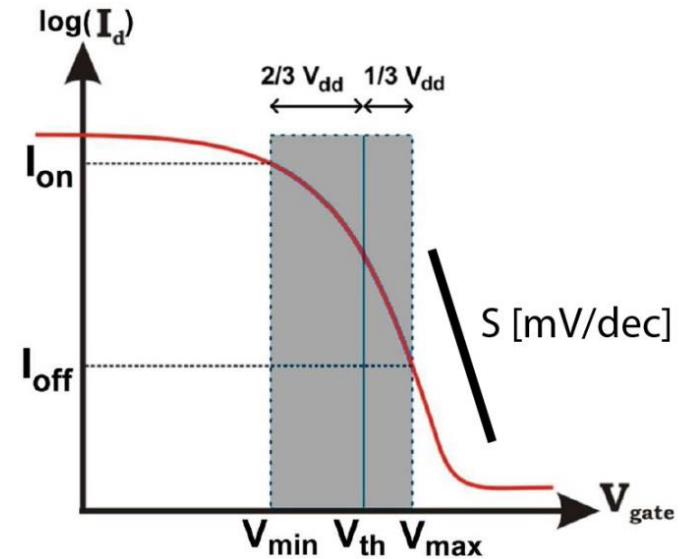


Improving the inverse subthreshold slope

- "conventional" FETs rely on thermionic emission over a barrier
- $S \geq \ln(10)k_B T = 60 \text{ mV/dec}$ at RT
- A decreased S enables a lower V_{dd} while keeping the same on/off ratio \rightarrow increased speed and reduced power consumption

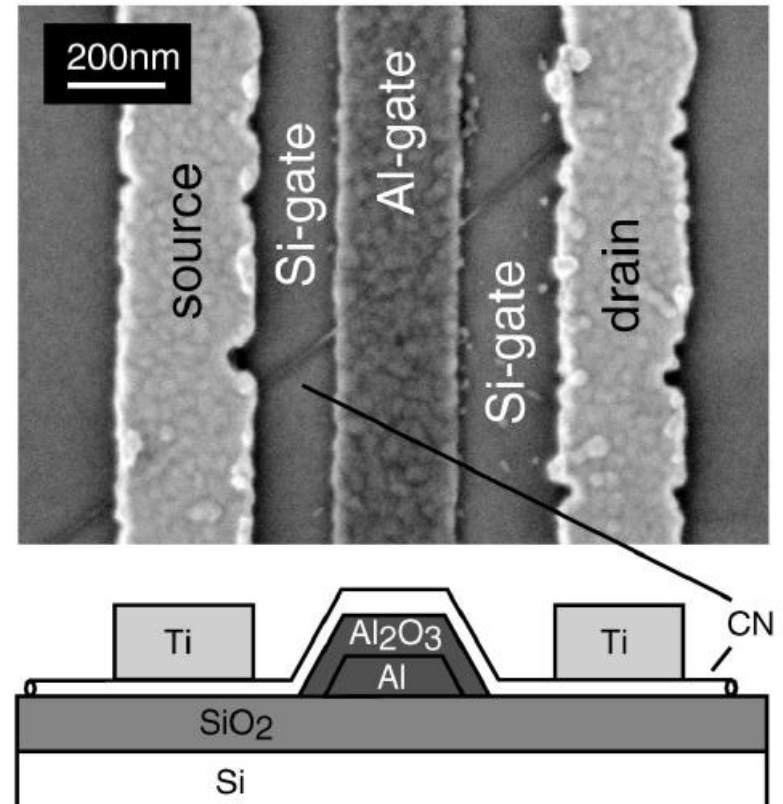


$$S = \left(\frac{d \log_{10}(I_d)}{dV_g} \right)^{-1}$$



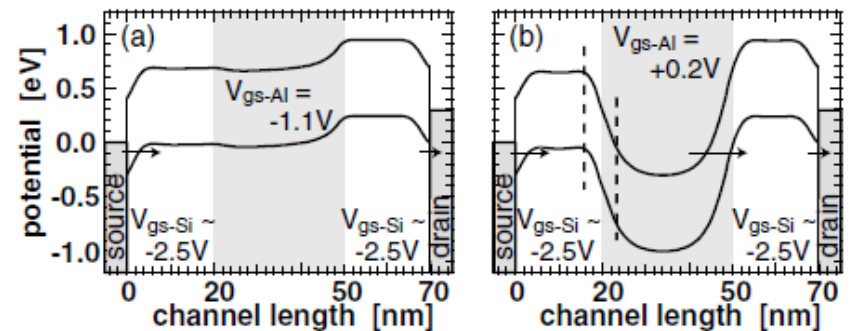
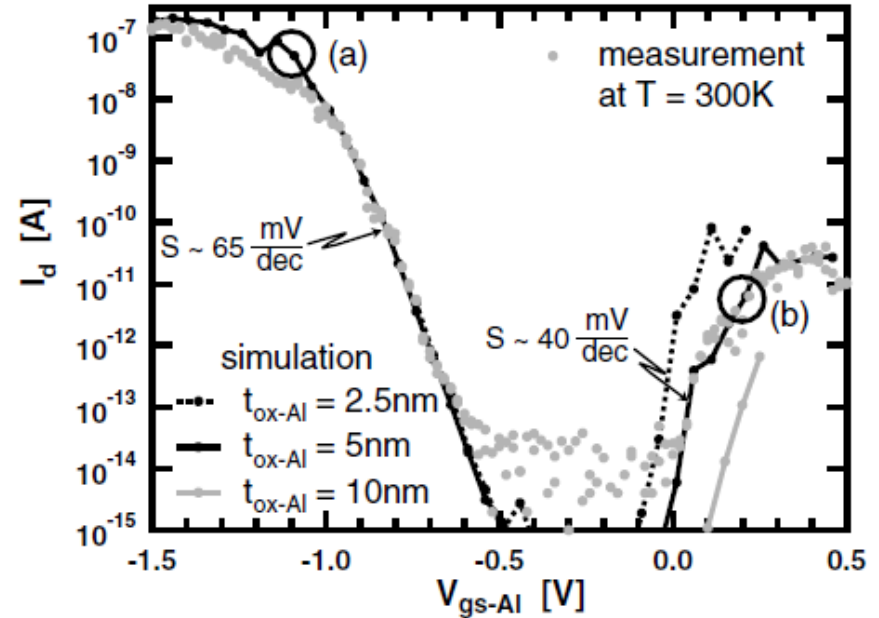
Band-to-band tunneling

- λ is a few nm in CNT - \rightarrow sharp band bending
- Low effective mass
- Long mfp
- Same effective mass of electrons and holes
- Direct band gap



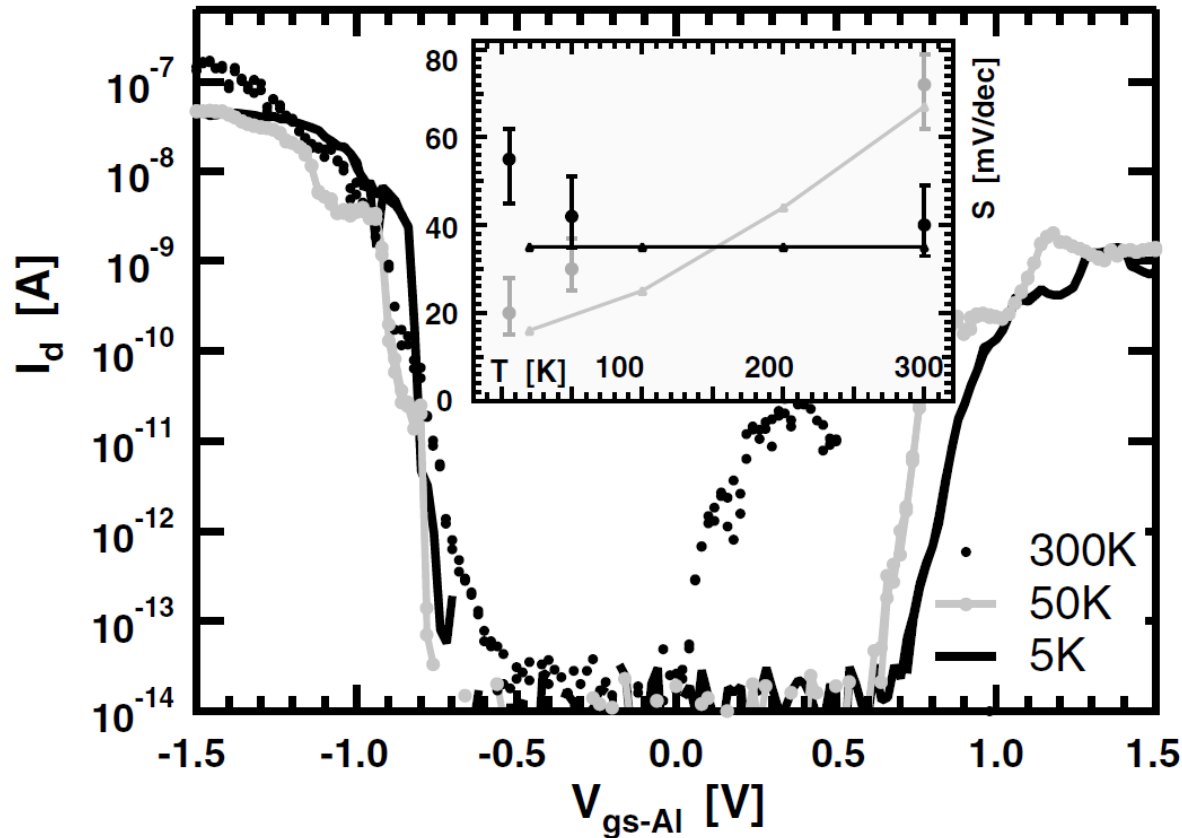
Electrical characteristics

- Back gate to form p-type regions
- Al gate to switch FET
- Ambipolar characteristics
- $S=40$ mV/dec for the n-branch
- Band-to-band tunneling at the border between the gates



Temperature dependence

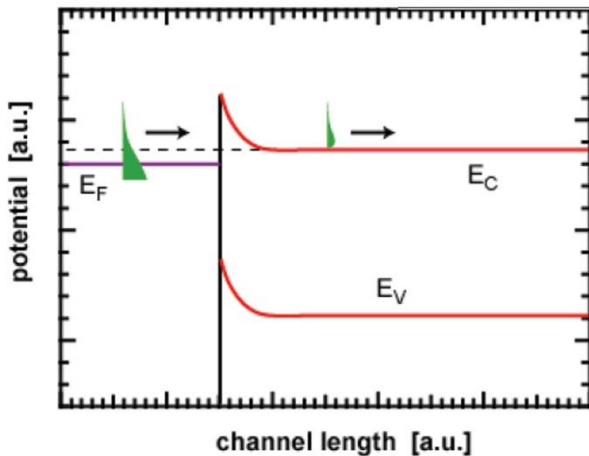
- S is not reduced with temperature for the n-branch -> tunneling
- S is reduced with temperature for the p-branch -> thermionic emission



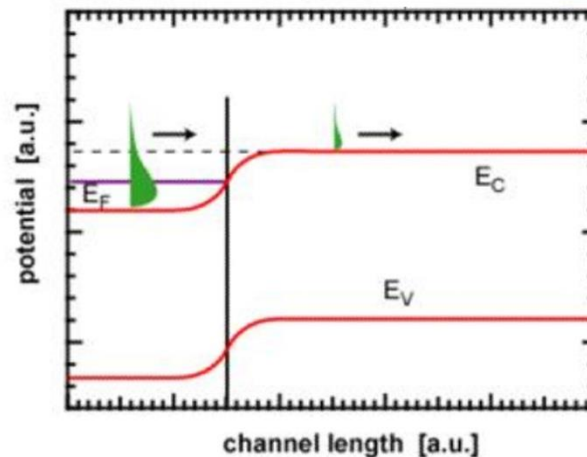
Mechanism of S reduction

- Only high energy tail of Fermi-Dirac distribution is transferred in thermionic emission or in tunneling through Schottky barrier
- Band-to-band tunneling "filters" the Fermi-Dirac distribution since the band edges "cut off" the high energy tail
- For BTB tunneling, small movement of bands give large change in current i.e. small S

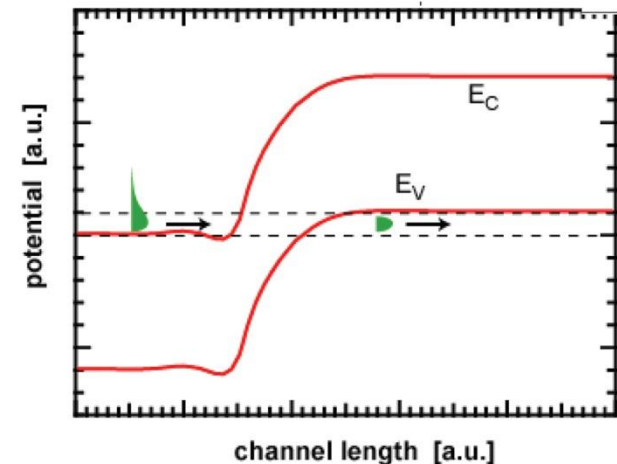
tunneling at Schottky barrier



thermionic emission

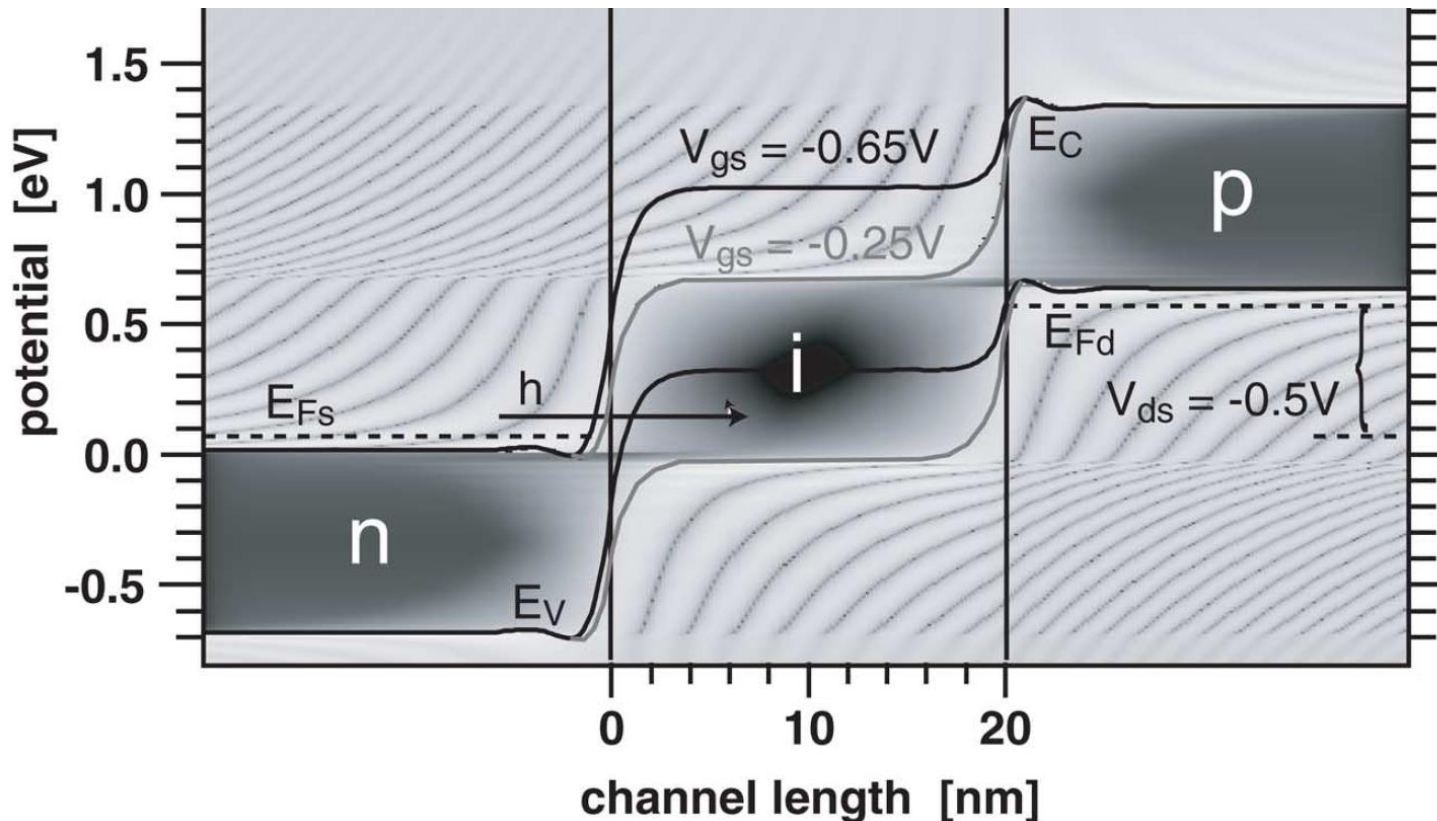
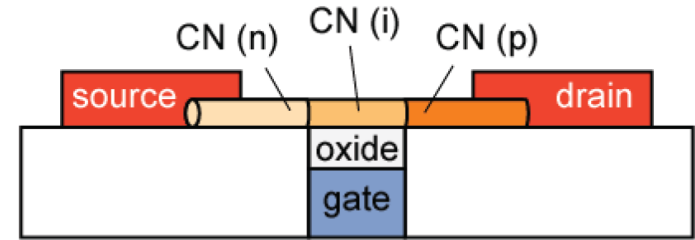


band-to-band tunneling



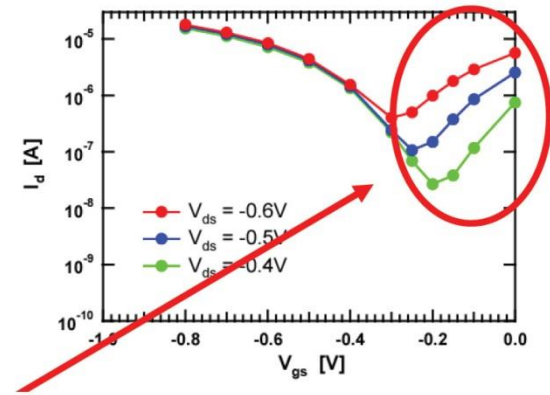
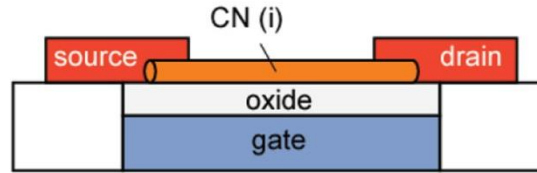
An improved tunneling CNTFET

- n-i-p doping
- Only one tunneling event
- Avoids charge pile-up in central region
- Difficult to make with a CNT

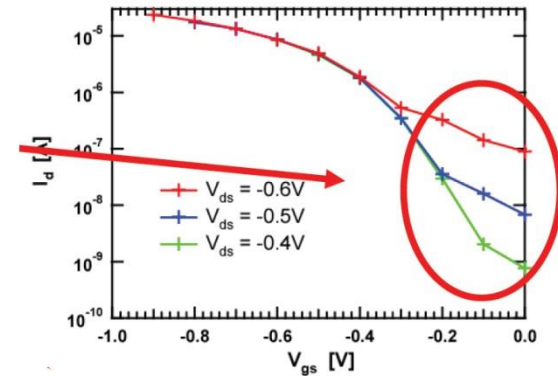
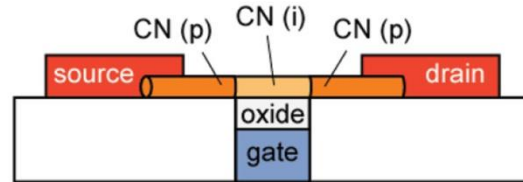


Three types of CNTFETs

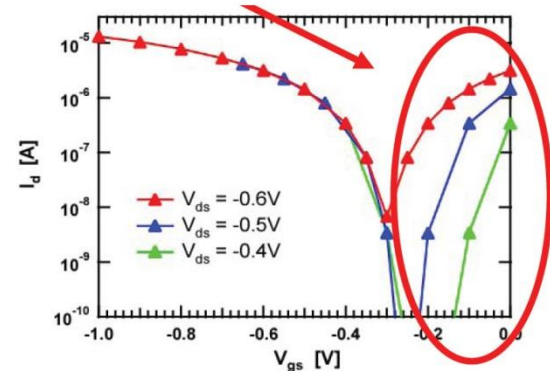
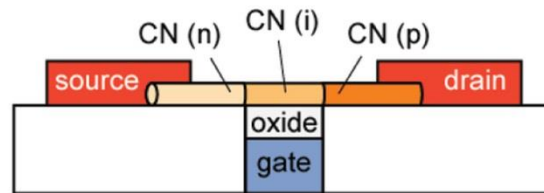
Schottky barrier



Doped contacts

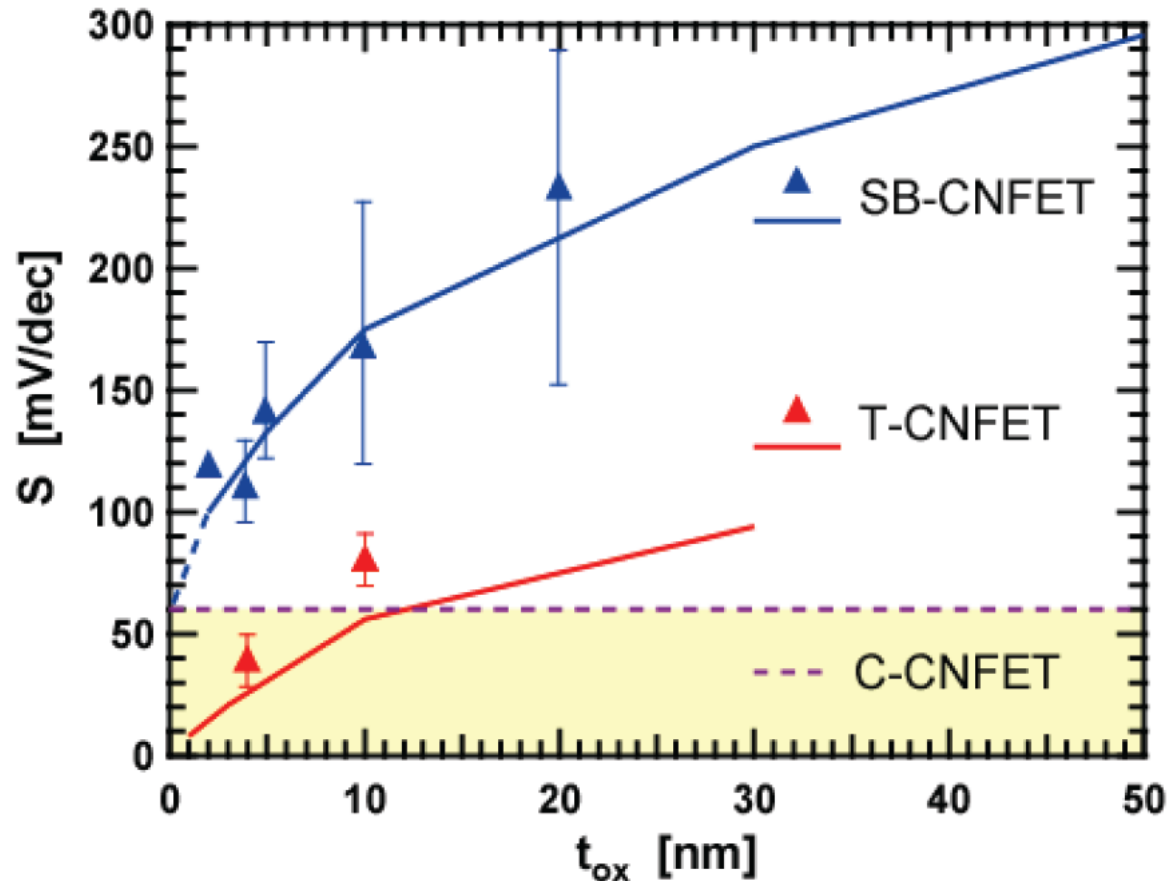


Band-to-band tunneling



Comparing devices

- For thin gate dielectrics the BTB tunneling FET can reach $S < 60$ mV/dec
- Very low I_{on} in n-branch



Outline

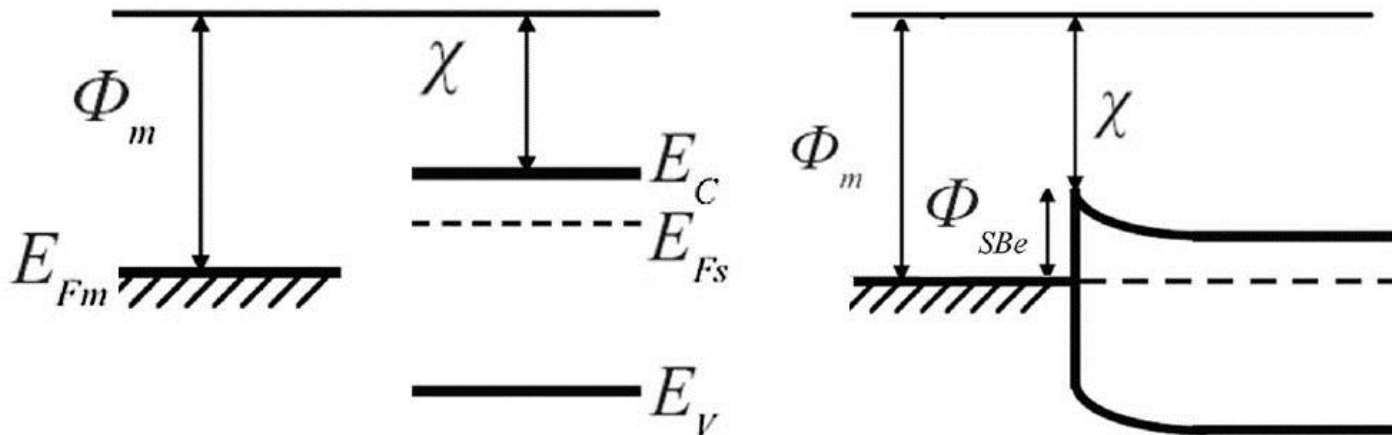
- Basics of graphene and CNTs
 - Structural
 - Electronic
 - Production of CNTs
- Advantages of CNTs for FETs
 - Gate length scaling
 - Coaxial gate
 - High-k compatibility
 - Band-to-band tunneling
- **Challenges of CNT integration**
 - **Contacts**
 - **Doping**
 - **Positioning**
 - **Chirality control**
- Towards integration
 - Flexible electronics
 - High frequency performance

Schottky barrier basics

- Potential barrier between metal and semiconductor
- Gives rectifying behaviour
- Change metal work function -> change SB height
- Too simple !!!

$$\Phi_{SBc} = \phi_m - \chi$$

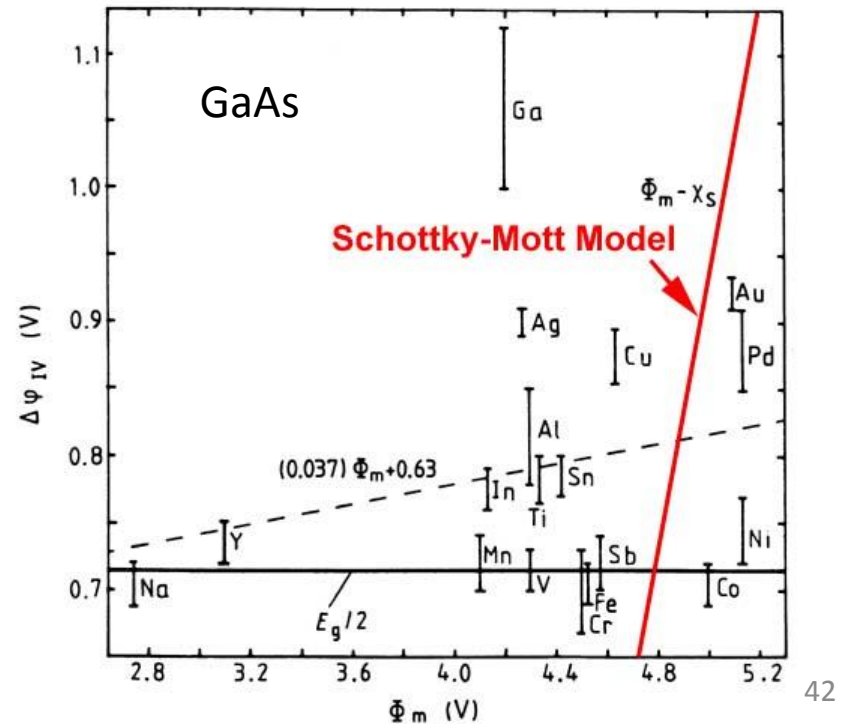
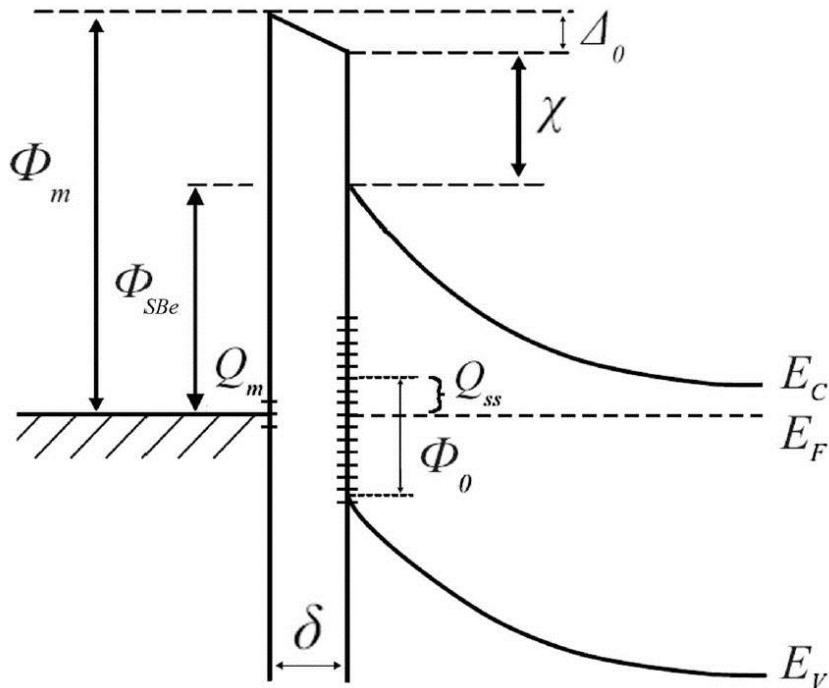
$$\Phi_{SBh} = \chi + E_g - \phi_m = I_s - \Phi_m$$



Fermi level pinning

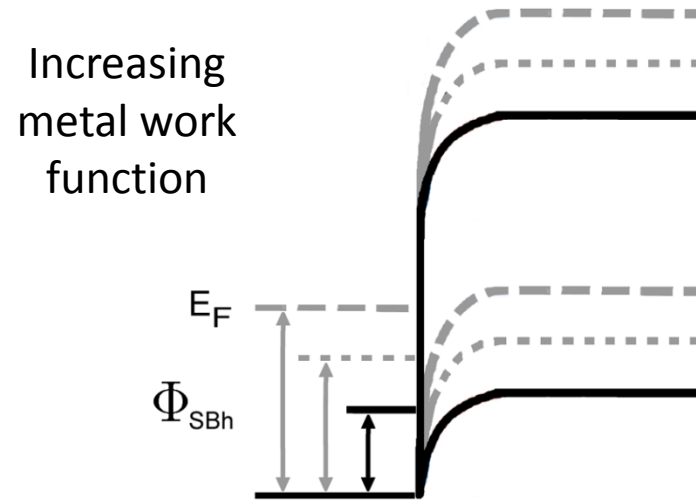
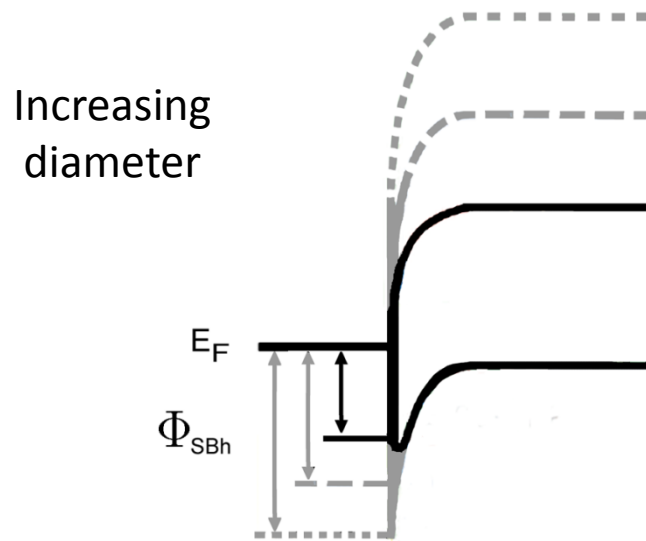
- Interface states form dipoles that shift bands
- SB height often independent on metal work function

$$\Phi_{SBe} = \gamma(\Phi_m - \chi) + (1 - \gamma)(E_g - \Phi_0) \quad \gamma = \frac{1}{1 + \frac{qD_{it}\delta}{\epsilon_i}}$$



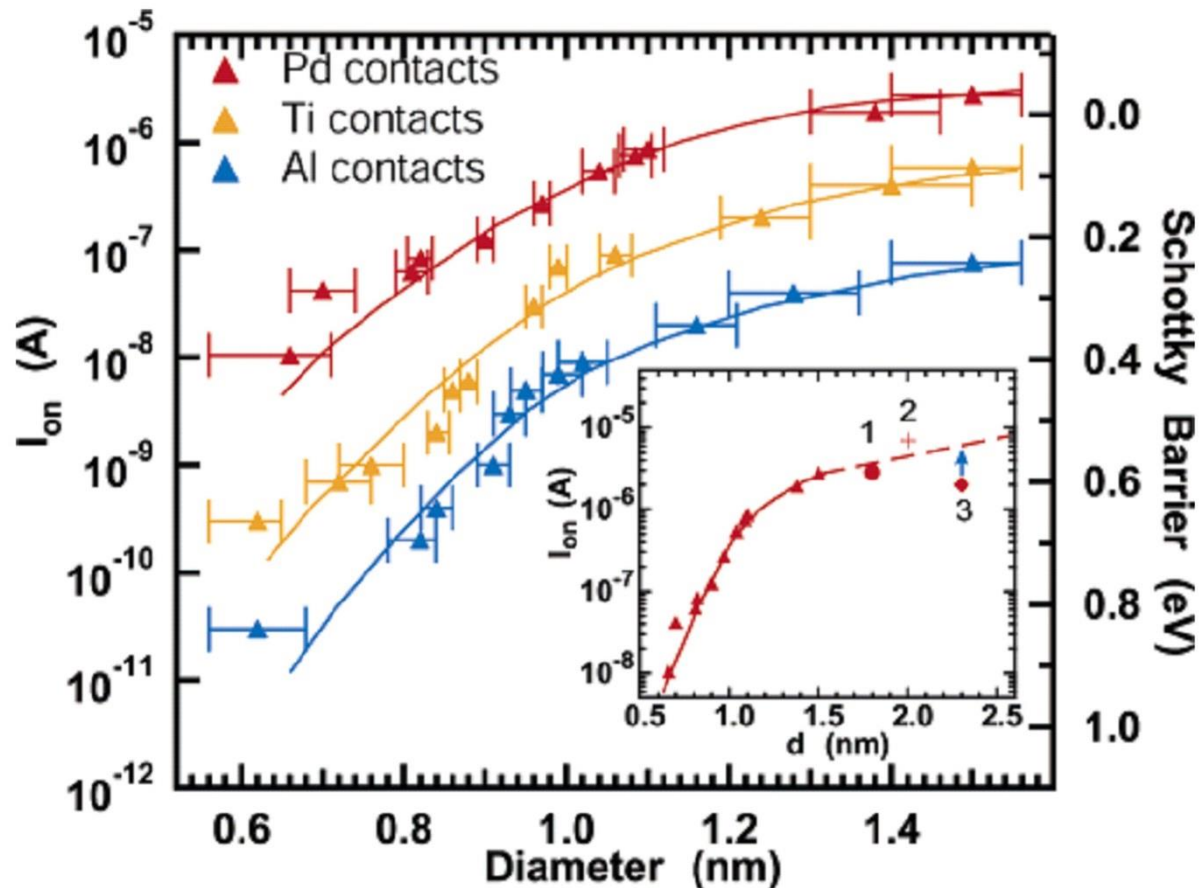
Schottky barrier to CNTs

- Theoretically predicted that interface states have no influence on CNT-metal contacts
- Increasing CNT diameter gives lower barriers
- Increasing metal work function gives lower hole barriers



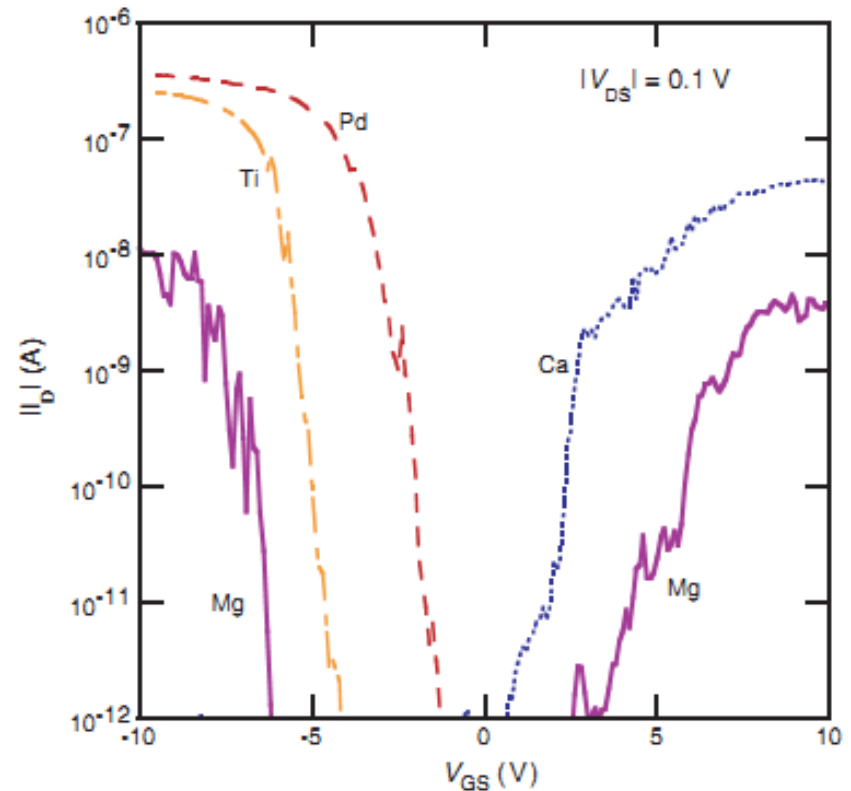
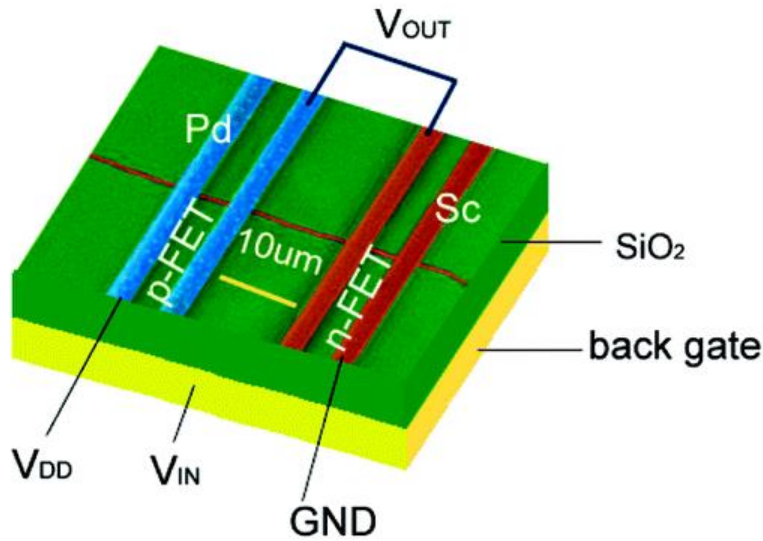
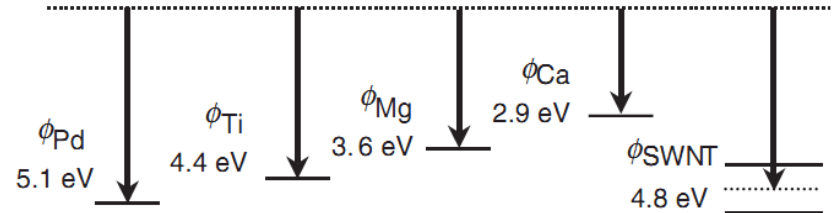
Different contact metals

- Increasing I_{on} with larger CNT diameter
- Increasing I_{on} with higher work function
- No or small effect of Fermi level pinning



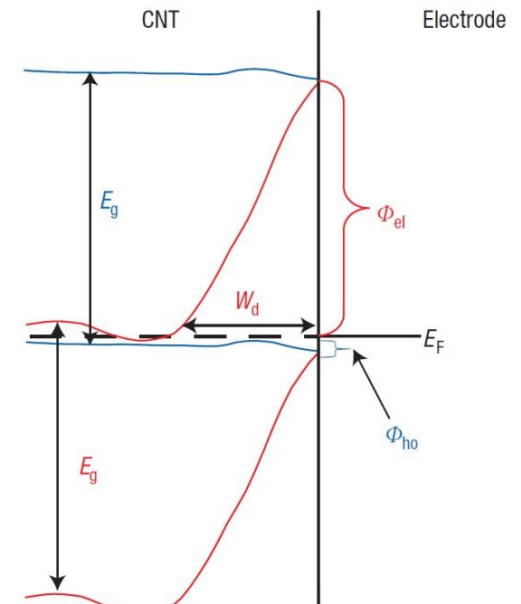
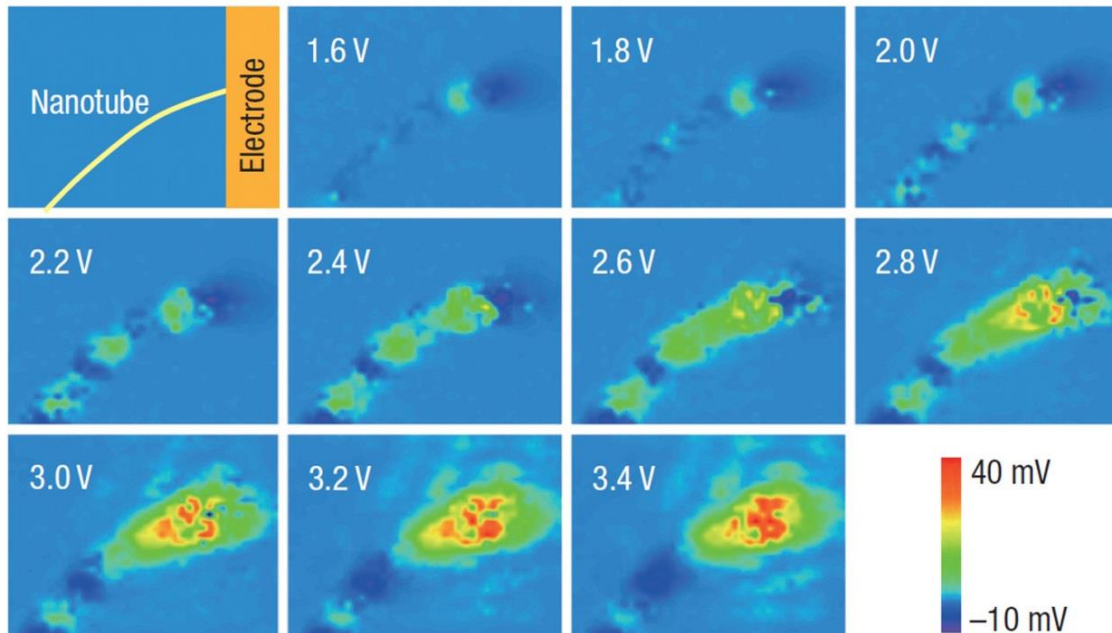
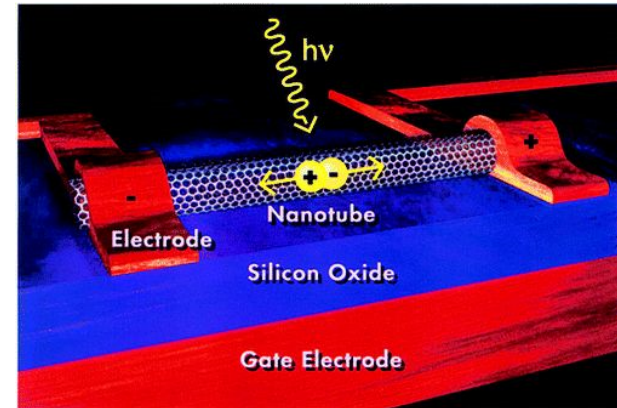
Metal work function impact

- Can form n or p-type devices using different metals
- Pd best for p-type
- Sc best for n-type



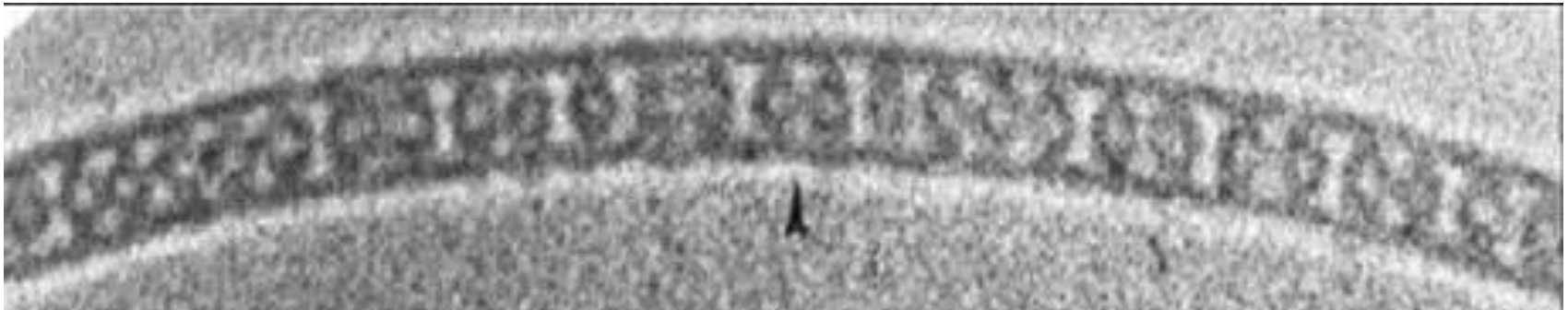
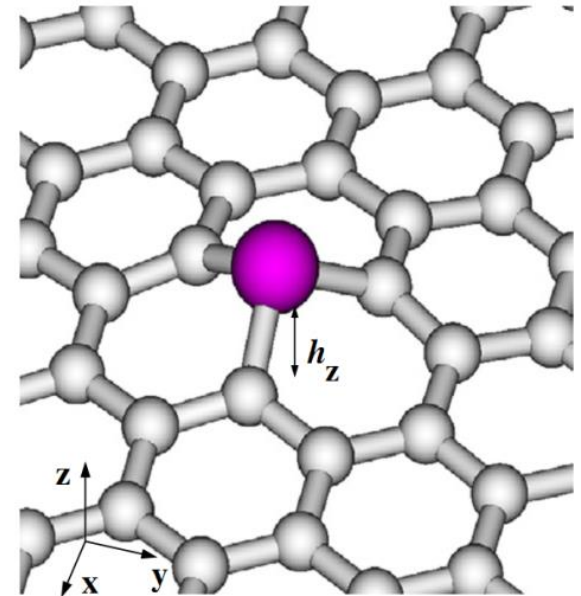
Imaging Schottky barriers

- Laser generates e-h pairs
- Pair separated by electric field -> photocurrent
- Scan laser spot and change gate voltage
- Obtains size of depletion width



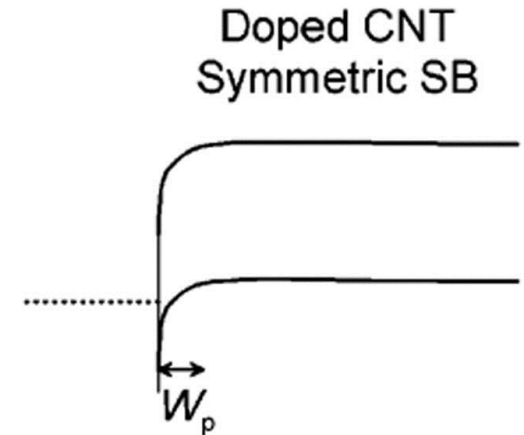
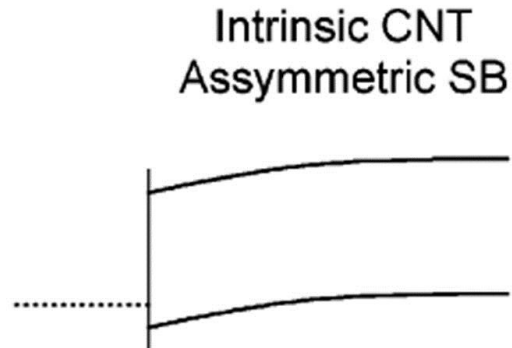
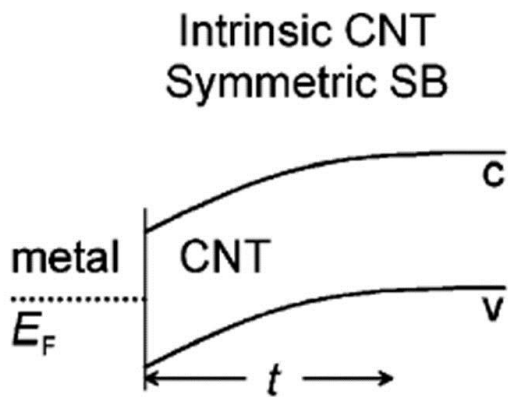
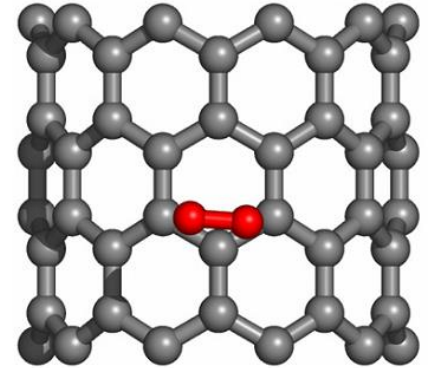
Doping

- Important for CMOS and good contacts
- Substitutional doping is difficult
- Use charge transfer doping
- Filling with C_{60} p-dopes
- Filling with $Gd@C_{82}$ n-dopes



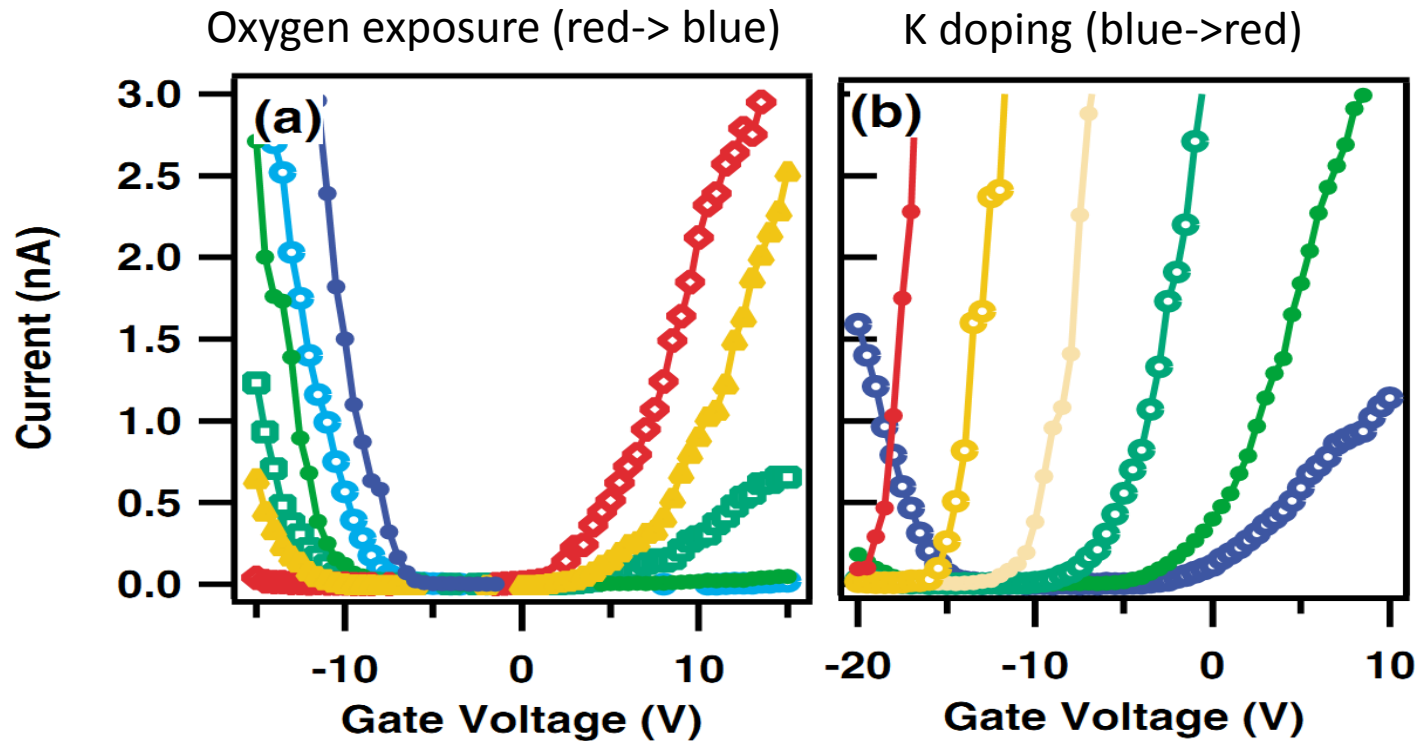
CNTFETs in air

- Physisorbed oxygen p-dopes CNT
OR
- Increases metal work function of contact



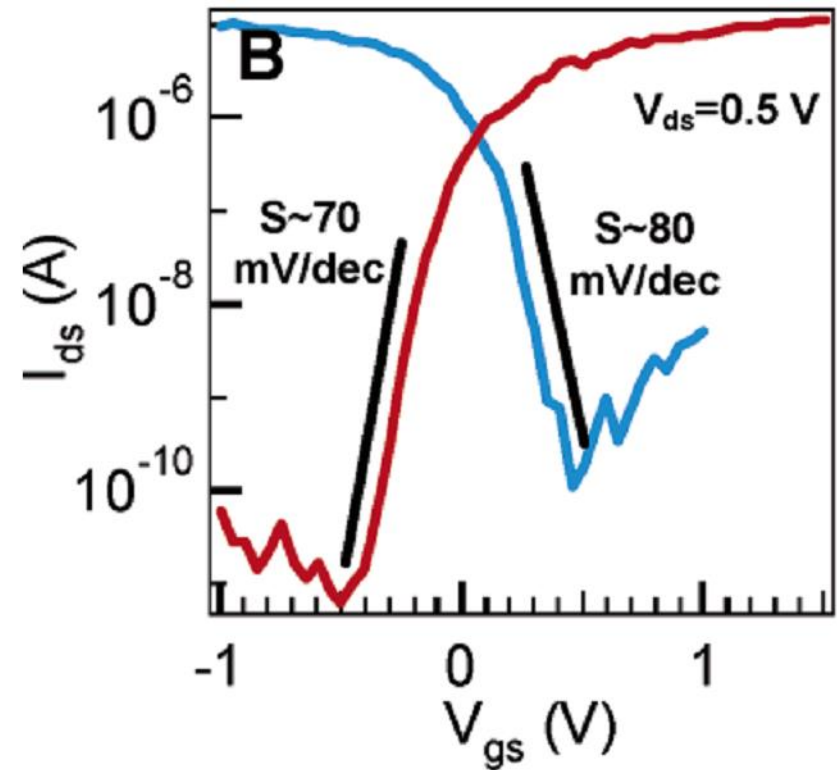
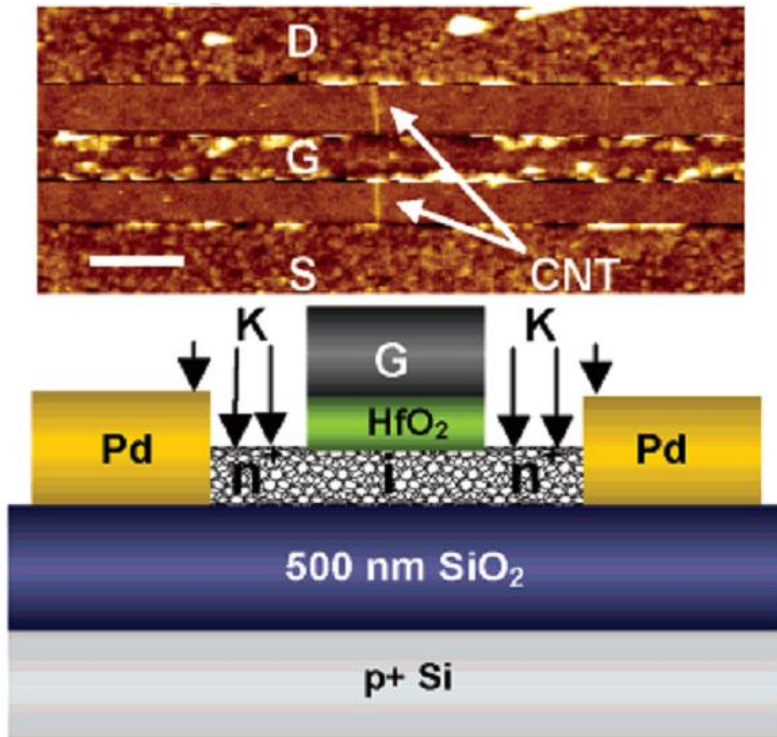
Potassium doping

- K physisorbed on CNT n-dopes by charge transfer
- p-branch is lowered, n-branch is increased, V_{th} shifted
- Not stable in air



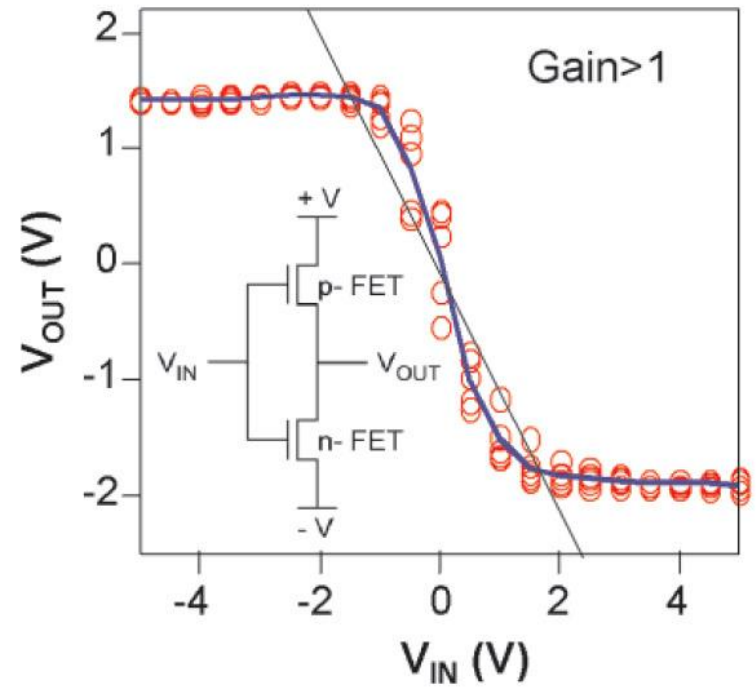
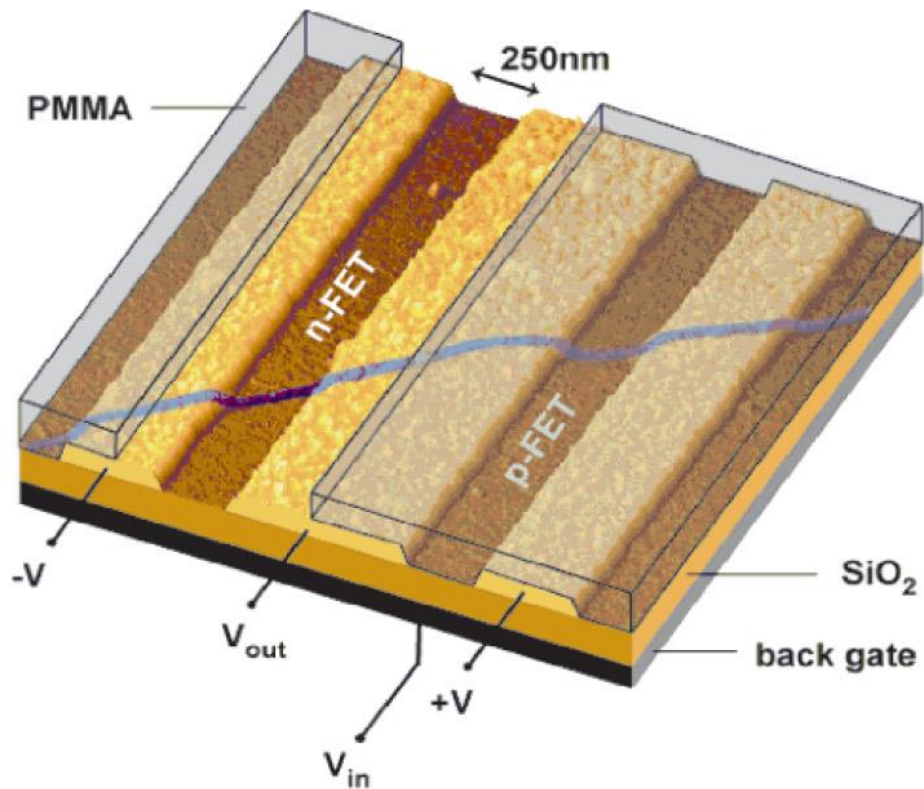
Doped contacts

- Dope outer CNT segments using K
- Removes influence from Schottky barrier at metal contact



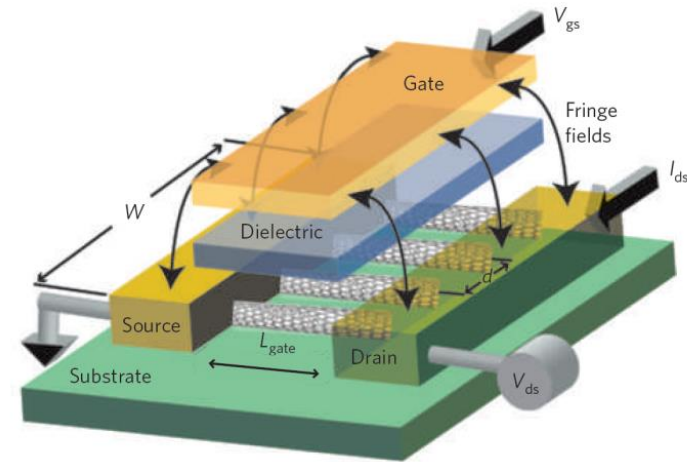
Logic gates

- Inverter from p and n CNTFET on the same CNT
- Use K doping or annealing to form n-CNTFET

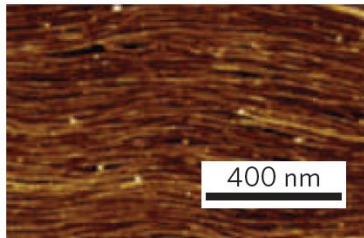


Positioning

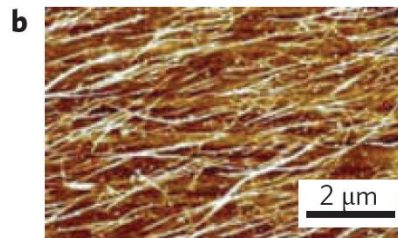
- Multiple parallel CNTs in each FET increases I_{on} , g_m
- Dense packing reduces parasitic capacitances
- Need to control position and orientation of CNTs pre- or postgrowth



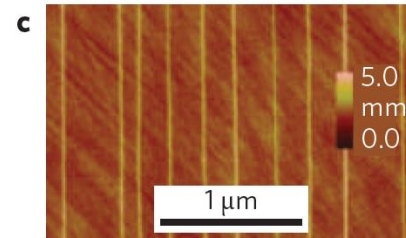
Langmuir-Blodgett



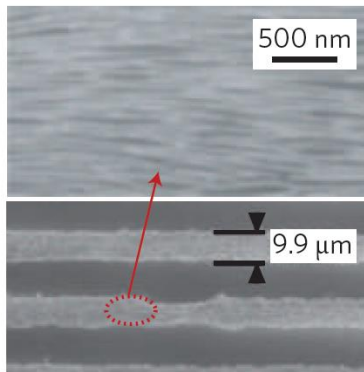
Spin-coating



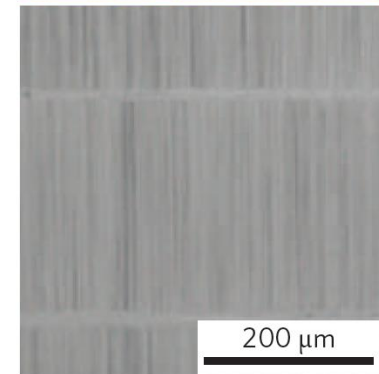
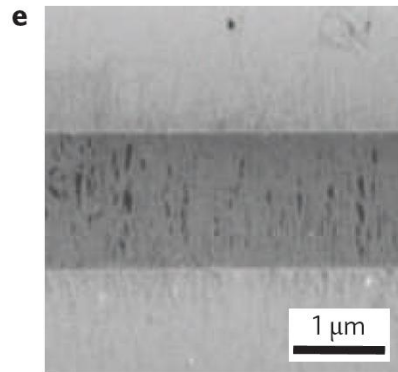
CVD



Droplet

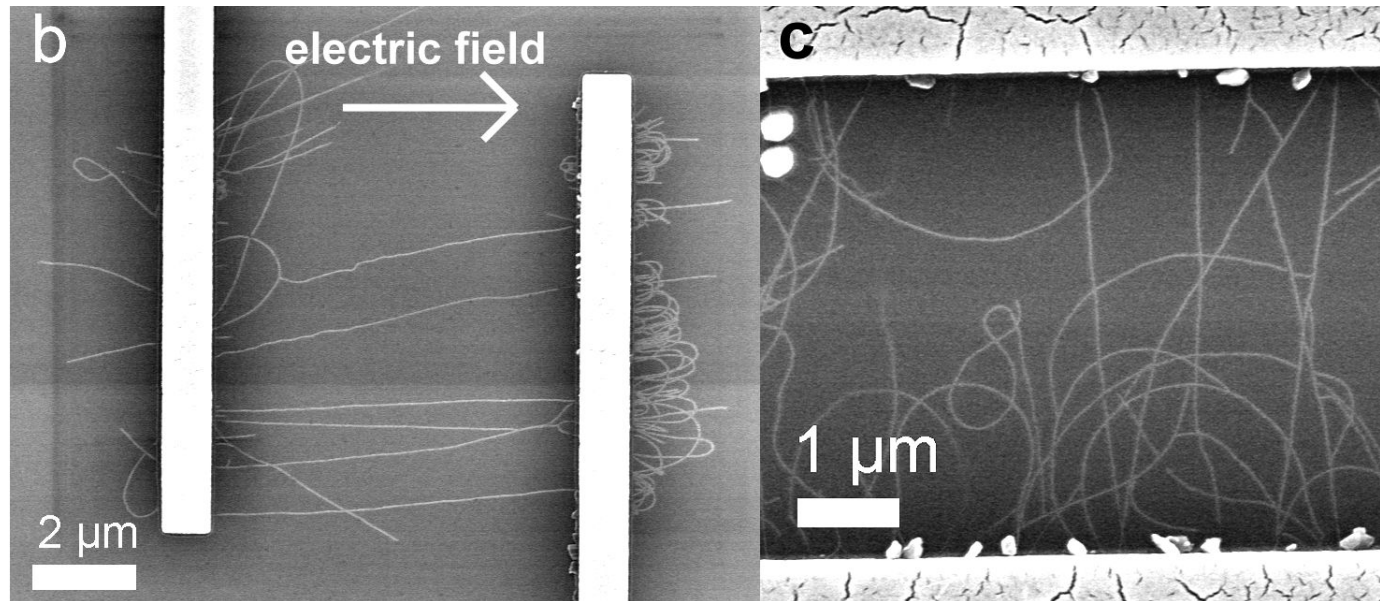
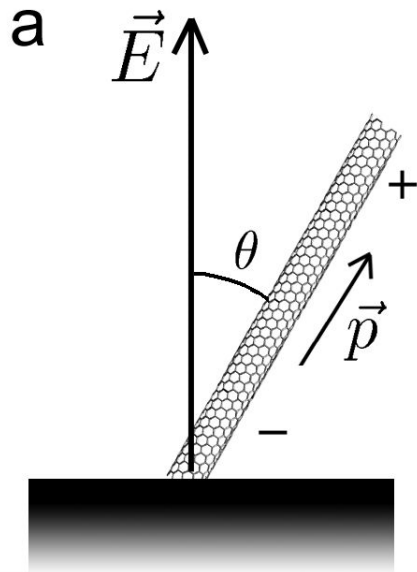


Dielectrophoresis



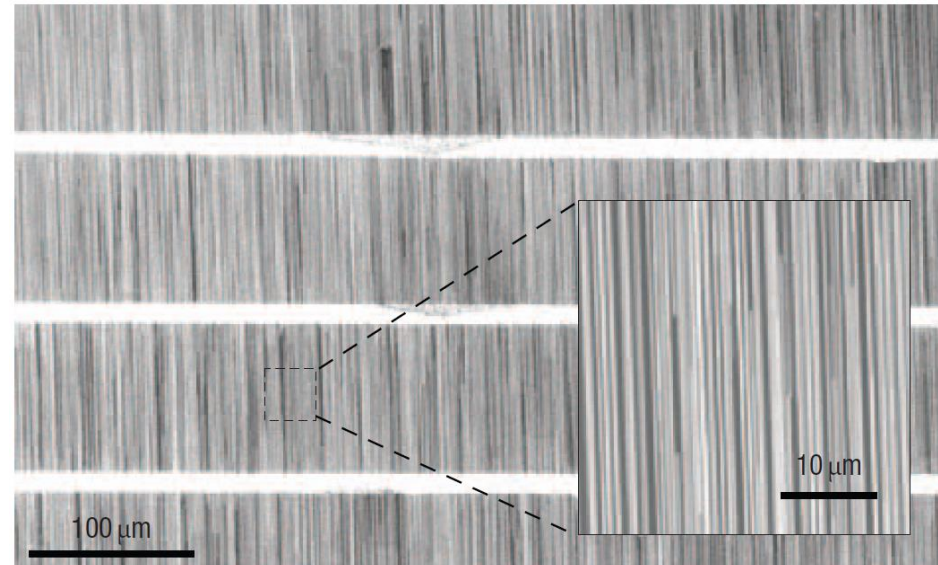
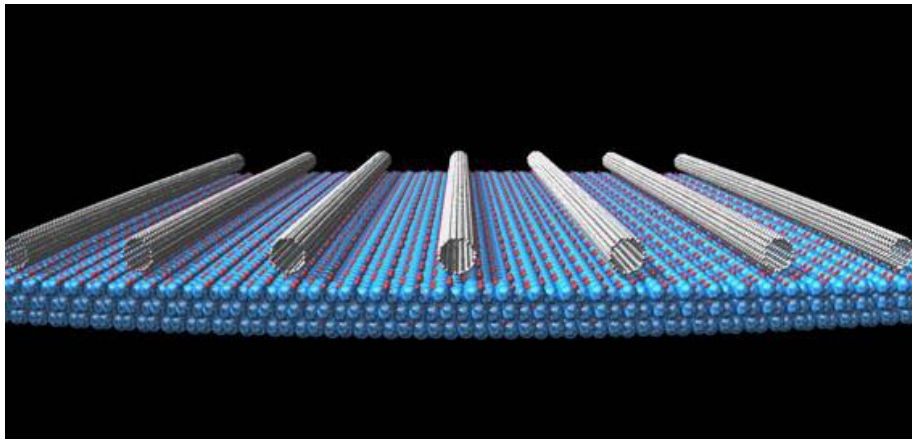
Electric field alignment

- Apply voltage to electrodes during CVD
- Dipole in CNTs align them with field lines
- Difficult to implement for large scale circuits



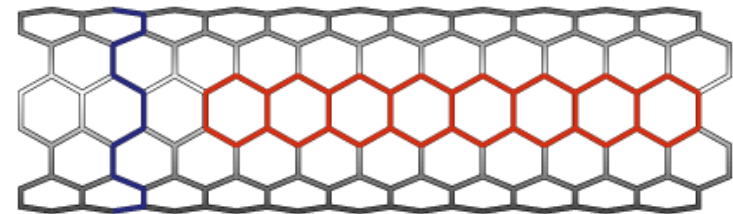
“epitaxial” alignment

- CNTs align in certain crystal orientations of sapphire or quartz substrates
- CNTs align at atomic steps
- Strong attractive interaction between CNTs and Al atoms
- 99.9% are aligned within 0.01°
- 10 CNTs / μm

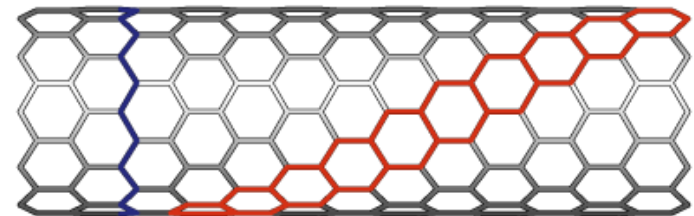


Chirality control

- Metallic CNTs in FETs -> leakage currents - > poor on/off ratio
- Need chirality control or at least control of CNT type
- Need to either:
 - Selectively grow only metallic or semiconducting
 - Separate the two types
 - Selectively destroy one type



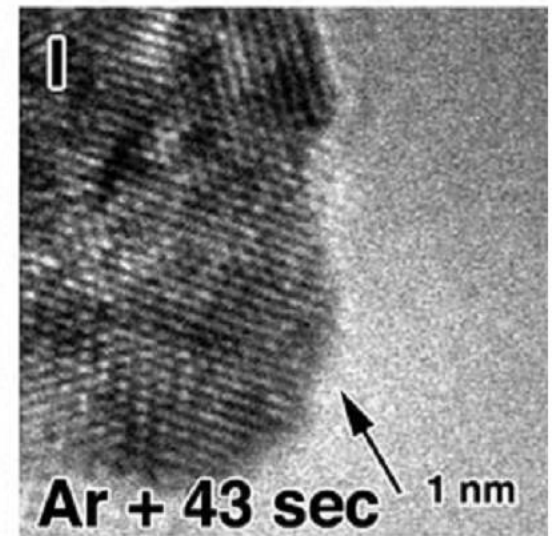
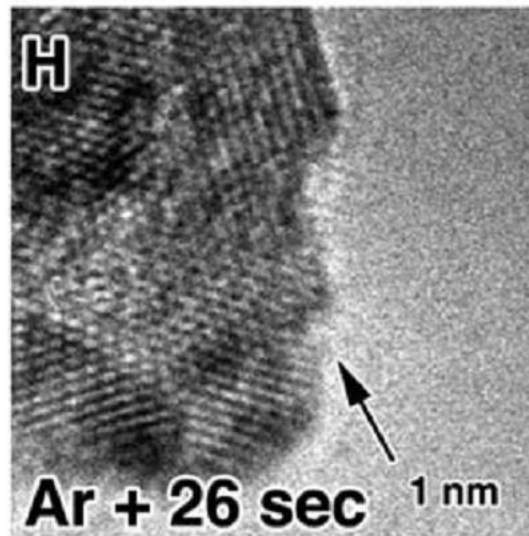
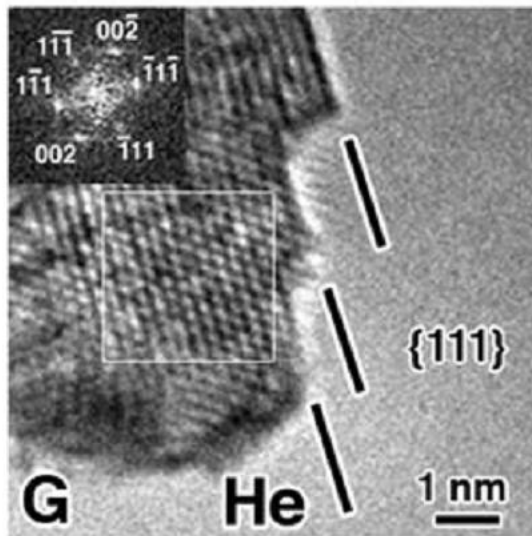
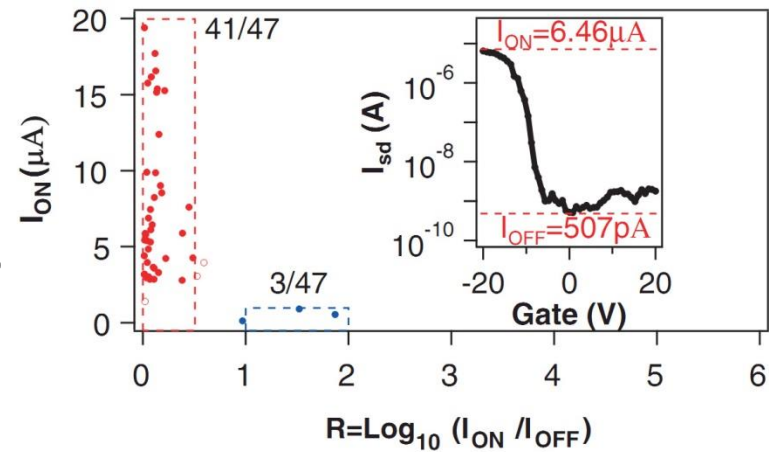
Armchair



Zig-zag

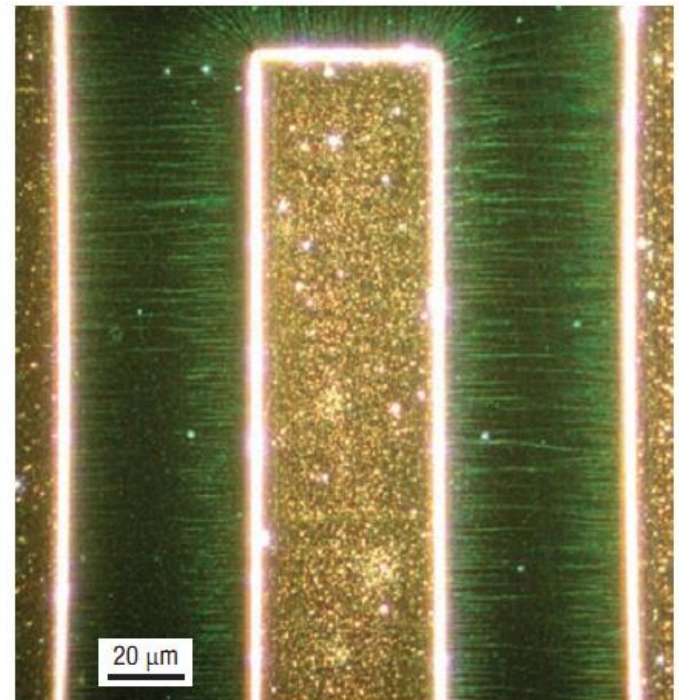
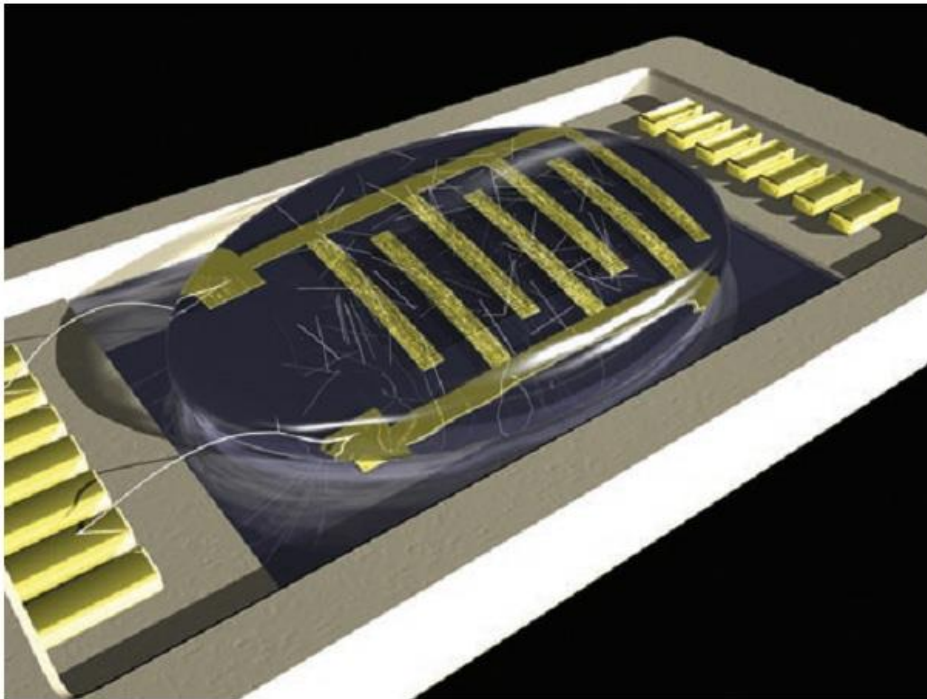
Selective growth

- Anneal metal catalyst in Ar, He or H₂
- Increased metallic CNT part from 33% to 91%
- Strong facets when annealed in He
- Steps in particle important for chirality control?
- Not so good or well understood



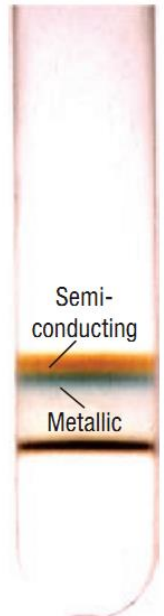
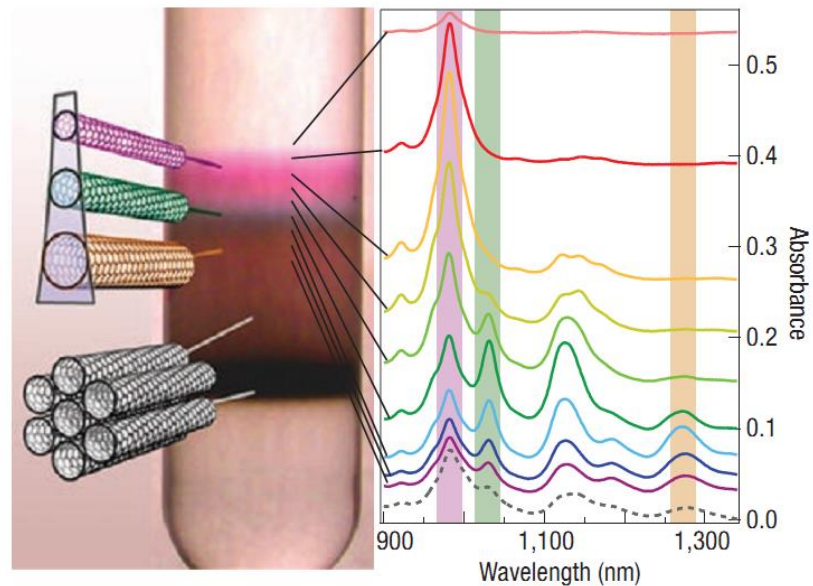
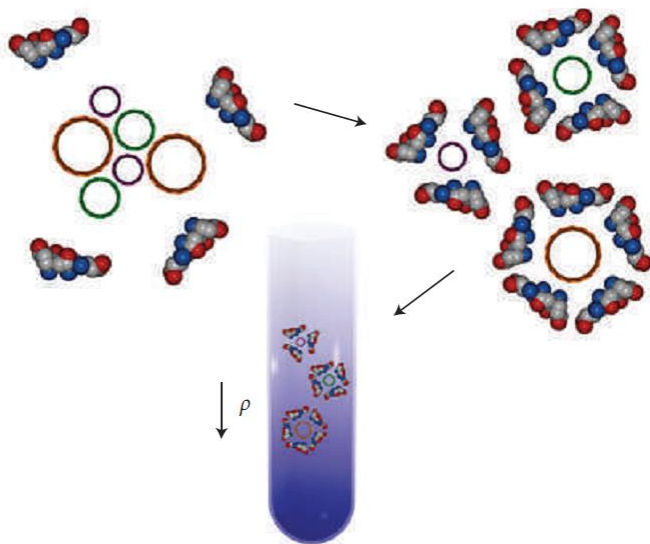
Separation by dielectrophoresis

- Apply AC voltage between electrodes
- Apply drop with CNTs
- Metallic CNTs are attracted to electrodes and removed from suspension
- Only small scale (nanograms)



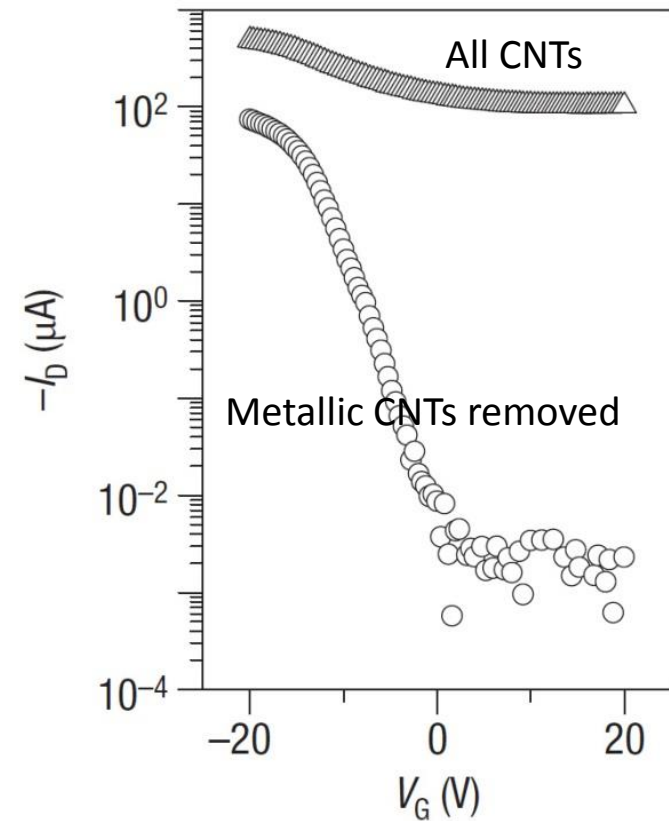
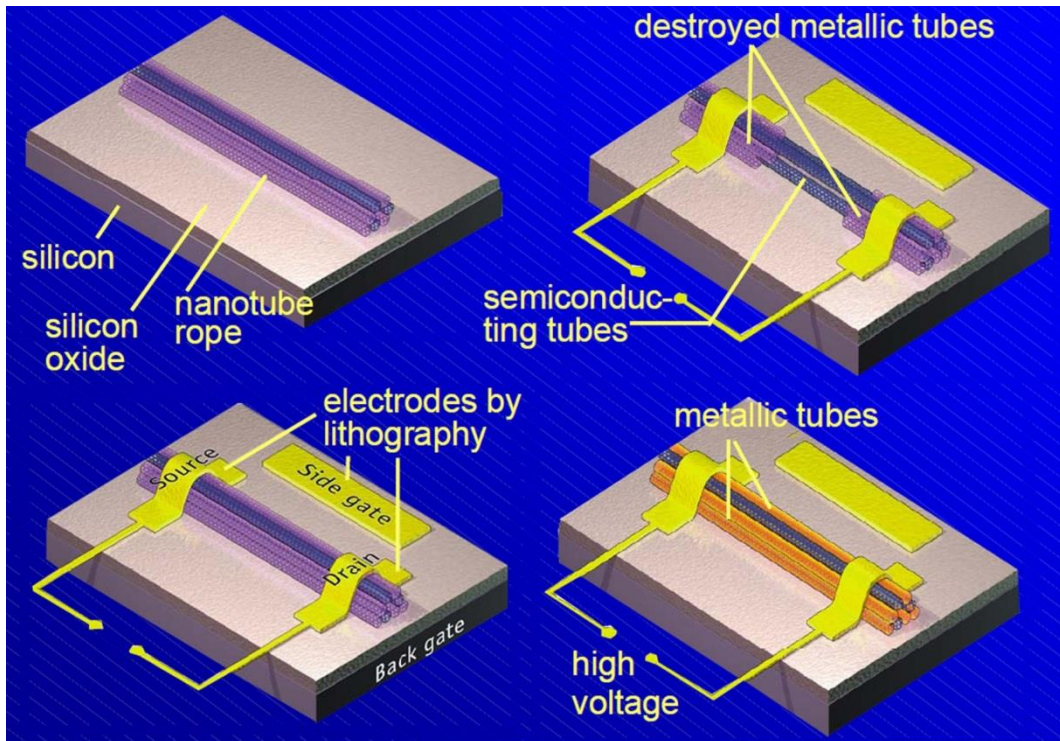
Separation by centrifugation

- Centrifuge CNT suspension at 64000 rpm \rightarrow 200000 g
- CNTs are sorted according to density
- Pick up some part of vial and repeat
- 97% of CNTs are within 0.2 Å of mean diameter

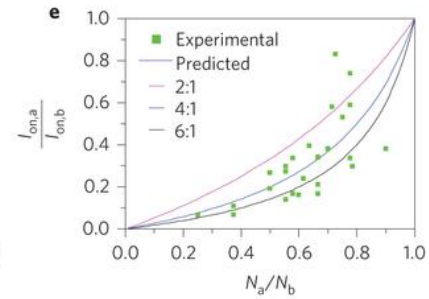
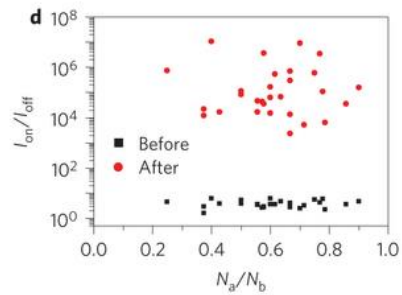
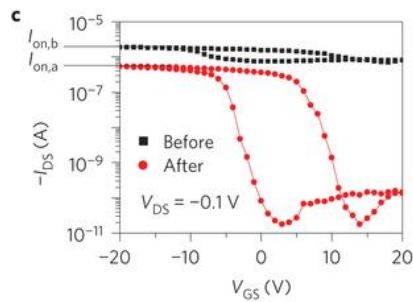
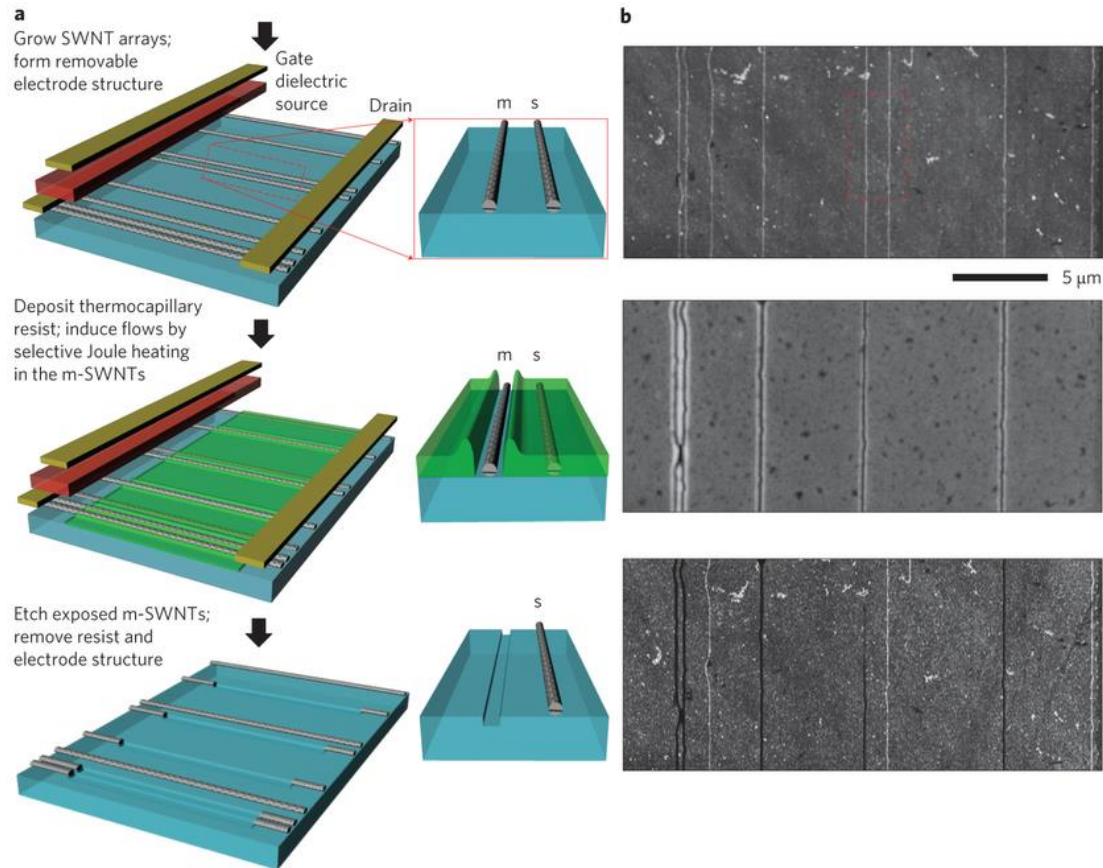


Selective destruction

- Apply gate voltage to switch off semiconducting CNTs
- Apply high S/D voltage
- Metallic CNTs are heated and destroyed
- Difficult for large scale circuits
- May destroy nearby CNTs



Selective destruction

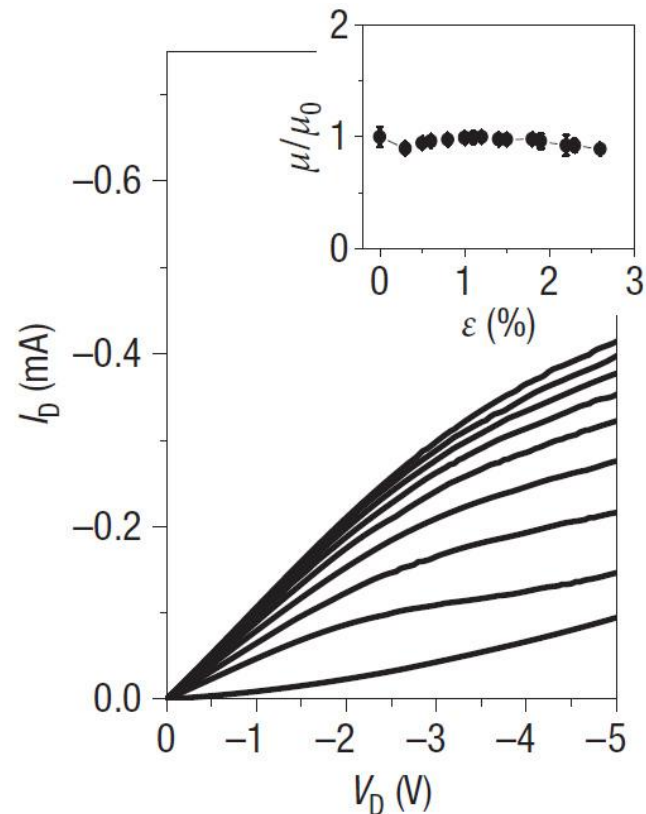
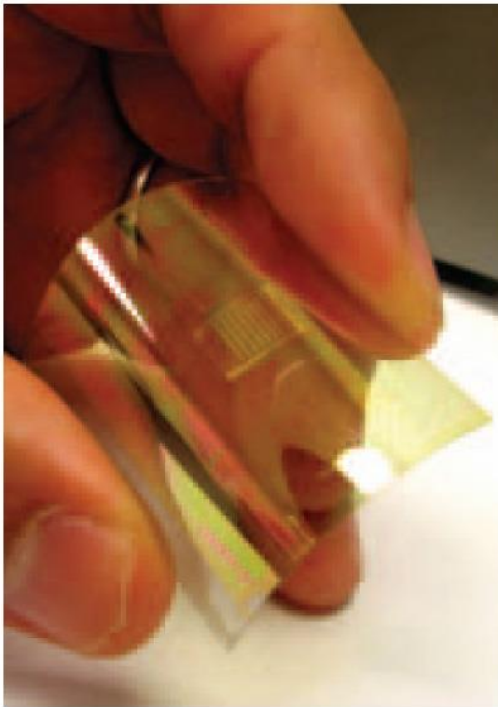


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 - Electronic
 - Production of CNTs
- Advantages of CNTs for FETs
 - Gate length scaling
 - Coaxial gate
 - High-k compatibility
 - Band-to-band tunneling
- Challenges of CNT integration
 - Contacts
 - Doping
 - Positioning
 - Chirality control
- **Towards integration**
 - **Flexible electronics**
 - **High frequency performance**

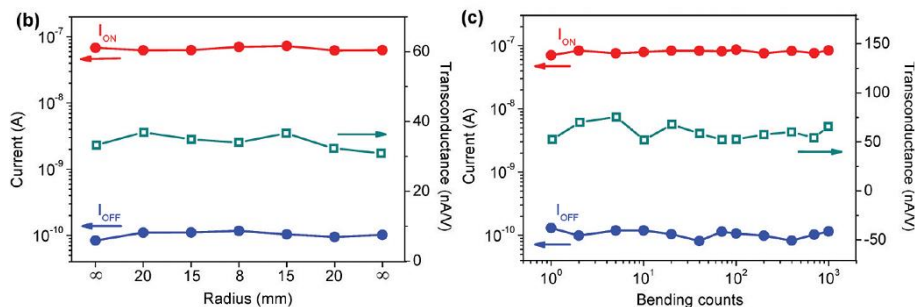
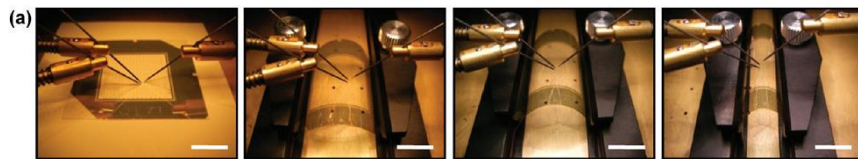
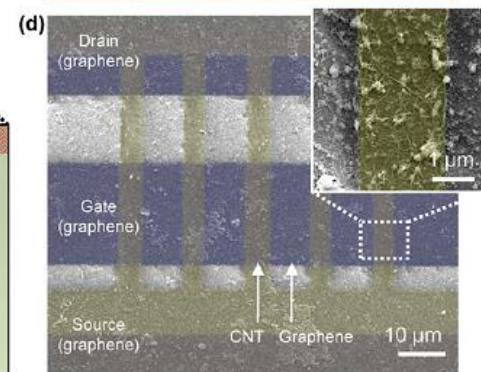
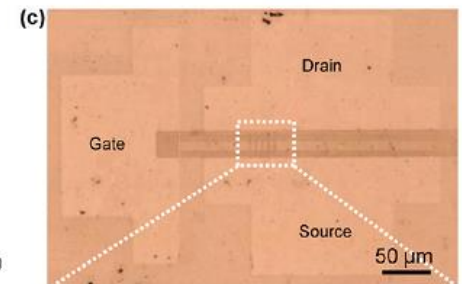
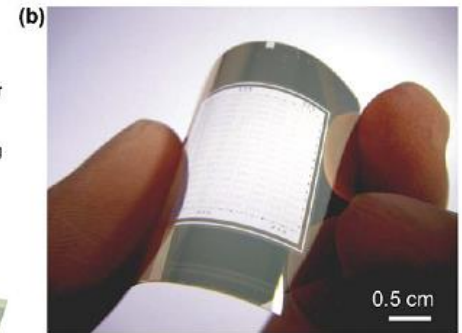
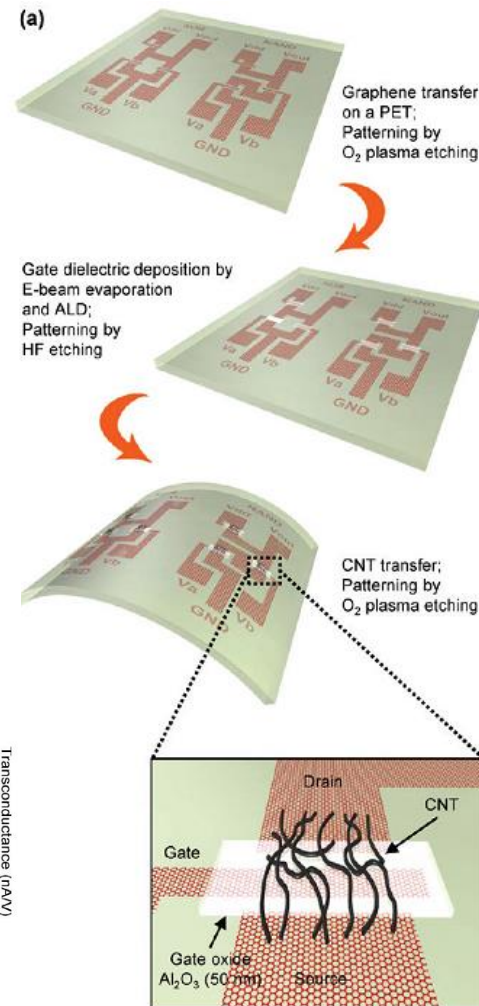
Flexible electronics

- Transfer aligned CNTs to plastic substrate
- Highest p-channel mobility (480 cm²/Vs)
- No degradation when bent


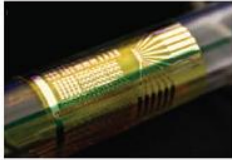
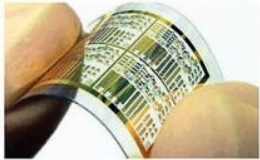
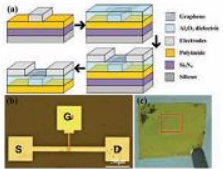
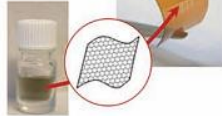


Flexible electronics 2

- Graphene for electrodes
- CNTs for channel

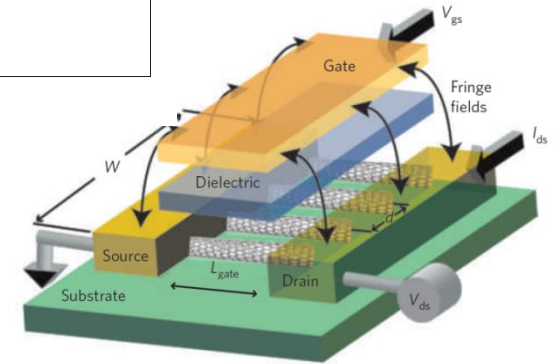
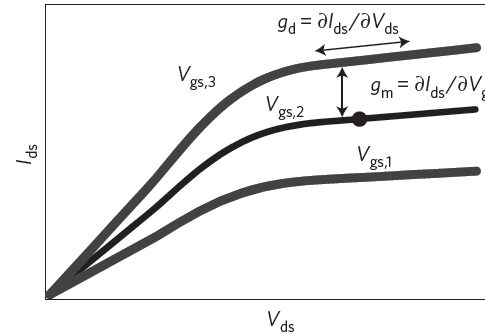


Transfer techniques

	Solid-phase	Liquid-phase	Gas-phase
CNT	<p>a</p> 	<p>c</p> 	<p>e</p> 
Graphene	<p>b</p> 	<p>d</p> 	<p>f</p> <p>No such technique</p>
Process	<p>CNT/graphene synthesis on rigid substrate</p> <p>↓</p> <p>Thin film transfer to flexible substrate</p> <p>↓</p> <p>Subsequent processes of transistor fabrication</p>	<p>CNT/graphene solution preparation</p> <p>↓</p> <p>Thin film formation by spin-coating, printing...</p> <p>↓</p> <p>Subsequent processes of transistor fabrication</p>	<p>CNT synthesis/collection in the gas phase</p> <p>↓</p> <p>Dry transfer thin film to flexible substrate</p> <p>↓</p> <p>Subsequent processes of transistor fabrication</p>
Feature	<ul style="list-style-type: none"> • On/off ratio control by post-treatment after thin film formation • Device dimension limited by size of rigid substrate • Demo for flexible electronics 	<ul style="list-style-type: none"> • Semiconducting inks prepared by purification, dispersion and separation process • Deterioration of material quality during solution process • High-throughput, large area manufacturing by R2R, inkjet printing... 	<ul style="list-style-type: none"> • CNT density control by adjusting collection time • As-grown CNT without contamination by solution • Challenge in sorting CNT, only sparse CNT thin film in the channel • Large area, continuous, fast and scale-up process

Requirements for RF applications

- on/off ratio not so important
- Need high g_m and low $g_d \rightarrow$ only semiconducting CNTs
- Minimize parasitic capacitance / CNT \rightarrow dense array of CNTs



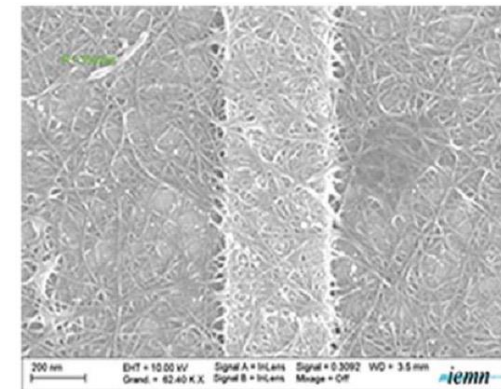
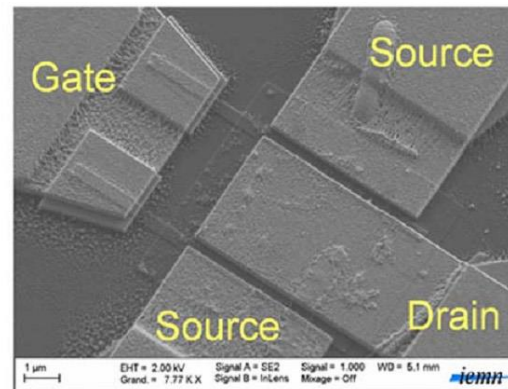
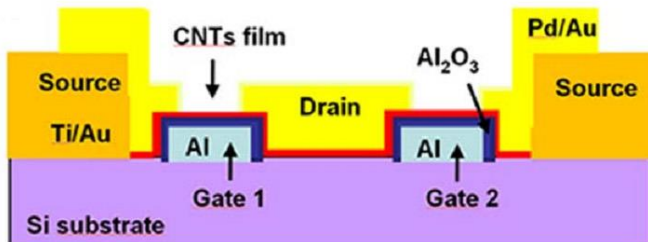
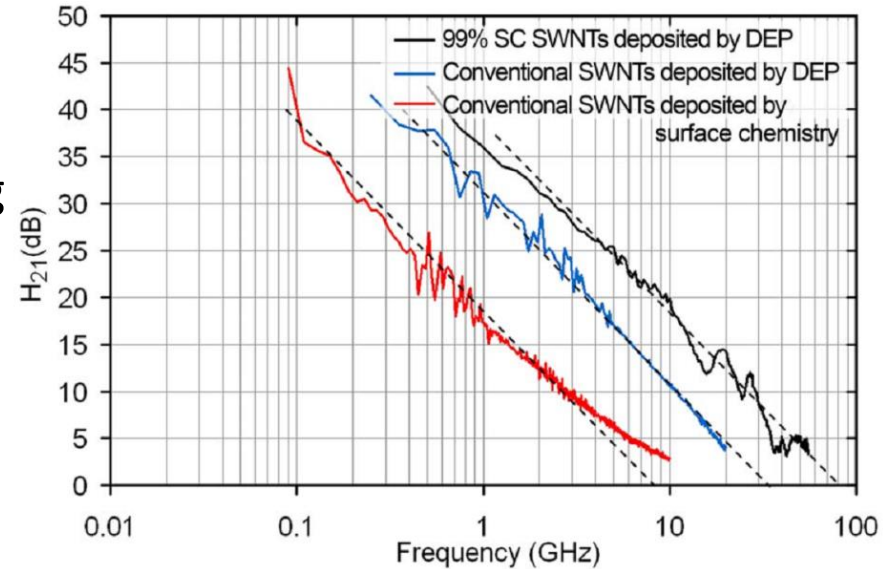
$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{gs} + C_{p,gs} + C_{p,gd})((R_{p,s} + R_{p,d})g_d + 1) + C_{p,gd}g_m(R_{p,s} + R_{p,d})}$$

Table 1 | Ideal parameter values for making a high-frequency field-effect transistor from single-walled nanotubes.

Property/parameter	Target value or range	Justification
Diameter	1.5–2.0 nm	Current is largest in this range ^{54–55} .
Chirality	Semiconducting and same (n,m)	To obtain identical transport properties.
Purity	>99% semiconducting nanotubes	No metallic nanotubes for high gain and high f_{max} .
Length	>1 μm	Nanotube length must be longer than the intended channel length.
Density	>10 nanotubes μm^{-1}	Reduces the parasitic capacitance per nanotube; increases current carrying capacity; improves impedance matching.
Alignment	All parallel	Results in higher transconductance and denser nanotube packing.
Uniformity	Wafer scale	Essential for large-scale processing.

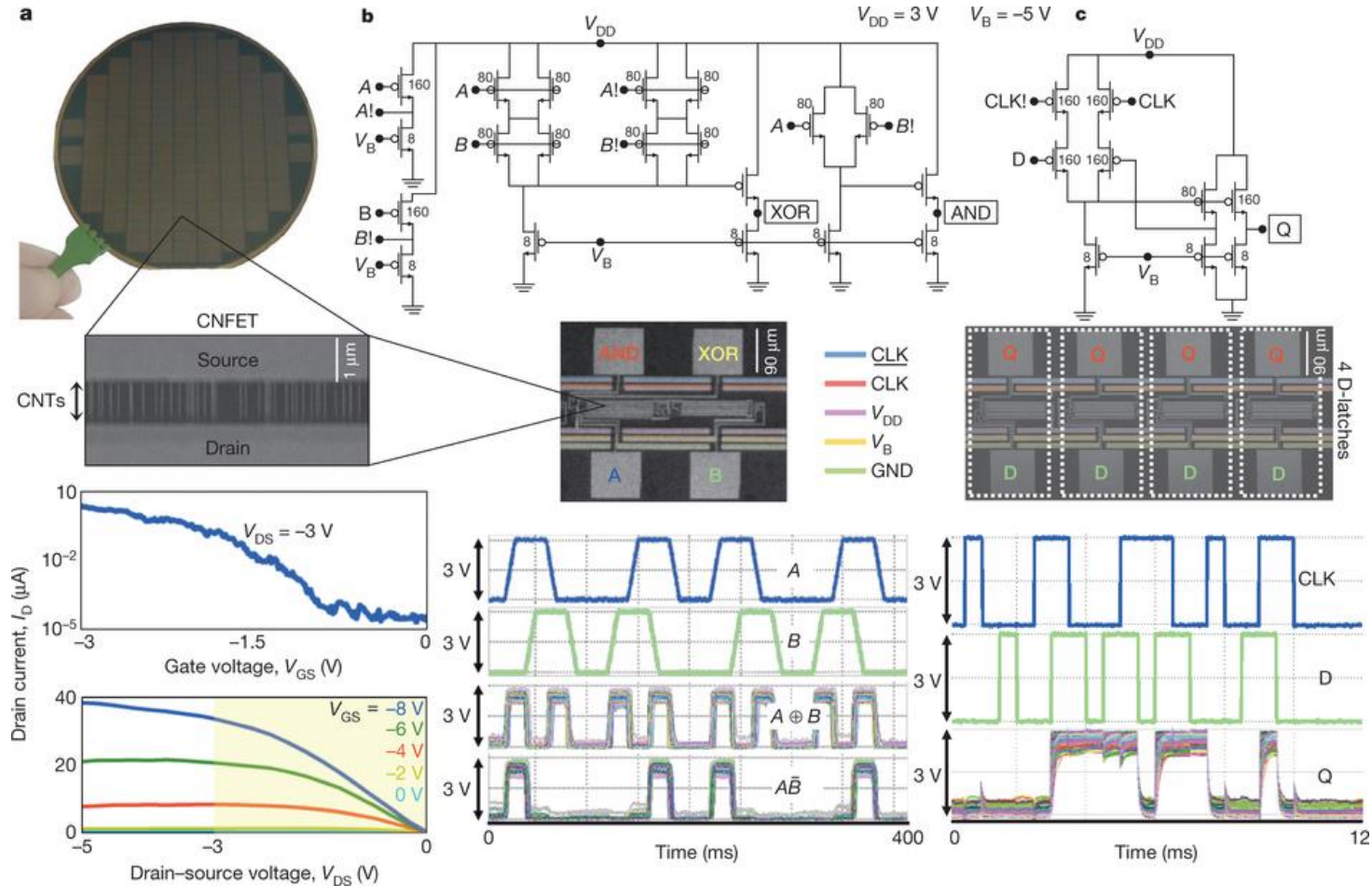
RF performance

- Difficult to measure on single CNT due to impedance mismatch
- Use dense net of separated semiconducting CNTs
- Extract current gain from S-parameters
- $f_T = 80$ GHz
- Much better than "original" CNT material



CNT computer

- 178 p-type CNTFETs. Aligned growth -> transfer -> burn-off
- Not CMOS
- Multitasking operating system for counting and number sorting. 1980's level.



Summary

- **Individual CNTs have great electronic properties**
 - High mobility
 - coaxial gate + thin -> good scaling
 - Compatible with high-k dielectrics
 - No surface scattering
- **CNTs are difficult to integrate in large scale circuits**
 - Schottky barriers at contacts
 - Unstable doping
 - Poor position control
 - Semiconducting / metallic mix

